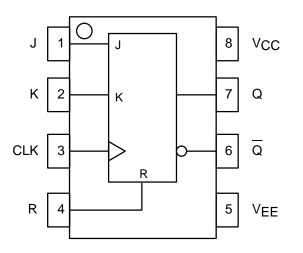
JK Flip-Flop

The MC10EL/100EL35 is a high speed JK flip-flop. The J/K data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

- 525ps Propagation Delay
- 2.2GHz Toggle Frequency
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



MC10EL35 MC100EL35



TRUTH TABLE												
J	к	R	CLK	Qn+1								
L L H H		L L L	Z Z Z Z X	Qn L <u>H</u> Qn								
Х	Х	Н	Х	L								
Z = LOW to HIGH Transition												

MOTOROLA

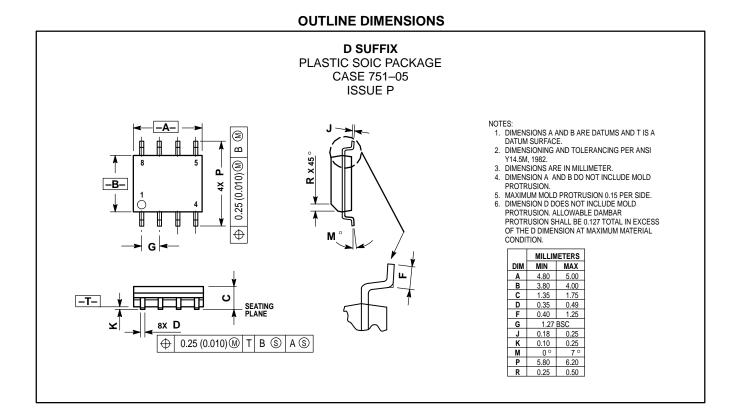
MC10EL35 MC100EL35

DC CHARACTERISTICS ($V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = GND$)

			–40°C				0°C			25°C			85°C		
Symbol	Characteristic		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
IEE	Power Supply Current	10EL 100EL		27 27	32 32		27 27	32 32		27 27	32 32		27 32	32 37	mA
VEE	Power Supply Voltage	10EL 100EL		-5.2 -4.5		-4.75 -4.20	-5.2 -4.5	5.5 5.5	-4.75 -4.20	-5.2 -4.5	5.5 5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	V
Iн	Input HIGH Curre	ent			150			150			150			150	μΑ

AC CHARACTERISTICS ($V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = GND$)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Unit									
^f MAX	Maximum Toggle Frequency	1.4	2.0		1.8	2.2		1.8	2.2		1.8	2.2		GHz
^t PLH ^t PHL	Propagation Delay CLK to Output MR	290 225	515 450	740 675	340 275	515 450	690 625	350 275	525 450	700 625	395 350	570 525	745 700	ps
tS	Setup Time J, K	150	0		150	0		150	0		150	0		ps
ťн	Hold Time J, K	250	100		250	100		250	100		250	100		ps
^t RR	Reset Recovery	400	200		400	200		400	200		400	200		ps
^t PW	Minimum Pulse Width CLK, Reset	400			400			400			400			ps
t _r t _f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps



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