# USB to Fast Ethernet/HomePNA Controller

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## Features

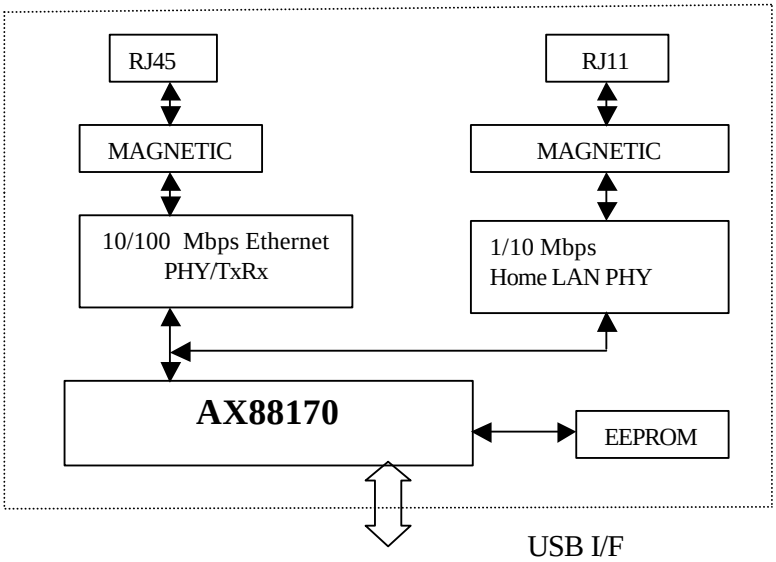
- Single chip USB to 10/100Mbps Fast Ethernet and 1/10Mbps HomePNA Network Controller
- Compliant with USB specification 1.0 and 1.1
- Full Speed USB Device with bus power capability
- USB Communication Class Spec 1.0 Compliant
- Support 4 endpoints on USB
- IEEE 802.3u 100BASE-T, TX, and T4 Compatible
- Embedded 5K*16 bit SRAM
- Support both full-duplex or half-duplex operation on Fast Ethernet
- Provides a MII port for both Ethernet and HomePNA PHY interface
- Supports suspended mode and remote wakeup (link_up or magic packet)
- Optional PHY power down mode for power saving
- Provides optional MII/RMII interface with PHY mode for multiple ports USB-to-USB bridge application.
- Support 256/512 bytes serial EEPROM (used for saving USB Descriptors)
- Support automatic loading of Ethernet ID, USB Descriptors and Adapter Configuration from EEPROM on power-on initialization
- External PHY loop-back diagnostic capability
- Small form factor 64-pin LQFP package
- 48MHz and 25MHz Operation, pure 3.3V operation with I/O 5V tolerance



## Product description

The AX88170 USB to Fast Ethernet/HomePNA Controller is a high performance and highly integrated Controller with embedded 5K*16 bit SRAM. The AX88170 contains a USB interface to host CPU and compliant with USB StandardV1.0 and V1.1. The interface between AX88170 and PC Host is compliant with USB Communication Class Specification 1.0. The AX88170 could be used for both 10M/100Mbps Fast Ethernet function based on IEEE802.3 / IEEE802.3u LAN standard and 1M/10M HomePNA standard. The AX88170 supports media-independent interface (MII) or RMII (Reduce MII) interface to simplify the design on implementing Fast Ethernet and HomePNA functions. The chip also provides an optional MII/RMII interface with PHY mode, combine with Ethernet repeater or switch IC can build a multiple ports USB-to-USB bridge application.

## System Block Diagram



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# 1.0 Introduction

## 1.1 General Description:

The AX88170 USB to Fast Ethernet Controller is a high performance and highly integrated USB bus Ethernet Controller with embedded 5K*16 bit SRAM. The AX88170 contains a full speed USB interface to host CPU and compliant with USB Communication Class Spec. 1.0. The AX88170 implements both 10Mbps and 100Mbps Ethernet function based on IEEE802.3 / IEEE802.3u LAN standard. The AX88170 supports media-independent interface (MII) or RMII (Reduce MII) interface to simplify the design on implementing Fast Ethernet and HomePNA functions. The chip also provides an optional MII/RMII interface with PHY mode, combines with Ethernet repeater or switch IC can build a multiple ports USB-to-USB bridge application.

AX88170 uses 64-pin LQFP low profile package, 48MHz operation for USB and 25MHz operation for Ethernet, CMOS process with pure 3.3V operation and 5 Volt I/O tolerance.

## 1.2 AX88170 Block Diagram:

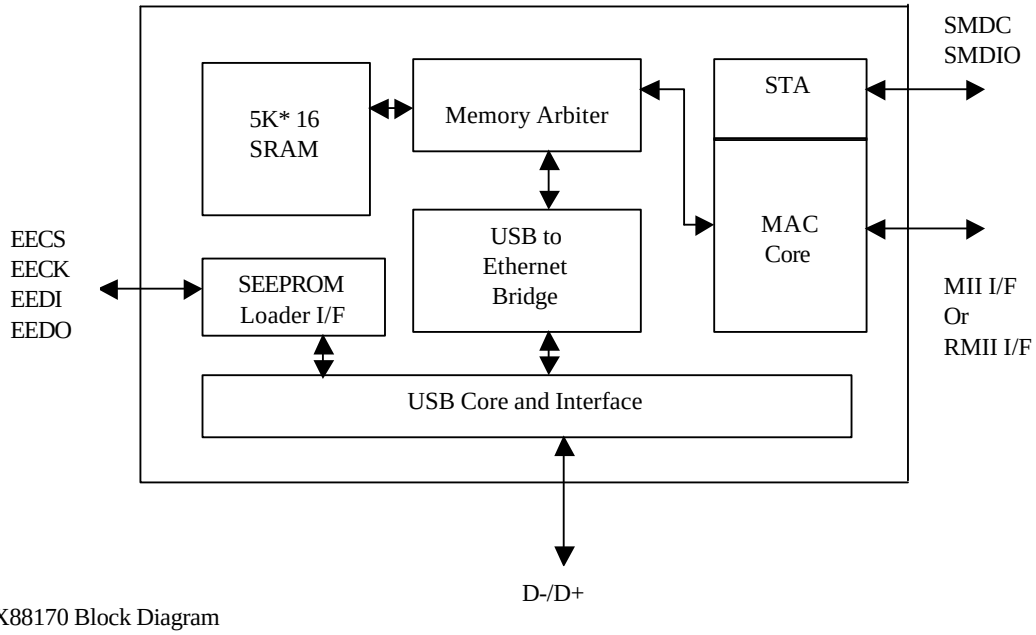



Fig – 1 AX88170 Block Diagram

## 1.3 AX88170 Pin Connection Diagram with MII Interface

The AX88170 is housed in the 64-pin plastic light quad flat pack. See Fig – 2 AX88170 Pin Connection Diagram.

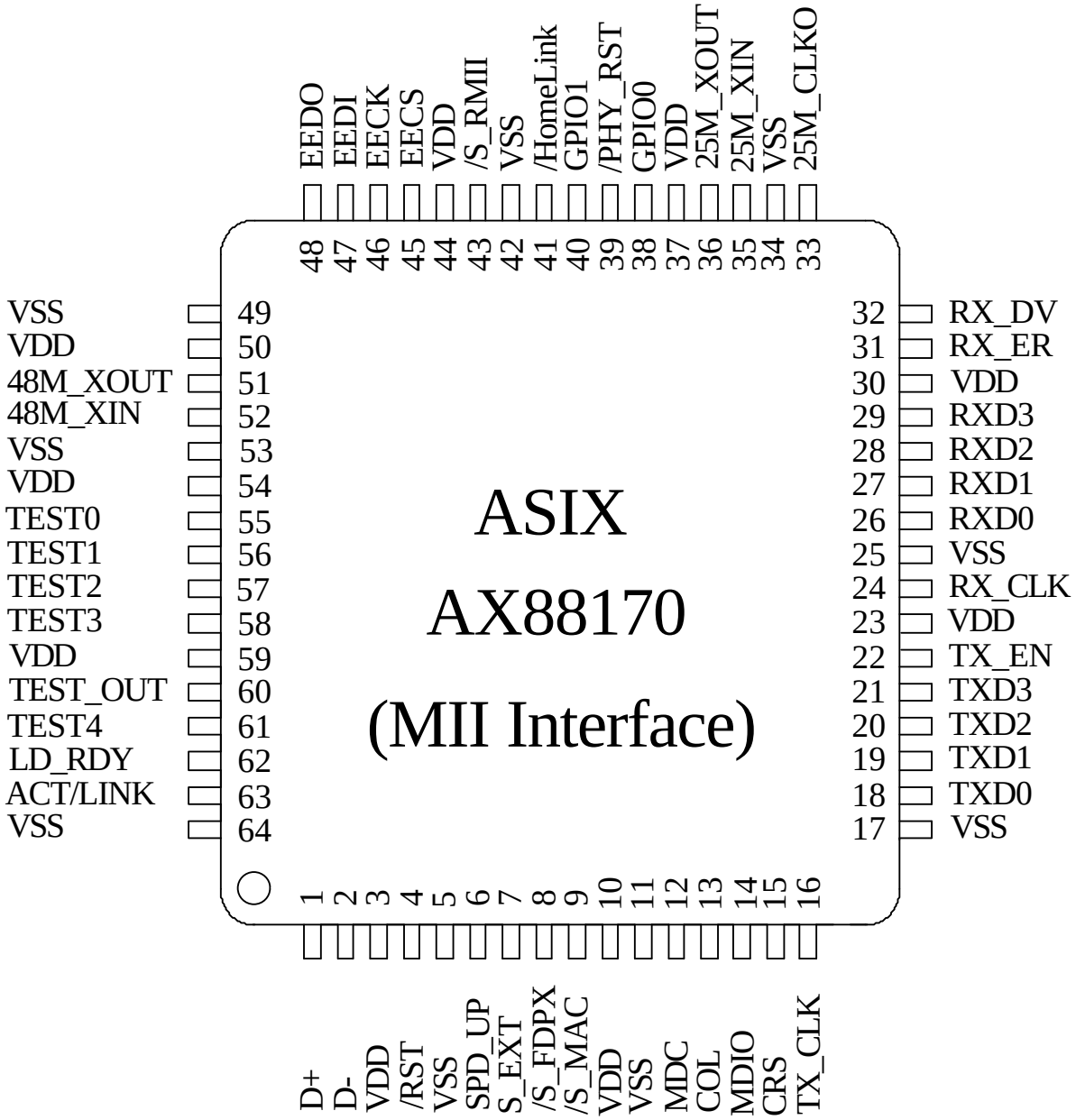



Fig – 2 AX88170 Pin Connection Diagram with MII Interface

## 1.4 AX88170 Pin Connection Diagram with RMII Interface

The AX88170 is housed in the 64-pin plastic light quad flat pack. See Fig – 3 AX88170 Pin Connection Diagram RMII Interface.

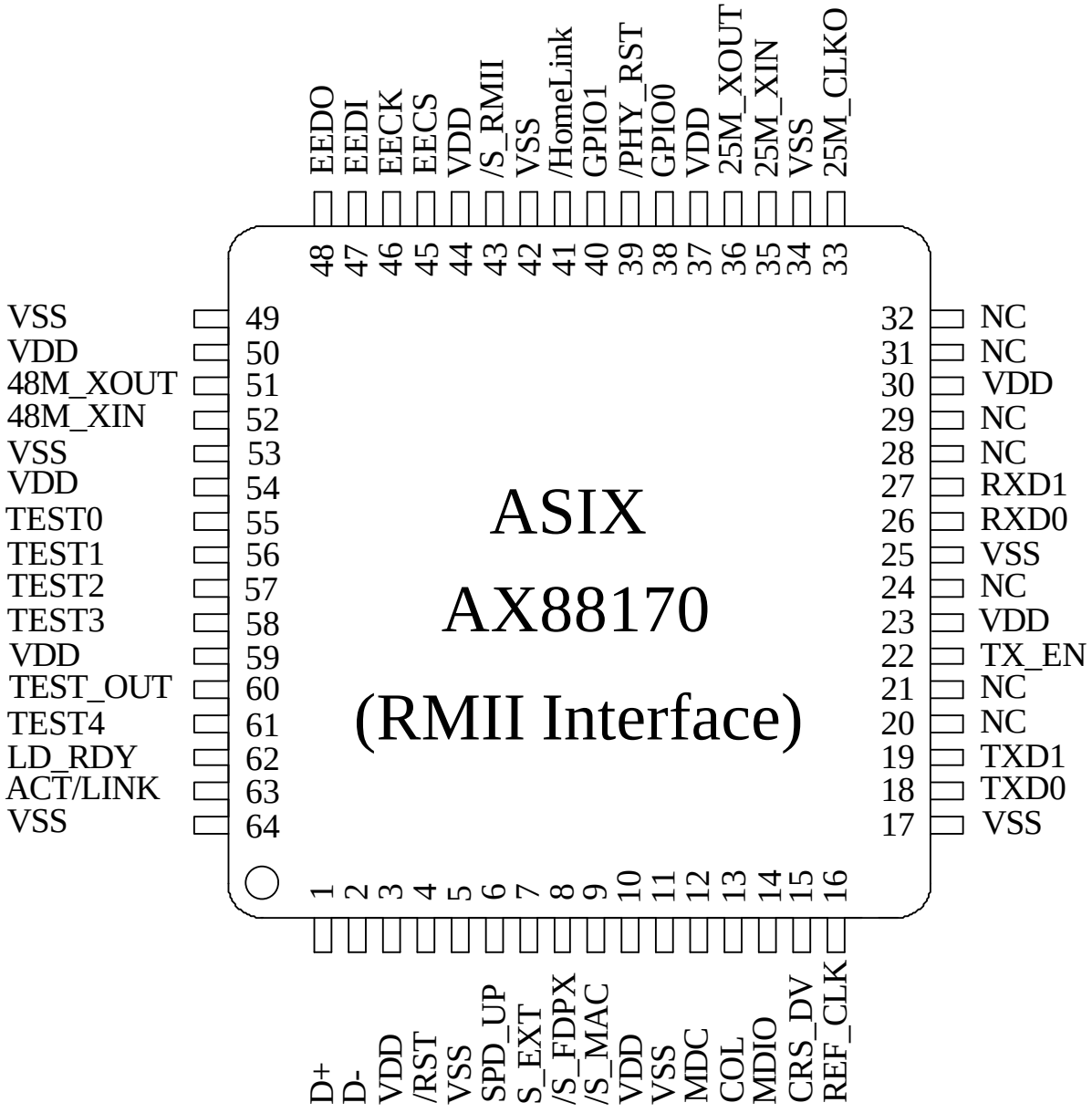



Fig – 3 AX88170 Pin Connection Diagram RMII Interface

# 2.0 Signal Description

The following terms describe the AX88170 pin-out:
All pin names with the "/" suffix are asserted low.
The following abbreviations are used in following Tables.

| | | | |
|---|---|---|---|
| **I** | **Input** | **PU** | **Pull Up** |
| **O** | **Output** | **PD** | **Pull Down** |
| **I/O** | **Input/Output** | **P** | **Power Pin** |
| **OD** | **Open Drain** | | |

## 2.1 USB Bus Interface Signals Group

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|---|---|---|---|
| D+ | I/O | 1 | USB Data Plus Pin |
| D- | I/O | 2 | USB Data Minus Pin |

Tab – 1 USB bus interface signals group

## 2.2 EEPROM Signals Group

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|---|---|---|---|
| EECS | O | 45 | EEPROM Chip Select : EEPROM chip select signal. |
| EECK | O | 46 | EEPROM Clock : Signal connected to EEPROM clock pin. |
| EEDI | O | 47 | EEPROM Data In : Signal connected to EEPROM data input pin. |
| EEDO | I/PU | 48 | EEPROM Data Out : Signal connected to EEPROM data output pin. |

Tab – 2 EEPROM bus interface signals group

## 2.3a MII interface signals group (MAC mode)

When /S_RMII=1 and /S_MAC=0

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|---|---|---|---|
| RXD[3:0] | I/PU | 29, 28<br>27, 26 | Receive Data: RXD[3:0] is driven by the PHY synchronously with respect to RX_CLK. |
| CRS | I/PD | 15 | Carrier Sense: Asynchronous signal CRS is asserted by the PHY when either the transmit or receive medium is non-idle. |
| RX_DV | I/PD | 32 | Receive Data Valid: RX_DV is driven by the PHY synchronously with respect to RX_CLK. Asserted high when valid data is present on RXD [3:0]. |
| RX_ER | I/PD | 31 | Receive Error: RX_ER is driven by PHY and synchronous to RX_CLK, is asserted for one or more RX_CLK periods to indicate to the port that an error has detected. |
| RX_CLK | I/PU | 24 | Receive Clock: RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV,RXD[3:0] and RX_ER signals from the PHY to the MII port of the MAC. |
| COL | I/PD | 13 | Collision: this signal is driven by PHY when collision is detected. |
| TX_EN | O | 22 | Transmit Enable: TX_EN is transition synchronously with respect to the rising edge of TX_CLK. TX_EN indicates that the port is presenting |

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|---|---|---|---|
| | | | nibbles on TXD [3:0] for transmission. |
| TXD[3:0] | O | 21, 20<br>19, 18 | Transmit Data: TXD[3:0] is transition synchronously with respect to the rising edge of TX_CLK. For each TX_CLK period in which TX_EN is asserted ,TXD[3:0] are accepted for transmission by the PHY. |
| TX_CLK | I | 16 | Transmit Clock: TX_CLK is a continuous clock from PHY. It provides the timing reference for the transfer of the TX_EN and TXD[3:0] signals from the MII port to the PHY. |
| MDC | O | 12 | Station Management Data Clock: The timing reference for MDIO. All data transfers on MDIO are synchronized to the rising edge of this clock. MDC is a 2.5MHz frequency clock output. |
| MDIO | I/O/PU | 14 | Station Management Data Input/Output: Serial data input/output transfers from/to the PHYs. The transfer protocol conforms to the IEEE 802.3u MII specification. |

Tab – 3 MII interface signals group (MAC mode)

## 2.3b MII interface signals group (PHY mode)

When /S_RMII=1 and /S_MAC=1

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|---|---|---|---|
| RXD[3:0] | O | 29, 28<br>27, 26 | Receive Data: Basically RXD[3:0] is transformed from TXD[3:0] of MAC mode of MII interface. |
| CRS | O | 15 | Carrier Sense: Basically CRS is transformed from TX_EN of MAC mode of MII interface. |
| RX_DV | O | 32 | Receive Data Valid: Basically RX_DV is transformed from TX_EN of MAC mode of MII interface. |
| RX_ER | O | 31 | Receive Error: No used |
| RX_CLK | O | 24 | Receive Clock: Basically RX_CLK is sourced from internal 25MHz local clock. |
| COL | O | 13 | Collision: this signal is generated by internal logic when collision is detected. |
| TX_EN | I/PD | 22 | Transmit Enable: Basically TX_EN is simulation from RX_DV of MAC mode of MII interface. |
| TXD[3:0] | I/PU | 21, 20<br>19, 18 | Transmit Data: Basically TXD[3:0] is simulation from RXD[3:0] of MAC mode of MII interface. |
| TX_CLK | O | 16 | Transmit Clock: Basically TX_CLK is sourced from intemal 25MHz local clock. |

Tab – 4 MII interface signals group (PHY mode)

## 2.4 RMII interface signal pins (PHY mode)

When /S_RMII=0 and /S_MAC=1

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|---|---|---|---|
| RXD[1:0] | O | 27, 26 | **Receive Data :** Basically RXD[1:0] is transformed from TXD[1:0] of MAC mode of RMII interface. |
| CRS_DV | O | 15 | **Carrier Sense _ Data Valid :** Basically CRS_DV is transformed of TX_EN from MAC mode of RMII interface. |
| TXD[1:0] | I/PU | 19, 18 | **Transmit Data :** Basically TXD[1:0] is transformed from RXD[1:0] of MAC mode of RMII interface. |
| TX_EN | I/PD | 22 | **Transmit Enable :** Basically TX_EN is transformed from RX_DV from MAC mode of RMII interface. |
| REF_CLK | I | 16 | **Reference clock :** The input is a continue clock at 50Mhz for timing reference with RMII interface. |

Tab – 5 RMII interface signal pins (PHY mode)

## 2.5 Miscellaneous pins group

| SIGNAL | TYPE | PIN NO. | DESCRIPTION |
|---|---|---|---|
| 25M_XIN | I | 35 | CMOS Local Clock : Typical a 25Mhz clock, +/- 100 ppm, 40%-60% duty cycle. ( See application note also )<br>Crystal Oscillator Input : Typical a 25Mhz crystal, +/- 25 ppm can be connected across 25M_XIN and 25M_XOUT. |
| 25M_XOUT | O | 36 | Crystal Oscillator Output : Typical a 25Mhz crystal, +/- 25 ppm can be connected across 25M_XIN and 25M_XOUT. If a single-ended external clock is connected to 25M_XIN, the crystal output pin should be left floating. |
| 48M_XIN | I | 52 | 48Mhz CMOS Clock In : Typical a 48Mhz clock, +/- 500 ppm, 40%-60% duty cycle. ( See application note also )<br>48Mhz Crystal Oscillator Input: Typical a 48Mhz crystal, +/- 100 ppm can be connected across 48M_XIN and 48M_XOUT. |
| 48M_XOUT | O | 51 | 48Mhz Crystal Oscillator Output: Typical a 48Mhz crystal, +/- 100 ppm can be connected across 48M_XIN and 48M_XOUT. If a single-ended external clock is connected to 48M_XIN, the crystal output pin should be left floating. |
| 25M_CLKO | O | 33 | Clock Output : This clock is source from 25M_XIN. |
| /RST | I/PD | 4 | Reset:<br>Reset is active low then place AX88170 into reset mode immediately. During Rising edge the AX88170 loads the EEPROM data. |
| /S_RMII | I/PU | 43 | Set to RMII mode:<br>0: RMII mode is selected.<br>1: MII mode is selected. (default) |
| /S_MAC | I/PD | 9 | Set MII/RMII interface to MAC mode:<br>0: MAC mode is selected. (default)<br>1: PHY mode is selected. |
| /S_FDPX | I/PD | 8 | Set duplex mode when PHY mode is selected or When S_EXT is set and MAC mode is selected:<br>0: full-duplex mode is selected. (default)<br>1: half-duplex mode is selected. |
| S_EXT | I/PD | 7 | Select where duplex mode is sourced from when MAC mode:<br>0: duplex mode depands on internal register. (default)<br>1: duplex mode depands on external signal /S_FDPX |
| SPD_UP | ID | 6 | The setting is enable speed up test mode: |

| | | | |
|---|---|---|---|
| | | | 0: Normal operation mode.<br>1: Speed up test mode enable. |
| TEST0 | I/PD | 55 | Test Pin: This pin for test purpose only.<br>Pull down the pin or keep no connection for normal operation. |
| TEST1 | I/PD | 56 | Test Pin: This pin for test purpose only.<br>Pull down the pin or keep no connection for normal operation. |
| TEST2 | I | 57 | Test Pin: This pin for test purpose only.<br>**Pull down** the pin for normal operation. |
| TEST3 | I/PD | 58 | Test Pin: This pin for test purpose only.<br>Pull down the pin or keep no connection for normal operation. |
| TEST4 | I/PD | 61 | Test Pin: This pin for test purpose only.<br>Pull down the pin or keep no connection for normal operation. |
| TEST_OUT | O | 60 | Test Output Pin: This pin for test purpose only. |
| LDRDY | O | 62 | Load EEPROM data completed indicator. Active high. |
| ACT/LINK | O | 63 | LED indicator: When link fail, drives logic high always. When link OK, the pin drives logic low and will drives high a period when line has activity (data transfer). |
| /PHY_RST | O | 39 | PHY Reset: This pin is used to reset PHY and is an active low signal. |
| GPIO0 | B/PD | 38 | General Purpose I/O 0: Refer to section 4.3 USB Vendor Commands |
| GPIO1 | B/PD | 40 | General Purpose I/O 1: Refer to section 4.3 USB Vendor Commands |
| /HOMELINK | I/PU | 41 | Link Status: For external HomePHY link state input active low |
| VDD | P | 3, 10, 23, 30<br>37, 44, 50<br>54,59 | Power Supply: +3.3V DC. |
| VSS | P | 5, 11<br>17, 25, 34<br>42, 49, 53<br>64 | Power Supply: +0V DC or Ground Power. |

Tab - 6 Miscellaneous pins group

## MII/RMII interface Cross Reference Table

| MII | RMII |
|---|---|
| RXD[0] | RXD[0] |
| RXD[1] | RXD[1] |
| RXD[2] | |
| RXD[3] | |
| CRS | CRS_DV |
| RX_DV | |
| RX_CLK | |
| RX_ER | |
| TX_EN | TX_EN |
| TX_CLK | REF_CLK (50MHz) |
| TXD[0] | TXD[0] |
| TXD[1] | TXD[1] |
| TXD[2] | |
| TXD[3] | |
| COL | |

# 3.0 EEPROM Memory Mapping

| EEPROM OFFSET | HIGH BYTE | LOW BYTE |
|---|---|---|
| 00H | RESERVED | WORD COUNT FOR PRELOAD |
| 01H | *FLAG | |
| 02H | LENGTH OF DEVICE DESCRIPTOR (BYTE) | EEPROM OFFSET OF DEVICE DESCRIPTOR |
| 03H | LENGTH OF CONFIGURATION DESCRIPTOR (BYTE) | EEPROM OFFSET OF CONFIGURATION DESCRIPTOR |
| 04H | NODE ID 1 | NODE ID 0 |
| 05H | NODE ID 3 | NODE ID 2 |
| 06H | NODE ID 5 | NODE ID 4 |
| 07H | LANGUAGE ID HIGH BYTE | LANGUAGE ID LOW BYTE |
| 08H | LENGTH OF STRING INDEX 1 | EEPROM OFFSET OF STRING INDEX 1 |
| 09H | LENGTH OF STRING INDEX 2 | EEPROM OFFSET OF STRING INDEX 2 |
| 0AH | LENGTH OF STRING INDEX 3 | EEPROM OFFSET OF STRING INDEX 3 |
| 0BH | LENGTH OF STRING INDEX 4 | EEPROM OFFSET OF STRING INDEX 4 |
| 0CH | LENGTH OF STRING INDEX 5 | EEPROM OFFSET OF STRING INDEX 5 |
| 0DH | LENGTH OF STRING INDEX 6 | EEPROM OFFSET OF STRING INDEX 6 |
| 0EH | LENGTH OF STRING INDEX 7 | EEPROM OFFSET OF STRING INDEX 7 |
| 0FH | LENGTH OF STRING INDEX 8 | EEPROM OFFSET OF STRING INDEX 8 (19H) |
| 10H | MAX PACKETSIZE HIGH BYTE | MAX PACKET LOW BYTE |
| 11H | HOMEPNA PHY ID | ETHERNET PHY ID |
| 12H | PAUSE PACKET HIGH WATER LEVEL | PAUSE PACKET LOW WATER LEVEL |
| 13H-18H | RESERVED | |
| 19H | 03H | 0CH |
| 1AH | BYTE 2 OF UNICODE MAC ADDRESS | **BYTE 1 OF UNICODE MAC ADDRESS |
| 1BH | BYTE 4 OF UNICODE MAC ADDRESS | BYTE 3 OF UNICODE MAC ADDRESS |
| 1CH | BYTE 6 OF UNICODE MAC ADDRESS | BYTE 5 OF UNICODE MAC ADDRESS |
| 1DH | BYTE 8 OF UNICODE MAC ADDRESS | BYTE 7 OF UNICODE MAC ADDRESS |
| 1EH | BYTE 10 OF UNICODE MAC ADDRESS | BYTE 9 OF UNICODE MAC ADDRESS |
| 1FH | BYTE 12 OF UNICODE MAC ADDRESS | BYTE 11 OF UNICODE MAC ADDRESS |
| 20H-4FH | DEVICE /CONFIGURATION /INTERFACE /ENDPOINT DESCRIPTOR | |
| 50H-FFH | STRINGS | |

Tab - 7 EEPROM Memory Mapping

Note:

*Flag: Bit 0 ➔ Self Powered (for USB GetStatus) Bit 1 ➔ Bus Powered (Reserved)
Bit 2 ➔ Remote Wakeup (for USB GetStatus) Bit 3 ➔ Interrupt Endpoint Enaable (Reserved)
Bit 4 ➔ ClkNoStop (for Self Power only) Bit 5 ➔ Reserved
Bit 6 ➔ Reserved Bit 7 ➔ Reserved
Bit 8 ➔ Capture Effective Mode Bit 9 ➔ Flow Control selector (1: software, o: read from PHY)
Bit A – F ➔ Reserved

Bit 4 also effect LED display, if high then LED display USB active only otherwise display USB link and activity.
(In Self power mode Bit_4 set to high)

**Unicode MAC Address:

If the MAC' s NODE ID is 01,23,45,67,89,ABh respect to NODE ID 0, NODE ID 1, … NODE ID5 Then the unicode will be 30-31,32-33,34-35,36-37,38-39,41-42h respects to BYTE 1 OF UNICODE MAC ADDRESS- BYTE 2 OF UNICODE MAC ADDRESS, …-BYTE 12 OF UNICODE MAC ADDRESS.

# 4.0 USB Commands

There are three command groups for Endpoint 0 in AX88170:

- The USB standard commands
- USB Communication Class commands
- USB vendor commands.

## 4.1 USB standard commands

** The Language ID is 0x0904 for English
** PPLL means buffer length
** CC means configuration number
** I I means Interface number

| SETUP COMMAND | DATA IN/OUT | DESCRIPTION |
|---|---|---|
| 80 06 00 01 00 00 LL PP | Data PPLL bytes | Get Device Descriptor |
| 80 06 00 02 00 00 LL PP | Data PPLL bytes | Get Configuration Descriptor |
| 80 06 00 03 00 00 LL PP | Data 2 bytes | Get Supported Language ID |
| 80 06 01 03 09 04 LL PP | Data PPLL bytes | Get Manufacture String |
| 80 06 02 03 09 04 LL PP | Data PPLL bytes | Get Product String |
| 80 06 03 03 09 04 LL PP | Data PPLL bytes | Get Serial Number String |
| 80 06 04 03 09 04 LL PP | Data PPLL bytes | Get Configuration String |
| 80 06 05 03 09 04 LL PP | Data PPLL bytes | Get Interface 0 String |
| 80 06 06 03 09 04 LL PP | Data PPLL bytes | Get Interface 1/0 String |
| 80 06 07 03 09 04 LL PP | Data PPLL bytes | Get Interface 1/1 Stirng |
| 80 06 08 03 09 04 LL PP | Data 12 bytes | Get Ethernet Address String |
| 80 08 00 00 00 00 01 00 | Data 1 bytes | Get Configuration |
| 00 09 CC 00 00 00 00 00 | No Data | Set Configuration |
| 81 0A 00 00 I I 00 01 00 | Data 1 byte | Get Interface |
| 01 0B AS 00 01 00 00 00 | No Data | Set Interface |

## 4.2 USB Communication Class Commands

** NN: number of multicast addresses
** BBAA: Ethernet Packet Filter
** TTSS: Number of Ethernet Statics

| SETUP COMMAND | DATA IN/OUT | DESCRIPTION |
|---|---|---|
| 21 40 NN 00 00 00 6*N 00 | Data 6*N bytes | Set Ethernet Multicast Filters |
| 21 41 00 00 00 00 10 00 | Data 16 bytes | Set Ethernet Power Management Pattern |
| A1 42 00 00 00 00 02 00 | Data 2 bytes | Get Ethernet Power Management Pattern |
| 21 43 AA BB 00 00 00 00 | No Data | Set Ethernet Packet Filter (AA BB) |

Description of Ethernet Packet Filter (AA BB) Bitmap
BB = [D15:D8]
AA = [D7:D0]

| Bit position | DESCRIPTION |
|---|---|
| D15..D5 | RESERVED (Reset to Zero) |
| D4 | PACKET_TYPE_MULTICAST<br>1: All multicast packets enumerated in the device's multicast address list are forwarded up to the host.<br>0: Disabled. |
| D3 | PACKET_TYPE_BROADCAST<br>1: All broadcast packet packets received by the networking device are forwarded up to the host.<br>0: Disable. |
| D2 | PACKET_TYPE_DIRECTED<br>1: Directed packets received containing a destination address equal to the MAC address of the networking device are forwarded up to the host.<br>0: Always not set to Zero. |
| D1 | PACKET_TYPE_ALL_MULTICAST<br>1 : ALL multicast frames received by the networking device are forwarded up to the host, not just the ones enumerated in the device's multicast address list.<br>0: Disabled. |
| D0 | PACKET_TYPE_PROMISCUOUS<br>1: ALL frames received by the networking device are forwarded up to the host.<br>0: Disabled. |

Tab - 9 Ethernet Packet Filter Bitmap

## 4.3 USB Vendor Commands

| SETUP COMMAND | DATA IN/OUT | DESCRIPTION |
|---|---|---|
| C0 02 XX YY 00 0M 02 00 | Data 2 bytes | Read Rx/Tx SRAM<br>M = 0 : Rx, M=1 : Tx |
| 40 03 XX YY PP QQ 00 00 | No Data | Write Rx SRAM |
| 40 04 XX YY PP QQ 00 00 | No Data | Write Tx SRAM |
| 40 06 00 00 00 00 00 00 | No Data | Disable H/W MII Operation |
| C0 07 PI 00 RG 00 02 00 | Data 2 Bytes | Read MII Register |
| 40 08 PI 00 RG 00 02 00 | Data 2 Bytes | Write MII Register |
| C0 09 00 00 00 00 01 00 | Data 1 Bytes | Read MII Operation Mode |
| 40 0A 00 00 00 00 00 00 | No Data | Enable H/W MII Operation |
| C0 0B DR 00 00 00 02 00 | Data 2 Bytes | Read SROM |
| 40 0C DR 00 MM SS 00 00 | No Data | Write SROM |
| 40 0D 00 00 00 00 00 00 | No Data | Write SROM Enable |
| 40 0E 00 00 00 00 00 00 | No Data | Write SROM Disable |
| C0 0F 00 00 00 00 02 00 | Data 2 Bytes | Read Rx Control Register |
| 40 10 RR 00 00 00 00 00 | No Data | Write Rx Control Register |
| C0 11 00 00 00 00 03 00 | Data 3 Bytes | Read IPG/IPG1/IPG2 Register |
| 40 12 II 00 00 00 00 00 | No Data | Write IPG Register |
| 40 13 II 00 00 00 00 00 | No Data | Write IPG1 Register |
| 40 14 II 00 00 00 00 00 | No Data | Write IPG2 Register |
| C0 15 00 00 00 00 08 00 | Data 8 Bytes | Read Multi-Filter Array |
| 40 16 00 00 00 00 08 00 | Data 8 Bytes | Write Multi-Filter Array |
| C0 17 00 00 00 00 06 00 | Data 6 Bytes | Read Node ID |
| C0 19 00 00 00 00 02 00 | Data 2 Bytes | Read Ethernet/HomePNA PhyID |
| C0 1A 00 00 00 00 01 00 | Data 1 Byte | Read Medium Status(*) |
| 40 1B MM 00 00 00 00 00 | No Data | Write Medium Mode(*) |
| C0 1C 00 00 00 00 01 00 | Data 1 Byte | Get Monitor Mode Status(**) |
| 40 1D MM 00 00 00 00 00 | No Data | Set Monitor Mode On/Off(**) |

Notes:

* Read / Write Medium status

| | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| Read | GPI1 | X | GPI0 | X | Home_Link | 100MHz | Full_Duplex | Link |
| Write | GPO1 | GPO1EN | GPO0 | GPO0EN | FRBI | 100MHz | Full_Duplex | Link |

** Read / Write Monitor Mode

| | Bit7-5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|
| Read | Reserved (Hardware_Version for ASIX only) | Flow_Contron_En | X | Magic_Packet_En | Link_UP_Wake | Monitor_Mode |
| Write | X | Flow_Contron_En | X | Magic_Packet_En | Link_UP_Wake | Monitor_Mode |

Interrupt Endpoint report link status format

| Byte Number | | |
|---|---|---|
| Byte 0 | A1 | Fixed value |
| Byte 1 | 00 | Fixed value |
| Byte 2 | NN | Bit_0 : Ethernet Link state, Bit_1 : Home PHY Link state (active high) |
| Byte 3 | 00 | Fixed value |
| Byte 4 | NN | Bit_0 : 100MHz speed detect |
| Byte 5 | NN | Reserved (Hardware version for ASIX only) |
| Byte 6 | NN | Bit_0 : Full Duplex |
| Byte 7 | 00 | Fixed value |

# 5.0 USB Configuration Structure

## 5.1 USB Configuration.

The AX88170 supports 1 Configuration only.

## 5.2 USB Interface Class.

The AX88170 supports 2 interfaces, the interface 0 is Data Interface and interface 1 is for Communication Interface.

## 5.3 USB Endpoints.

The AX88170 supports 4 endpoints.
Endpoint 0 ➔ Control endpoint, it is for configuring device.
Endpoint 1 ➔ (optional) Interrupt endpoint, it is for reporting status change
Endpoint 2➔ Bulk Out endpoint, it is for Transmitting Ethernet Packet.
Endpoint 3 ➔ Bulk In endpoint, it is for Receiving Ethernet Packet.

# 6.0 Electrical Specification and Timings

## 6.1 Absolute Maximum Ratings

| Description | SYM | Min | Max | Units |
|---|---|---|---|---|
| Operating Temperature | Ta | 0 | +85 | °C |
| Storage Temperature | Ts | -55 | +150 | °C |
| Supply Voltage | Vdd | -0.3 | +3.6 | V |
| Input Voltage | Vin | -0.3 | Vdd+0.3 | V |
| Output Voltage | Vout | -0.3 | Vdd+0.3 | V |
| Lead Temperature (soldering 10 seconds maximum) | Tl | -55 | +240 | °C |

Note: Stress above those listed under Absolute M aximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability.

## 6.2 General Operation Conditions

| Description | SYM | Min | Tpy | Max | Units |
|---|---|---|---|---|---|
| Operating Temperature | Ta | 0 | 25 | +70 | °C |
| Supply Voltage | Vdd | +3.0 | +3.30 | +3.6 | V |

## 6.3 DC Characteristics

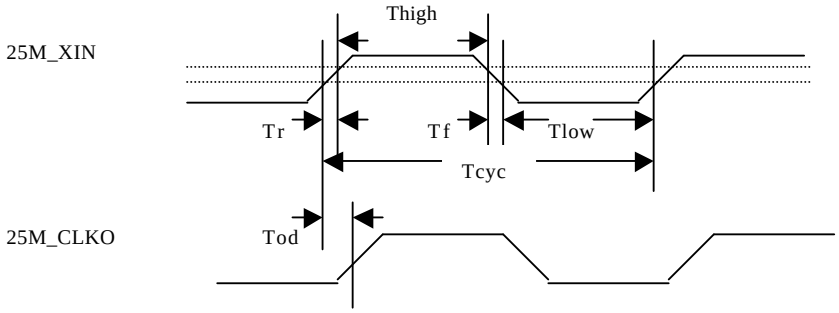
(Vdd=3.0V to 3.6V, Vss=0V, Ta=0°C to 70°C)

| Description | SYM | Min | Tpy | Max | Units |
|---|---|---|---|---|---|
| Low Input Voltage | Vil | - | | 0.3*Vdd | V |
| High Input Voltage | Vih | 0.7*Vdd | | - | V |
| Low Output Voltage | Vol | - | | 0.4 | V |
| High Output Voltage | Voh | 2.4 | | - | V |
| Input Leakage Current | Iil | -1 | | +1 | uA |
| Output Leakage Current | Iol | -10 | | +10 | uA |
| Input Pull-up / down resistance | Ri | | 75 | | K ohm |

| Description | SYM | Min | Tpy | Max | Units |
|---|---|---|---|---|---|
| Power Consumption (3.3V) | SPt3v | | 40 | | mA |

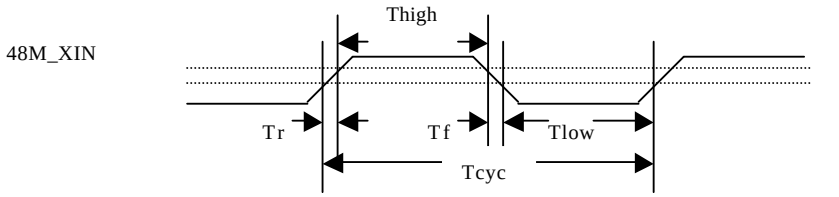
# 6.4 A.C. Timing Characteristics

## 6.4.1 25M_XIN



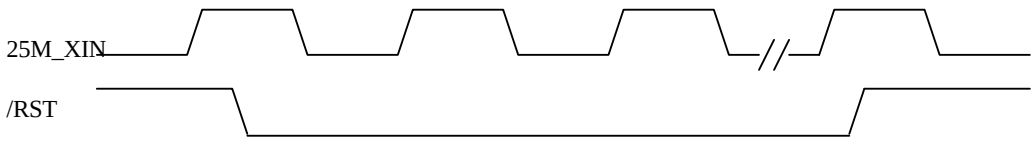

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Tcyc | CYCLE TIME | | 40 | | ns |
| Thigh | CLK HIGH TIME | 16 | 20 | 24 | ns |
| Tlow | CLK LOW TIME | 16 | 20 | 24 | ns |
| Tr/Tf | CLK SLEW RATE | 1 | - | 4 | ns |
| Tod | LCLK/XTALIN TO 25M_CLKO OUT DELAY | 8 | | 29 | ns |

## 6.4.2 48M_XIN



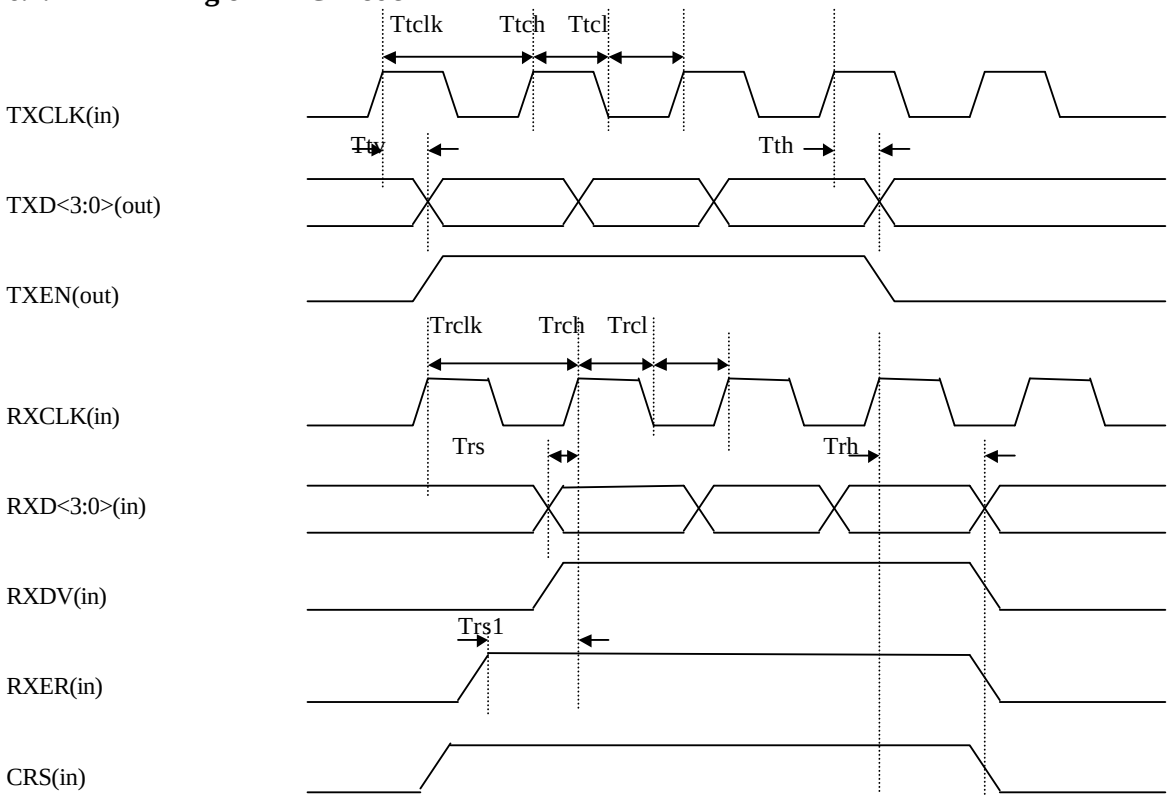

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Tcyc | CYCLE TIME | | 20.83 | | ns |
| Thigh | CLK HIGH TIME | 8.3 | 10.42 | 12.5 | ns |
| Tlow | CLK LOW TIME | 8.3 | 10.42 | 12.5 | ns |
| Tr/Tf | CLK SLEW RATE | 1 | - | 4 | ns |

## 6.4.3 Reset Timing



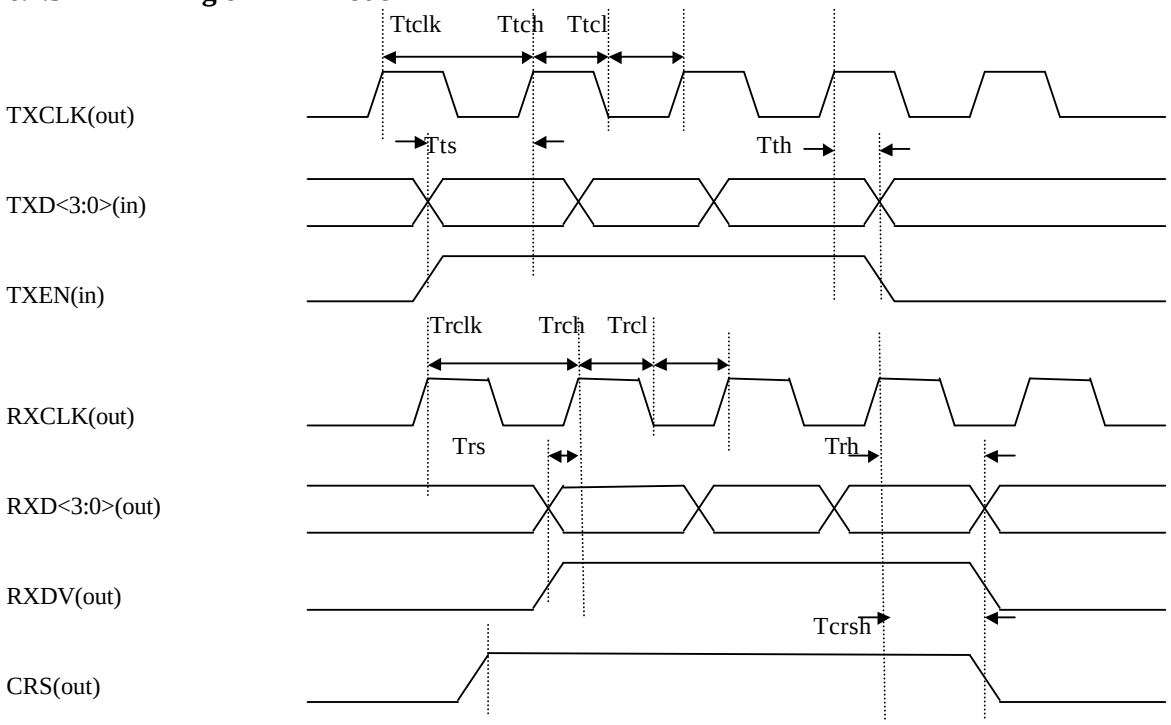

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Trst | Reset pulse width | 100 | - | - | 25M _XIN |

### 6.4.4 MII Timing of MAC mode



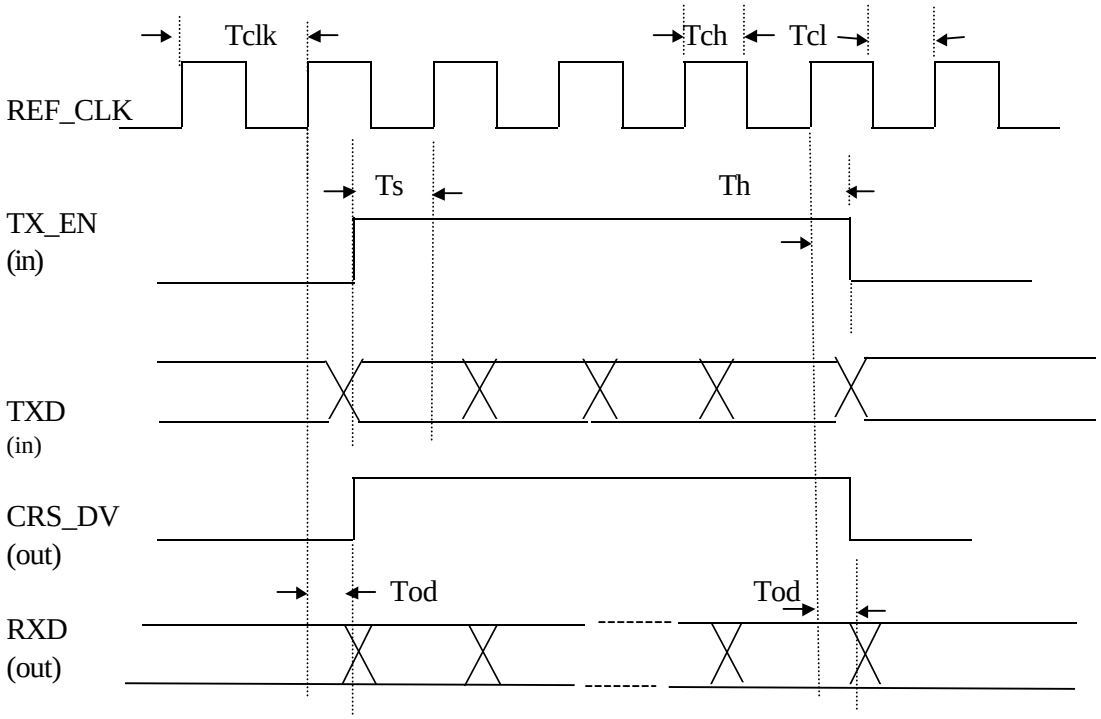

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Ttclk | Cycle time(100Mbps) | - | 40 | - | ns |
| Ttclk | Cycle time(10Mbps) | - | 400 | - | ns |
| Ttch | high time(100Mbps) | 14 | - | 26 | ns |
| Ttch | high time(10Mbps) | 140 | - | 260 | ns |
| Trch | low time(100Mbps) | 14 | - | 26 | ns |
| Trch | low time(10Mbps) | 140 | - | 260 | ns |
| Ttv | Clock to data valid | - | - | 20 | ns |
| Tth | Data output hold time | 5 | - | - | ns |
| Trclk | Cycle time(100Mbps) | - | 40 | - | ns |
| Trclk | Cycle time(10Mbps) | - | 400 | - | ns |
| Trch | high time(100Mbps) | 14 | - | 26 | ns |
| Trch | high time(10Mbps) | 140 | - | 260 | ns |
| Trcl | low time(100Mbps) | 14 | - | 26 | ns |
| Trcl | low time(10Mbps) | 140 | - | 260 | ns |
| Trs | data setup time | 6 | - | - | ns |
| Trh | data hold time | 10 | - | - | ns |
| Trs1 | RXER data setup time | 10 | - | - | ns |

### 6.4.5 MII Timing of PHY mode



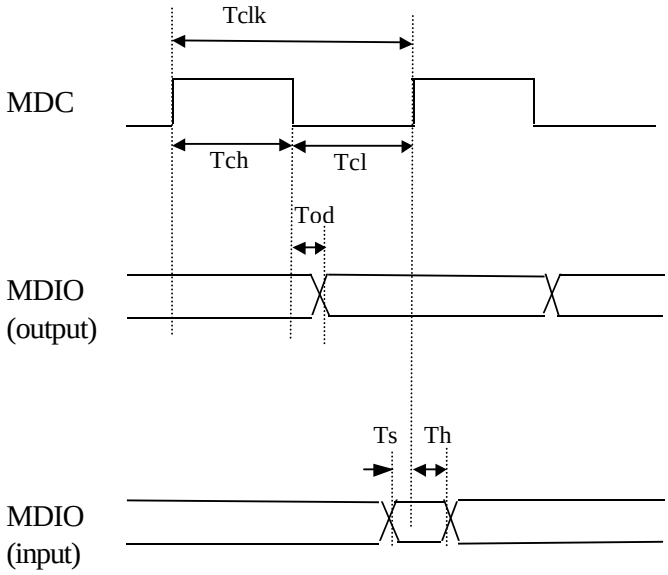

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Ttclk | Cycle time(100Mbps) | - | 40 | - | ns |
| Ttclk | Cycle time(10Mbps) | - | 400 | - | ns |
| Ttch | high time(100Mbps) | 14 | - | 26 | ns |
| Ttch | high time(10Mbps) | 140 | - | 260 | ns |
| Trch | low time(100Mbps) | 14 | - | 26 | ns |
| Trch | low time(10Mbps) | 140 | - | 260 | ns |
| Tts | TXD, TXEN setup to TXCLK high | 15 | - | - | ns |
| Tth | TXD, TXEN hold to TXCLK high | 0 | - | - | ns |
| Trclk | Cycle time(100Mbps) | - | 40 | - | ns |
| Trclk | Cycle time(10Mbps) | - | 400 | - | ns |
| Trch | high time(100Mbps) | 14 | - | 26 | ns |
| Trch | high time(10Mbps) | 140 | - | 260 | ns |
| Trcl | low time(100Mbps) | 14 | - | 26 | ns |
| Trcl | low time(10Mbps) | 140 | - | 260 | ns |
| Trv | RXD, RXDV valid to RXCLK high | 10 | - | - | ns |
| Trh | RXCLK high to RXD, RXDV invalid | 10 | - | - | ns |
| Tcrsh | RXCLK high to CRS invalid | 10 | - | - | ns |

### 6.4.6 RMII Interface Timing of PHY Mode



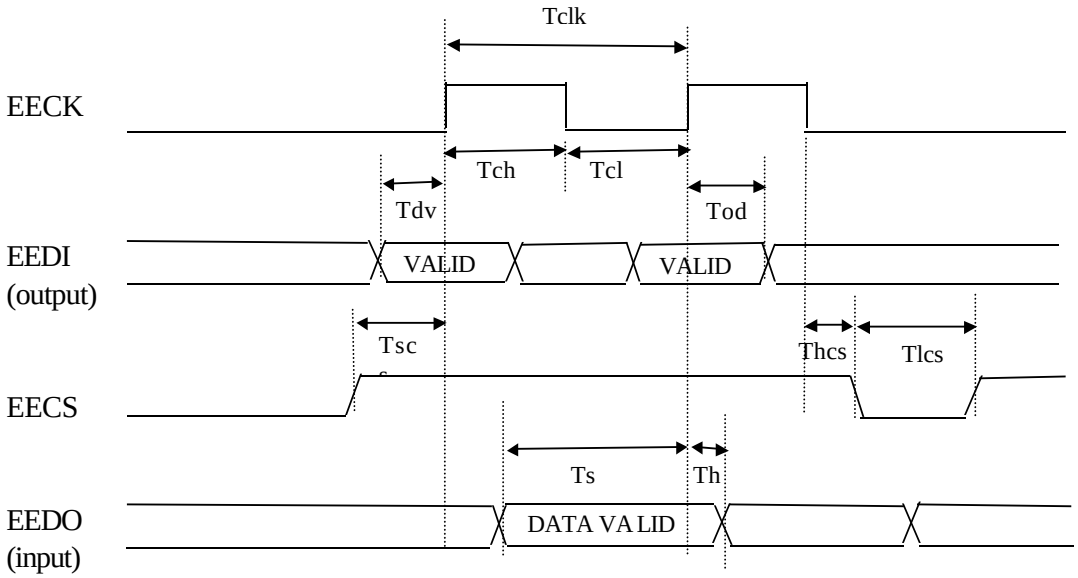

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Tclk | REF_CLK Clock Cycle Time | 19.998 | 20 | 20.002 | ns |
| Tch | REF_CLK Clock High Time | 7 | 10 | 13 | ns |
| Tcl | REF_CLK Clock Low Time | 7 | 10 | 13 | ns |
| Ts | TXEN and TXD data setup to REF_CLK high | 4 | | | ns |
| Th | TXEN and TXD data hold from REF_CLK high | 2 | | | ns |
| Tod | REF_CLK rising edge to CRS_DV, RXD delay | 4 | | | ns |

### 6.4.7 STATION MANAGEMENT TIMING



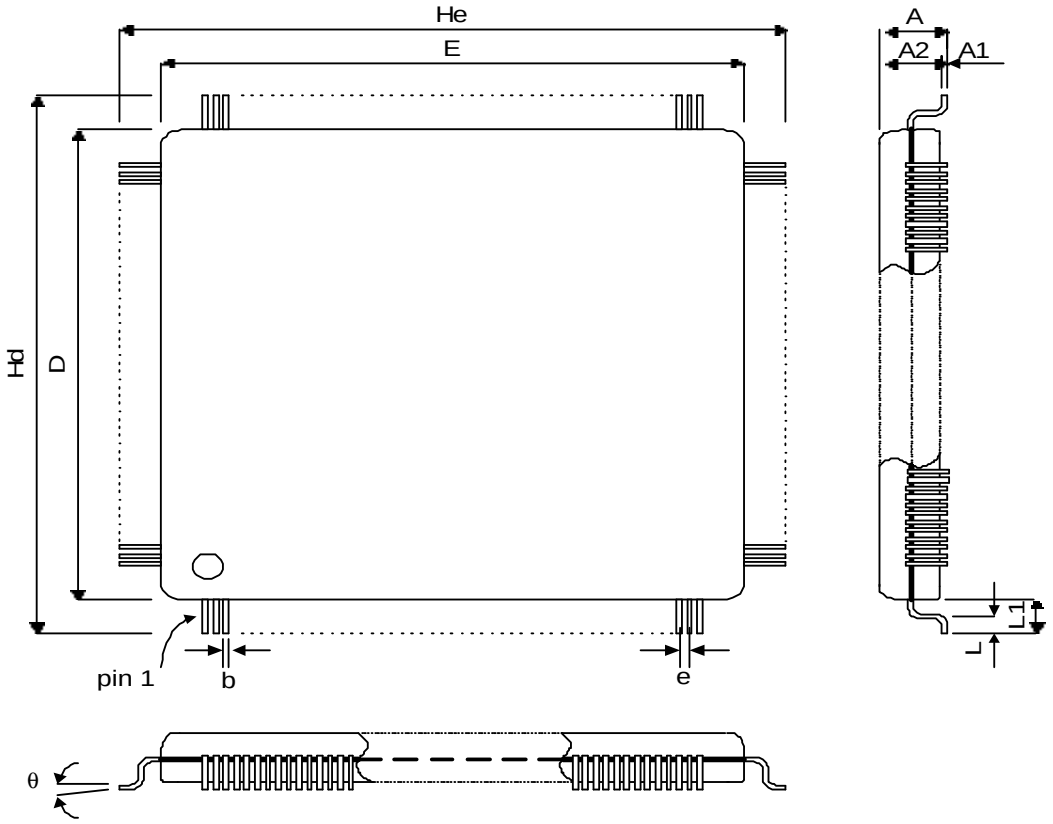

| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Tclk | MDC Clock Cycle Time | | 2560 | | ns |
| Tch | MDC Clock High Time | | 1280 | | ns |
| Tcl | MDC Clock Low Time | | 1280 | | ns |
| Tod | Clock Falling Edge to Output Valid Delay | 2 | | 9 | ns |
| Ts | Data In Setup Time | 10 | | | ns |
| Th | Data In Hold Time | 100 | | | ns |

### 6.4.8 SERIAL EEPROM TIMING




| Symbol | Description | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Tclk | EECK Clock Cycle Time | | 5120 | | ns |
| Tch | EECK Clock High Time | 2500 | | 9 | ns |
| Tcl | EECK Clock Low Time | 2500 | | 9 | ns |
| Tdv | EEDI Data Valid Output to EECK High Time | 500 | | | ns |
| Tod | EECK High to EEDI Data Output Delay Time | 500 | | | ns |
| Tscs | EECS Valid to EECK High Time | 300 | | | ns |
| Thcs | EECK Low to EECS Invalid Time | 0 | | | ns |
| Tlcs | Minimum EECS Low Time | 2500 | | | ns |
| Ts | Data Input Setup Time | 10 | | | ns |
| Th | Data Input Hold Time | 100 | | | ns |

# 7.0 Package Information

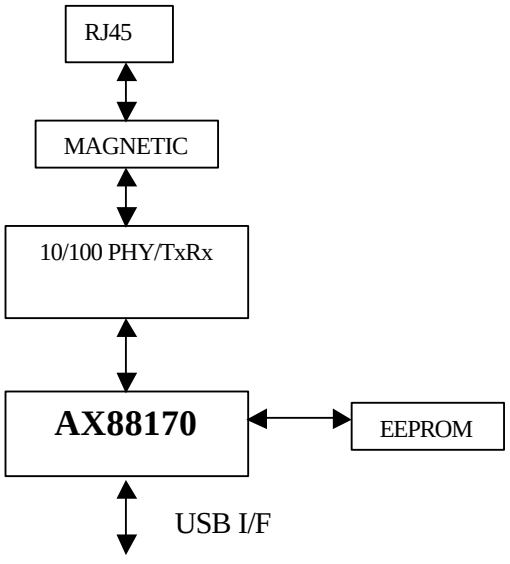


| SYMBOL | MILIMETER | | |
|---|---|---|---|
| | MIN. | NOM | MAX |
| A1 | 0.05 | 0.1 | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A | | | 1.60 |
| b | 0.17 | 0.22 | 0.27 |
| D | | 10.00 | |
| E | | 10.00 | |
| e | | 0.5 | |
| Hd | | 12.00 | |
| He | | 12.00 | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 | |
| θ | 0° | 3.5° | 7° |

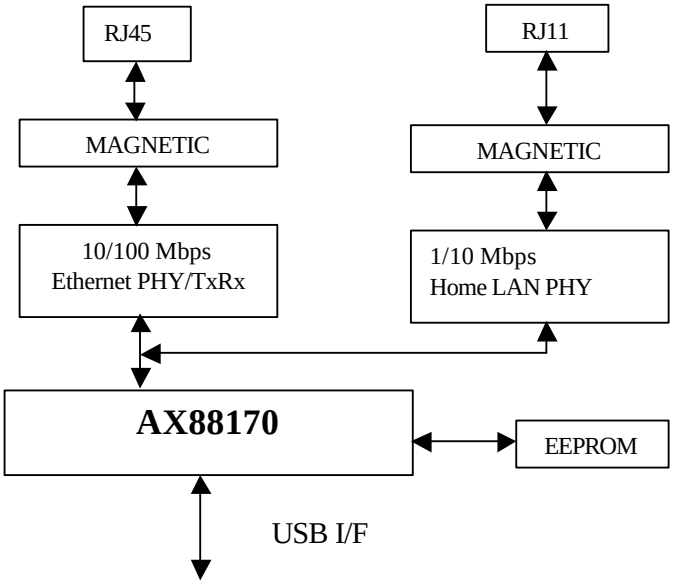
# Appendix A: System Applications

Some typical applications for AX88170 are illustrated bellow.

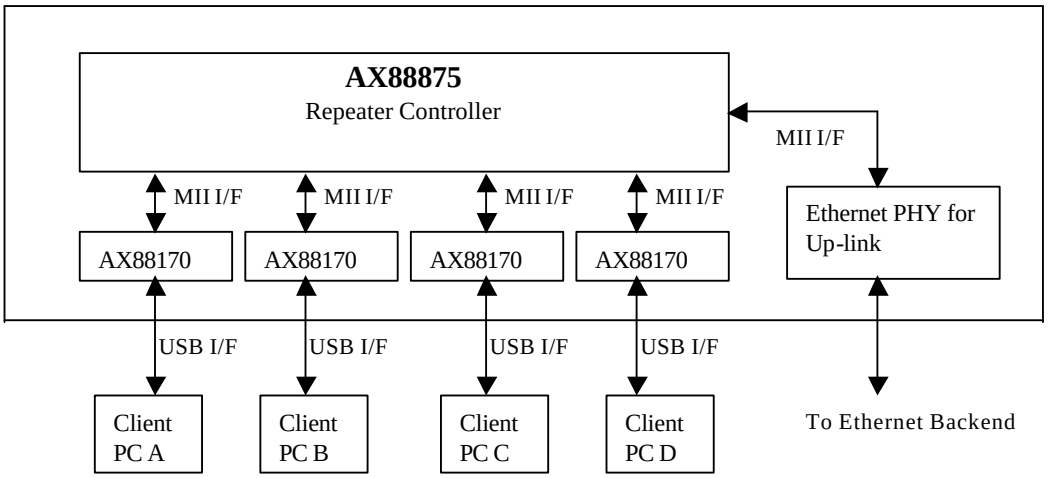
### A.1 USB to Fast Ethernet Converter



### A.2 USB to Fast Ethernet and/or HomeLAN Combo solution

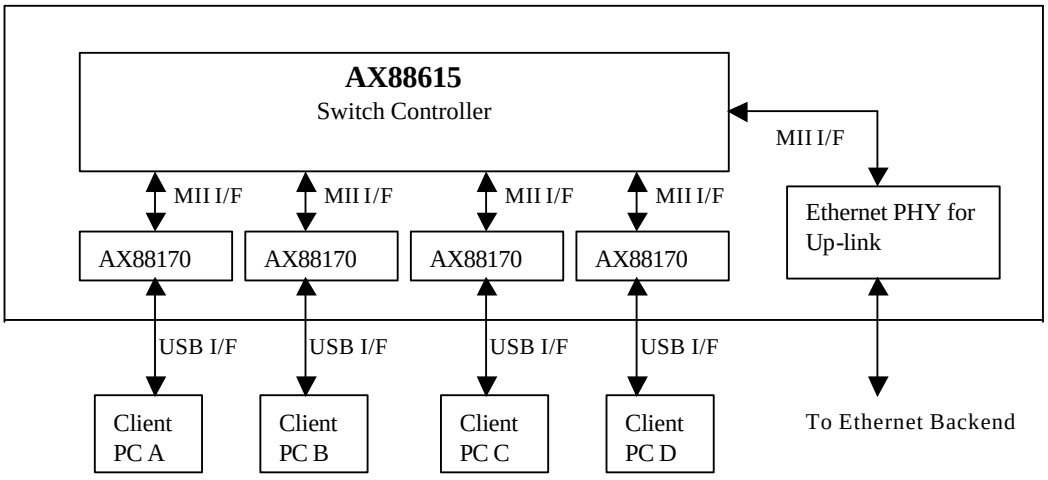


### A.3 USB-to-USB or USB-to-Ethernet Bridge through Ethernet Repeater Controller

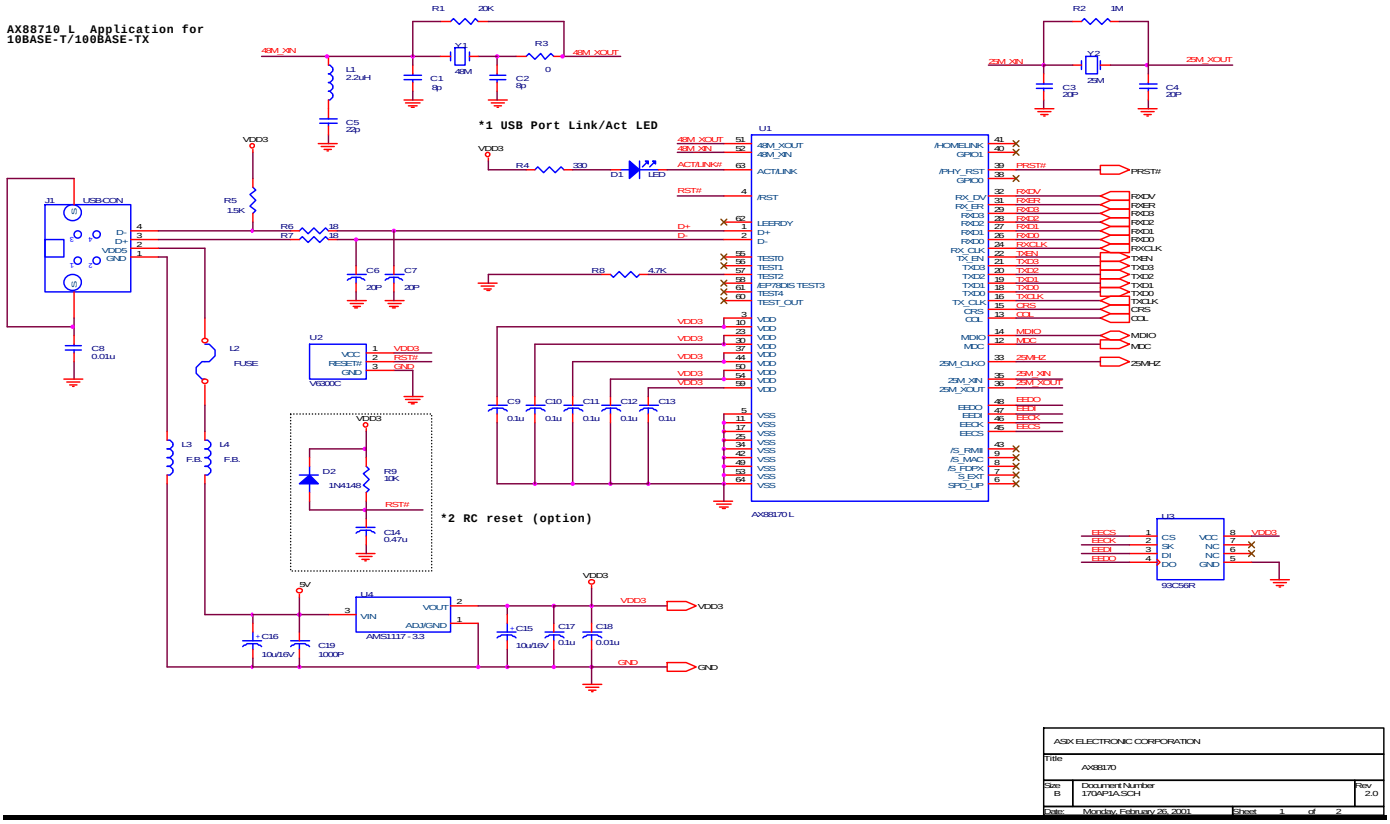


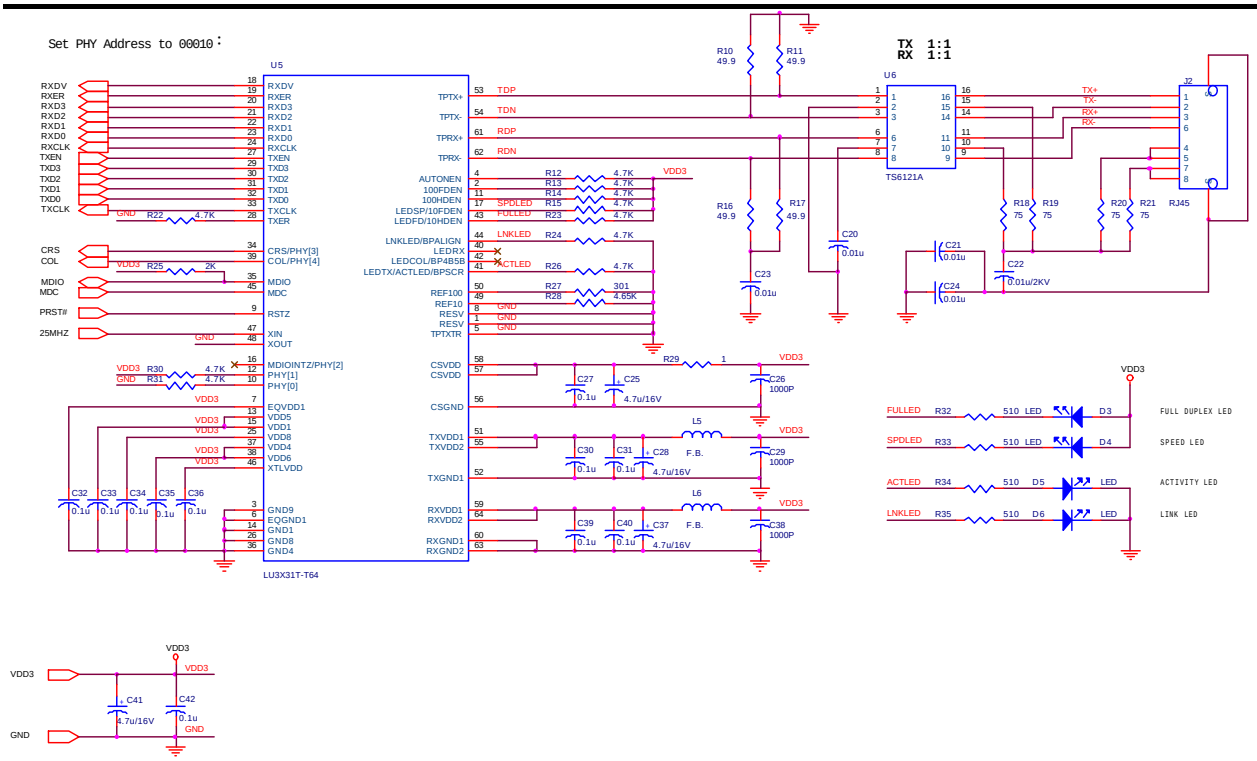

Note : Using AX88871 for 8-port or less then 8-port solutions.

### A.4 USB-to-USB or USB-to-Ethernet Bridge through Ethernet Switch Controller



## Demonstration Circuit A: AX88170 + Ethernet PHY









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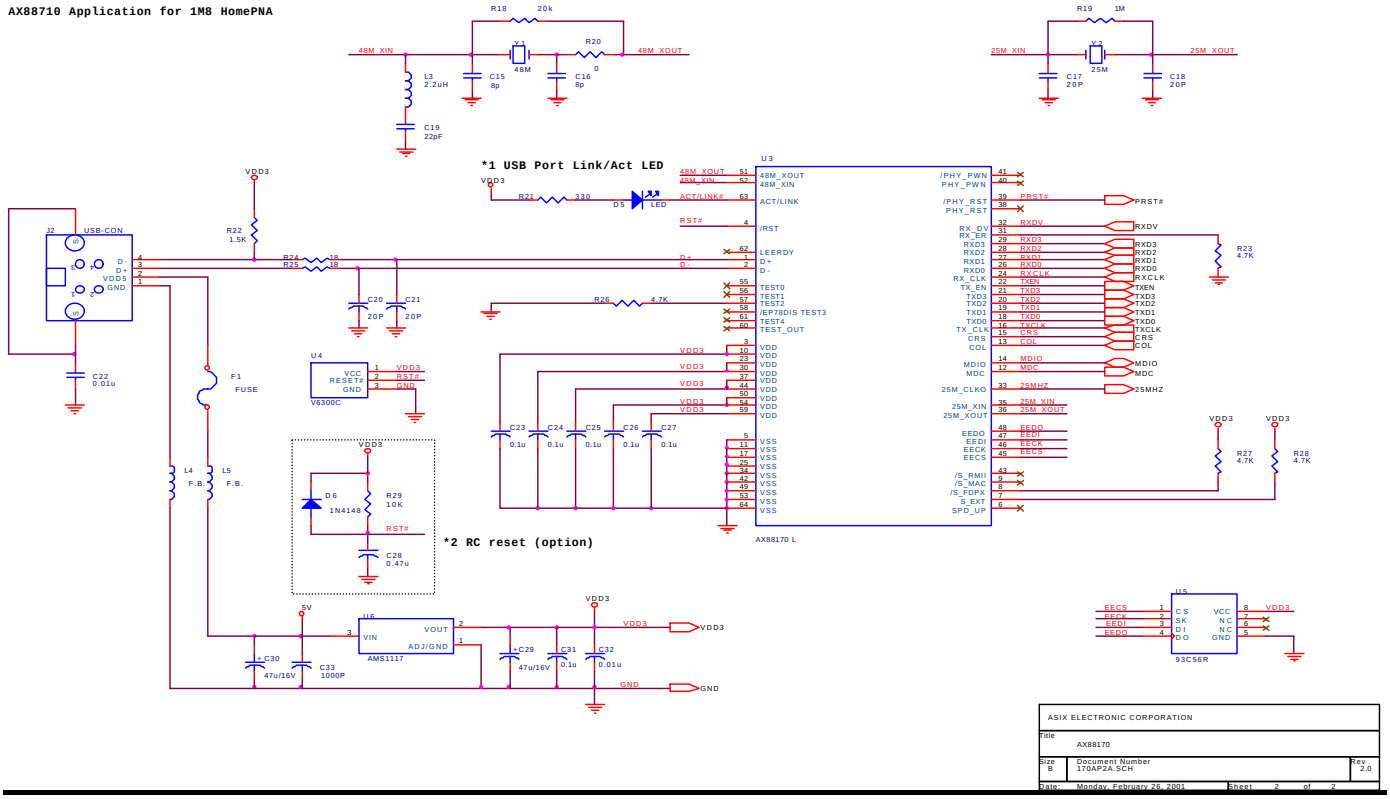
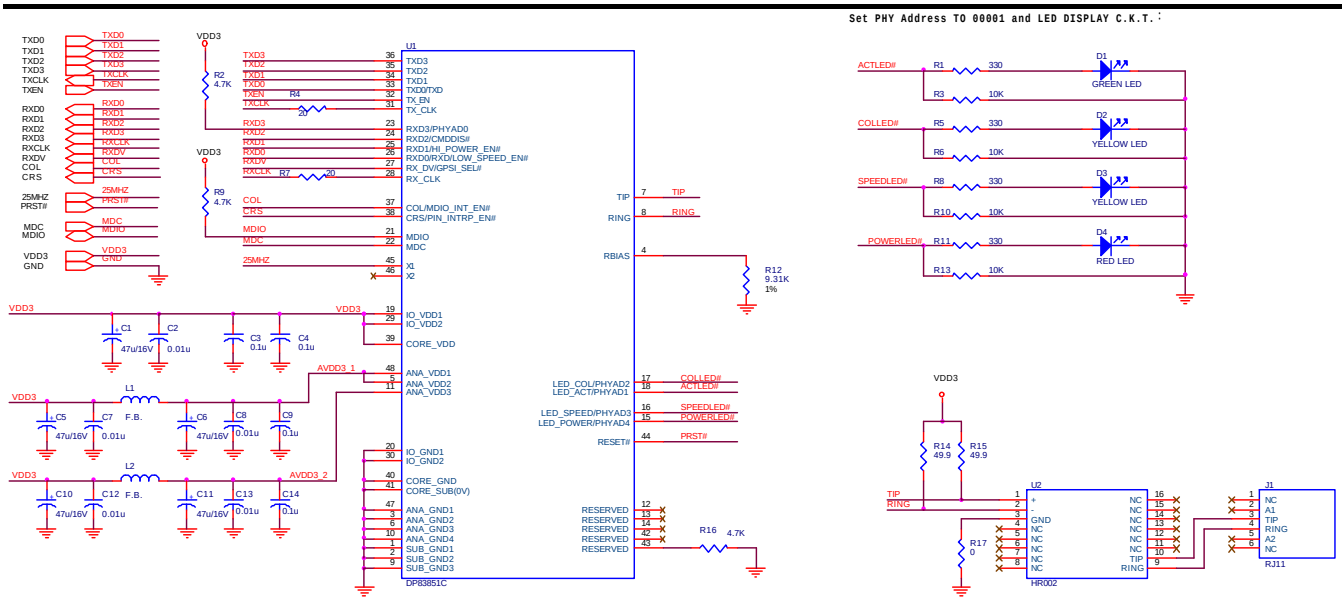
| ASIX ELECTRONIC CORPORATION | | |
| Title: LU3X31 | | |
| Size: B | Document Number: 170AP1A1.SCH | Rev: 2.0 |
| Date: Monday, February 26, 2001 | Sheet 2 of 2 | |

## Demonstration Circuit B: AX88170 + HomePNA 1M8 PHY



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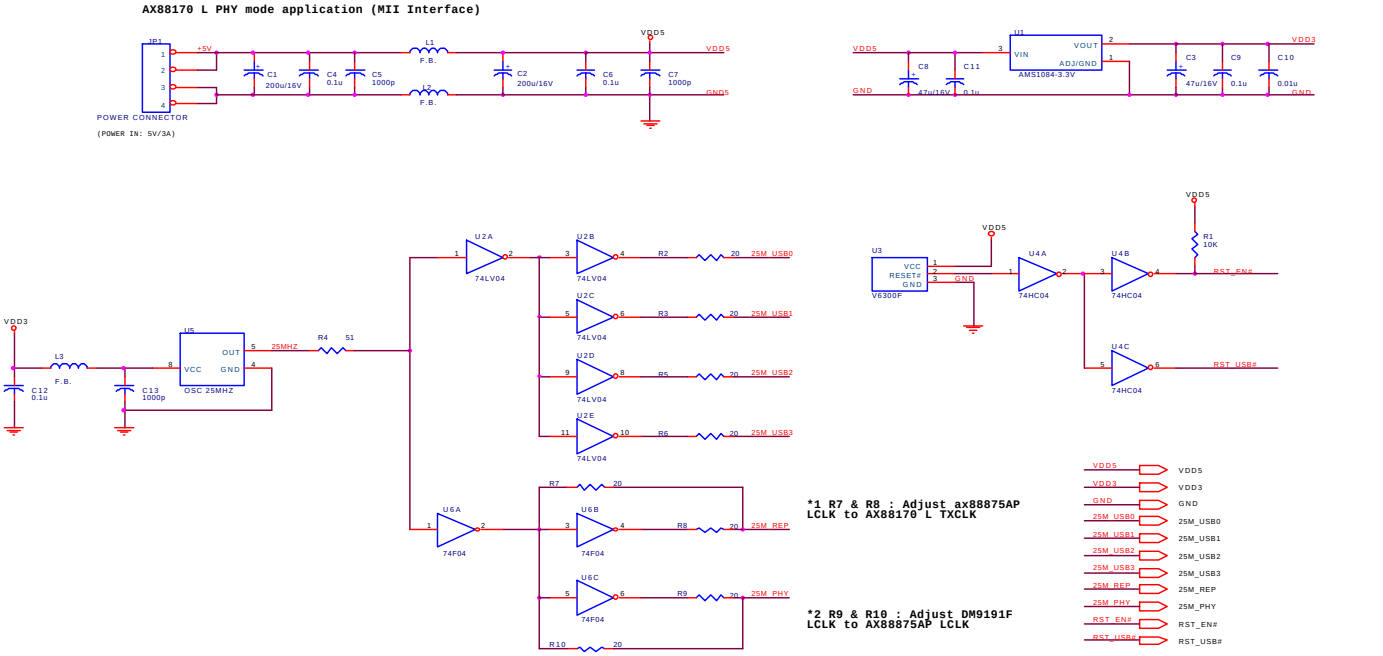
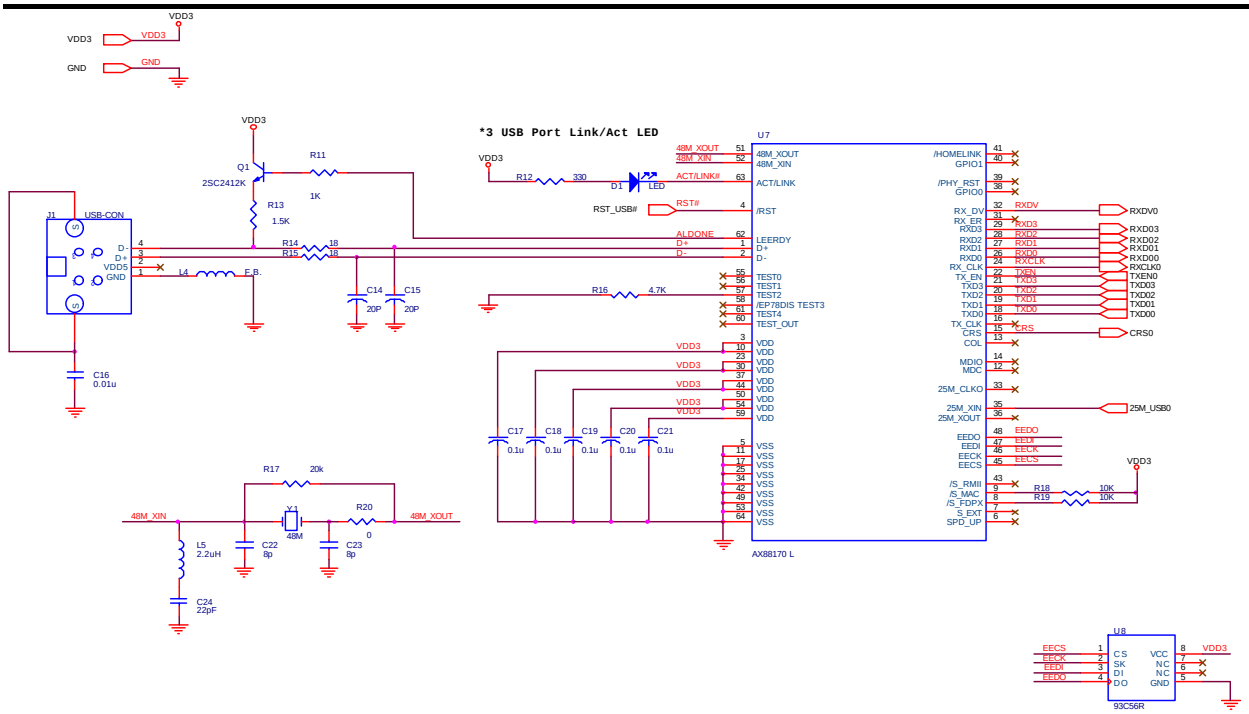
| Title | HOMENET PHY C.K.T. | |
| Size B | Document Number 170AP2A1.SCH | Rev 2.0 |
| Date: Monday, February 26, 2001 | Sheet 1 of 2 | |

## Demonstration Circuit C: 4 USB Ports + 1 Ethernet Port Bridge AP



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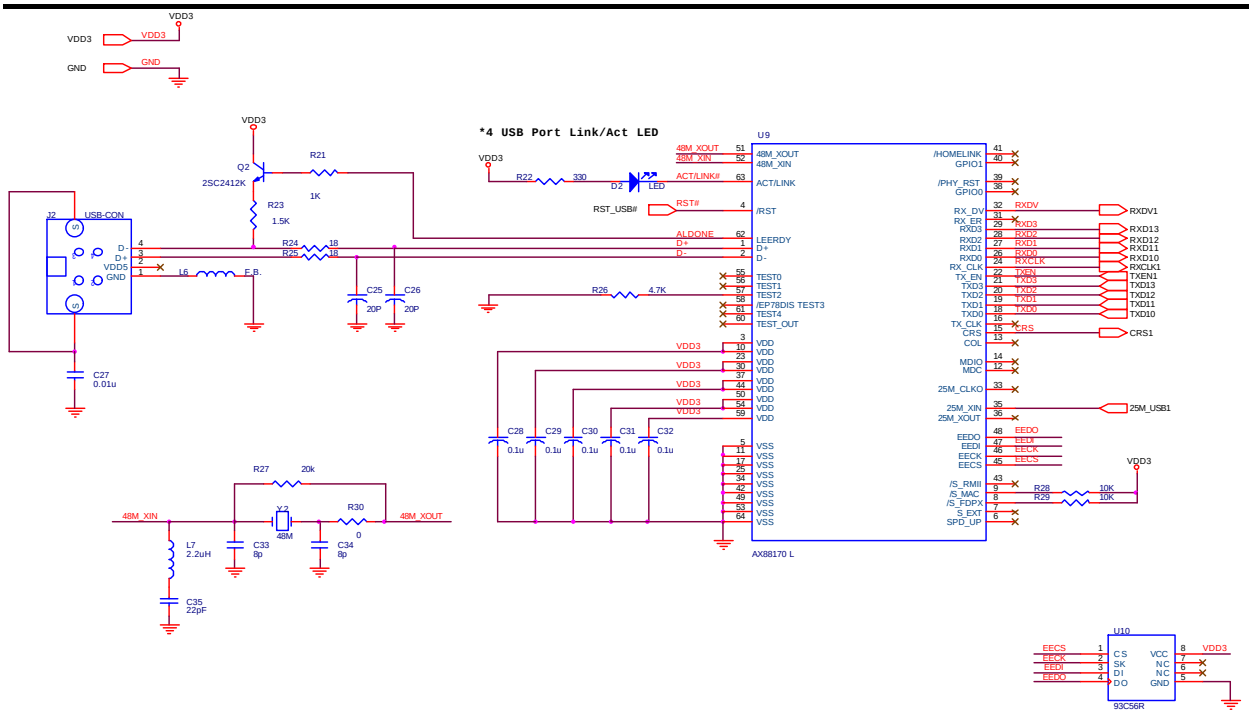
| Size: B | Document Number: 170APSA1.SCH | Rev: 2.0 |
| Date: Monday, February 26, 2001 | Sheet 2 of 7 | |

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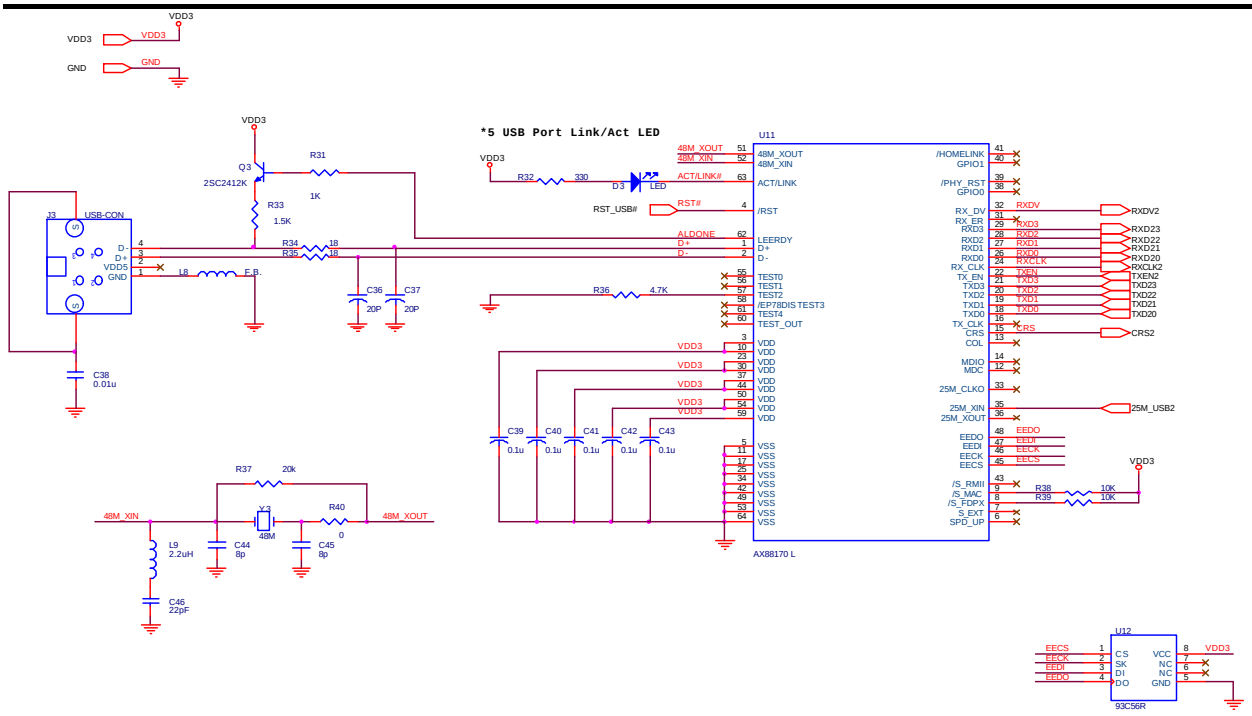
| Title: AX88170 CIRCUIT 2 | | |
| Size: B | Document Number: 170APSA2.SCH | Rev: 2.0 |
| Date: Monday, February 26, 2001 | Sheet 3 of 7 | |

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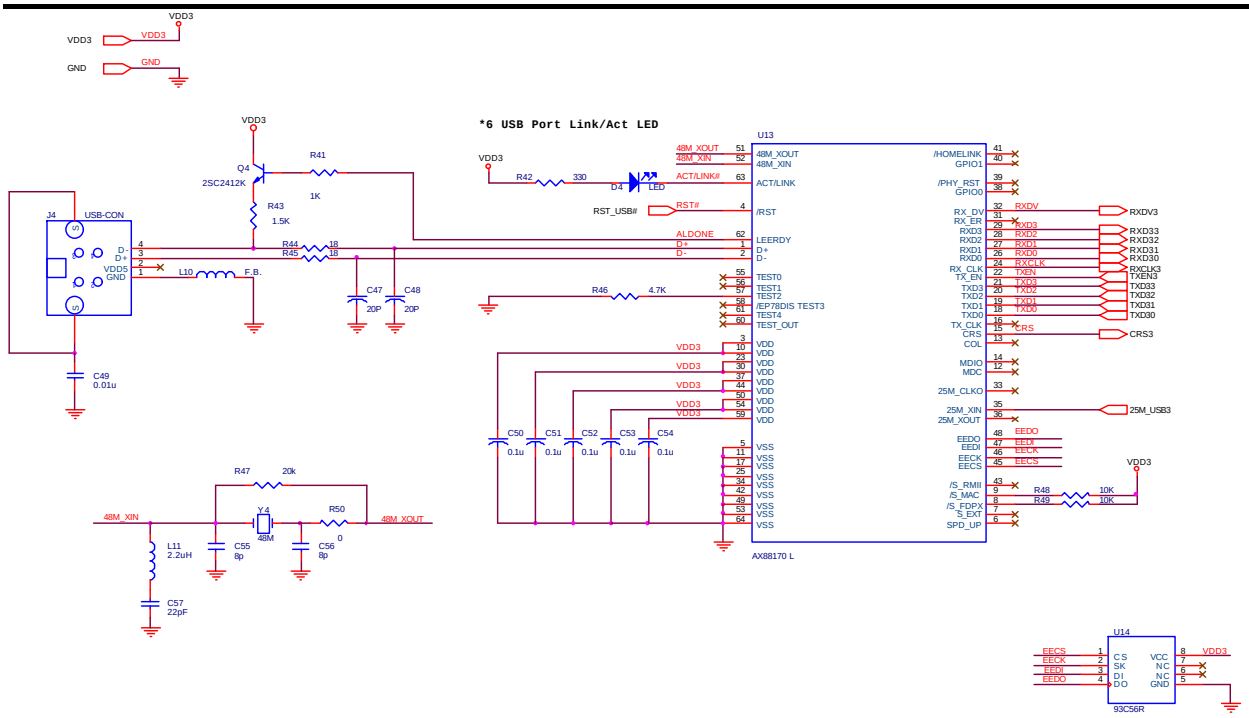


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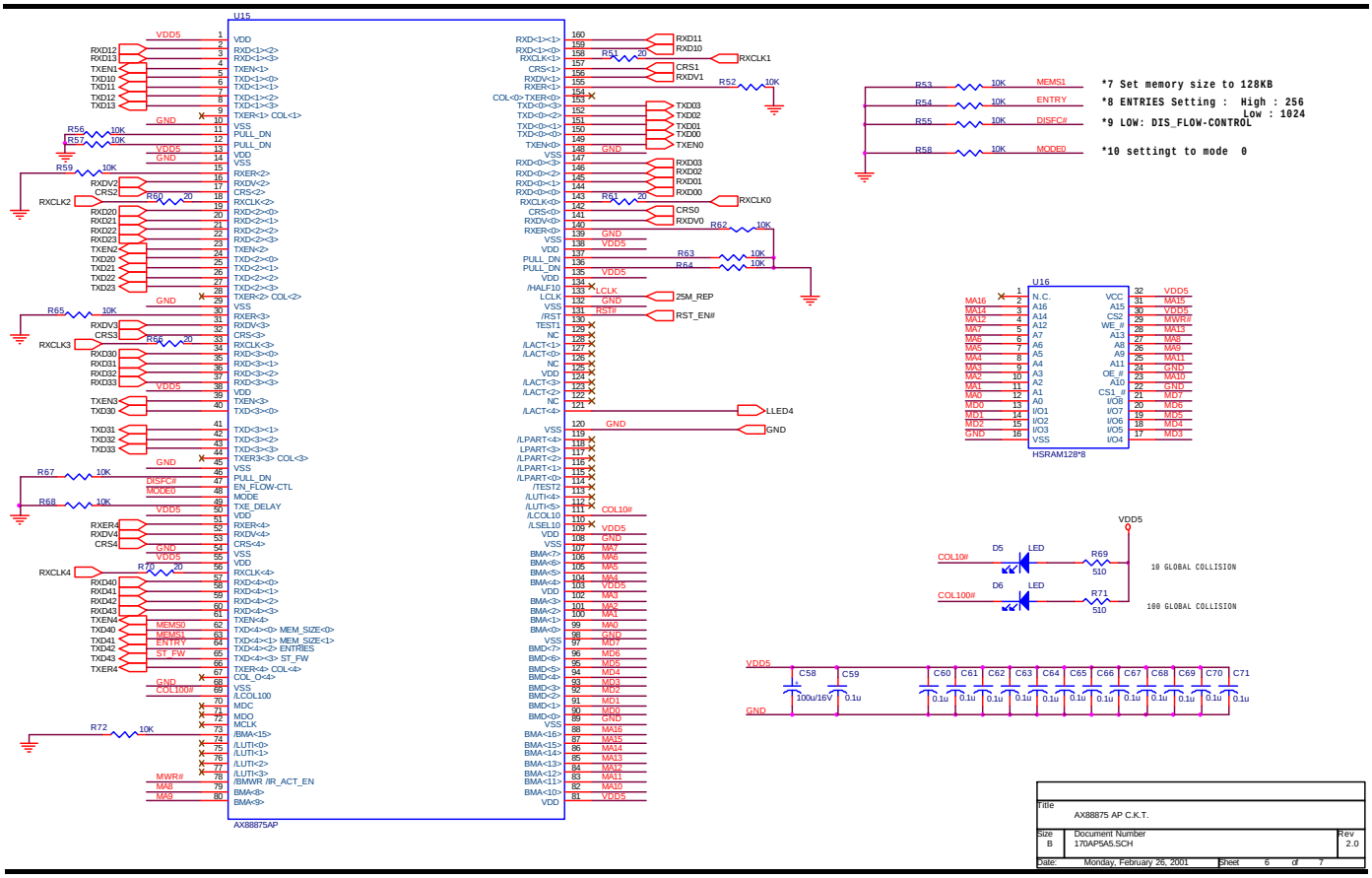
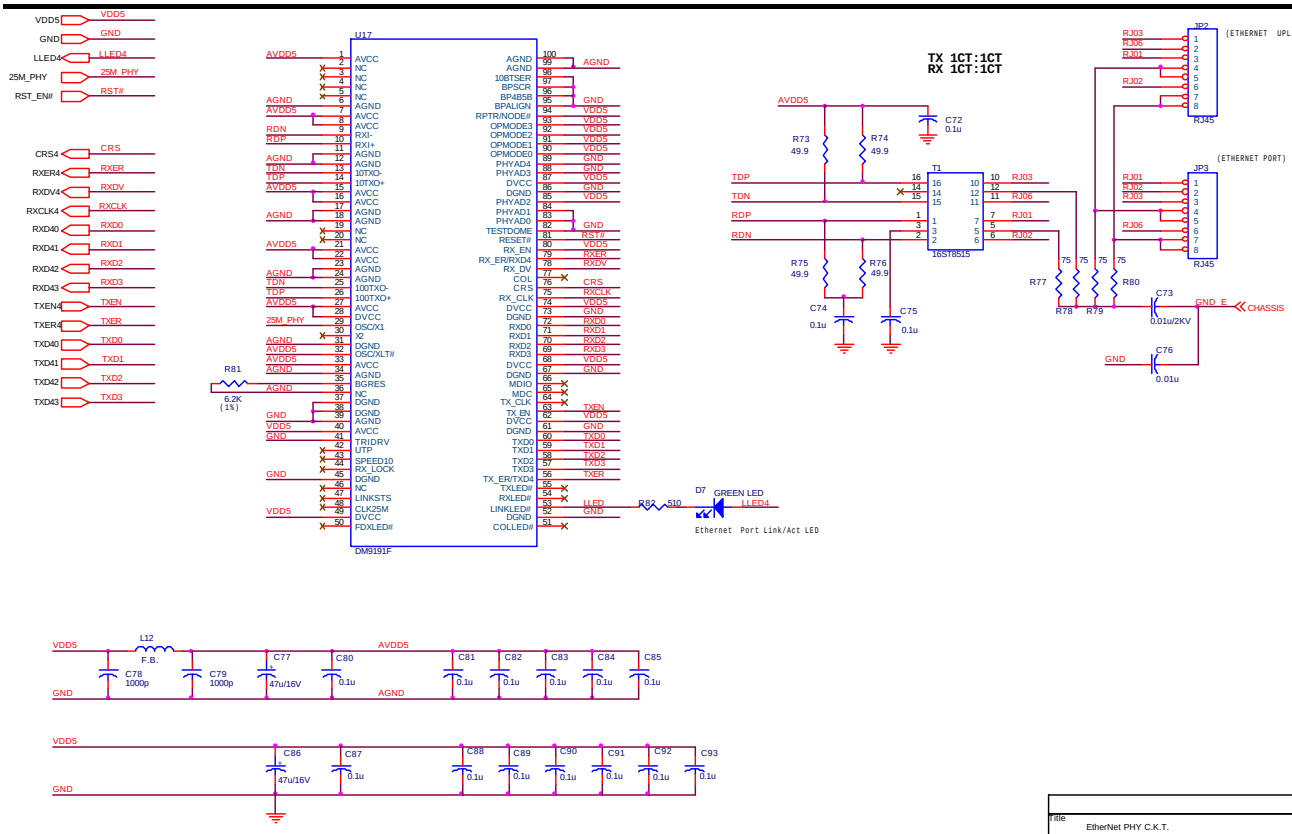
| Date: Monday, February 26, 2001 | Sheet 5 of 7 | |



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| Rev | 2.0 |
| Date: | Monday, February 26, 2001 |
| Sheet | 7 of 7 |