16M bit Synchronous Dynamic RAM
524,288-word × 16-bit × 2-bank
2,048 Refresh

P/N: MN4SV17160BT-80
MN4SV17160BT-90
MN4SV17160BT-10

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524,288-word × 16bit × 2-bank synchronous dynamic RAM

■ Description

The MN4SV17160BT is 16,777,216-bit CMOS synchronous dynamic random access memory, organized as 524,288-word × 16-bit × 2-bank.

With advanced CMOS process technology and circuit configuration, high-speed data transfer and low power dissipation have been realized.

With high-frequency operation with wide data I/O bus, MN4SV17160BT is suitable for multimedia applications.

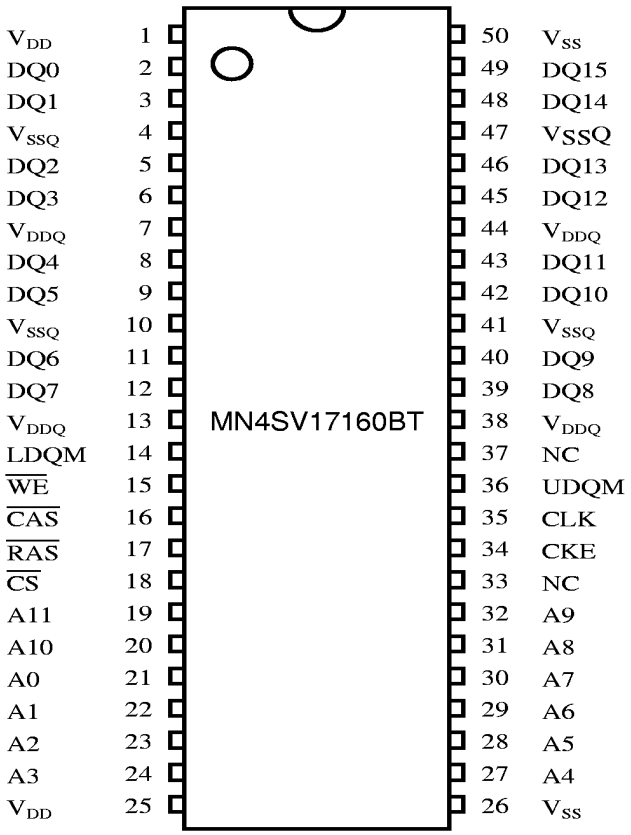
■ Features

Part Number	Organization (word × bit × bank)	Clock Frequency (Max.)	Package
MN4SV17160BT-80	524,288 × 16 × 2	125MHz	50 pin Plastic TSOP (II) (400mil)
-90		111MHz	
-10		100MHz	

- Single power supply : + 3.3V ± 0.3V
- Interface : LVTTL compatible
- Refresh Cycle : 2,048 refresh cycles / 32 ms
- All Input and Output signals refer to rising edge of the clock (CLK) input
- Dual Internal banks can be controlled by A11 (Bank Select)
- CAS Latency : 2, 3
- Programmable Burst Length : 1, 2, 4, 8, full page (256)
- Wrap sequence : Sequential, Interleave
- Burst Read & Burst Write, Burst Read & Single Write
- Auto Precharge and All Banks Precharge can be controlled by A10 (Precharge Control)
- Byte data can be controlled by LDQM and UDQM
- Two variations of refresh : CBR (Auto) refresh, Self Refresh
- DQ suspend and Power Down mode can be controlled by CKE (Clock Enable)

■ Pin Assignment

(524,288 × 16 × 2)

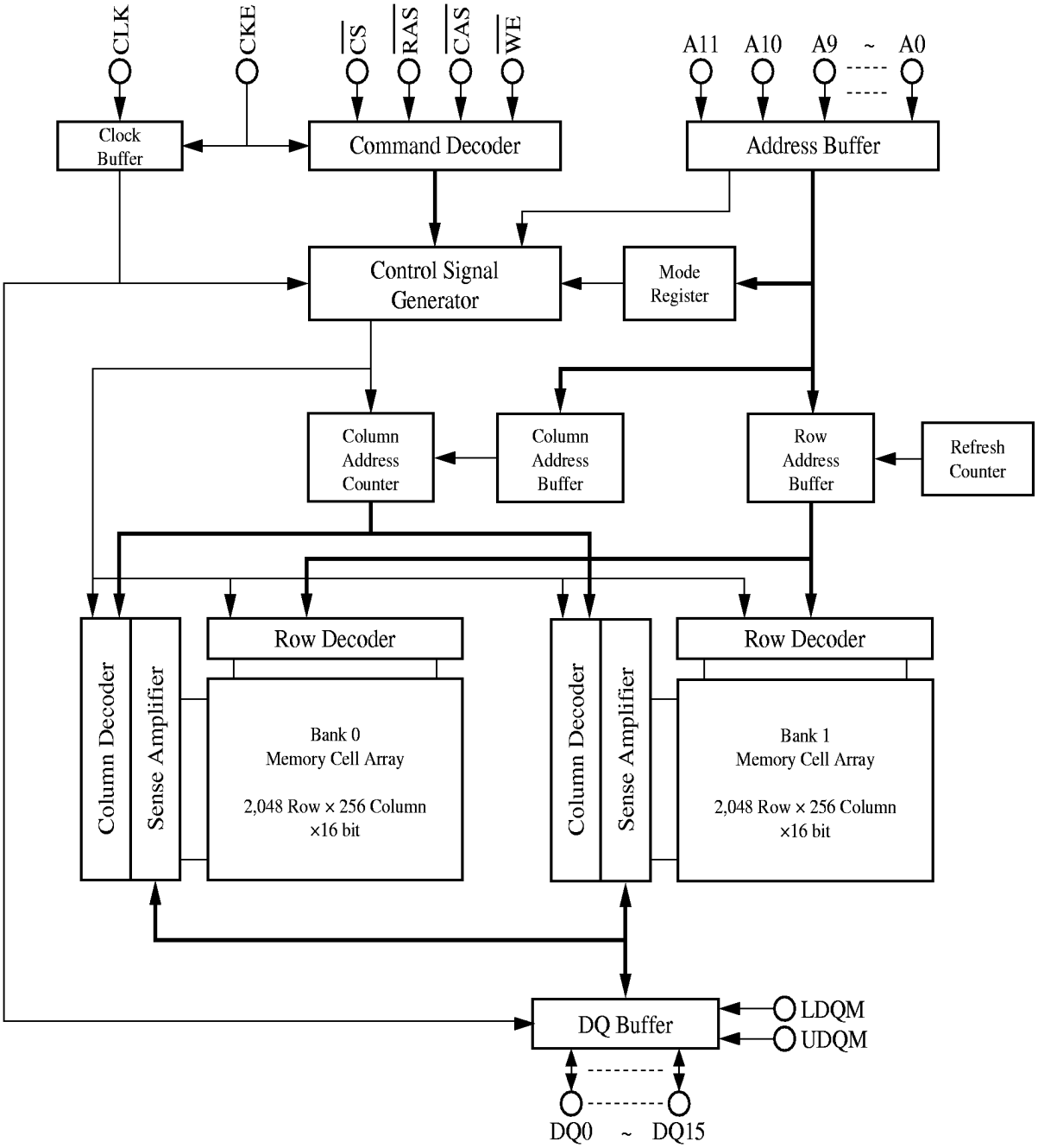


(Top View)

■ Pin Names

Name	Function	Name	Function
A0~11	Address Inputs A0 ~ 10 : Row Address Inputs A0 ~ 7 : Column Address Inputs A11 : Bank Select	$\overline{WE}$	Write Enable
		UDQM	Upper Byte DQ Mask
		LDQM	Lower Byte DQ Mask
DQ0~15	Data Inputs / Outputs	V_{DD}	Supply Voltage (+3.3V)
CLK	Clock Input	V_{SS}	Ground (0V)
CKE	Clock Enable	V_{DDQ}	Supply Voltage for DQ (+3.3V)
$\overline{CS}$	Chip Select	V_{SSQ}	Ground for DQ (0V)
$\overline{RAS}$	Row Address Strobe	NC	No Connection
$\overline{CAS}$	Column Address Strobe		

■ Block Diagram



■ Pin Functions

●Clock Input : CLK (Input pin)

CLK is the reference clock for SDRAM operations.

All Inputs and Outputs are synchronized to the rising edge of CLK.

●Chip Select Input : $\overline{CS}$ (Input pin)

$\overline{CS}$ enables all command inputs defined by $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and address inputs. When $\overline{CS}$ is high level, all input commands are ignored, but operations started at previous cycles are continued.

●Row Address Strobe : $\overline{RAS}$ (Input pin)

Column Address Strobe : $\overline{CAS}$ (Input pin)

Write Enable : $\overline{WE}$ (Input pin)

Operation commands are defined by the levels of these pins.

$\overline{RAS}$ signal is related to the commands of Bank Active, Bank Precharge, Refresh and Mode Register Set.

$\overline{CAS}$ signal is related to the commands of Read, Write, Refresh and Mode Register Set.

$\overline{WE}$ signal is related to the commands of Write, Bank Precharge, ModeRegister Set.

Details are described in command operation section.

●Address Inputs : A0~A10 (Input pin)

The memory cell to be accessed is pointed by Row and Column addresses. Row address is determined by A0 ~ A10 at Bank Active command cycle. Column address is determined by A0 ~ A7 at Read or Write command cycles.

	Row Address	Column Address
MN4SV17160BT	A0 ~A10	A0 ~A7

A0 ~ A9 inputs are latched as set data of the internal mode register at Mode Register Set cycle.

Also, A10 input controls the Precharge operation. When A10 is high at Precharge Bank command cycle, All Banks Precharge is performed (Precharge All Banks Command). When A10 is high at Read/Write command cycles, Auto Precharge is performed after Read/Write operation (Read with Auto Precharge/ Write with Auto Precharge).

●Bank Select : A11 (Input pin)

A11 input selects the bank for operation. If A11 is "low", bank 0 is selected, and if A11 is "high", bank 1 is selected.

● Clock Enable : CKE (Input pin)

CKE enables the internal clock. If CKE is "high", CLK of next cycle is validated. If CKE is "low", CLK of next cycle is invalidated and Burst Read/Write is suspended or the Self Refresh mode is activated or the Power Down mode is activated.

● Upper Byte DQ Mask : UDQM (Input pin)
Lower Byte DQ Mask : LDQM (Input pin)

UDQM and LDQM mask the upper byte (DQ8 ~ DQ15) and lower byte (DQ0 - DQ7) of DQ data respectively.
In Read command cycle, outputs set to high-impedance at two cycles after asserting (U/L)DQM.
In Write command cycle, input data on the DQ pins are masked at the same cycle of asserting (U/L)DQM.

● Data Input/Output : DQ0 ~ DQ15 (Input/Output pin)

Data Inputs/Outputs through the DQ0 ~ DQ15 pins are synchronized with the rising edges of CLK .

● Power Supply : V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} (Power supply pin)

+3.3V is supplied by V_{DD} and V_{DDQ} pins. V_{DD} is the power supply or internal circuit, and V_{DDQ} is power supply for output buffer.

Ground level is supplied by V_{SS} and V_{SSQ} pins. V_{SS} is the ground for internal circuit, and V_{SSQ} is ground for output buffer.

■ Command Operation

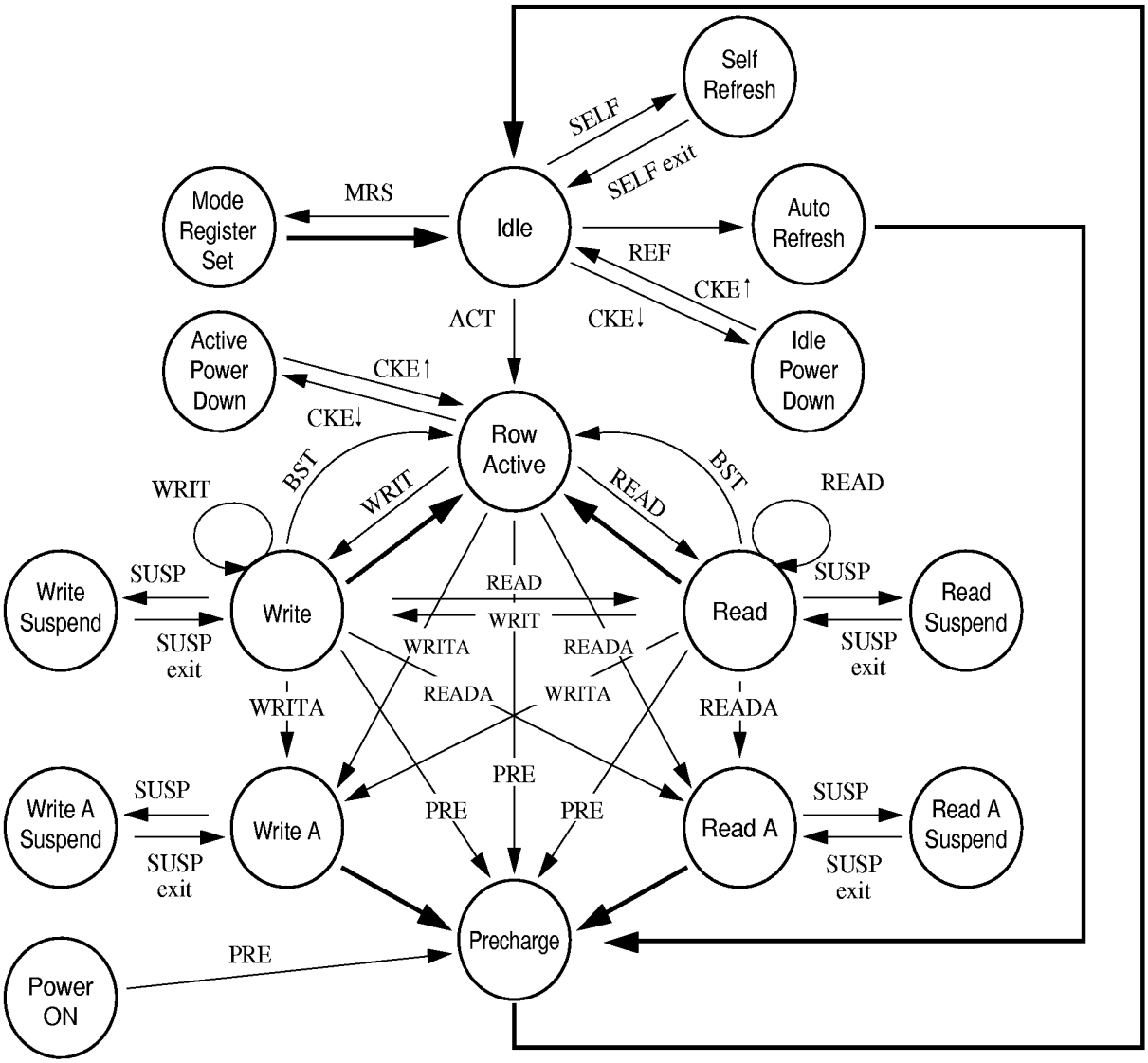
All operations are performed by the command inputs at the rising edge of CLK.
Commands are set by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Command Truth Table

Command	Current State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9~0	Symbol
		n-1	n								
Device Deselect	ANY	H	×	H	×	×	×	×	×	×	DESL
No Operation	ANY	H	×	L	H	H	H	×	×	×	NOP
Burst Stop	READ, WRITE	H	×	L	H	H	L	×	×	×	BST
Read	ACTIVE	H	×	L	H	L	H	BS	L	Col.	READ
Read with Auto Precharge	ACTIVE	H	×	L	H	L	H	BS	H	Col.	READA
Write	ACTIVE	H	×	L	H	L	L	BS	L	Col.	WRIT
Write with Auto Precharge	ACTIVE	H	×	L	H	L	L	BS	H	Col.	WRITA
Bank Active	IDLE	H	×	L	L	H	H	BS	Row Address (1)		ACT
Precharge Select Bank	ANY	H	×	L	L	H	L	BS	L	×	PRE
Precharge All Banks	ANY	H	×	L	L	H	L	×	H	×	PALL
Mode Register Set (3)	IDLE	H	×	L	L	L	L	OP. CODE (2)			MRS
CBR Refresh (3)	IDLE	H	H	L	L	L	H	×	×	×	REF
Self Refresh Entry (3)	IDLE	H	L	L	L	L	H	×	×	×	SELF
Self Refresh Exit	Self Ref.	L	H	L	H	H	H	×	×	×	
				H	×	×	×	×	×	×	
Clock Suspend Mode Entry	READ, WRITE	H	L	×	×	×	×	×	×	×	SUSP
Clock Suspend Mode Exit	Suspend	L	H	×	×	×	×	×	×	×	
Power Down Mode Entry	IDLE, ACTIVE	H	L	L	H	H	H	×	×	×	
				H	×	×	×	×	×	×	
Power Down Mode Exit	Power Down	L	H	L	H	H	H	×	×	×	
				H	×	×	×	×	×	×	

H: High level , L: Low level , ×: Don't care , BS: Bank select address , Col.: Column address
(1) Row address input. (2) Operation code input. (3) Valid when all banks are idle state.

■ State Diagram



Transit with command input

Automatic transition after command completion

Note: After the auto-refresh is performed, precharge is performed automatically, and transit to idle state.

■ Command Functions

● Device Deselect [DESL]

($\overline{CS}$ = "H")

Any inputs are ignored. The device keeps previous internal state.

● No Operation [NOP]

($\overline{CS}$ = "L", $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = "H")

No internal operation is performed by this command. The device keeps previous internal state.

● Burst Stop [BST]

($\overline{CS}$ = "L", $\overline{RAS}$, $\overline{CAS}$ = "H", $\overline{WE}$ = "L")

Burst Read/Write operation is stopped by this command. If Burst Length is full page, data Inputs/ Outputs don't stop without this command or Precharge [PRE] command.

● Read [READ]

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", A11 ="Bank Select", A10 ="L", A7 ~ A0 ="Column Address")

Burst Read operation starts with this command. Internal bank and column address are selected by A11 and A7 ~ A0 respectively. Latency from this command input to first Read data output is defined by CAS Latency which is set at Mode Register Set cycle. Burst output length are defined by Burst Length which is set at Mode Register Set cycle. Output turns high-impedance after this operation.

A9 ~ A8 inputs are "don't care" at MN4SV17160BT series.

● Read with Auto Precharge [READA]

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", A11 ="Bank Select", A10 ="H", A7 ~ A0 ="Column Address")

If A10 is "high" at READ command, the bank selected by A11 is precharged automatically after internal Read operation is finished. But, this command is not allowed for full page Burst Read operation.

A9 ~ A8 inputs are "don't care" at MN4SV17160BT series.

● Write [WRIT]

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$, $\overline{WE}$ ="L", A11 ="Bank Select", A10 ="L", A7 ~ A0 ="Column Address")

Burst Write operation starts with this command. Internal bank and column address are selected by A11 and A7 ~ A0 respectively. Burst data input length are defined by Burst Length which is set at Mode Register Set cycle.

A9 ~ A8 inputs are "don't care" at MN4SV17160BT series.

● Write with Auto Precharge [WRITA]

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$, $\overline{WE}$ ="L", A11 ="Bank Select", A10 ="H", A7 ~ A0 ="Column Address")

If A10 is "high" at WRIT command, the bank selected by A11 is precharged automatically after internal Write operation is finished. But, this command is not allowed for full page Burst Write operation.

A9 ~ A8 inputs are "don't care" at MN4SV17160BT series.

● Bank Active [ACT]

($\overline{CS}$, $\overline{RAS}$ ="L", $\overline{CAS}$, $\overline{WE}$ ="H", A11 ="Bank Select", A10 ~ A0 ="Row Address")

This command activates the internal bank selected by A11 and the row address selected by A0 ~ A10. If A11 is "low", bank 0 is selected, and if A11 is "high", bank 1 is selected.

● Precharge Select Bank [PRE]

($\overline{CS}$, $\overline{RAS}$ ="L", $\overline{CAS}$ ="H", $\overline{WE}$ ="L", A11 ="Bank Select", A10 ="L")

The internal bank selected by A11 is precharged by this command. After Precharge operation is performed, the selected bank turns to be idle state automatically. If A11 is "low", bank 0 is selected, and if A11 is "high", bank 1 is selected.

● Precharge All Banks [PALL]

($\overline{CS}$, $\overline{RAS}$ ="L", $\overline{CAS}$ ="H", $\overline{WE}$ ="L", A10 ="H")

If A10 is "high" at PRE command, all internal banks are precharged. After Precharge operation is performed, all banks turn to be idle state automatically.

● Mode Register Set [MRS]

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ="L", A11 ~ A0 ="Operation Code")

The mode register is set by this command. The data on the A0 ~ A11 pins in this command cycle are set as the operation code. But, A11 ~ A10 inputs are "don't care" at MN4SV17160BT series. After power-on and All Banks Precharge, Mode Register Set command must be executed.

The mode register can be set during device operation, but all banks must be idle state before this command execution.

● CBR (Auto) Refresh [REF]

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ ="L", $\overline{WE}$ ="H")

This command starts CBR (Auto) refresh operation. Row address is generated by internal refresh address counter. The refresh address is incremented by this command input.

MN4SV17160BT series need 2,048 times input of this command to refresh all memory cells.

All internal banks must be idle state before this command input. After refresh operation is performed, precharge operation is performed automatically, then all banks return to idle state. Any next commands cannot input during t_{RC} period after this command execution.

● Self Refresh Entry [SELF]

(CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ ="L", $\overline{WE}$ ="H")

Self Refresh operation starts with this command execution. All banks must be idle state before this command execution. Self Refresh operation continues while CKE is low after this command execution, and any commands cannot be accepted. Self Refresh mode is terminated when CKE is high (Self Refresh Exit command).

● Self Refresh Exit

(CKE ="H", $\overline{CS}$ ="L", $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ="H" or CKE, $\overline{CS}$ ="H")

Self Refresh mode is terminated by this command execution. After this command execution, internal state is returned to idle state. Any next commands cannot input during t_{RC} period after this command execution.

●Clock Suspend Mode Entry [SUSP]

(CKE ="L")

When CKE is negated (CKE is set to "low"), internal clock is suspended from next CLK rising.

If CKE is negated during Read/Write operation, internal state entries Clock Suspend mode.The variety of Clock Suspend mode depends on the state of previous cycle as follows.

[Previous cycle]	[Clock Suspend Mode]
READ	READ Suspend
READA	READA Suspend
WRIT	WRIT Suspend
WRITA	WRITA Suspend

• READ Suspend / READA Suspend

If CKE is negated during READ/READA mode, the output of next cycle is suspended. And it is continued until the next cycle of asserting CKE (Clock Suspend Mode Exit).
Internal state and Read address don't change.

• WRIT Suspend / WRITA Suspend

If CKE is negated during WRIT/WRITA mode, the input of next cycle is not accepted. And it is continued until the next cycle of asserting CKE (Clock Suspend Mode Exit).
Internal state and Write address don't change.

●Clock Suspend Mode Exit

(CKE ="H")

If CKE is asserted (CKE is set to "high") during Clock Suspend mode, internal clock restarts from next CLK rising. And internal state exit Clock Suspend mode.

●Power Down Mode Entry

(CKE, $\overline{CS}$ = "L", $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ="H" or CKE = "L", $\overline{CS}$ = "H")

If CKE is negated (CKE is set to "low") when no READ/READA or WRIT/WRITA command is in progress, the device enters Power Down mode. The device has two Power Down mode for the state of device when Power Down mode is entered.

[Previous cycle]	[Power Down Mode]
Idle	Idle Power Down
Row Active	Active Power Down

• Idle Power Down

If CKE is negated during Idle mode, the input buffers are disabled of next cycle and power consumption is reduced to the minimum.

• Active Power Down

If CKE is negated during active mode, the input buffers are disabled of next cycle and power consumption is reduced.

●Power Down Mode Exit

(CKE = "H", $\overline{CS}$ = "L", $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ="H" or CKE, $\overline{CS}$ = "H")

If CKE is asserted (CKE is set to "high") during Power Down mode, internal clock restarts from CLK rising. And internal state exit Power Down mode.

■ I/O Control

The data of DQ0 ~ DQ7 (lower byte) pins and DQ8 ~ DQ15 (upper byte) pins can be masked by LDQM pin and UDQM pin respectively.

I/O control can be executed with command operations.

DQM Truth Table

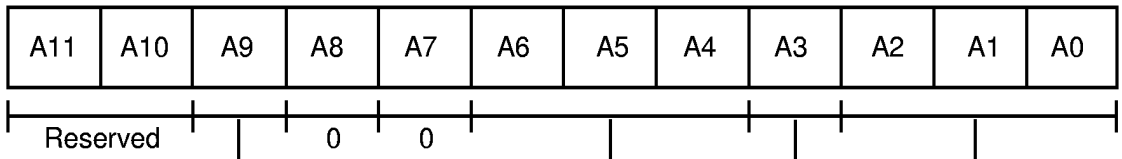
Function	CKE		DQM		Symbol
	n-1	n	U	L	
Upper byte Write Enable / Output Enable	H	×	L	×	ENBU
Lower byte Write Enable / Output Enable	H	×	×	L	ENBL
Upper byte Write Inhibit / Output Disable	H	×	H	×	MASKU
Lower byte Write Inhibit / Output Disable	H	×	×	H	MASKL

H: High level , L: Low level , ×: Don't care

■ Mode Register

The data on the A0 ~ A11 pins in Mode Register Set command cycle are set as the operation code. Mode register consists of following parts.

- A2, A1, A0 : BL (Burst Length)
  Burst Length = 1, 2, 4, 8, full page
  (Full page length : 256 bits)
- A3 : WT (Wrap Type)
  Wrap Type : Sequential, Interleave
- A6, A5, A4 : CL (CAS Latency)
  CAS Latency = 2, 3
- A9 : Read/Write mode
  Burst Read and Burst Write, Burst Read and Single Write



A9	Single Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

A3	Wrap Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	
1	1	0	
1	1	1	

A2	A1	A0	Burst Lemgth
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	
1	1	0	
1	1	1	Full Page

■ Burst Length and Wrap Type

● BL =2

Starting Address (Column Address A0,binary)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
0	0,1	0,1
1	1,0	1,0

● BL =4

Starting Address (Column Address A1~A0,binary)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
00	0,1,2,3	0,1,2,3
01	1,2,3,0	1,0,3,2
10	2,3,0,1	2,3,0,1
11	3,0,1,2	3,2,1,0

● BL =8

Starting Address (Column Address A2~A0,binary)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

● BL =Full Page

Only Sequential Addressing is executed. Burst Read/Write operation continues until Burst Stop command or Precharge command input. And the address of Input/Output data return to first access address if full page data access is completed.

Full page data length = 256 bits

■ Command Operations

[Read command (READ)]

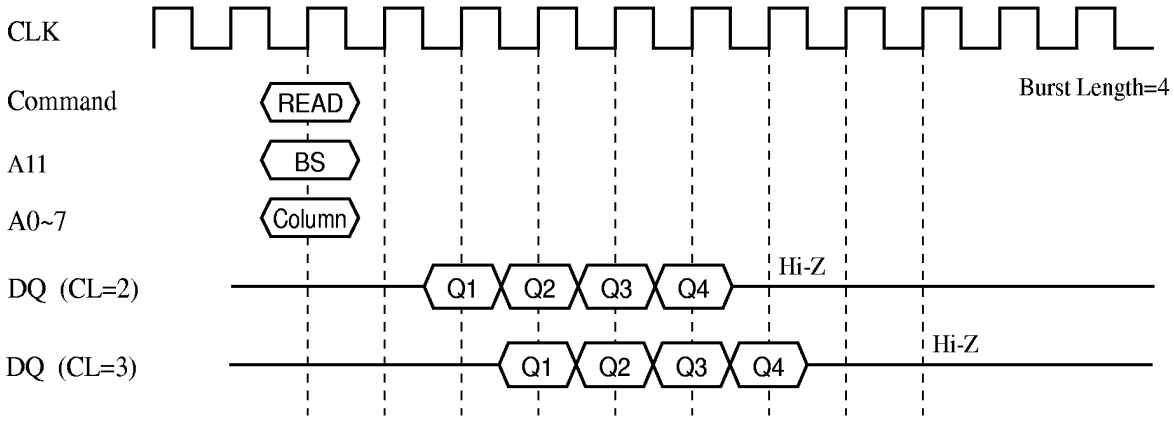
Bank and first column address are selected by A11 and A0 ~ A7 respectively. Latency from this command input to first Read data output is defined by CAS Latency which is set at Mode Register Set cycle. Burst output length is defined by the Burst Length which is set at Mode Register Set cycle. Output turns high-impedance after this operation.

Following operation mode can be programmed in Mode Register Set command cycle.

Burst Length = 1, 2, 4, 8, full page (256)

When Burst Length is full page, only Sequential Addressing is executed. Burst Read/Write operation continues until Burst Stop command or Precharge command input. And the address of Input/Output data return to the first access address if full page data access is completed.

< Burst Read (READ) >



[Write command (WRIT)]

If you selected A9 = 0 at the Mode Register Set command cycle, Write mode is Burst Write mode. If you selected A9 = 1, Write mode is Single Write mode. (Read mode is Burst Read mode in both case.)

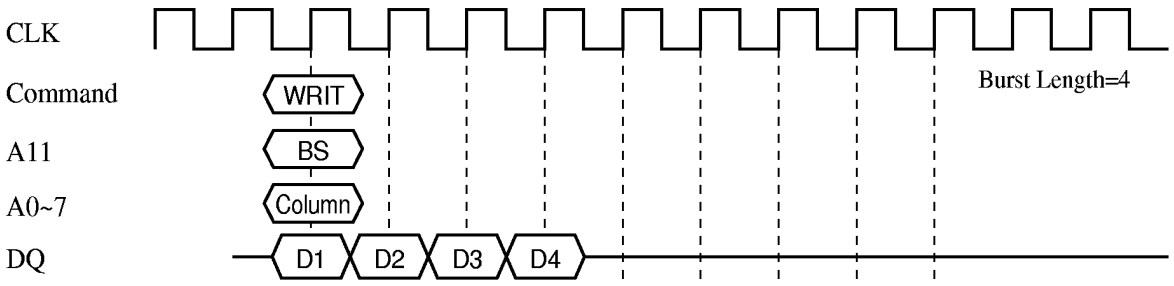
1. Burst Write Mode

Bank and first column address are selected by A11 and A0 ~ A7 respectively. Latency from Write command input to first Write data input is zero.

Burst Write data input length are defined by the Burst Length which is set in the mode register. Following operation mode can be programmed in Mode Register Set command cycle.

Burst Length = 1, 2, 4, 8, full page (256)

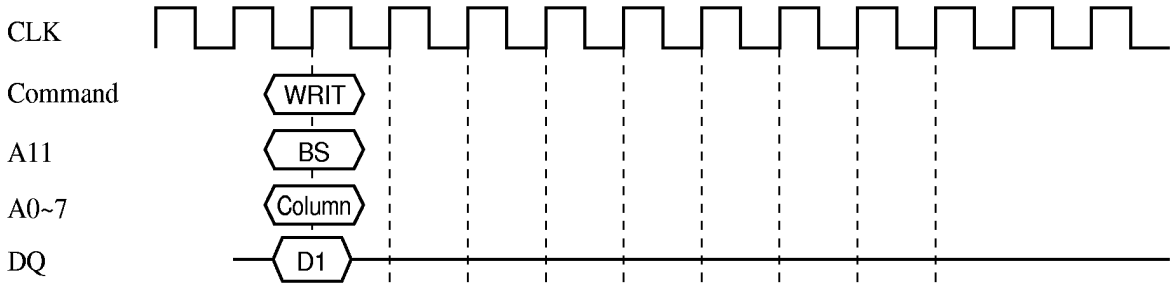
< Burst Write (WRIT) >



2. Single Write Mode

Bank and first column address are selected by A11 and A0 ~ A7 respectively. Write data is inputted at the only WRIT or WRITA command cycle. So, Write data input length is 1 without reference to the Burst Length in mode resister.

< Single Write (WRIT) >



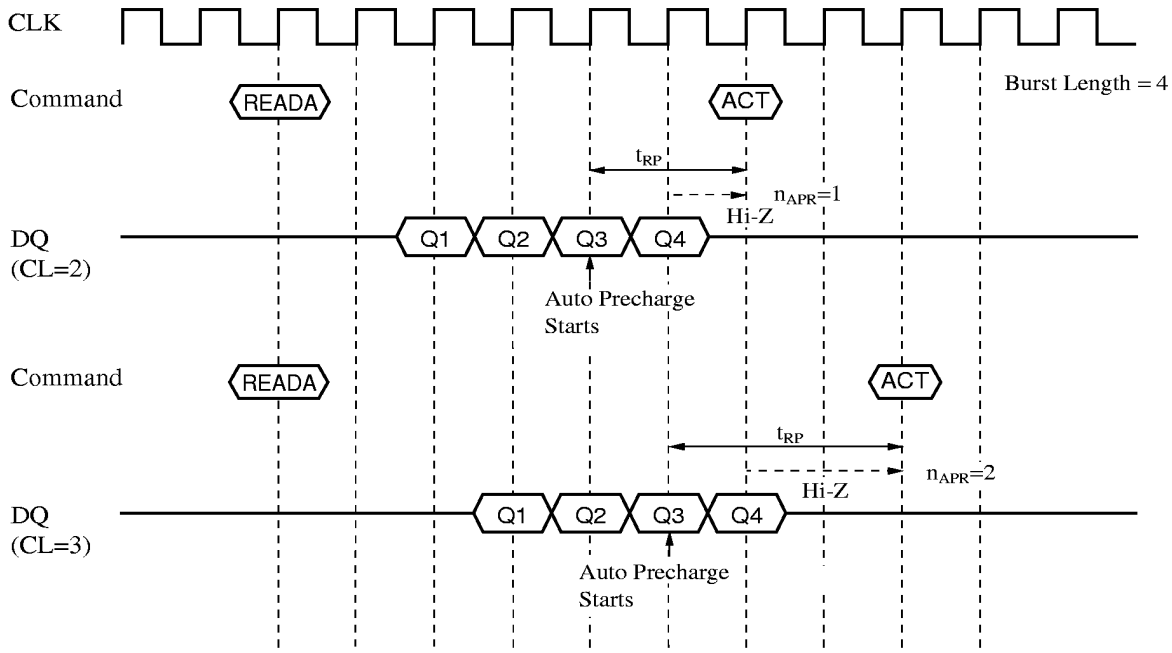
[Auto Precharge command (READA [Read with Auto Precharge] /
WRITA [Write with Auto Precharge])]

1. Read with Auto Precharge (READA)

If A10 is "high" at READ command, the bank selected by A11 is precharged automatically after internal Read operation is finished. So, Precharge command (PRE) need not to be executed for the selected bank after Read operation.

After READA command is executed, an interval defined by n_{APR} (Last data-out to Bank Active command delay) cycle is required before Bank Active command (ACT) execution for the same bank. Minimum n_{APR} depends on CAS Latency. This command is not allowed for full page Burst Read operation.

< READ with Auto Precharge Command (READA) >

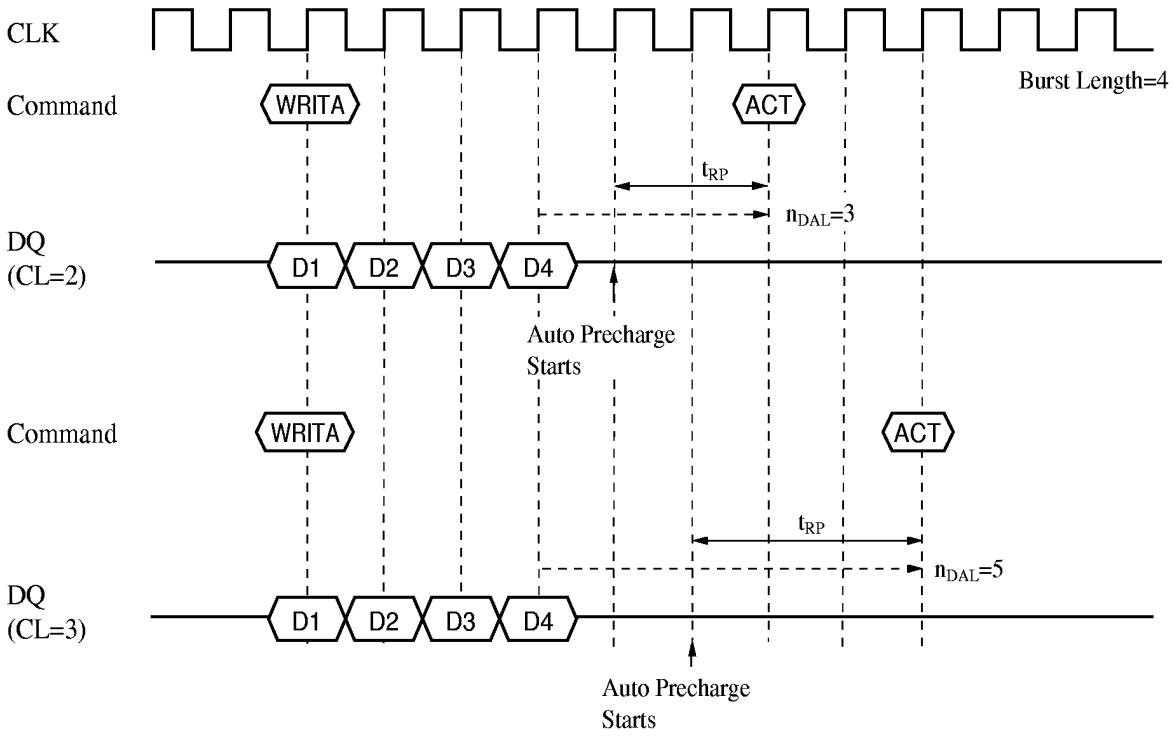


2. Write with Auto Precharge (WRITA)

If A10 is "high" at WRIT command, the bank selected by A11 is precharged automatically after internal Write operation is finished. So, Precharge command (PRE) need not to be executed for the selected bank after Write operation.

After WRITA command is executed, an interval defined by n_{DAL} (Last data-in to Bank Active command delay) cycle is required before Bank Active command (ACT) execution for the same bank. Minimum n_{DAL} depends on CAS Latency. This command is not allowed for full page Burst Read operation.

< WRITE with Auto Precharge Command (WRITA) >

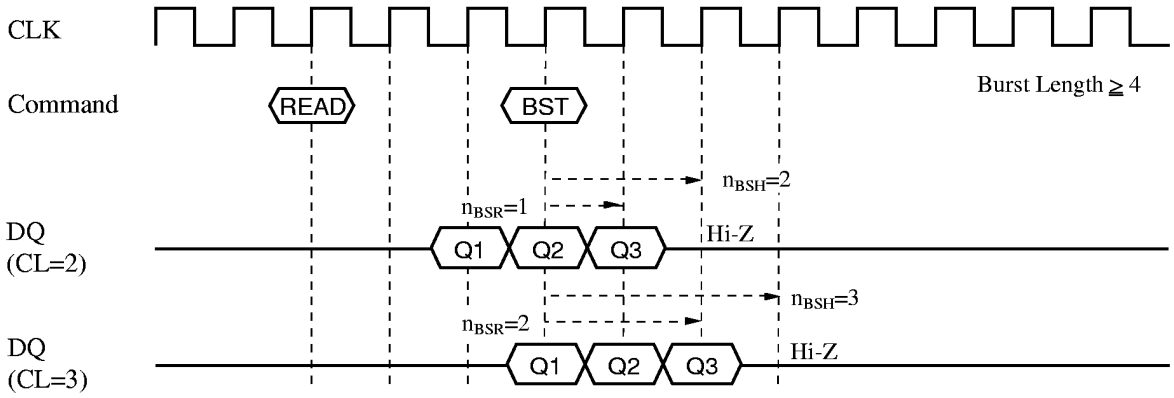


[Burst Stop command (BST)]

1. Burst Read Stop

Burst data output can be terminated by Burst Stop command (BST). An interval from Burst Stop command execution to last valid data output are defined by n_{BSR} (Burst Stop command to last valid data-out delay) cycle. Output buffer turned to Hi-Z at n_{BSH} (Burst Stop command to output buffer turn off delay) cycle after Burst Stop command input or when Burst Read operation is completed. Minimum n_{BSR} and n_{BSH} depend on CAS Latency.

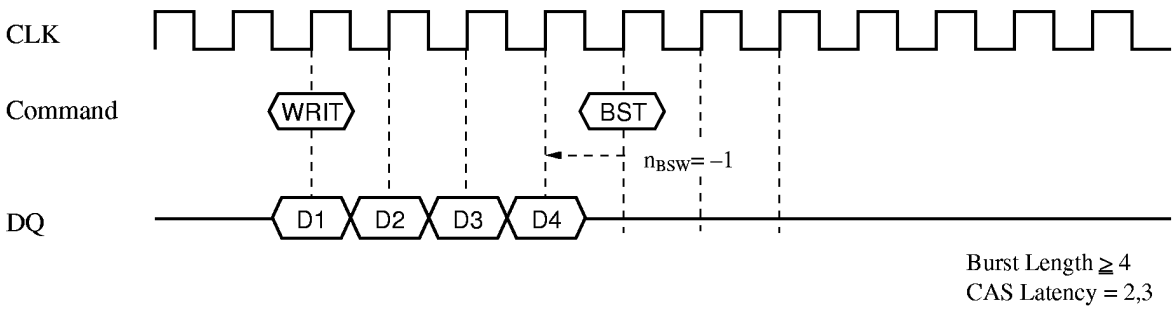
< Burst Stop Command (Burst READ Stop) >



2. Burst Write Stop

Burst data-input can be terminated by Burst Stop command (BST). Data-in at the same and following cycles are ignored.

< Burst Stop Command (Burst WRITE Stop) >



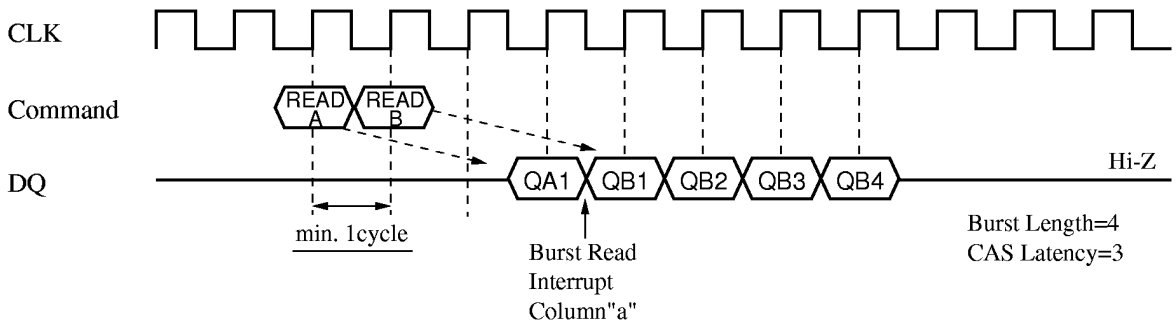
■ Command Interval

[READ to READ command interval]

[Case 1] Same row address in same bank

When a Read command (READ) is issued for the same row address in the same bank with previous Read command (READ), a minimum interval from READ to READ is 1 cycle. Although previous Burst Read operation is not completed, subsequent Read operation is started after CAS Latency cycles. Then the previous Burst Read operation is interrupted.

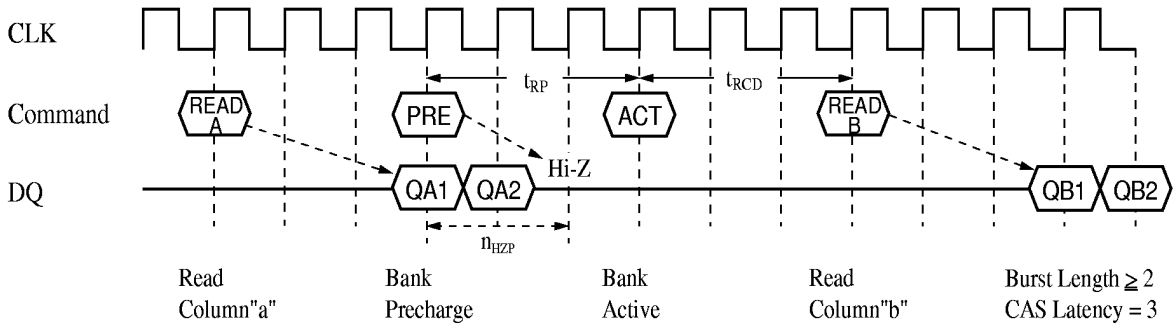
< READ to READ Command Interval (same ROW address in same bank) >



[Case 2] Different row address in same bank

When subsequent Read command (READ) is issued for a different row address in the same bank, Precharge command (PRE) and Bank Active command (ACT) must be executed before executing subsequent Read command.

< READ to READ Command Interval (different ROW address in same bank) >

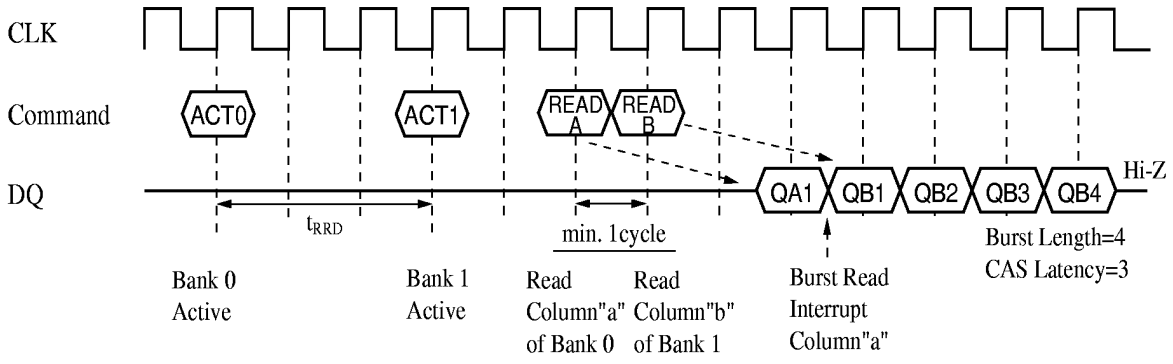


[Case 3] Different bank

When a Read command (READ) is issued for a different bank from the previous Read command (READ), a minimum interval from READ to READ is 1 cycle. Although previous Burst Read operation is not completed, subsequent Read operation is started after CAS Latency cycles. Then the previous Burst Read operation is interrupted.

If another bank is not activated, Bank Active command (ACT) need to be executed before subsequent Read command execution.

< READ to READ Command Interval (different bank) >

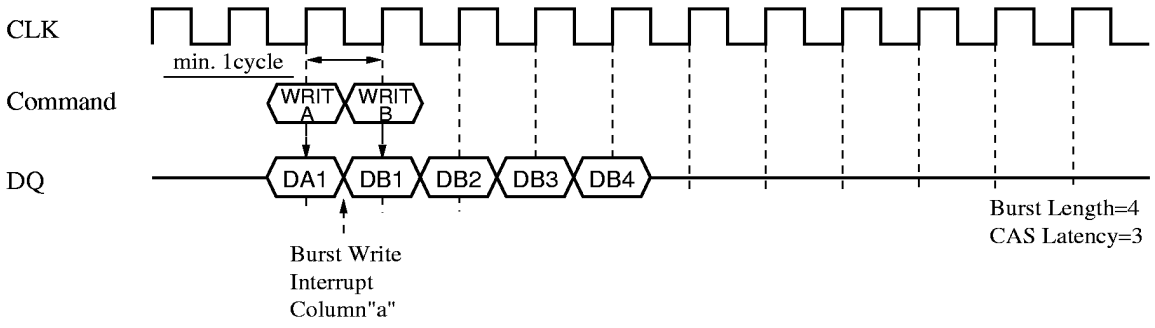


[WRIT to WRIT command interval]

[Case 1] Same row address in same bank

When a Write command (WRIT) is issued for the same row address in the same bank with previous Write command (WRIT), a minimum interval from WRIT to WRIT is 1 cycle. Although previous Burst Write operation is not completed, subsequent Write operation is started. Then the previous Burst Write operation is interrupted.

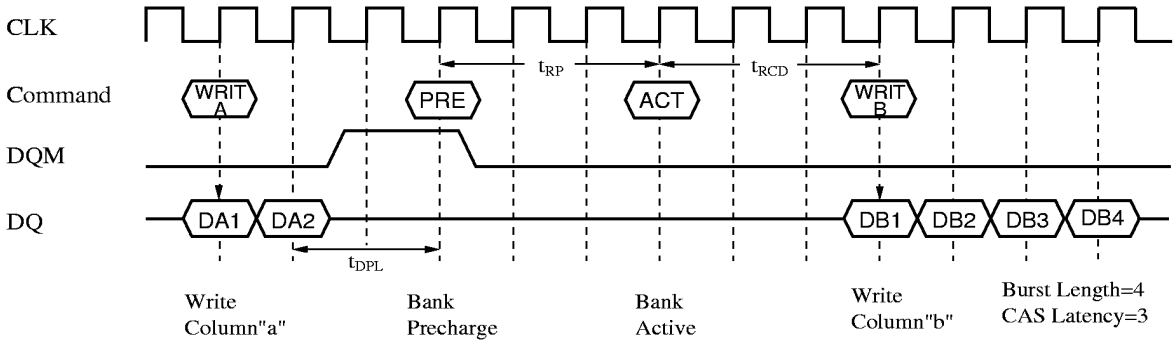
< WRIT to WRIT Command Interval (same ROW address in same bank) >



[Case 2] Different row address in same bank

When subsequent Write command (WRIT) is issued for a different row address in the same bank, Precharge command (PRE) and Bank Active command (ACT) must be executed before executing subsequent Write command.

< WRIT to WRIT Command Interval (different ROW address in same bank) >

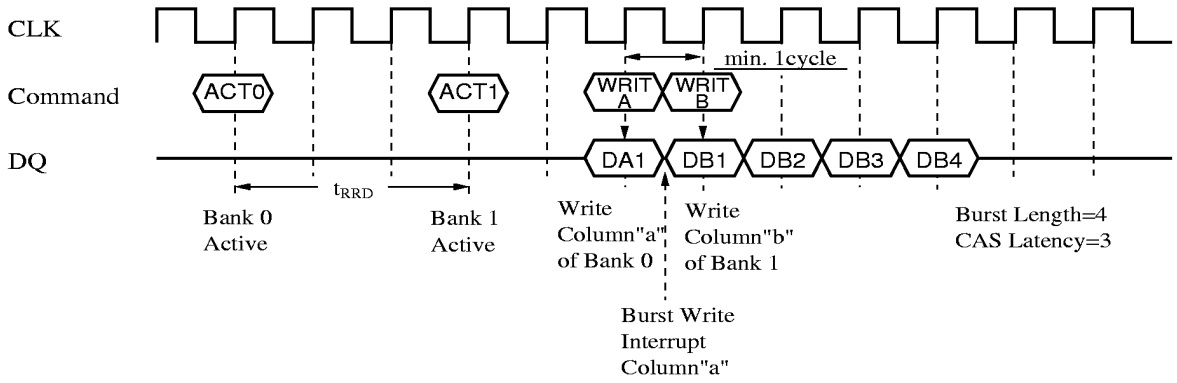


[Case 3] Different bank

When subsequent Write command (WRIT) is issued for a different bank from the previous bank, a minimum interval from WRIT to WRIT is 1 cycle. Although previous Burst Write operation is not completed, subsequent Write operation is started. Then the previous Burst Write operation is interrupted.

If another bank is not activated, Bank Active command (ACT) need to be executed before subsequent Write command execution.

< WRIT to WRIT Command Interval (different bank) >



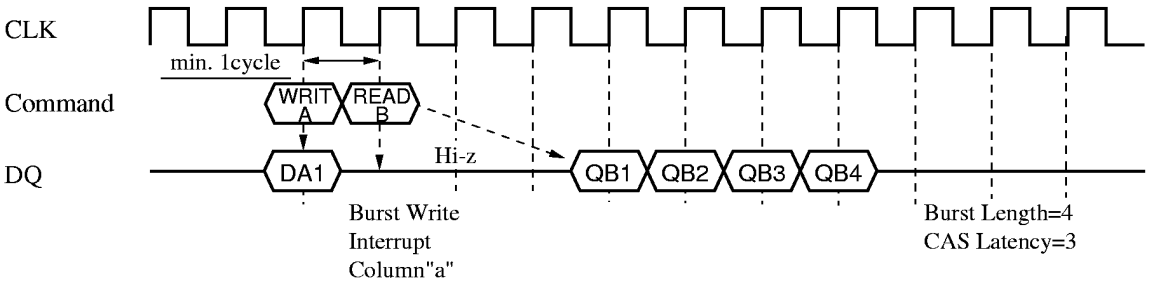
[WRIT to READ command interval]

[Case 1] Same row address in same bank

When a Read command (READ) is issued for the same row address in the same bank with previous Write command (WRIT), a minimum interval from WRIT to READ is 1 cycle. Although previous Burst Write operation is not completed, data-input is interrupted by next Read command. Only the data before READ command is written.

Data bus must be high-impedance at least one cycle before first Read data-out.

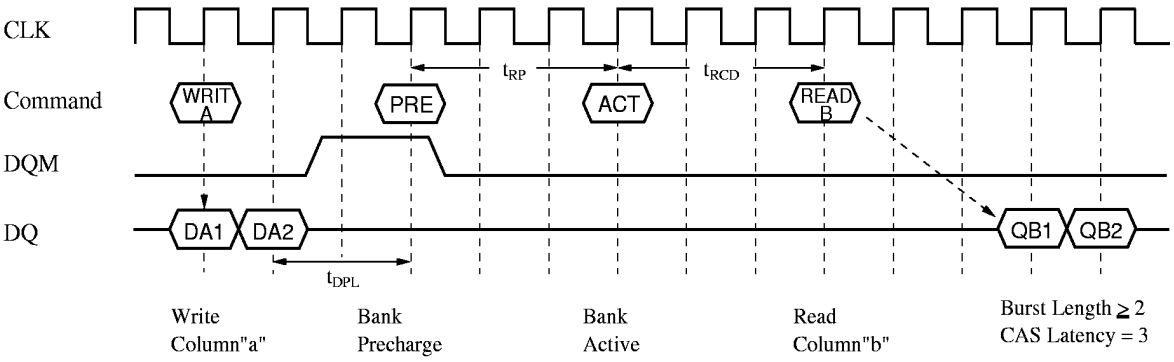
< WRIT to READ Command Interval (same ROW address in same bank) >



[Case 2] Different row address in same bank

When subsequent Read command (READ) is issued for a different row address in the same bank, Precharge command (PRE) and Bank Active command (ACT) must be executed before executing subsequent Read command.

< WRIT to READ Command Interval (different ROW address in same bank) >



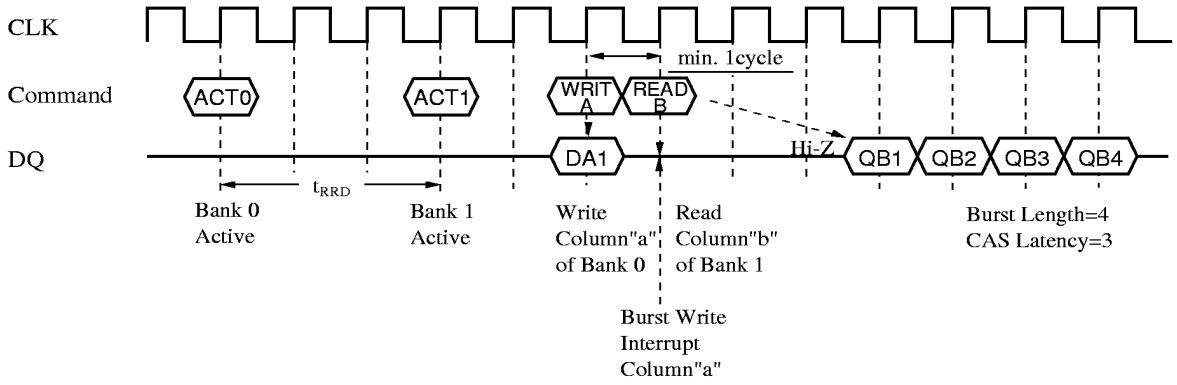
[Case 3] Different bank

When a Read command (READ) is issued for a different bank from the previous bank, a minimum interval from WRIT to READ is 1 cycle. Although previous Burst Write operation is not completed, data-input is interrupted by next Read command. Only the data before READ command is written.

If another bank is not activated, Bank Active command (ACT) need to be executed before subsequent Read command execution.

Data bus must be high-impedance at least one cycle before first Read data out.

< WRIT to READ Command Interval (different bank) >



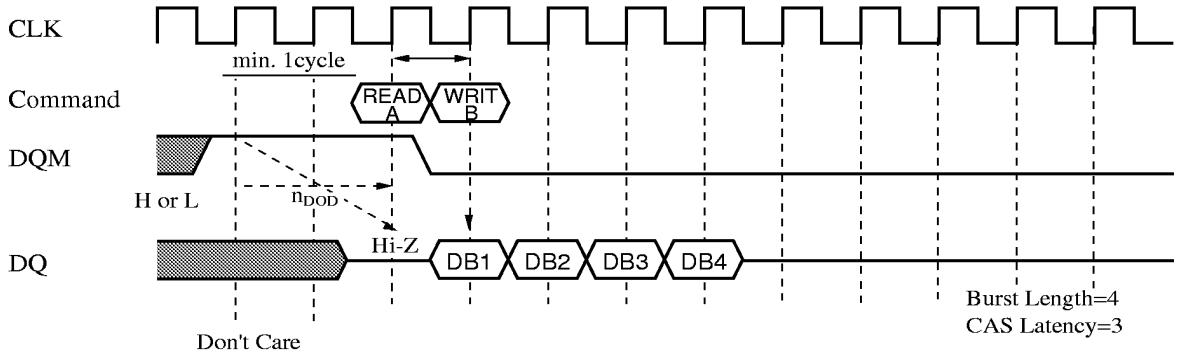
[READ to WRIT command interval]

[Case 1] Same row address in same bank

When a Write command (WRIT) is issued for the same row address in the same bank with previous Read command (READ), a minimum interval from READ to WRIT is 1 cycle. Although previous Burst Read operation is not completed, data output is interrupted by next Write command.

Output buffer must be high-impedance at least one cycle before Write command by asserting DQM(U/L) to avoid data conflict. The latency from DQM(U/L) assert to output buffer turn-off (n_{DOD}) is 2 cycles, so DQM (U/L) must be asserted at least 3 cycles before Write command.

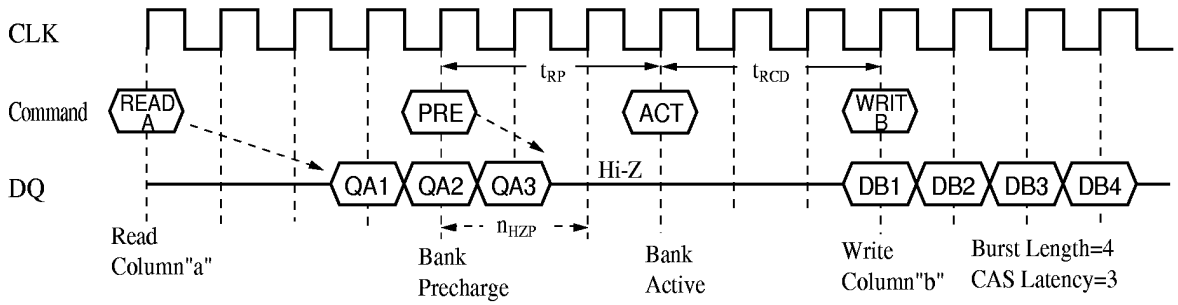
< READ to WRITE Command Interval (same ROW address in same bank) >



[Case 2] Different row address in same bank

When subsequent Write command (WRIT) is issued for a different row address in the same bank, Precharge command (PRE) and Bank Active command (ACT) must be executed before executing subsequent Write command.

< READ to WRIT Command Interval (different ROW address in same bank) >



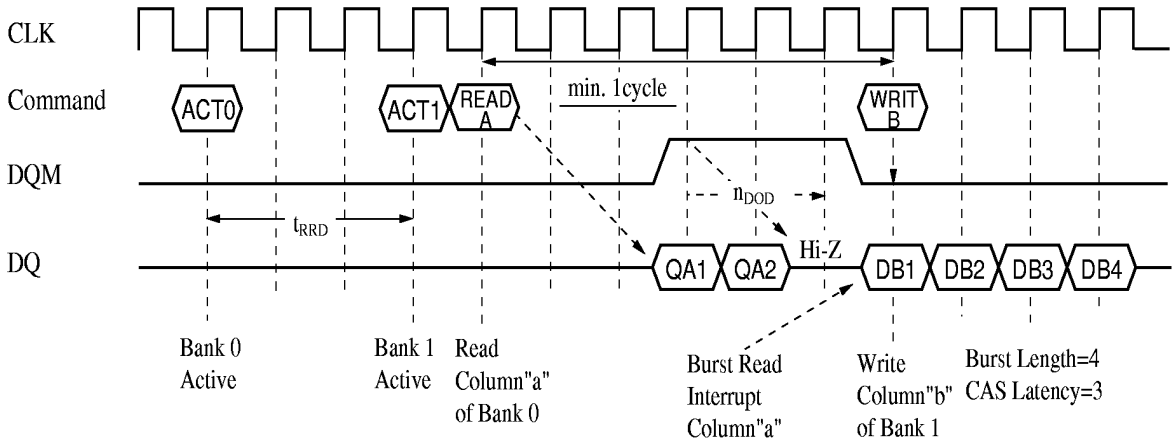
[Case 3] Different bank

When a Write command (WRIT) is issued for a different bank from the previous bank, an minimum interval from READ to WRIT is 1 cycle. Although previous Burst Read operation is not completed, data output is interrupted by next Write command. Only the Read data before WRIT command are put out.

If another bank is not activated, Bank Active command (ACT) need to be executed before Write command execution.

Output buffer must be high-impedance at least one cycle before Write command by asserting DQM(U/L) to avoid data conflict. The latency from DQM(U/L) assert to output buffer turn-off (n_{DOD}) is 2 cycles, so DQM (U/L) must be asserted at least 3 cycles before Write command.

< READ to WRIT Command Interval (different bank) >



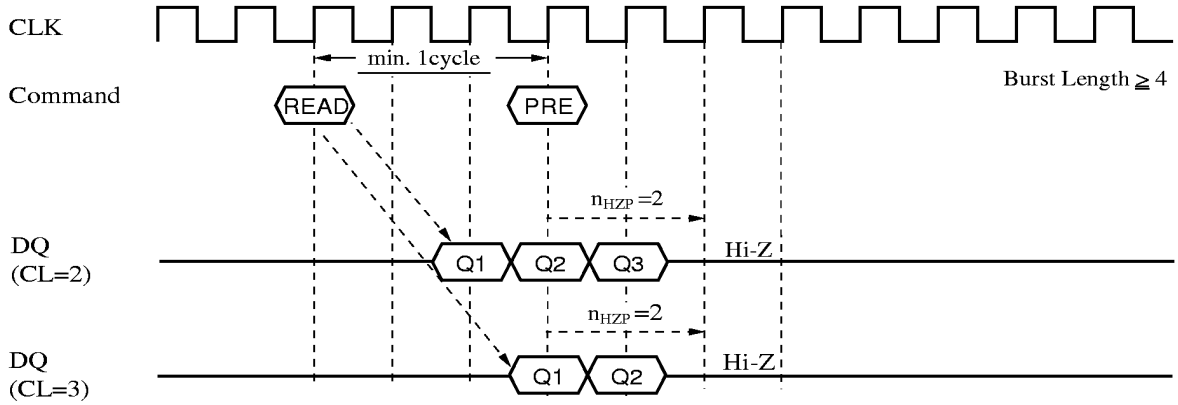
[READ to PRE [Precharge Select Bank] command interval (Same bank)]

When a Precharge command (PRE) is issued for the same bank with previous Read command (READ), a minimum interval from READ to PRE is 1 cycle. Although previous Burst Read operation is not completed, output buffer turn to high-impedance n_{HZP} (Precharge command to output buffer turn-off delay) cycles after executing Precharge command. Then the previous Burst Read operation is interrupted.

An interval defined by n_{EP} (last data-out to Precharge command delay) is required to complete Burst Read operation.

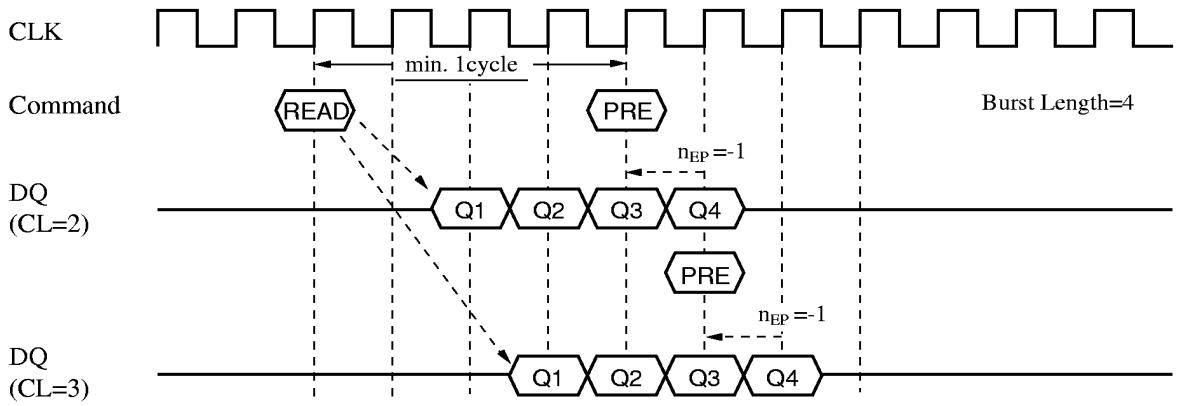
● Burst READ Interrupt

< READ to PRE Command Interval (same bank, Burst READ Interrupt) >



● Burst READ Complete

< READ to PRE Command Interval (same bank, Burst READ Complete) >



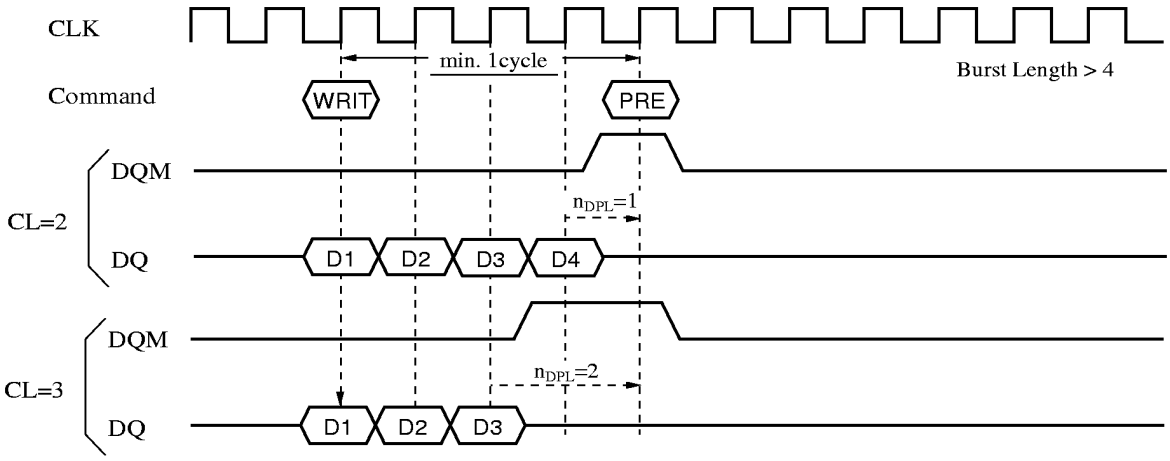
[WRIT to PRE [Precharge Select Bank] command interval (Same bank)]

When a Precharge command (PRE) is issued for the same bank with previous Write command (WRIT), a minimum interval from WRIT to PRE is 1 cycle. Although previous Burst Write operation is not completed, precharge operation starts. Then the previous Burst Write operation is interrupted.

An interval defined by n_{DPL} (last data-in to Precharge command period) is required from last data-in to Precharge command.

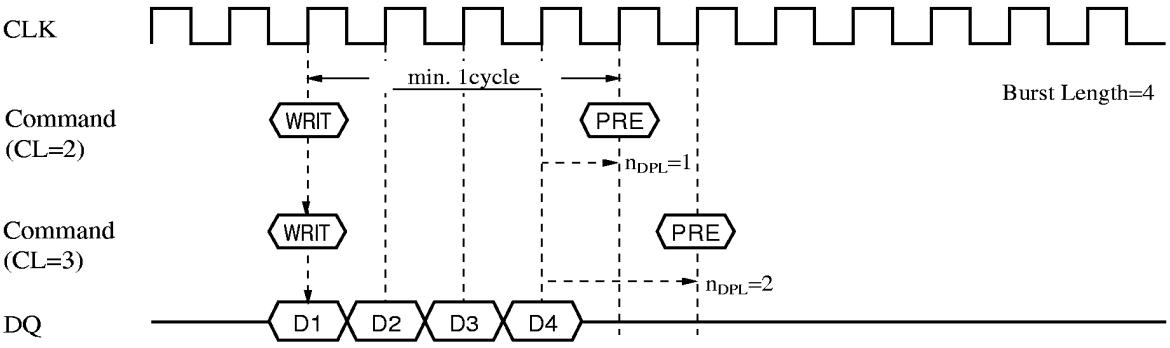
● Burst WRITE Interrupt

< WRIT to PRE Command Interval (same bank, Burst WRITE Interrupt) >



● Burst WRITE Complete

< WRIT to PRE Command Interval (same bank, Burst WRITE Complete) >



■ Power-On Sequence

1. Apply power and clock with NOP or DESL command input.
   Maintain stable power, stable clock, and NOP or DESL input conditions for a minimum of 100μs.
   During above operation, CKE and DQM(U/L) inputs must be held "high".
2. Execute All Banks Precharge by issuing PRE or PALL commands.
3. After minimum t_{RP} period from last Precharge command execution, issue Mode Register Set (MRS) command to initialize mode register.
4. With the interval of nRSA after MRS command, issue CBR (auto) refresh command (REF) at least two times with t_{RC} interval.

After executing above power-on sequence, the device is in the idle state. And command input is possible at any cycle.

(The sequence of Mode Register Set and CBR refresh can be transposed.)

■ Note For Self Refresh

Before Self Refresh Entry command input and after Self Refresh Exit command input, execute CBR refresh at least 2,048 times at maximum 15.6 μs interval.

■ Electrical Specifications

[Absolute Maximum Ratings] (V_{SS} = 0V)

Item	Symbol	Rating	Unit
Supply Voltage (1)	V_{DD}, V_{DDQ}	-0.5 ~ +4.6	V
Input/Output Voltage (1)	V_{IN}, V_{OUT}	-0.5 ~ +4.6	V
Short Circuit Output Current	I_{OS}	20	mA
Power Dissipation	Pd	1	W
Operating Ambient Temperature	Topr	0 ~ +70	°C
Storage Temperature	Tstg	-55 ~ +125	°C

Notes

(1) V_{SS} terminal reference

Stresses greater than those listed under "Absolute Maximum Ratings" (ex. excess voltage input or reverse insertion) may affect reliability of the device and cause unusual heat, deterioration of characteristics or breakdown of the device.

[Recommended Operating Conditions] (Ta = 0 ~ +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD} V_{DDQ}	3.0	3.3	3.6	V
	V_{SS} V_{SSQ}	0	0	0	V
Input Voltage “H” Level	V_{IH}	2.0		V_{DD}+0.3	V
Input Voltage “L” Level	V_{IL}	-0.3		0.8	V

[Terminal Capacitance] (V_{DD}= 3.3V ± 0.3V, Ta = 0 ~ +70℃, 1MHz)

Item		Symbol	Min.	Typ.	Max.	Unit
Input	Address	C_{I1}			6	pF
	Clock	C_{I2}			6	pF
Data Input/Output		C_{IO}			8	pF

[DC Characteristics] (V_{DD}= 3.3V ± 0.3V, Ta = 0 ~ +70℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Leakage Current	I_{LI}	-5	0.1	5	µA	(1)
Output Leakage Current	I_{LO}	-5	0.1	5	µA	(2)
Output Voltage “H” level	V_{OH}	2.4			V	(3)
Output Voltage “L” level	V_{OL}			0.4	V	(4)

Notes

(1) $0V \leq V_{IN} \leq 3.6V$, Input pins other than measurement pins are at 0V, or V_{DD}.

(2) $0V \leq V_{OUT} \leq 3.6V$, Output is in a high-impedance state.

(3) I_{OH} = -2mA

(4) I_{OL} = 2mA

[DC Operating Conditions] (V_{DD}= 3.3V ± 0.3V, Ta = 0 ~ +70°C)

Item	Symbol	Condition	Grade	Max.	Unit	Note
Operating Current (1 bank active)	I_{CC1}	Burst Length=1 t_{RC}=Min.	-80	100	mA	2,3
			-90	90		
			-10	80		
Standby Current (All banks inactive)	I_{CC2P}	CKE ≤ V_{IL} t_{CK}=Min. (Power Down mode)		2	mA	2
	I_{CC2PS}	CKE ≤ V_{IL} t_{CK}=V_{IL} or V_{IH} (Power Down mode)		1	mA	
	I_{CC2N}	CKE ≥ V_{IH} t_{CK}=Min.	-80	28	mA	2
			-90	25		
			-10	22		
Standby Current (All banks active)	I_{CC3P}	CKE ≤ V_{IL} t_{CK}=Min. (Power Down mode)		2	mA	2
	I_{CC3N}	CKE ≥ V_{IH} t_{CK}=Min.	-80	28	mA	2
			-90	25		
			-10	22		
Burst Operating Current (Bank interleave)	I_{CC4}	t_{CK}=Min.	-80	150	mA	2,3
			-90	135		
			-10	120		
Refresh Current	I_{CC5}	t_{RC}=Min.	-80	120	mA	2
			-90	105		
			-10	90		
Self Refresh Current	I_{CC6}	CKE ≤ V_{IL}		2	mA	

[Electrical Characteristics and Recommended AC Operating Conditions (Synchronous)]

(V_{DD}= 3.3V ± 0.3V, Ta = 0 ~ +70˚C)

Item		Symbol	-80		-90		-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
CLK Cycle Time	CL=3	t_{CK}	8		9		10		ns	4
	CL=2		12		13.5		15			
Access Time from CLK	CL=3	t_{AC}		6.5		7		8	ns	4,5
	CL=2			9		10.5		12		
CLK High Level Width		t_{CH}	3		3		3.5		ns	4,6
CLK Low Level Width		t_{CL}	3		3		3.5		ns	4,6
Data-out Hold Time		t_{OH}	2		2.5		2.5		ns	4
Data-out Low-impedance Time		t_{LZ}	0		0		0		ns	4
Data-out High-impedance Time		t_{HZ}		10		10		10	ns	4
Data-in Setup Time		t_{DS}	2.5		3		3		ns	4,6
Data-in Hold Time		t_{DH}	1		1		1		ns	4,6
Address Setup Time		t_{AS}	2.5		3		3		ns	4,6
Address Hold Time		t_{AH}	1		1		1		ns	4,6
CKE Setup Time		t_{CKS}	2.5		3		3		ns	4,6
CKE Hold Time		t_{CKH}	1		1		1		ns	4,6
Command Setup Time ($\overline{CS}$,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$,DQM)		t_{CMS}	2.5		3		3		ns	4,6
Command Hold Time ($\overline{CS}$,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$,DQM)		t_{CMH}	1		1		1		ns	4,6

[Electrical Characteristics and Recommended AC Operating Conditions (Asynchronous)]

(V_{DD}= 3.3V ± 0.3V, Ta = 0 ~ +70℃)

Item		Symbol	-80		-90		-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
ACT (REF) to ACT (REF) Command Period (Same Bank)		t_{RC}	80		90		100		ns	4,7
ACT to PRE Command Period (Same Bank)		t_{RAS}	56	120,000	63	120,000	70	120,000	ns	4,7
PRE to ACT Command Period (Same Bank)		t_{RP}	24		27		30		ns	4,7
ACT to READ/WRIT Command Period (Same Bank)		t_{RCD}	24		27		30		ns	4,7
ACT to ACT Command Period (Different Bank)		t_{RRD}	24		27		30		ns	4,7
Data-in to PRE Command Period	CL=3	t_{DPL}	1CLK +8		1CLK +9		1CLK +10		ns	4,7
	CL=2		8		9		10		ns	
Data-in to ACT (REF) Command Period (Auto Precharge)	CL=3	t_{DAL}	2CLK +24		2CLK +27		2CLK +30		ns	4,7
	CL=2		1CLK +24		1CLK +27		1CLK +30		ns	
Transition Time		t_T	1	30	1	30	1	30	ns	
Refresh Time		t_{REF}		32		32		32	ms	

[Correlation Between Frequency and Minimum Latency]

Speed Version		-80		-90		-10		UNIT
CLK Cycle Time		8	12	9	13.5	10	15	ns
Frequency		125	83	111	74	100	66	MHz
CAS Latency		3	2	3	2	3	2	cycle
n_{RCD}		3	2	3	2	3	2	cycle
RAS Latency [t_{RCD}+CAS Latency]		6	4	6	4	6	4	cycle
n_{RC}		10	7	10	7	10	7	cycle
n_{RAS}		7	5	7	5	7	5	cycle
n_{RRD}		3	2	3	2	3	2	cycle
n_{RP}		3	2	3	2	3	2	cycle
n_{DPL}		2	1	2	1	2	1	cycle
n_{DAL}		5	3	5	3	5	3	cycle
n_{RSA}	MRS to ACT Command Period	2	2	2	2	2	2	cycle
n_{DOD}	DQM to data-out Hi-Z Command period	2	2	2	2	2	2	cycle
n_{DID}	DQM to data-in Command period	0	0	0	0	0	0	cycle
n_{HZP}	PRE to Data-out Hi-Z Command Period	2	2	2	2	2	2	cycle
n_{EP}	Last Data-out to PRE Command Period	-1	-1	-1	-1	-1	-1	cycle
n_{APR}	Last Data-out to ACT Command Period	2	1	2	1	2	1	cycle
n_{CLE}	CKE to CLK Disable Period	1	1	1	1	1	1	cycle
n_{CDD}	DESEL to Command Disable Period	0	0	0	0	0	0	cycle

[Correlation Between Frequency and Minimum Latency]

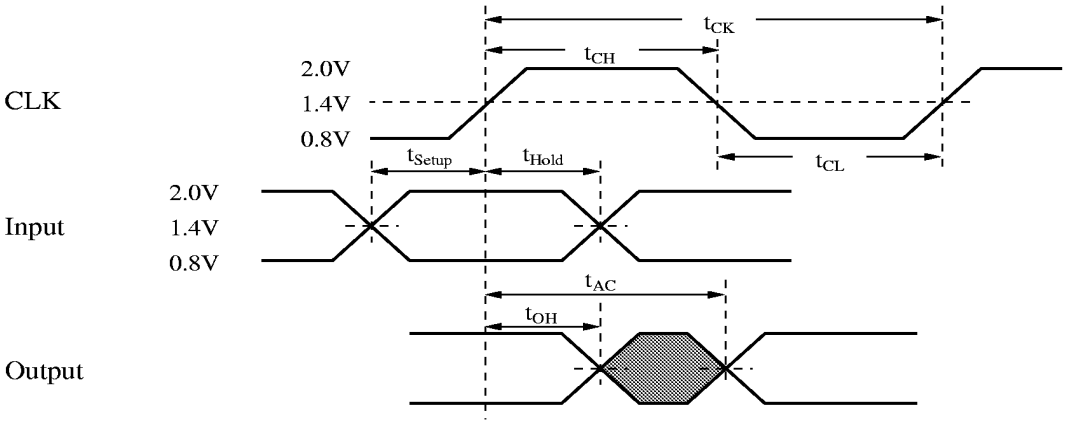
Speed Version		-80		-90		-10		UNIT
CLK Cycle Time		8	12	9	13.5	10	15	ns
Frequency		125	83	111	74	100	66	MHz
CAS Latency		3	2	3	2	3	2	cycle
n_{BSR}	BST to Last Valid Data-out Period	2	1	2	1	2	1	cycle
n_{BSH}	BST to Output Buffer Turn-off Period	3	2	3	2	3	2	cycle
n_{BSW}	BST to Last Valid Data-in Period	-1	-1	-1	-1	-1	-1	cycle
n_{PEC}	Power down mode Exit to Command Input Period	1	1	1	1	1	1	cycle

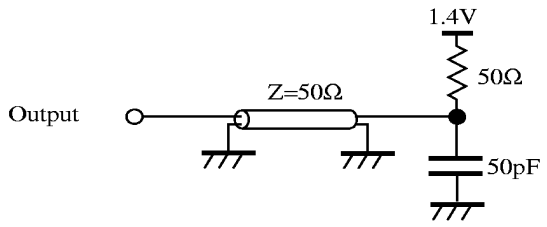
[NOTES]

1. All voltages are referenced to V_{SS}.
2. These parameters depend on cycle rates. These values are measured under the value of t_{CK}(Min.) and t_{RC}(Min.). And input signals are changed only one time during t_{CK}(Min.).
3. These parameters depend on output loading. These values are measured with the output open.
4. AC measurement assumes t_T=1ns. Reference level for measuring timing of input signals is 1.4V. Transition times are measured between V_{IH} and V_{IL}.
5. AC access time is measured at 1.4V.
6. If t_T is longer than 1ns, reference level for measuring timing of input signals is V_{IH} and V_{IL}.
7. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows :

   the number of clock cycle = specified value of timing/clock period
   (count fraction as a whole number)
   See "Correlation Between Frequency and Minimum Latency".

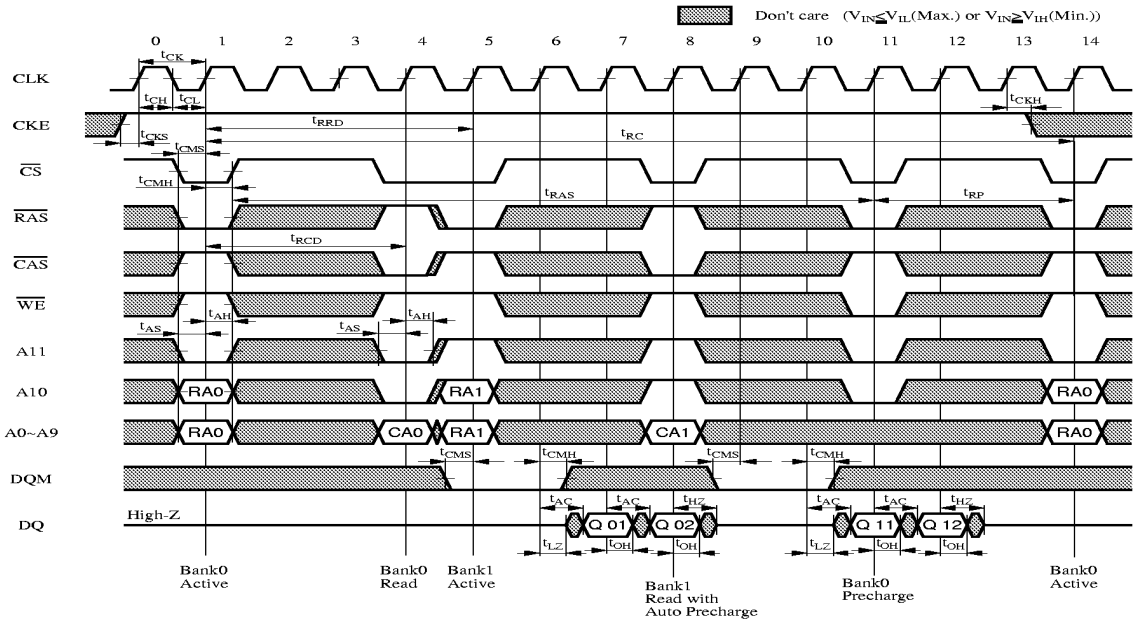
[AC Test Conditions]





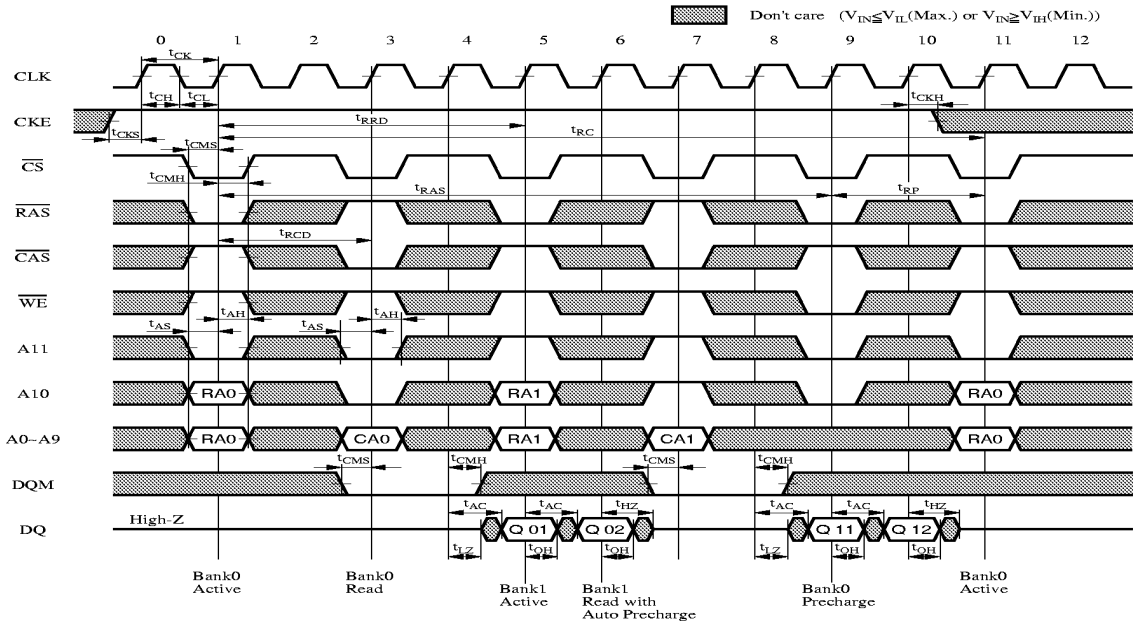
Output Load

[AC Timing (Read)] Burst Length=2, CAS Latency=3



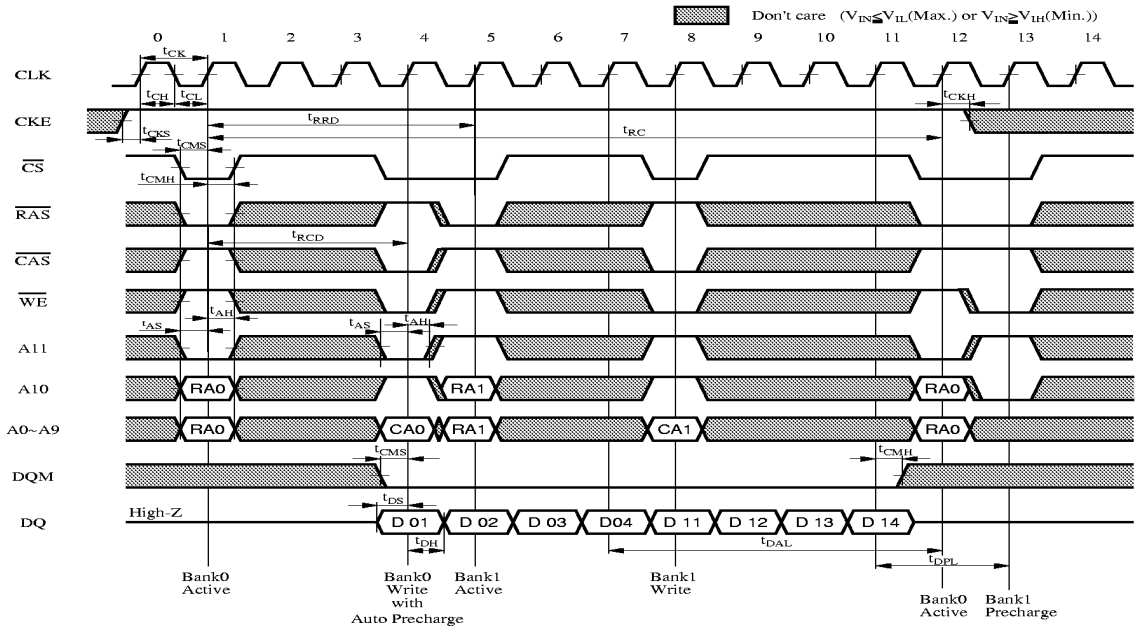
RA0/1 : Row Address (Bank 0/1), CA0/1 : Column Address (Bank 0/1), Q0×/1× : Output Data (Bank 0/1)

[AC Timing (Read)] Burst Length=2, CAS Latency=2



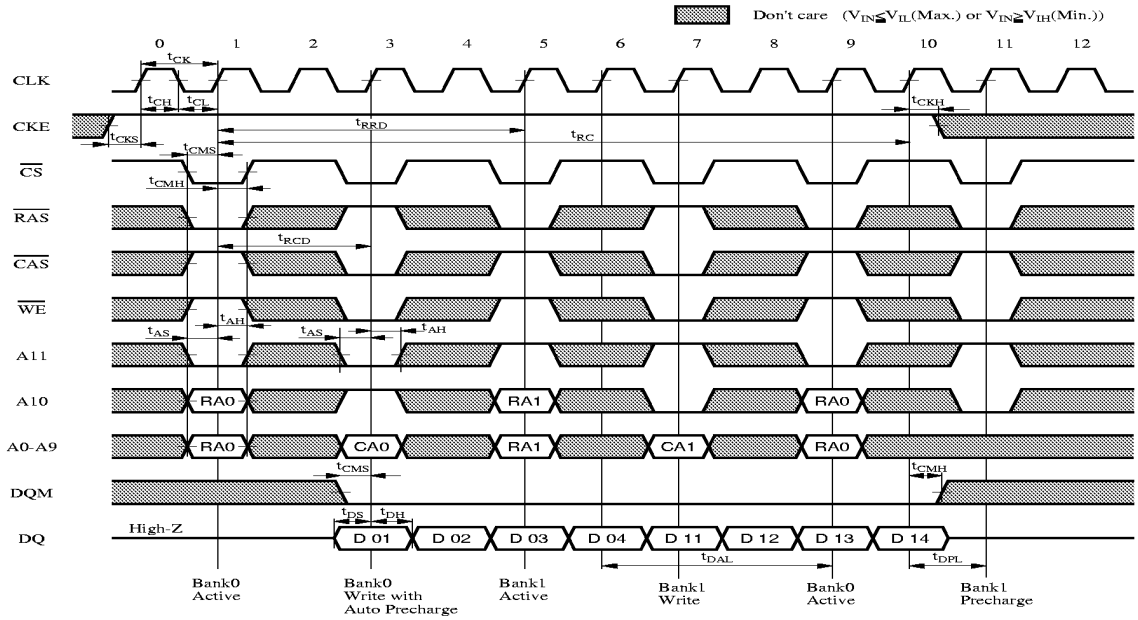
RA0/1 : Row Address (Bank 0/1), CA0/1 : Column Address (Bank 0/1), Q0×/1× : Output Data (Bank 0/1)

[AC Timing (Write)] Burst Length=4, CAS Latency=3



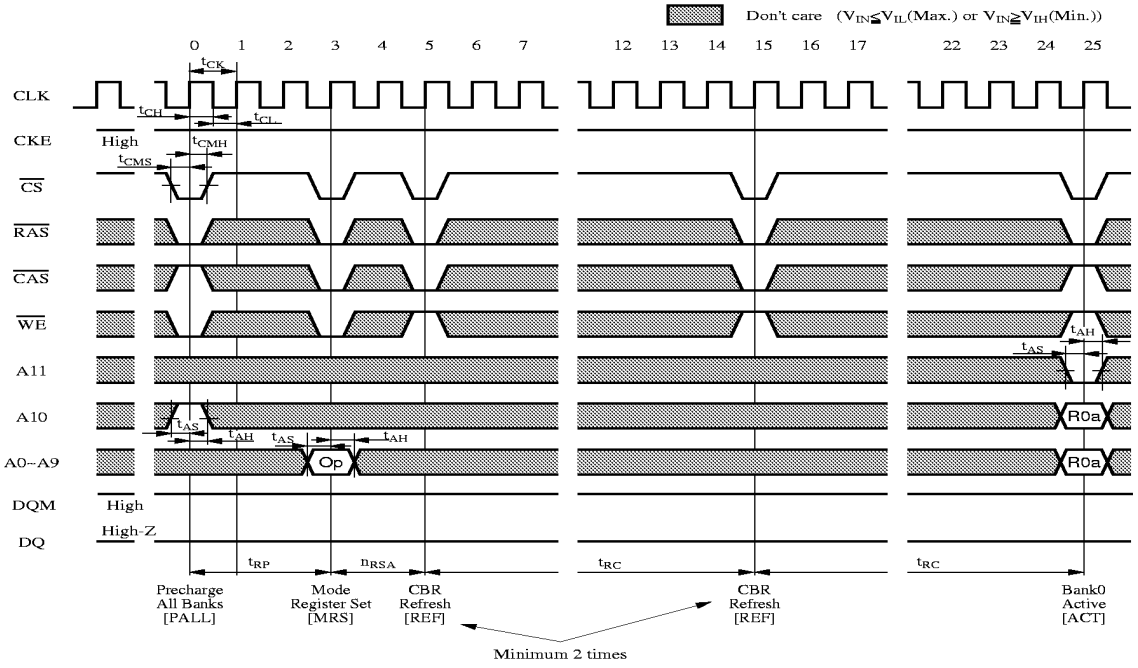
RA0/1 : Row Address (Bank 0/1), CA0/1 : Column Address (Bank 0/1), Q0×/1× : Output Data (Bank 0/1)

[AC Timing (Write)] Burst Length=4, CAS Latency=2



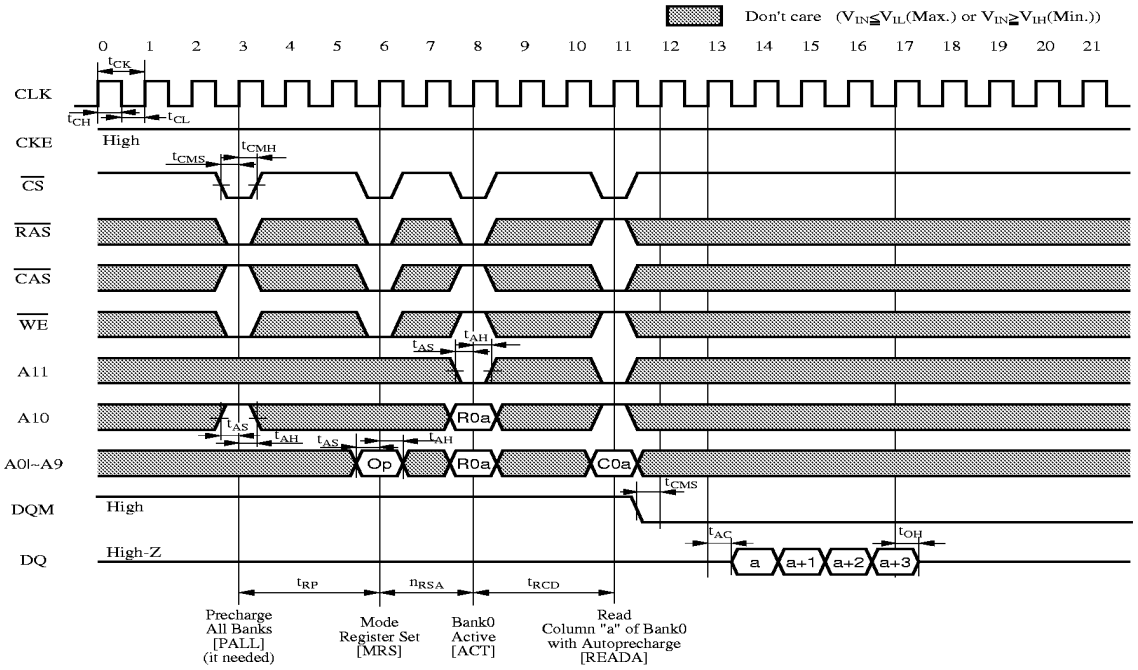
RA0/1 : Row Address (Bank 0/1), CA0/1 : Column Address (Bank 0/1), Q0×/1× : Output Data (Bank 0/1)

[Power On Sequence]



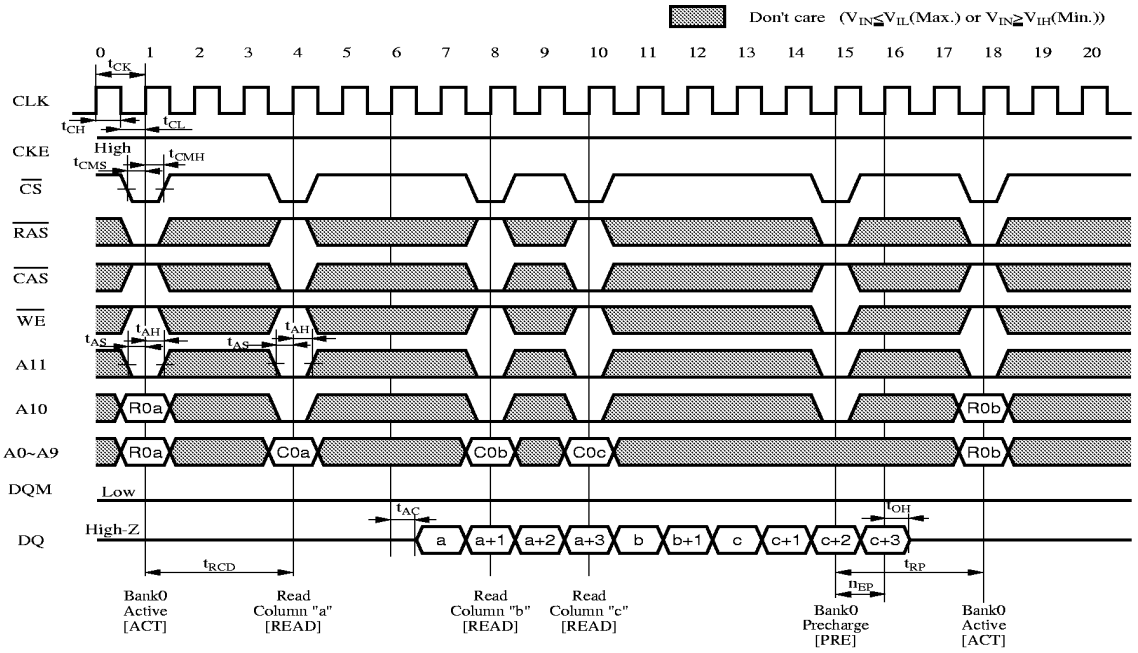
OP : Operation Code, R0 : Row Address (Bank 0)

[Mode Register Set during operation] Burst Length=4, CAS Latency=3



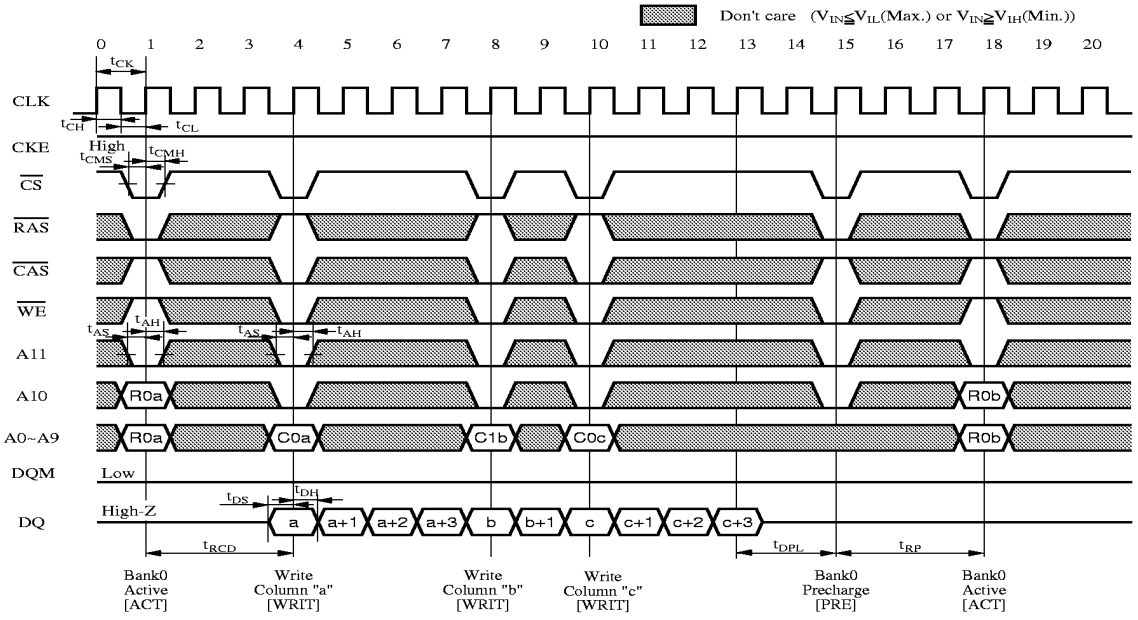
OP : Operation Code, R0 : Row Address (Bank 0), C0 : Column Address (Bank 0)

[Read (Same Row & Random Column)] Burst Length=4, CAS Latency=3



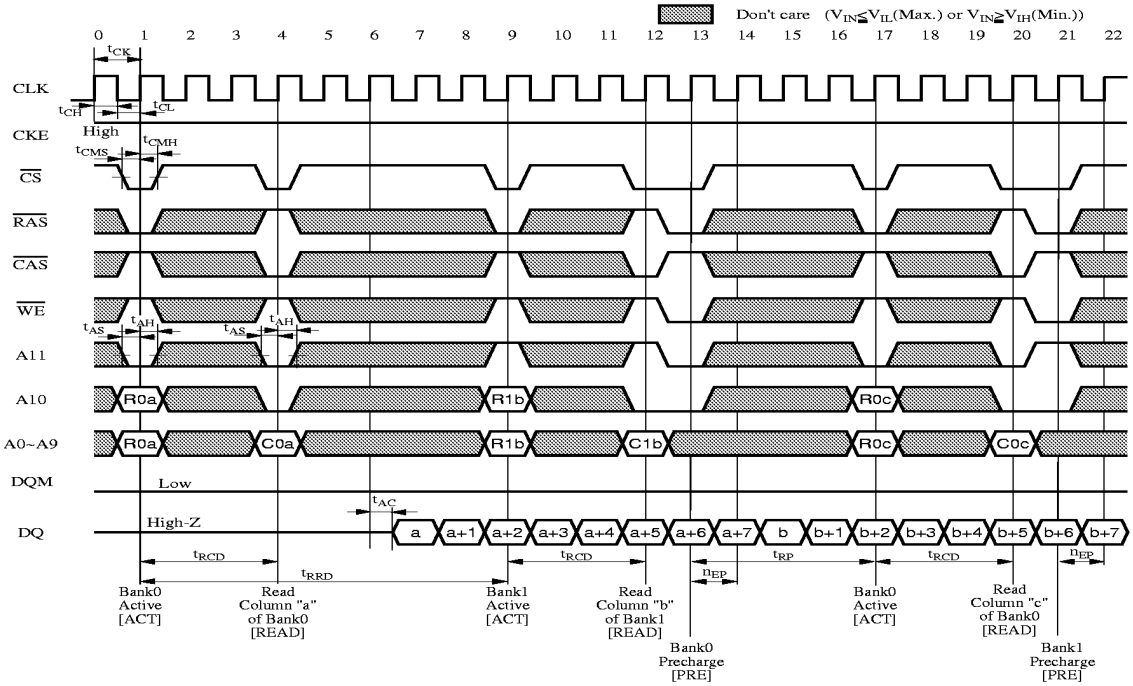
RA0/1 : Row Address (Bank 0), C0 : Column Address (Bank 0)

[Write (Same Row & Random Column)] Burst Length=4, CAS Latency=3



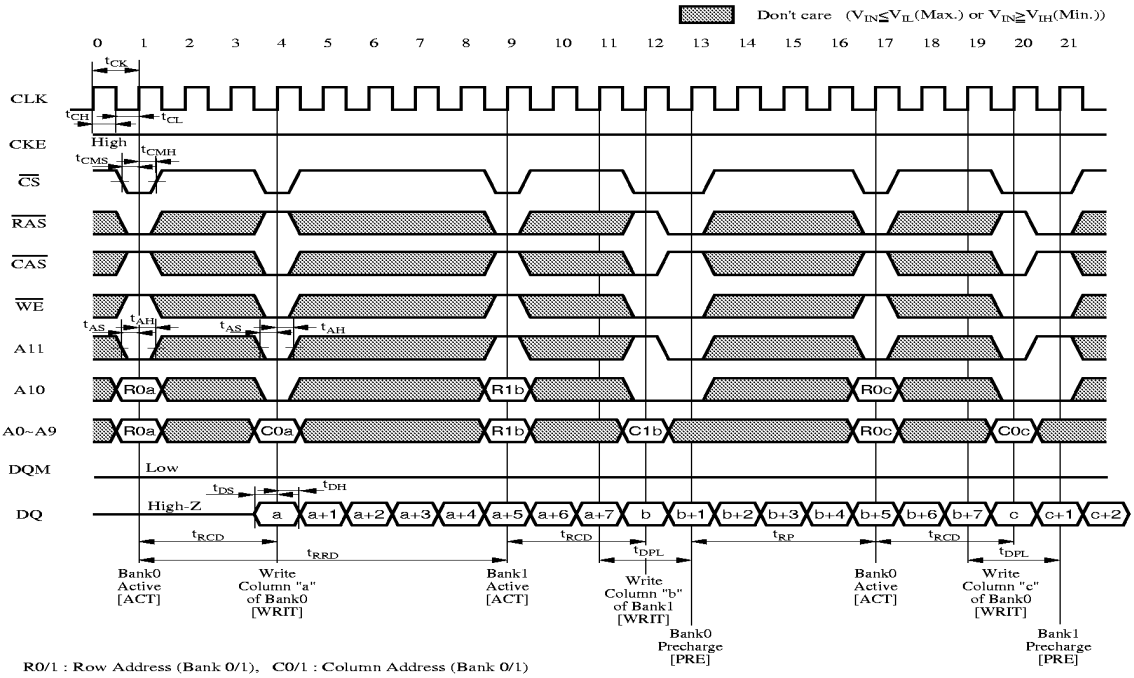
R0 : Row Address (Bank 0), C0 : Column Address (Bank 0)

[Read (Random Row & Bank Interleave)] Burst Length=8, CAS Latency=3



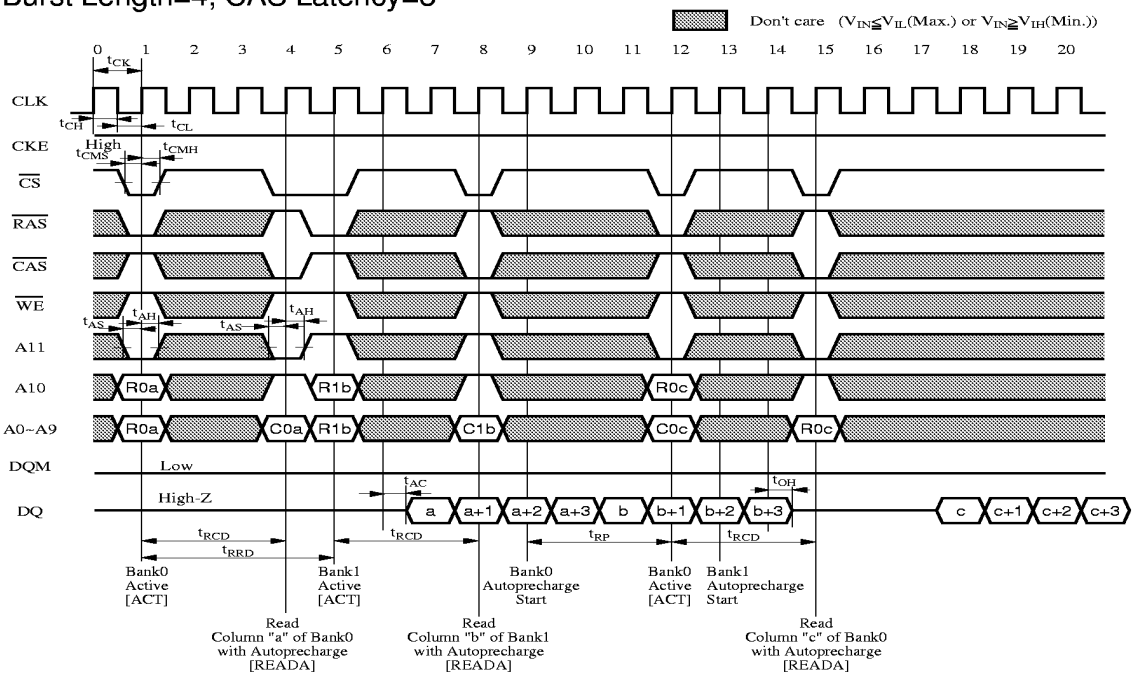
R0/1 : Row Address (Bank 0/1), C0/1 : Column Address (Bank 0/1)

[Write (Random Row & Bank Interleave)] Burst Length=8, CAS Latency=3



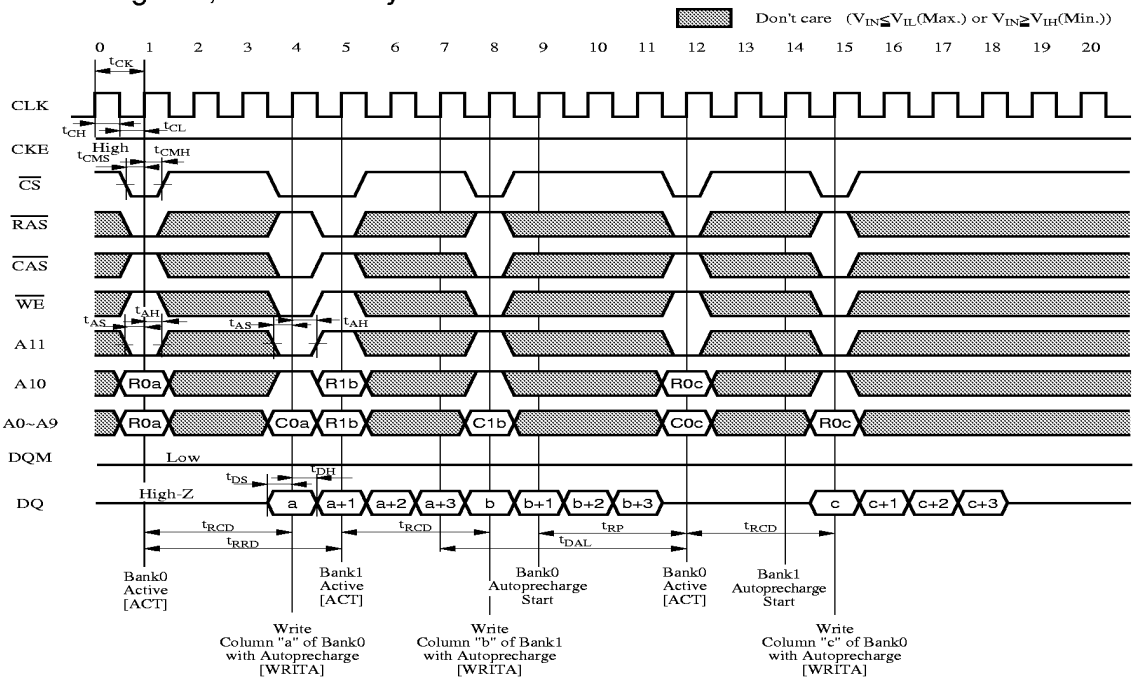
R0/1 : Row Address (Bank 0/1), C0/1 : Column Address (Bank 0/1)

[Read with Autoprecharge (Random Row & Bank Interleave)]
Burst Length=4, CAS Latency=3



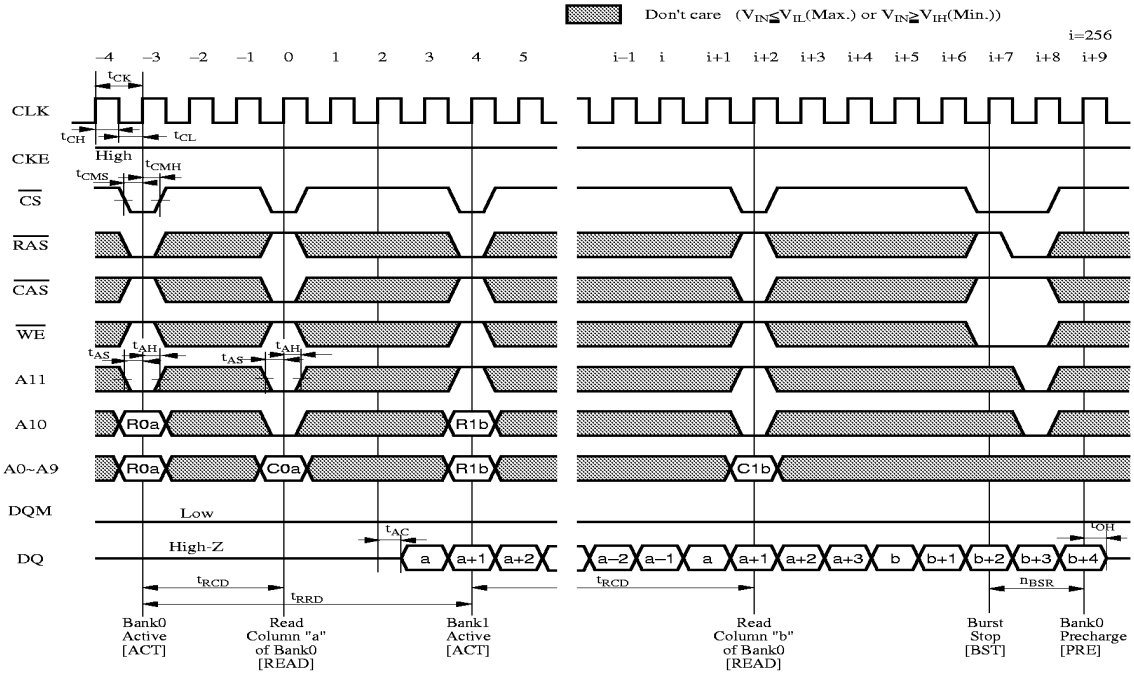
R0/1 : Row Address (Bank 0/1), C0/1 : Column Address (Bank 0/1)

[Write with Autoprecharge (Random Row & Bank Interleave)]
Burst Length=4, CAS Latency=3



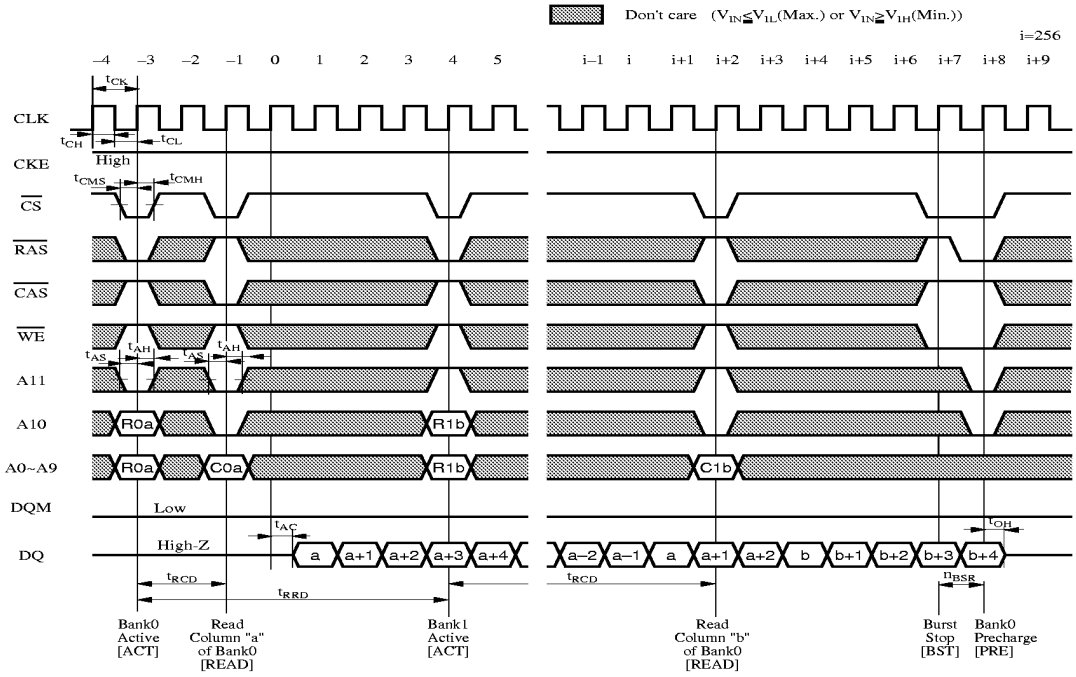
R0/1 : Row Address (Bank 0/1), C0/1 : Column Address (Bank 0/1)

[Full Page Read] Burst Length= Full Page, CAS Latency=3



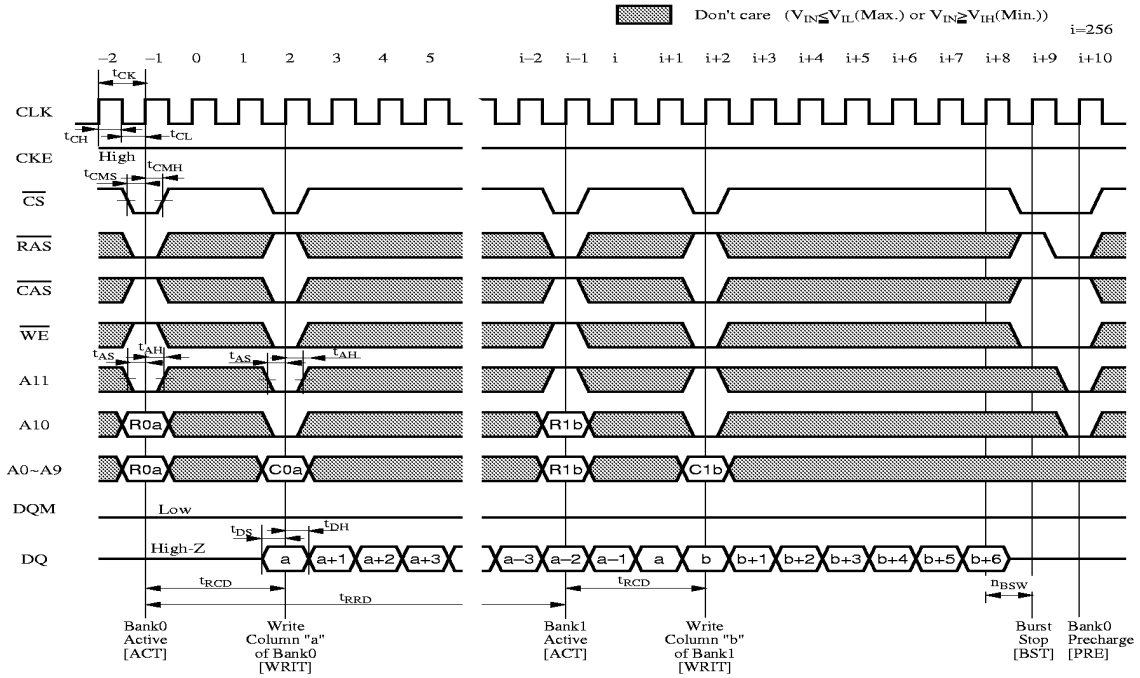
R0/1 : Row Address (Bank 0/1), C0/1 : Column Address (Bank 0/1)

[Full Page Read] Burst Length= Full Page, CAS Latency=2



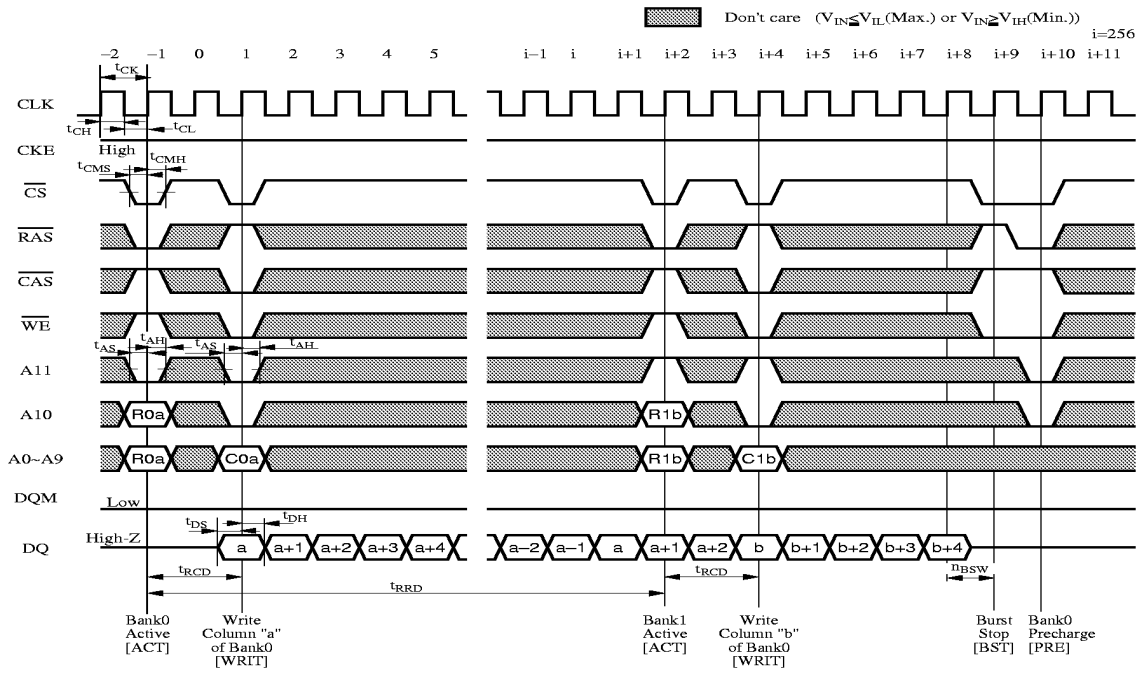
R0/1 : Row Address (Bank 0/1), C0/1 : Column Address (Bank 0/1)

[Full Page Write] Burst Length=Full Page, CAS Latency=3



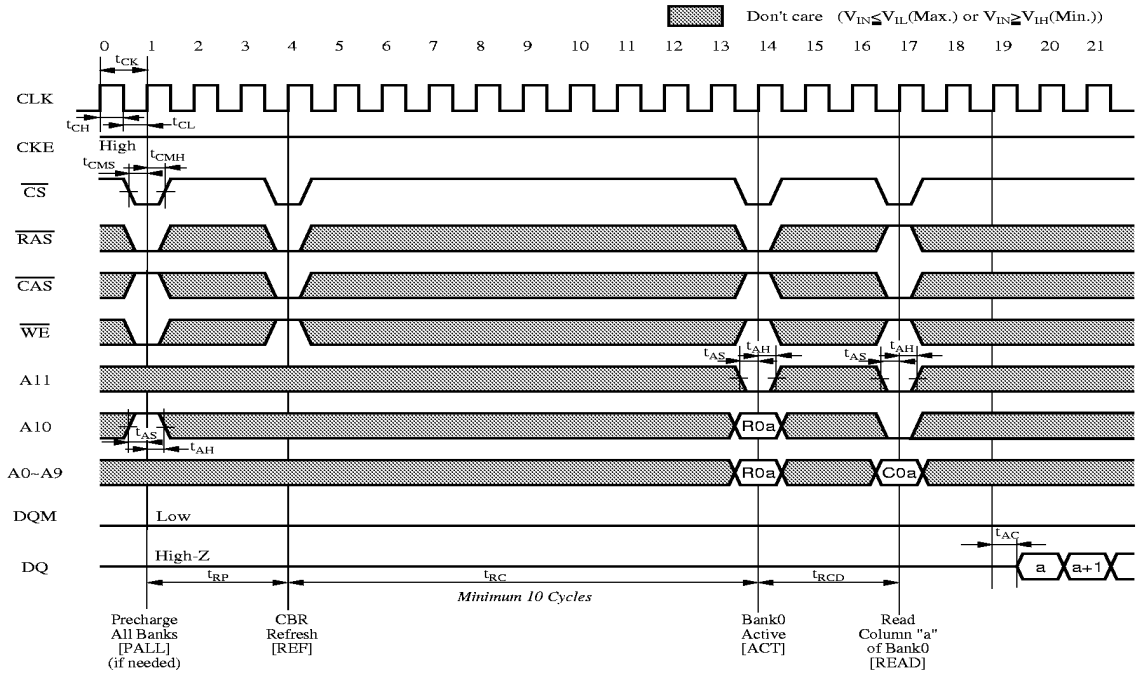
R0/1 : Row Address (Bank 0/1), C0/1 : Column Address (Bank 0/1)

[Full Page Write] Burst Length=Full Page, CAS Latency=2



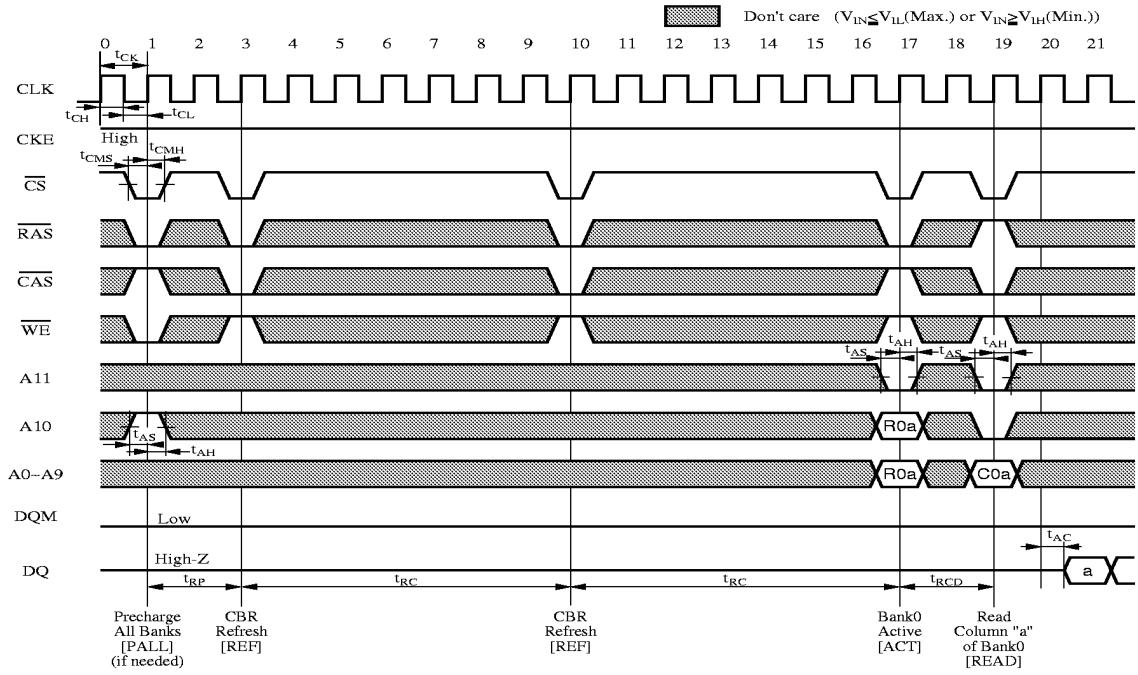
R0/1 : Row Address (Bank 0/1), C0/1 : Column Address (Bank 0/1)

[CBR (Auto) Refresh] CAS Latency=3



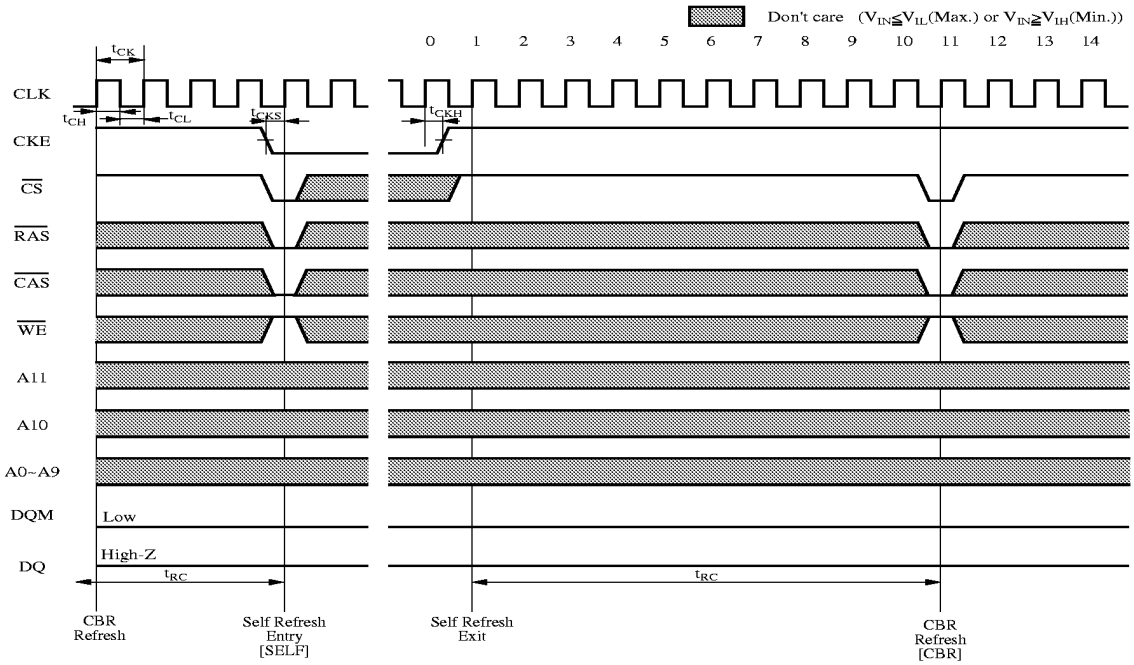
R0 : Row Address (Bank 0), C0 : Column Address (Bank 0)

[CBR (Auto) Refresh] CAS Latency=2



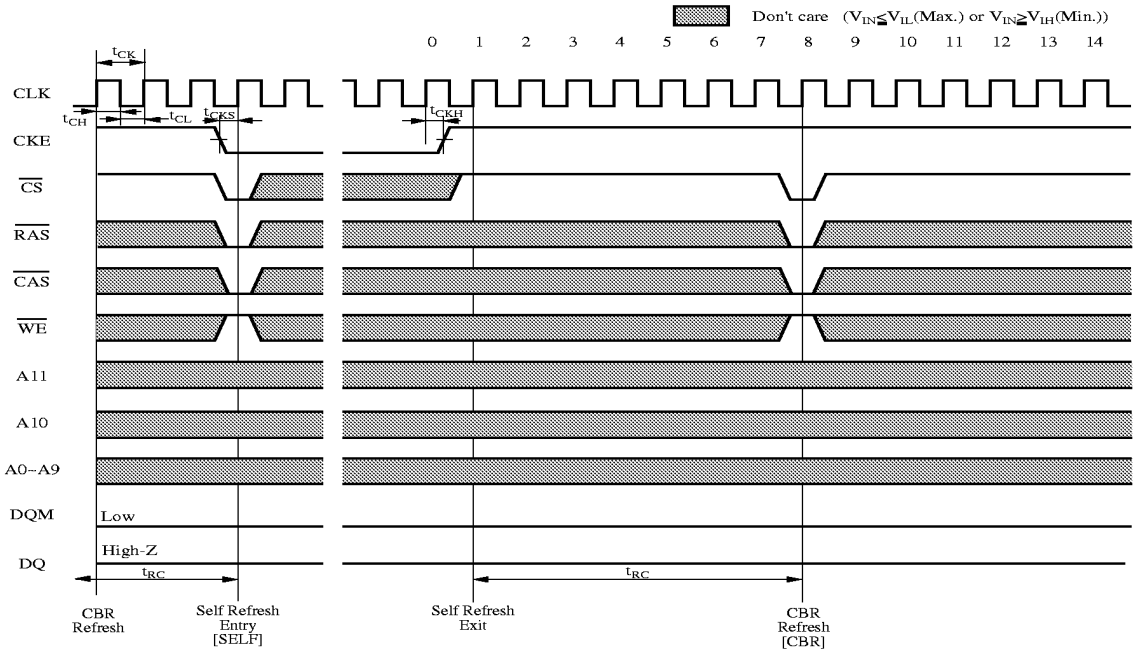
R0 : Row Address (Bank 0), C0 : Column Address (Bank 0)

[Self Refresh] CAS Latency=3



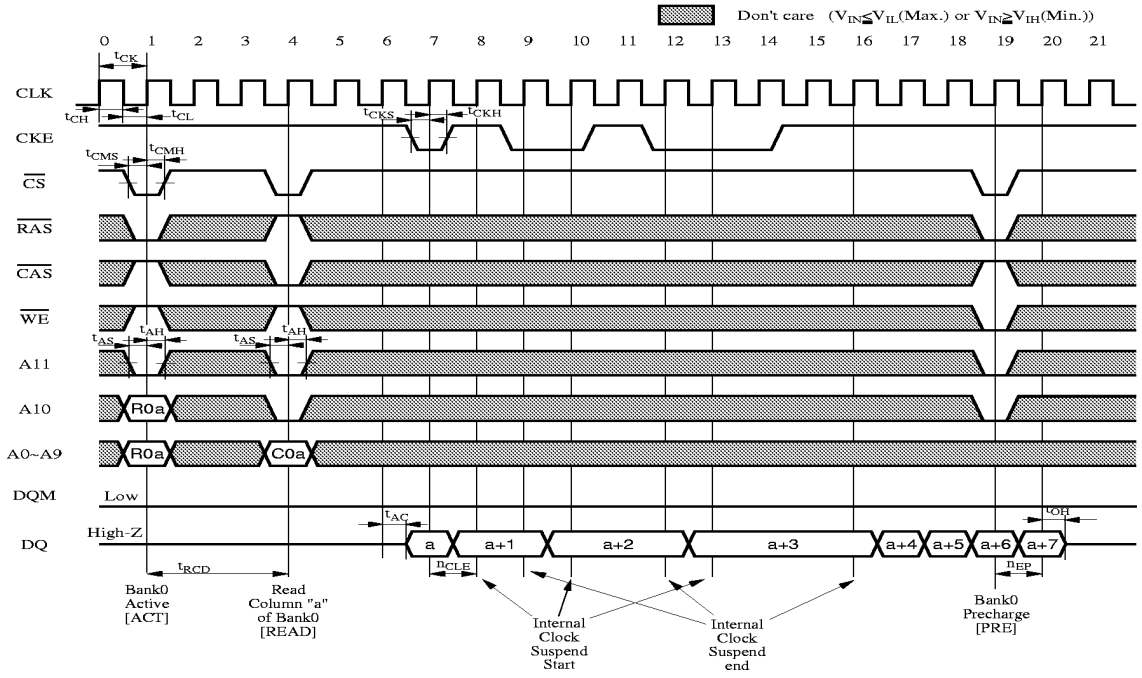
R0 : Row Address (Bank 0), C0 : Column Address (Bank 0)

[Self Refresh] CAS Latency=2



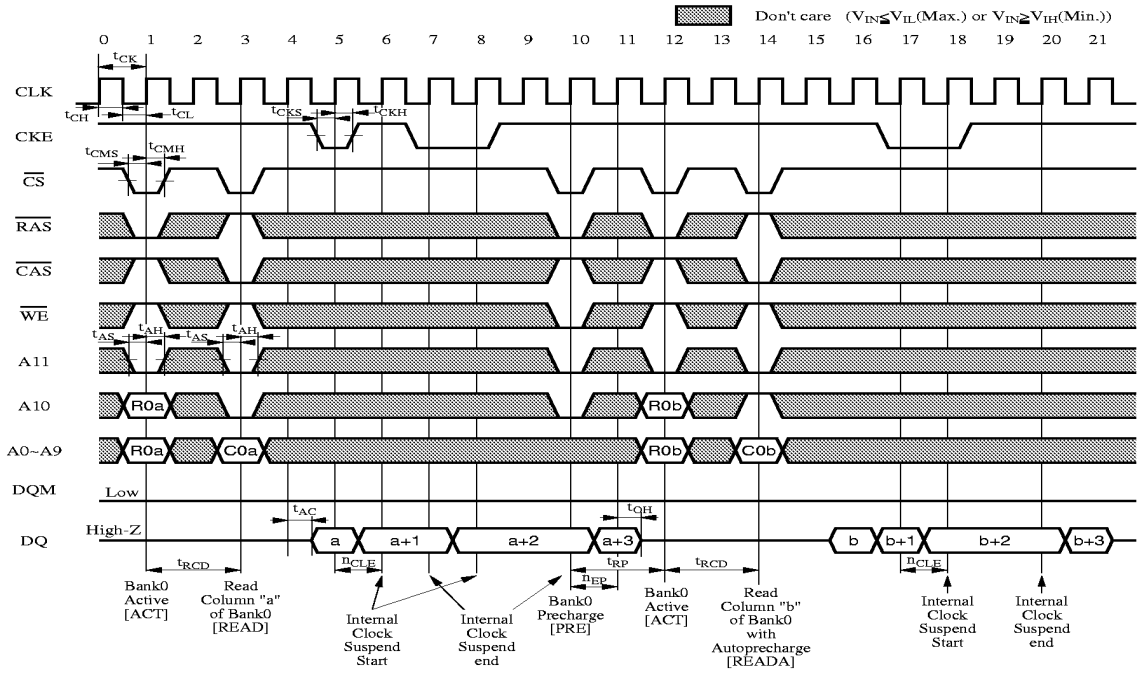
R0 : Row Address (Bank 0), C0 : Column Address (Bank 0)

[Clock Suspend (during Burst Read)] Burst Length=8, CAS Latency=3



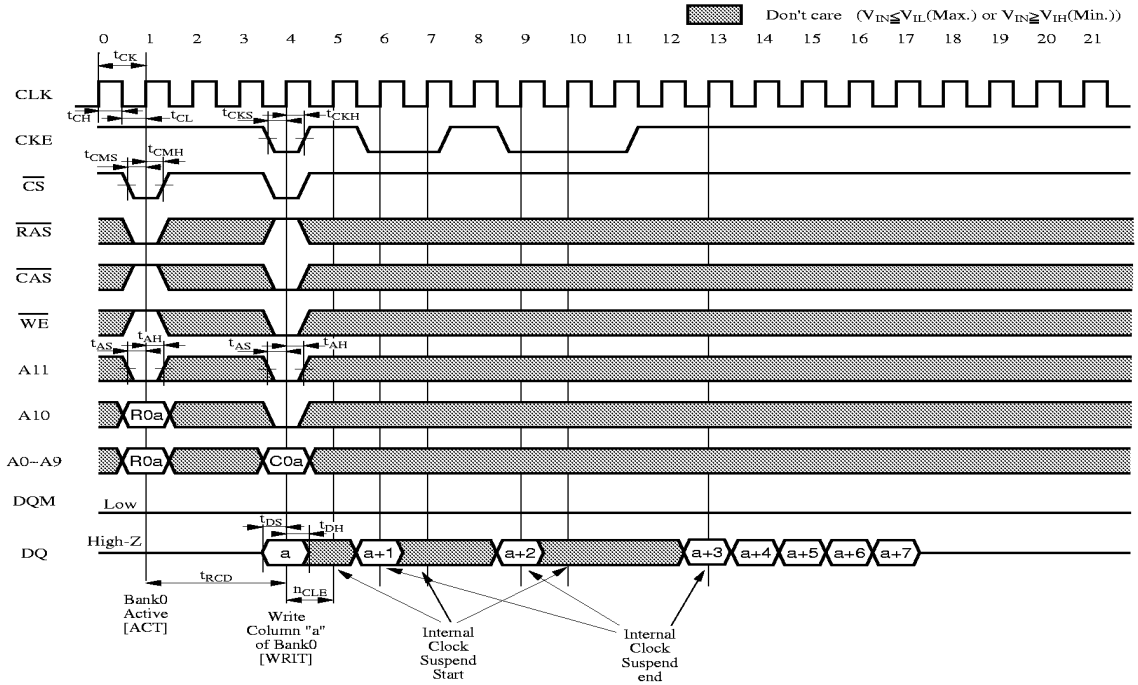
R0 : Row Address (Bank0), C0 : Column Address (Bank0)

[Clock Suspend (during Burst Read)] Burst Length=4, CAS Latency=2



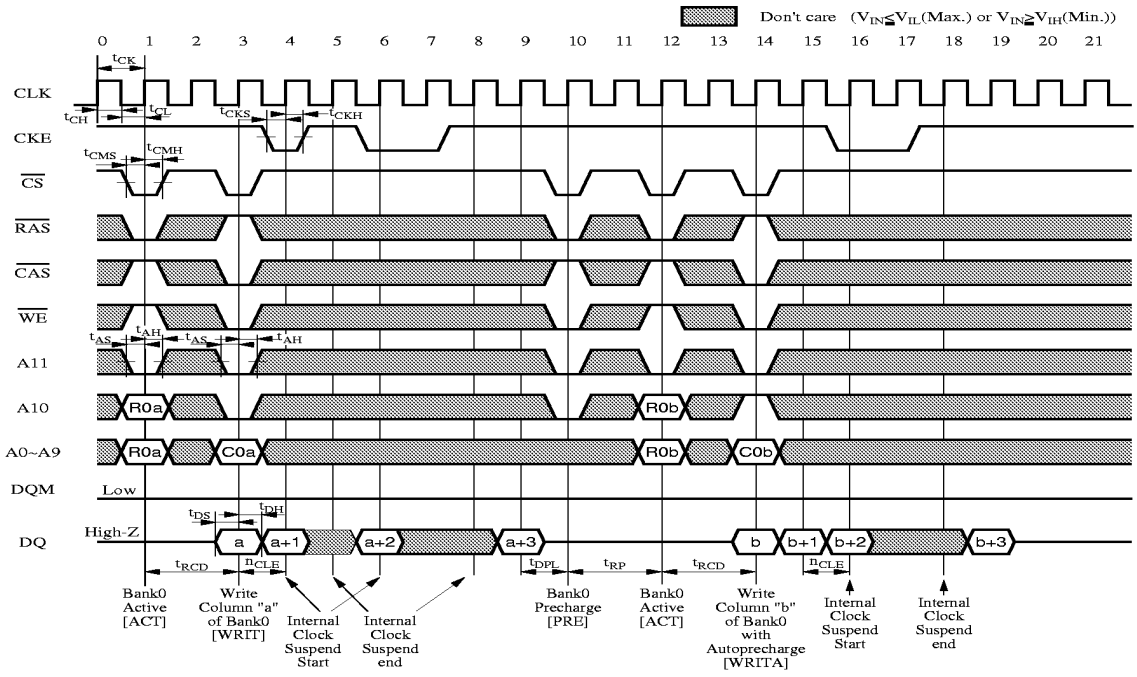
R0 : Row Address (Bank0), C0 : Column Address (Bank0)

[Clock Suspend (during Burst Write)] Burst Length=8, CAS Latency=3



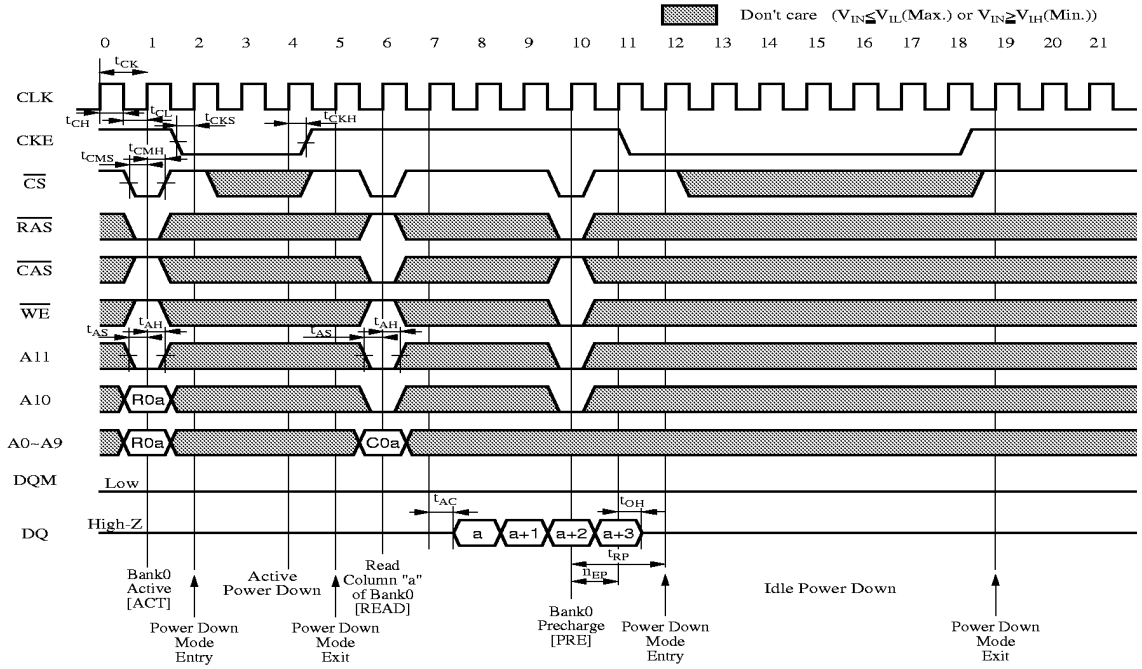
R0 : Row Address (Bank0), C0 : Column Address (Bank0)

[Clock Suspend (during Burst Write)] Burst Length=4, CAS Latency=2



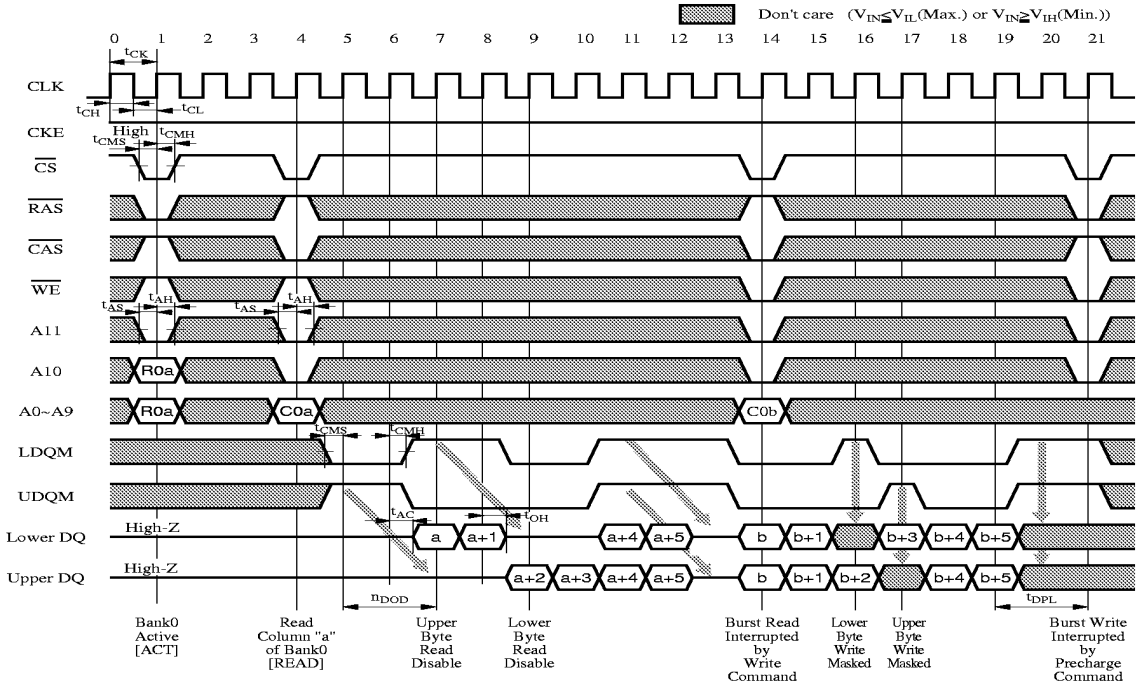
R0 : Row Address (Bank0), C0 : Column Address (Bank0)

[Power Down Mode] Burst Length=4, CAS Latency=2



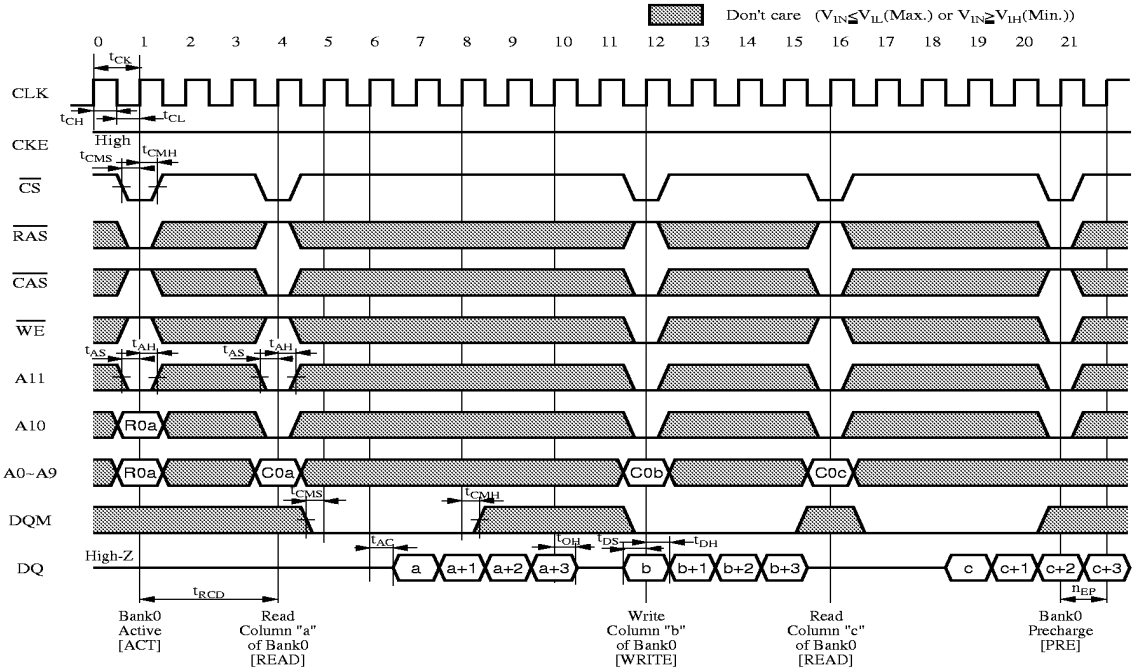
R0 : Row Address (Bank0), C0 : Column Address (Bank0)

[Byte Mask Control] Burst Length≧8, CAS Latency=3



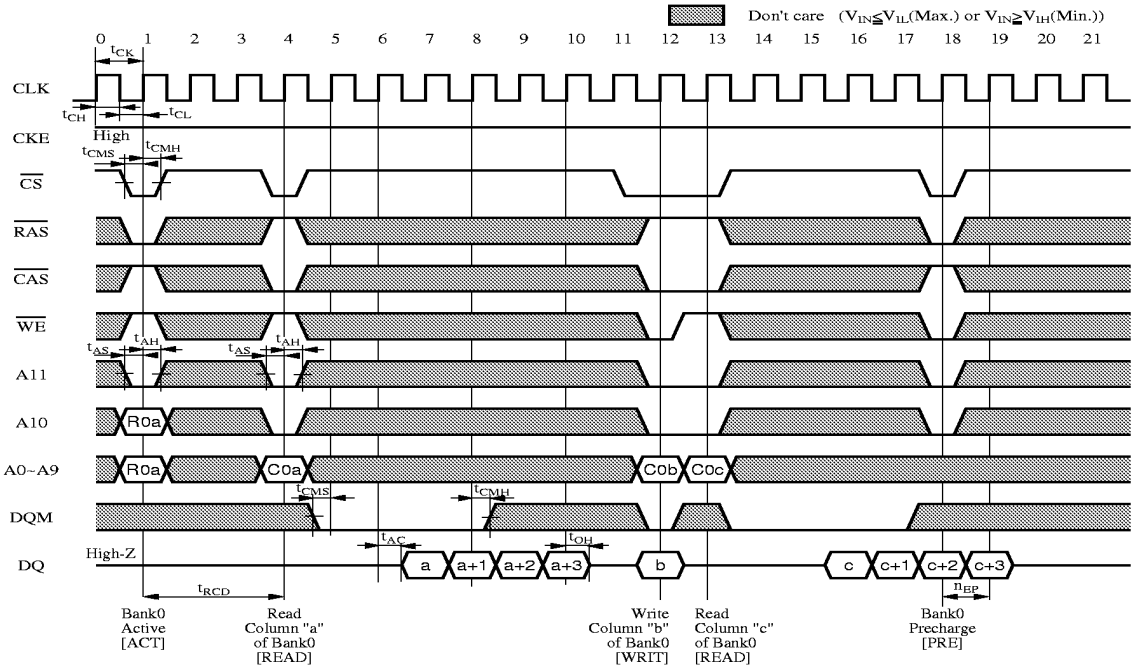
R0 : Row Address (Bank0), C0 : Column Address (Bank0)

[Burst Read & Burst Write] Burst Length=4, CAS Latency=3



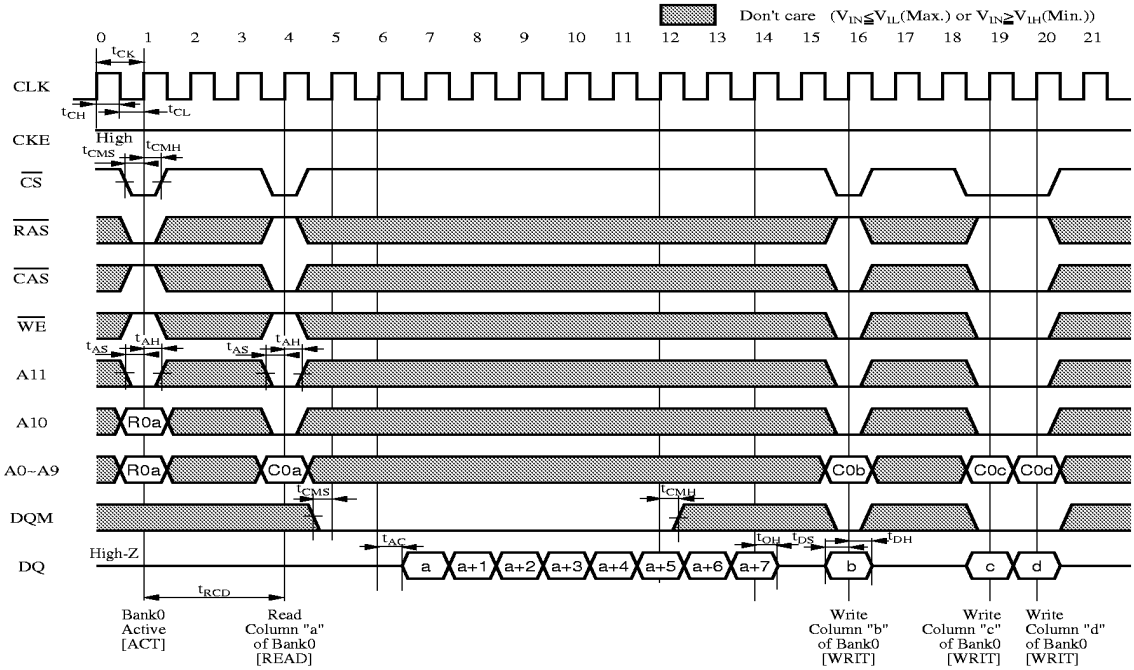
R0 : Row Address (Bank 0), C0 : Column Address (Bank 0)

[Burst Read & Single Write] Burst Length=4, CAS Latency=3



P0 : Row Address (Bank 0), C0 : Column Address (Bank 0)

[Burst Read & Single Write] Burst Length=8, CAS Latency=3



R0 : Row Address (Bank 0), C0 : Column Address (Bank 0)