FEATURES

- Form, Fit, and Function Compatible with the Intel^a 8237A and Harris^a 82C37A
- Packaging options available: 40 Pin Plastic Dip or 44 Pin Plastic Leaded Chip Carrier
- Static Read/Write or Handshaking Modes
- Direct Bit Set/Reset Capability
- Memory-to-Memory Transfers

The IA8237 uses **innovASIC**'s innovative new f^3 **Program** to provide industry with parts that other vendors have declared obsolete. By specifying parts through this program a customer is assured of never having a component become obsolete again. This advanced information sheet assumes the original part has been designed in, and so provides a summary of capabilities only. For new designs contact **innovASIC** for more detailed information.

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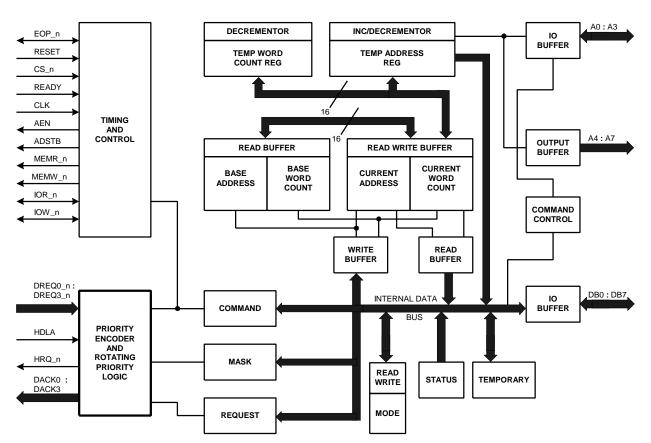
> MEMR_n IOW_n IOR_n IOR_n ↔ (1) MEMW (40) ➡ A7 READY IA8237 ö EOP IOW_n ↔ (2) (39) → A6 40 Pin DIP A7 A6 A5 **A**4 ż MEMR_n 🔺 (3) (38) → A5 1 MEMW_n 🔶 (4) (37) → A4 (6)
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> (7) N. C. (5) (44) (43) (42) (41) (40) (36) ←→ EOP_n N. C. (7) READY -(6) (39) 🔶 A3 (35) **←→** A3 N. C. (8) HLDA (7) (38) + A2 (34) 🔸 🔶 A2 HLDA -(9) ADSTB -(8) (37) + A1 (33) **4 →** A1 IA8237 ADSTB + (10) (36) 📥 A0 AEN 🔶 (9) ♦ A0 (32) 44 Pin LCC AEN 🔶 (11) HRQ 🔶 (10) - VCC (35) - VCC (31) CS_n → (11) → DB0 HRQ 🗕 (12) (34) - DB0 (30) CS_n → (13) CLK -(12) (29) ← DB1 (33) + DB1 RESET (13) → DB2 CLK -(14) (32) DB2 (28) DACK2 🛶 RESET -(15) (31) ← DB3 (14) ←► DB3 (27) DACK2 🗲 (16) DACK3 🔶 (30) DB4 (15)← DB4 (26) (17) DREQ3 (16) DACK0 N. C. (29) N. C. (25) DREQ2 -(17) DACK1 (18) (24) (19) (20) (21) (22) (22) (23) (23) (23) (23) (25) (26) (26) (27) (28) (28) DREQ1 -(18) (23) ◆ DB5 \$ 1 \$ ŧ ţ DREQ0 -(19) (22) ←→ DB6 DREQ3 DREQ2 DACK3 DREQ1 DREQ0 VSS DB7 DB6 DB5 DACK1 DACK0 (21) ←→ DB7 VSS (20)

Package Pinout

IA8237 Programmable DMA Controller

The IA8237 is a programmable direct memory access (DMA) mega-function designed to be functionally equivalent to the Intel 8237A and Harris 82C37A devices. The A8237 controls data transfers between memory and peripherals, memory-to-memory transfers, and block memory initialization. Four independently programmable channels are available, and requests may be generated via hardware or software.

A block diagram is shown in Figure 1.



Functional Block Diagram Figure 1

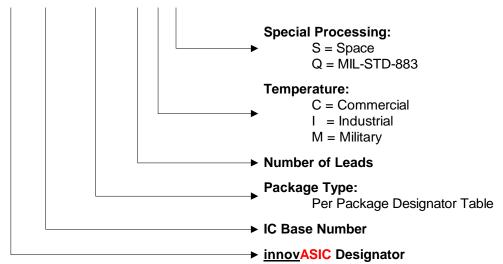
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IA8237 Programmable DMA Controller

Qualification Levels

Table 1	·
Part Number	Environmental/ Qual Level
IA8237-PDW40C	Commercial
IA8237-PLC44C	Commercial
IA8237-PDW40I	Industrial
IA8237-PLC44I	Industrial

The following diagram depicts the **innovASIC** Product Identification Number.



IAXXXXX-PPPPNNNT/SP

Package Designator Table

Package Type	<u>innov</u> ASIC Designator
Ceramic side brazed Dual In-line	CDB
Cerdip with window	CDW
Ceramic leaded chip carrier	CLC
Cerdip without window	CD
Ceramic leadless chip carrier	CLL
PLCC	PLC
Plastic DIP standard (300 mil)	PD
Plastic DIP standard (600 mil)	PDW
Plastic metric quad flat pack	PQF
Plastic thin quad flat pack	PTQ
Skinny Cerdip	CDS
Small outline plastic gull-wing(150 mil body)	PSO
Small outline medium plastic gull-wing (207 mil body)	PSM
Small outline narrow plastic gull wing (150 mil body)	PSN
Small outline wide plastic gull wing (300 mil body)	PSW
Skinny Plastic Dip	PDS
Shrink small outline plastic (5.3mm .208 body)	PS
Thin shrink small outline plastic	PTS
Small outline large plastic gull wing (330 mil body)	PSL
Thin small outline plastic gull-wing (8 x 20mm) [TSOP]	PST
PGA	CPGA
BGA	CBGA

Contact **<u>innovASIC</u>** for other package and processing options.