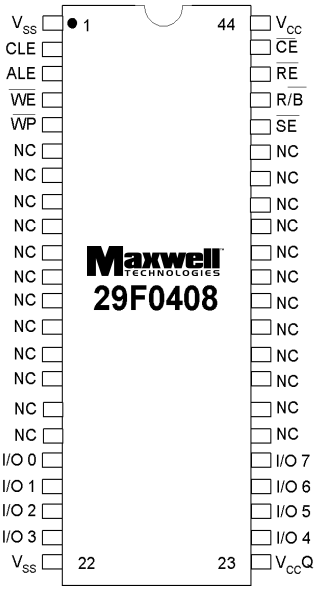
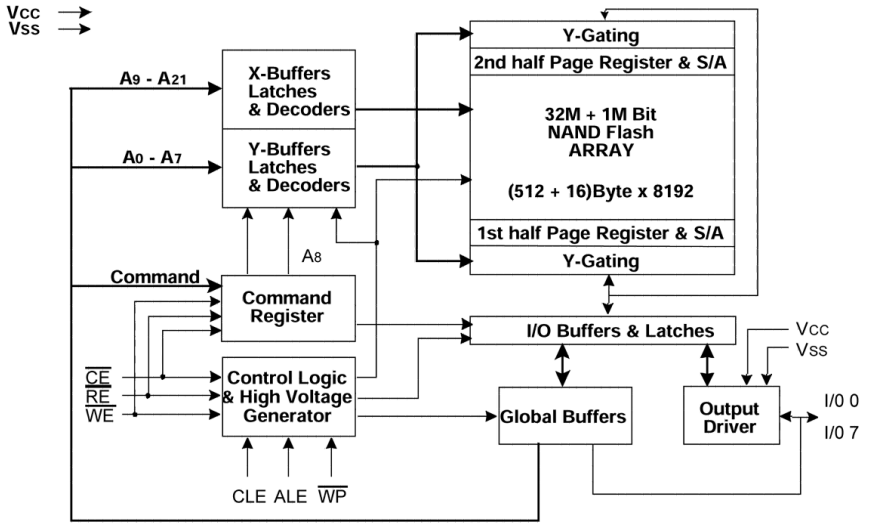
29F0408
32 Megabit (4M x 8-Bit) Flash Memory





Logic Diagram

FEATURES:

- Single 5.0 V supply
- Excellent Single Event Effect
  - SEL_{TH}: > 60 MeV/mg/cm^2
  - SEU_{TH}: = 37 MeV/mg/cm^2
  - SEU saturated cross section: 2E-6 cm^2/bit
- Organization:
  - Memory cell array: (4M + 128k) bit x 8bit
  - Data register: (512 + 16) bit x 8bit
- Automatic program and erase
  - Page program: (512 + 16) Byte
  - Block erase: (8K + 256) Byte
  - Status register
- 528-Byte page read operation
  - Random access: 10 µs (max)
  - Serial page access: 50 ns (min)
- Fast write cycle time
  - Program time: 250 µs (typ)
  - Block erase time: 2 ms (typ)
- Command/address/data multiplexed I/O port
- Hardware data protection
  - Program/erase lockout during power transitions
- Reliable CMOS floating-gate technology
  - Endurance: 1,000,000 program/erase cycles
  - Data retention: 10 years
- Command register operation
- 44 pin flat package

DESCRIPTION:

Maxwell Technologies' 29F0408 high-performance flash memory. The 29F0408 is a 4M (4,194,304) x 8-bit NAND Flash Memory with a spare 128K (131,072) x 8-bit. A program operation programs the 528-byte page in 250 µs and an erase operation can be performed in 2 ms on an 8K-byte block. Data within a page can be read out at 50 ns cycle time per byte. The on-chip write controller automates all program and erase functions, including pulse repetition, where required, and internal verify and margining of data. Even write-intensive systems can take advantage of the 29F0408's extended reliability of 1,000,000 program/erase cycles by providing either ECC (Error Correction Code) or real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications. The spare 16 bytes of a page combined with the other 512 bytes can be utilized by system-level ECC. The 29F0408 is an optimum solution for large non-volatile storage applications such as solid state storage, digital voice recorder, digital still camera and other portable applications requiring nonvolatility.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. Capable of surviving in space environments, the 29F0408 is ideal for satellite, spacecraft, and space probe missions. It is available with packaging and screening up to Class S.

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TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
2	Command Latch Enable (CLE)	The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
3	Address Latch Enable (ALE)	The ALE input controls the path activation for address and input data to the internal address/data register. Addresses are latched on the rising edge or $\overline{WE}$ with ALE high, and input data is latched when ALE is low.
43	Chip Enable ($\overline{CE}$)	The $\overline{CE}$ input is the device selection control. When $\overline{CE}$ goes high during a read operation, the device is returned to standby mode. However, when the device is in the busy state during program or erase, $\overline{CE}$ high is ignored, and does not return the device to standby mode.
4	Write Enable ($\overline{WE}$)	The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
42	Read Enable ($\overline{RE}$)	The $\overline{RE}$ inputs is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE which also increments the internal column address counter by one.
40	Spare Area Enable ($\overline{SE}$)	The $\overline{SE}$ input controls the spare area selection when $\overline{SE}$ is high, the device is deselected the spare area during Read1, Sequential data input and page Program.
18-21, 24-27	I/O Port: I/O0 ~ I/O7	The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to High-Z when the chip is deselected or when the outputs are disabled.
5	Write Protect ($\overline{WP}$)	The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
41	Read/Busy (R/$\overline{B}$)	The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to High-Z condition when the chip is deselected or when outputs are disabled.
6-17, 28-39	NC	Not Connected
1, 22	V_{SS}	Ground
44	V_{CC}	Supply Voltage
23	$V_{CC}Q$	Output Buffer Voltage

TABLE 2. 29F0408 ABSOLUTE MAXIMUM RATINGS [1,2]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}	-0.6	7.0	V
Operating Temperature	T_{BIAS}	-40	125	˚C
Storage temperature	T_{STG}	-65	150	˚C
Short circuit output current	I_{OS}	--	5	mA

1. Minimum DC voltage is -0.3 V on input/output pins. During transitions, this level may undershoot to -2.0 V for periods < 30 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.3 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods < 20 ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.

TABLE 3. 29F0408 RECOMMENDED OPERATING CONDITIONS

(VOLTAGE REFERENCE TO GND, T_A = -40 TO 125˚C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Supply voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	--	V_{CC} ±0.5	V
Input Low Voltage	V_{IL}	-0.3	--	0.8	V

TABLE 4. DELTA LIMITS

PARAMTER	CONDITION
$I_{CC}1$	±10%
$I_{SB}1$	±10%
$I_{SB}2$	±10%

TABLE 5. 29F0408 AC TEST CONDITION

(V_{CC} = 5 V ± 10%, T_A = -40 TO 125˚C, UNLESS OTHERWISE NOTED)

PARAMETER	MIN	MAX	UNIT
Input pulse levels	0.4	2.6	V
Input rise times	--	5.0	ns
Input and output timing levels	0.8	2.0	V

TABLE 6. 29F0408 DC AND OPERATING CHARACTERISTICS

(V_{CC} = 5 V ± 10%, T_A = -40 TO 125°C, UNLESS OTHERWISE NOTED)

PARAMETER		SYMBOL	TEST CONDITIONS		SUBGROUPS	MIN	TYP	MAX	UNIT
Operating current	Sequential read	I_{CC1}	t_{CYCLE} = 50 ns	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA	1, 2, 3	--	15	30	mA
	Program	I_{CC2}			1, 2, 3	--	15	30	
	Erase	I_{CC3}			1, 2, 3	--	25	40	
Stand-by-current (TTL)		I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{WP}$ = $\overline{SE}$ = 0V/V_{CC}		1, 2, 3	--	--	1	mA
Stand-by current (CMOS)		I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2, $\overline{WP}$ = $\overline{SE}$ = 0V/V_{CC}		1, 2, 3	--	10	100	uA
Input leakage current		I_{LI}	V_{IN} = 0 to 5.5 V		1, 2, 3	-10	--	10	uA
Output leakage current		I_{LO}	V_{OUT} = 0 to 5.5 V		1, 2, 3	-10	--	10	uA
Input high voltage, all inputs		V_{IH}			1, 2, 3	2.0	--	--	V
Input low voltage, all inputs		V_{IL}			1, 2, 3	--	--	0.8	V
Output high voltage level		V_{OH}	I_{OH} = -400 µA		1, 2, 3	2.4	--	--	V
Output low voltage level		V_{OL}	I_{OL} = 2.1 mA		1, 2, 3	--	--	0.4	V
Outuput low current (R/B)		I_{OL} (R/B)	V_{OL} = 0.4 V		1, 2, 3	8	10	--	mA

TABLE 7. 29F0408 CAPACITANCE [1]

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input/Output capacitance	$C_{I/O}$	V_{IL} = 0V	--	10	pF
Input capacitance	C_{IN}	V_{IN} = 0V	--	10	pF

1. Capacitance Guarenteed by design.

TABLE 8. 29F0408 MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{SE}$	$\overline{WP}$	MODE	
H	L	L		H	X	X	Read Mode	Command Input
L	H	L		H	X	X		Address Input (3 Clock)
H	L	L		H	X	H	Write Mode	Command Input
L	H	L		H	X	H		Address Input (3 Clock)
L	L	L		H	L/H [1]	H	Data Input	

TABLE 8. 29F0408 MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{SE}$	$\overline{WP}$	MODE
L	L	L	H	↓	L/H [1]	X	Sequential Read & Data Output
L	L	L	H	H	L/H [1]	X	During Read (Busy)
X	X	X	X	X	L/H [1]	H	During Program (Busy)
X	X	X	X	X	X	H	During Erase (Busy)
X	X [2]	X	X	X	X	L	Write Protect
X	X	H	X	X	0V/V_{CC} [3]	0V/V_{CC} [3]	Stand-by

1. When SE is high, spare area is deselected.
2. X can be V_{IL} or V_{IH}.
3. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

TABLE 9. 29F0408 PROGRAM/ERASE CHARACTERISTICS

(V_{CC} = 5 V ± 10%, T_A =-40 TO +125C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program time	t_{PROG}	--	0.25	1.5	ms
Number of partial program cycles in the same page	N_{OP}	--	--	10	cycles
Block erase time	t_{BERS}	--	2	10	ms

TABLE 10. 29F0408 AC TIMING CHARACTERISTICS FOR COMMAND/ADDRESS/DATA INPUT

(V_{CC} = 5 V ± 10%, T_A =-40 TO +125 C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
CLE set-up time	t_{CLS}	9, 10, 11	0	--	ns
CLE hold time	t_{CLH}	9, 10, 11	10	--	ns
$\overline{CE}$ setup time	t_{CS}	9, 10, 11	0	--	ns
$\overline{CE}$ hold time	t_{CH}	9, 10, 11	10	--	ns
$\overline{WE}$ pulse width	t_{WP}	9, 10, 11	25	--	ns
ALE setup time	t_{ALS}	9, 10, 11	0	--	ns
ALE hold time	t_{ALH}	9, 10, 11	10	--	ns
Data setup time	t_{DS}	9, 10, 11	20	--	ns
Data hold time	t_{DH}	9, 10, 11	10	--	ns
Write cycle time	t_{WC}	9, 10, 11	50	--	ns
$\overline{WE}$ high hold time	t_{WH}	9, 10, 11	15	--	ns

TABLE 11. 29F0408 AC CHARACTERISTICS FOR OPERATION

(V_{CC} = 5 V ± 10%, T_A = -40 TO +125˚C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
Data transfer from cell to register	t_R	9, 10, 11	--	10	µs
ALE to $\overline{RE}$ delay (read ID)	t_{AR1}	9, 10, 11	150	--	ns
ALE to $\overline{RE}$ delay (read cycle)	t_{AR2}	9, 10, 11	50	--	ns
$\overline{CE}$ to $\overline{RE}$ delay (ID read)	t_{CR}	9, 10, 11	100	--	ns
Ready to $\overline{RE}$ low[1]	t_{RR}	9, 10, 11	20	--	ns
$\overline{RE}$ pulse width	t_{RP}	9, 10, 11	30	--	ns
$\overline{WE}$ high to busy	t_{WR}	9, 10, 11	--	100	ns
Read cycle time	t_{RC}	9, 10, 11	50	--	ns
$\overline{RE}$ access time	t_{REA}	9, 10, 11	--	35	ns
$\overline{RE}$ high to output Hi-Z	t_{RHZ}	9, 10, 11	15	30	ns
$\overline{CE}$ high to output Hi-Z	t_{CHZ}	9, 10, 11	--	20	ns
$\overline{RE}$ high hold time	t_{REH}	9, 10, 11	15	--	ns
Output Hi-Z to $\overline{RE}$ low	t_{IR}	9, 10, 11	0	--	ns
Last $\overline{RE}$ high to busy (at sequential read)	t_{RB}	9, 10, 11	--	100	ns
$\overline{CE}$ high to ready (in case of interception by CE at read) [2]	t_{CRY}	9, 10, 11	--	50 + tr (R/$\overline{B}$) [3]	ns
$\overline{CE}$ high hold time (at the last serial read) [4]	t_{CEH}	9, 10, 11	100	--	ns
$\overline{RE}$ low to status output	t_{RSTO}	9, 10, 11	--	35	ns

TABLE 11. 29F0408 AC CHARACTERISTICS FOR OPERATION

(V_{CC} = 5 V ± 10%, T_A = -40 TO +125°C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
$\overline{CE}$ low to status output	t_{CSTO}	9, 10, 11	--	45	ns
$\overline{RE}$ high to $\overline{WE}$ low	RHW_Y	9, 10, 11	0	--	ns
$\overline{WE}$ high to $\overline{RE}$ low	t_{WHR}	9, 10, 11	60	--	ns
$\overline{RE}$ access time (read ID)	t_{READID}	9, 10, 11	--	35	ns
Device resetting time (read/program/erase/after erase suspend)	t_{RST}	9, 10, 11	--	5/10/500	µs

1. Not Tested
2. If $\overline{CE}$ goes high within 30 ns after the rising edge of the last $\overline{RE}$, R/$\overline{B}$ will not return to V_{OL}.
3. The time to Ready depends on the value of the pull-up resistor tied to R/$\overline{B}$ pin.
4. To break the sequential read cycle, $\overline{CE}$ must be held high for longer than t_{CEH}.

TABLE 12. 29F0408 VALID BLOCK [1,2]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Valid Block Number	N_{VB}	502	508	512	Blocks

1. The device may include valid blocks. Invalid blocks are defined as blocks that contain one or more bad bits. Do not try to access these invalid blocks for program and erase. During its lifetime of 10 years and/or 1 million program/erase cycles, the minimum number of valid blocks are guaranteed though its initial number could be reduced. (Refer to following technical note)
2. The 1st block, which is placed on the 00h block address, is guaranteed to be a valid block.

NAND FLASH TECHNICAL NOTES

Invalid Block(s)

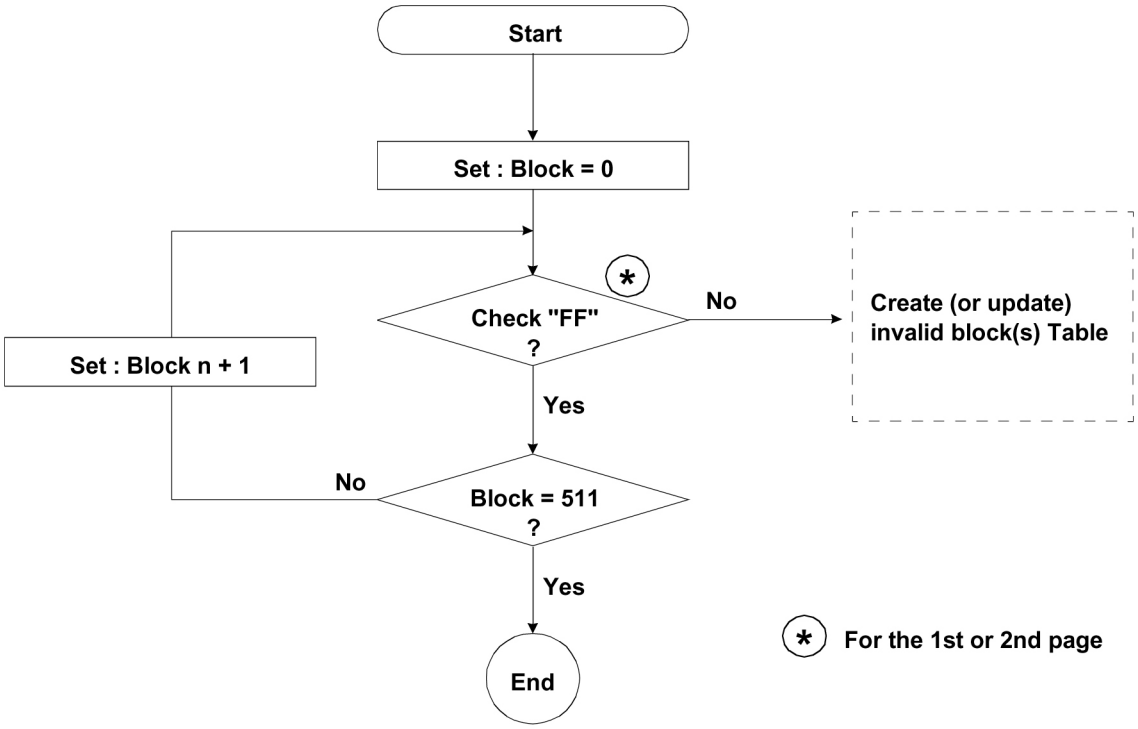
Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by the manufacturer. Typically, an invalid block will contain a single bad bit. The information regarding the invalid block(s) is called as the invalid block information. The invalid block information is written to the 1st or the 2nd page of the invalid block(s) with 00h data. Devices with invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block of the NAND Flash, however, is fully guaranteed to be a valid block.

Identifying Invalid Block(s)

All device locations are erased (FFh) except locations where the invalid block information is written prior to shipping. Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid

block information and create the invalid block table via the following suggested flow chart (Figure 1). Any intentional erasure of the original block information is prohibited.

FIGURE 1. FLOW CHART TO CREATE INVALID BLOCK TABLE



Error in write or read operation

Over its lifetime, the additional invalid blocks may occur. Through the tight process control and intensive testing, additional block failure rate is minimized which is projected below 0.1% until 1 million program/erase cycles. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

FAILURE MODE		DETECTION AND COUNTERMEASURE
Write	Erase failure	Status read after erase Æ Block replacement
	Program failure	Status read after program Æ Block replacement Read back (verify after program) Æ Block replacement or ECC correction
Read	Single bit failure	Verify ECC Æ ECC correction

ECC: Error Correcting Code Æ Hamming Code, etc.

Example. 1-bit correction and 2-bit detection

FIGURE 2. PROGRAM FLOW CHART

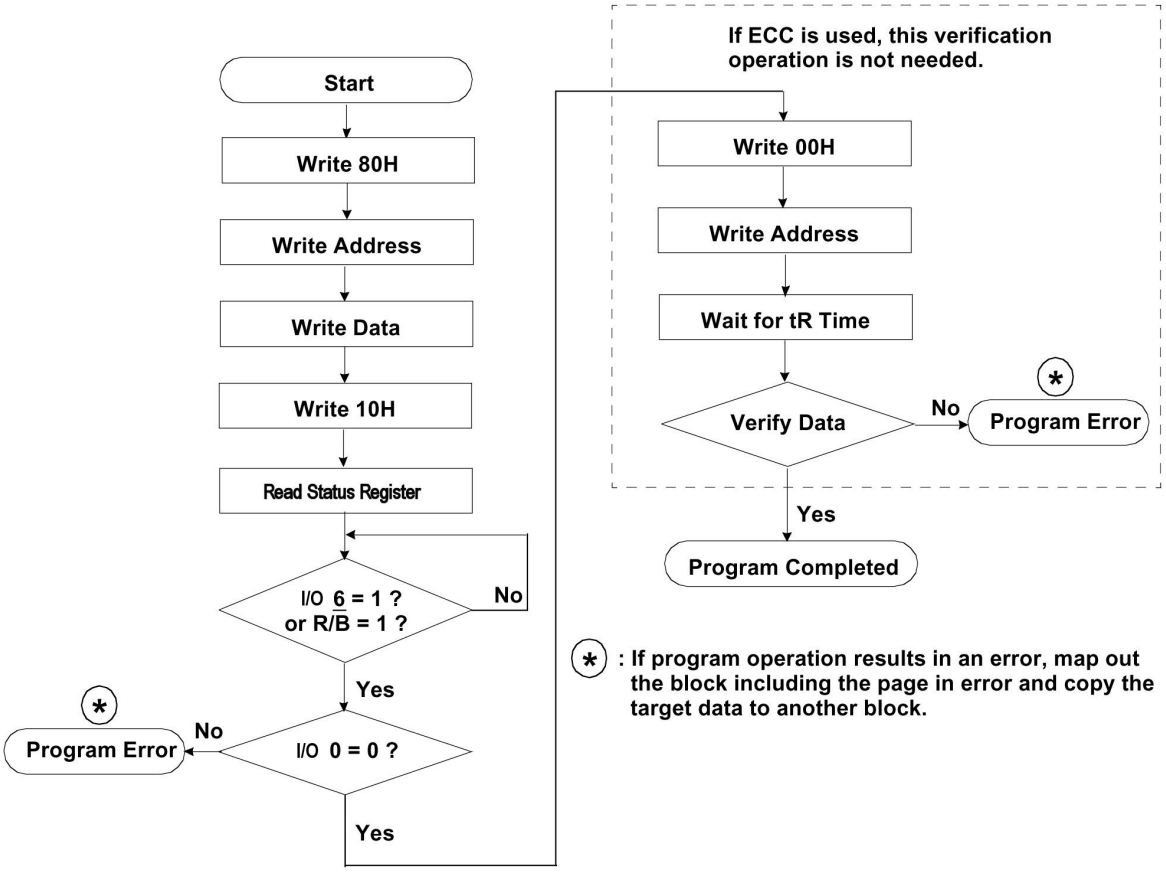


FIGURE 3. ERASE FLOW CHART

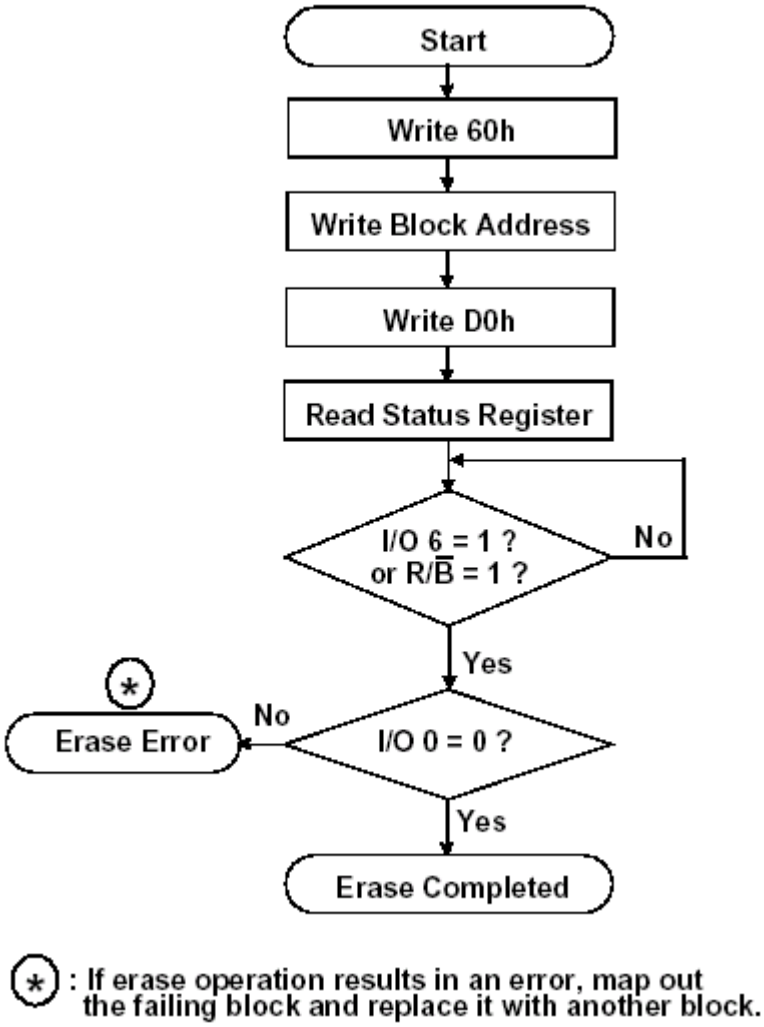


FIGURE 4. READ FLOW CHART

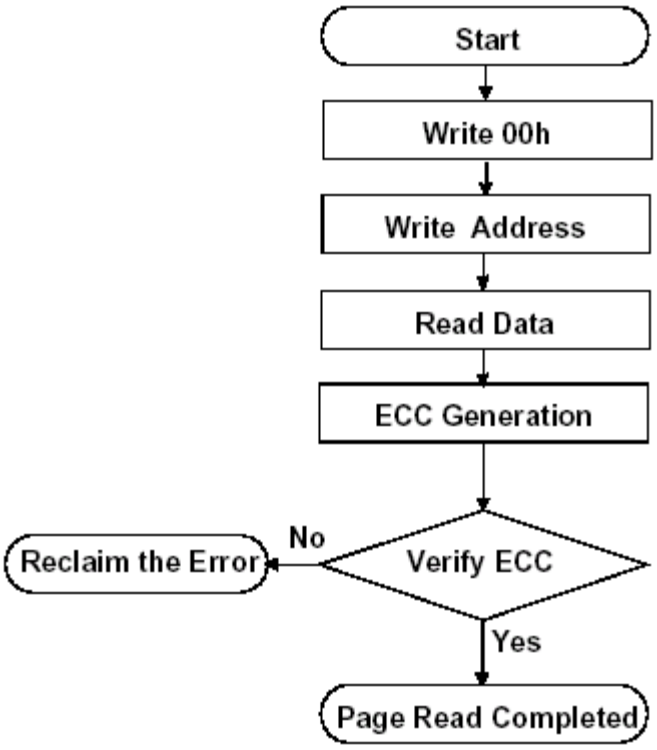
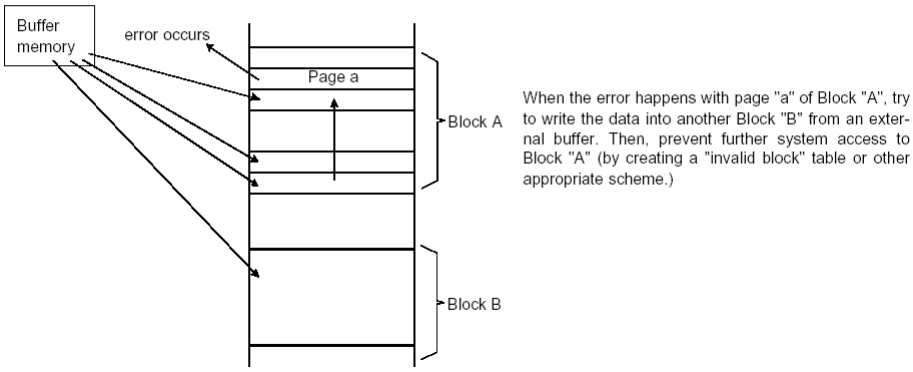


FIGURE 5. BLOCK REPLACEMENT

Block Replacement



Pointer Operation:

The 29F0408 has three modes to set the destination of the pointer. The pointer is set to “A” area by the “00h” command, to “B” area by the “01h” command, and to “C” area by the “50h” command. The Destination Pointer Table shows the destination of the pointer, and the block diagram shows the diagram of its operation.

TABLE 12. DESTINATION OF POINTER TABLE

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

FIGURE 6. BLOCK DIAGRAM OF POINTER OPERATION

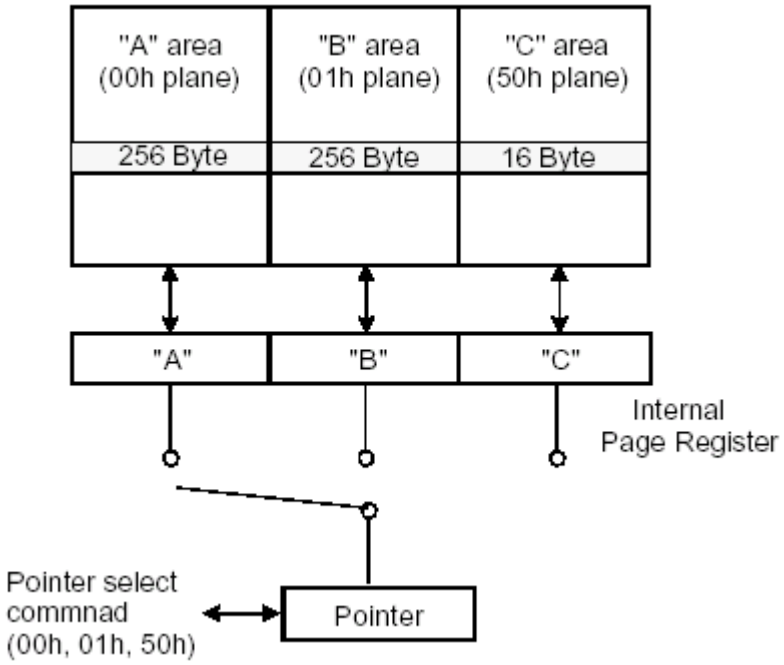


FIGURE 7. EXAMPLES OF PROGRAMMING WITH SUCCESSIVE POINTER OPERATION

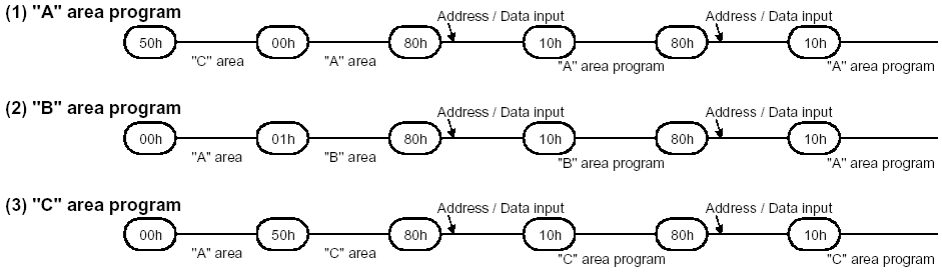


TABLE 13. POINT STATUS AFTER EACH OPERATION

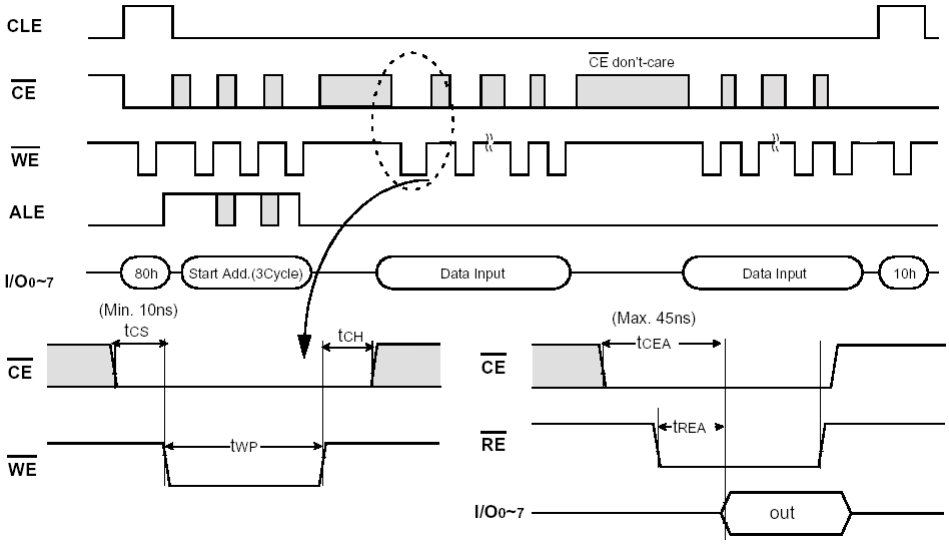
Operation	Pointer status after operation
Program	With previous 00h, Device is set to 00h Plane With previous 01h, Device is set to 00h Plane* With previous 50h, Device is set to 50h Plane
Reset	"00h" Plane("A" area)
Power up	"00h" Plane("A" area)

* 01h command is valid just one time when it is used as a pointer for program/erase.
* Erase operation does not affect the pointer status. Previous pointer status is maintained.

System Interface Using $\overline{CE}$ don't-care.

For a easier system interface, CE may be inactive during the data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating CE during the data-loading and reading would provide significant savings in power consumption.

FIGURE 8. PROGRAM OPERATION WITH CE DON'T CARE



Timing requirements: If $\overline{CE}$ is is exerted high during data-loading, tCS must be minimum 10ns and tWC must be increased accordingly.

Timing requirements: If $\overline{CE}$ is is exerted high during sequentialdata-reading, the falling edge of CE to valid data(tCEA) must be kept greater than 45ns.

FIGURE 9. READ OPERATION WITH $\overline{CE}$ DON'T CARE

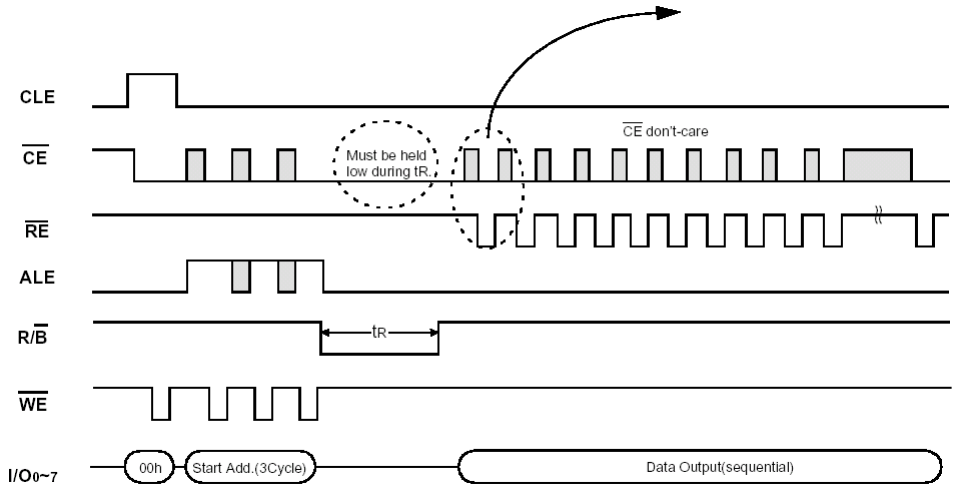


FIGURE 10. COMMAND LATCH CYCLE

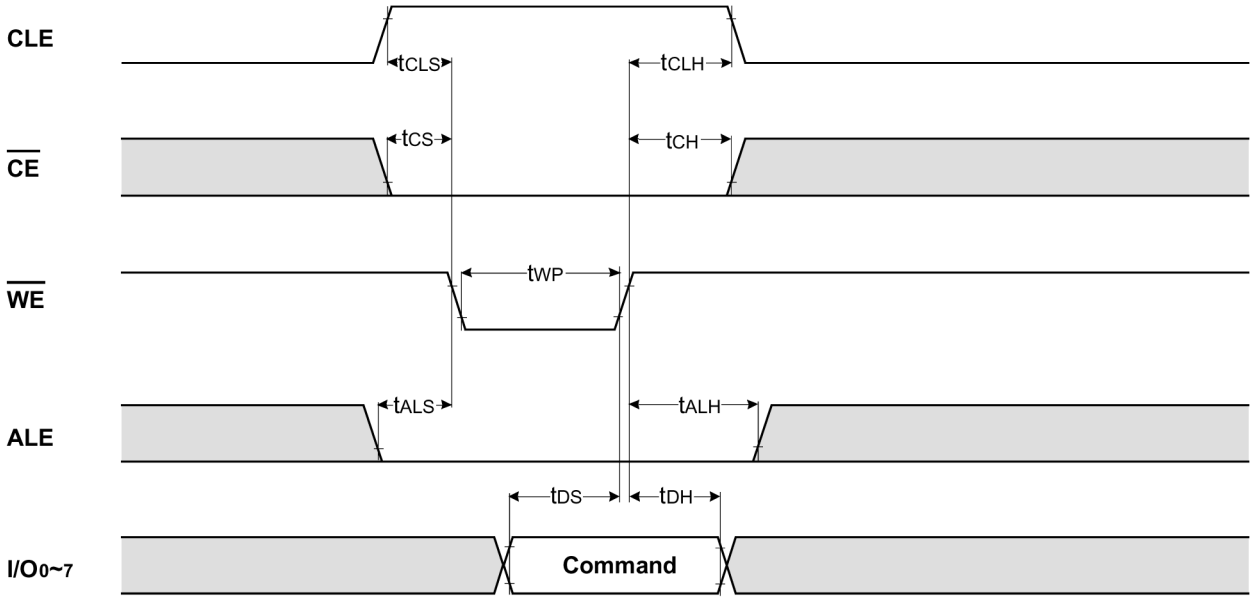


FIGURE 11. ADDRESS LATCH CYCLE

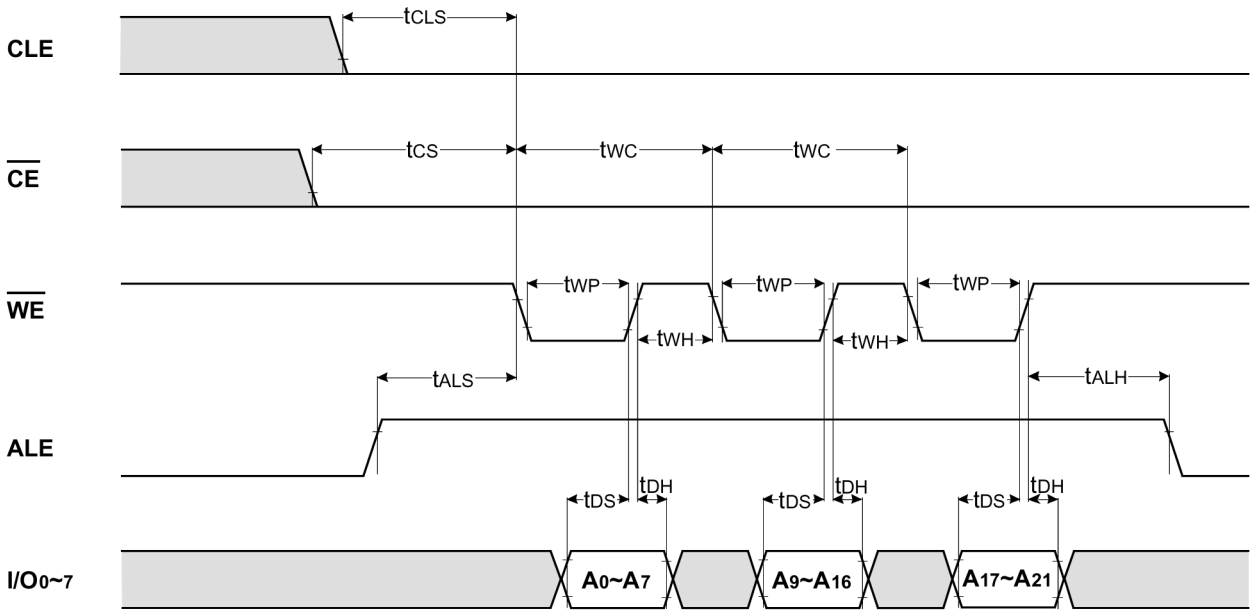


FIGURE 12. INPUT DATA LATCH CYCLE

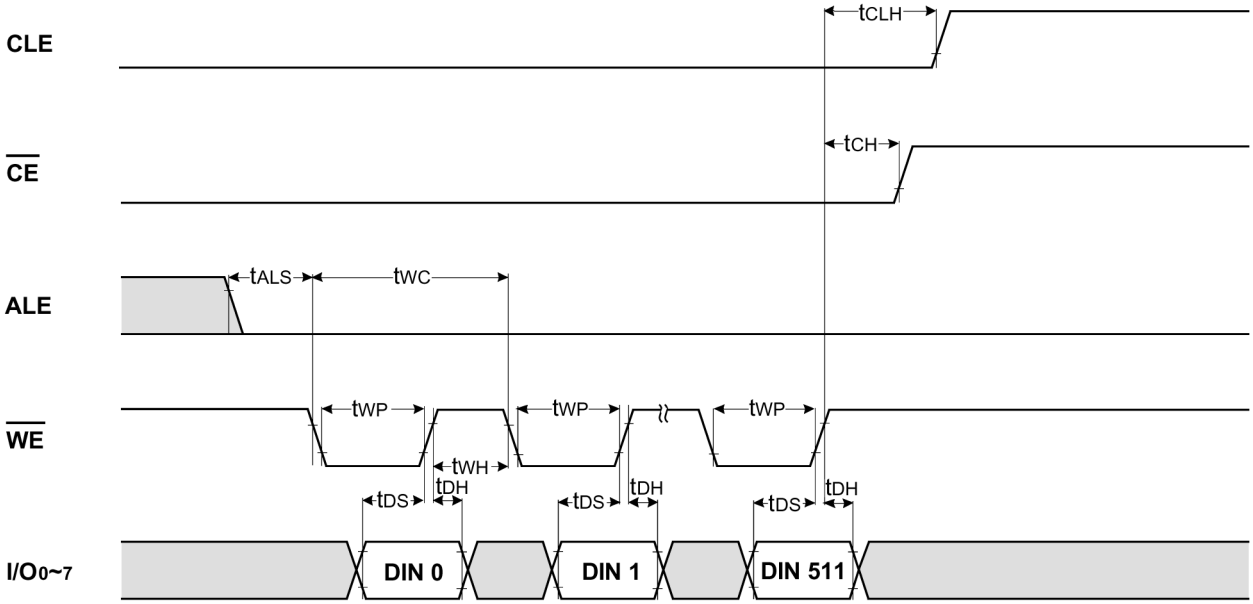


FIGURE 13. SEQUENTIAL OUT CYCLE AFTER READ (CLE = L, $\overline{WE}$ = H, ALE = L)

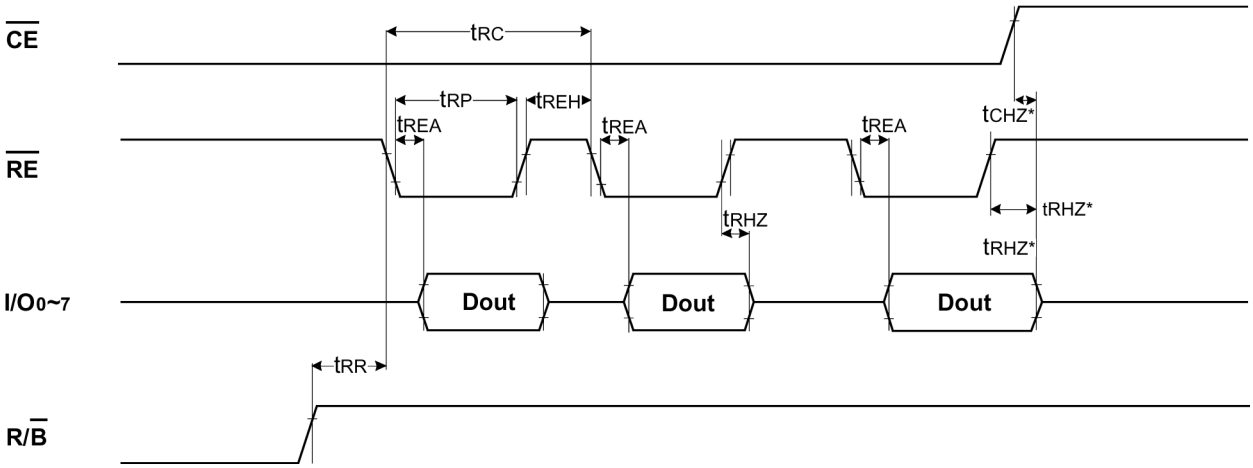


FIGURE 14. STATUS READ CYCLE

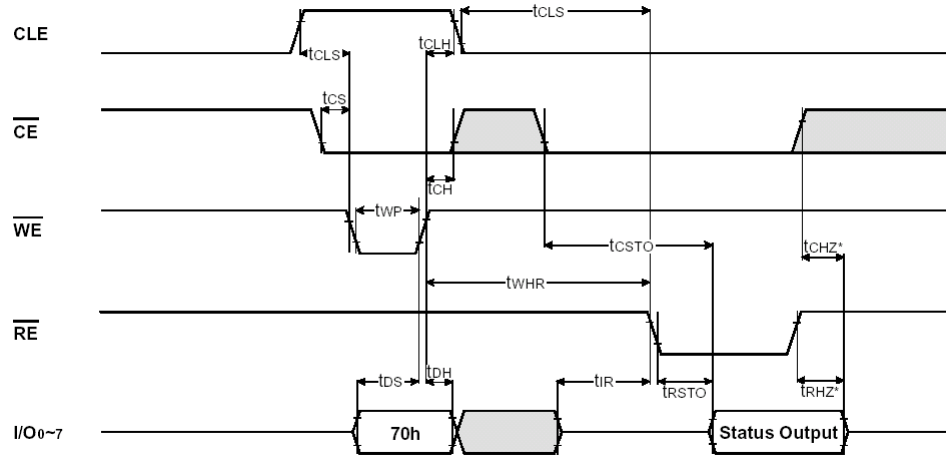


FIGURE 15. READ1 OPERATION (READ ONE PAGE)

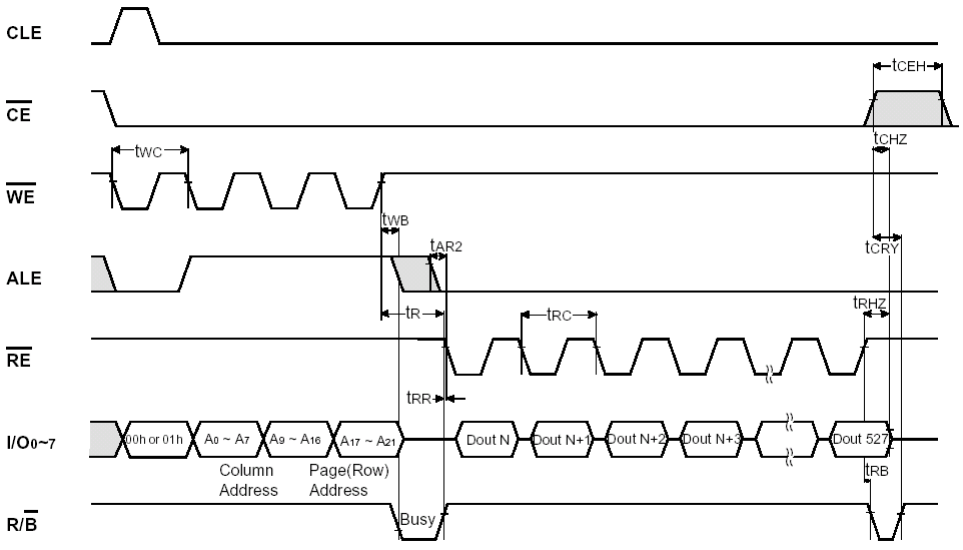


FIGURE 16. READ1 OPERATION (INTERCEPTED BY $\overline{CE}$)

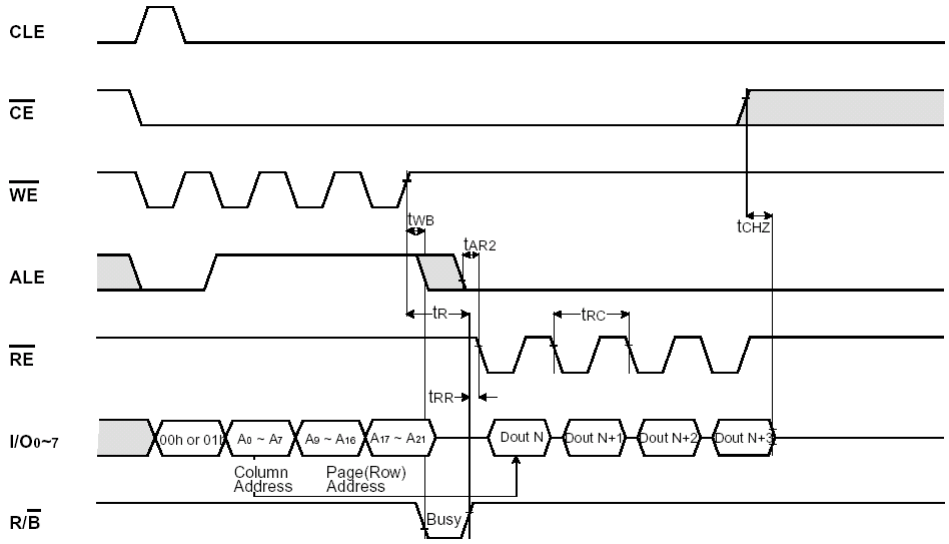


FIGURE 17. READ2 OPERATION (READ ONE PAGE)

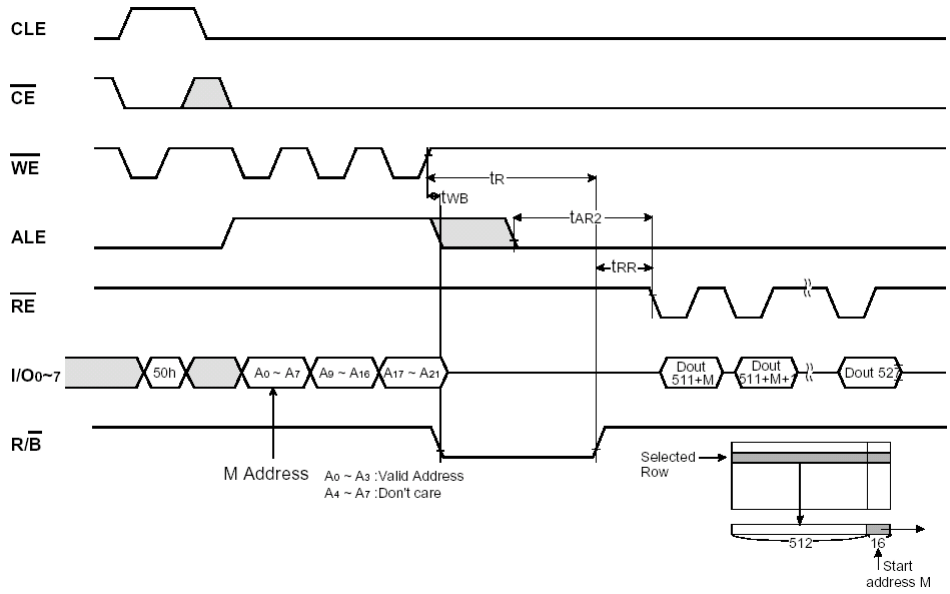


FIGURE 18. SEQUENTIAL ROW READ OPERATION

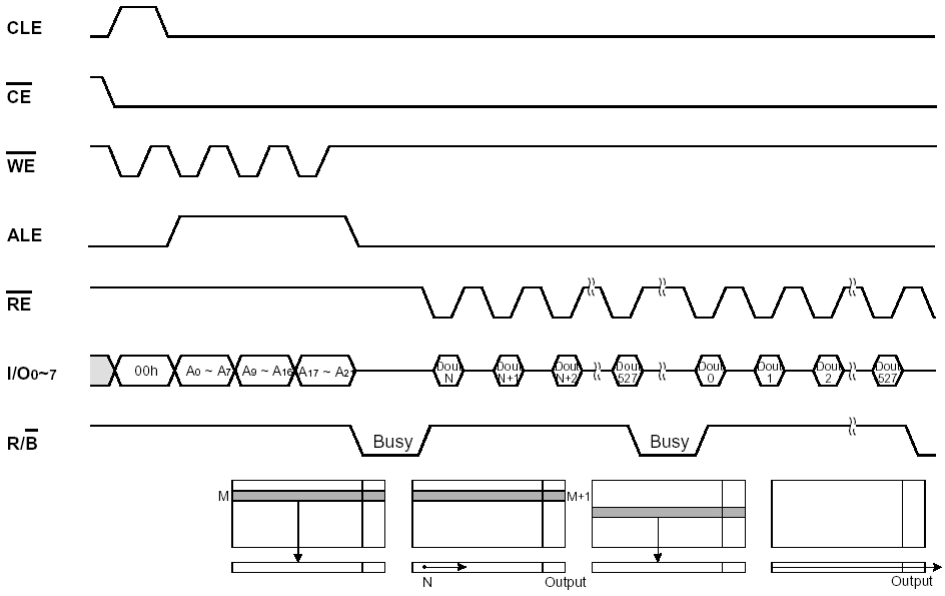


FIGURE 19. PAGE PROGRAM OPERATION

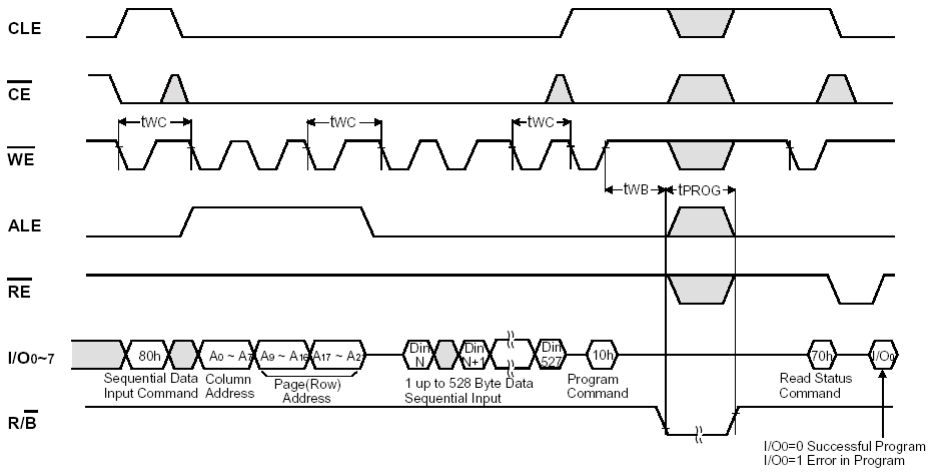


FIGURE 20. BLOCK ERASE OPERATION (ERASE ONE BLOCK)

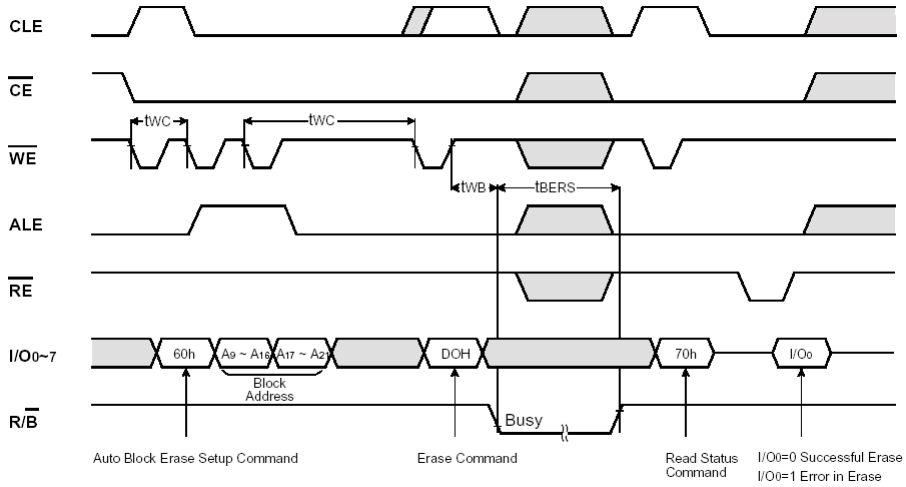
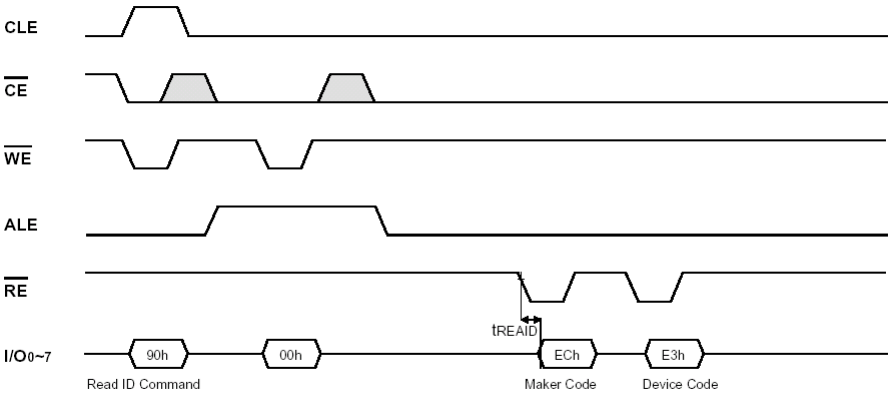


FIGURE 21. MANUFACTURE & DEVICE ID READ OPERATION



DEVICE OPERATION

PAGE READ

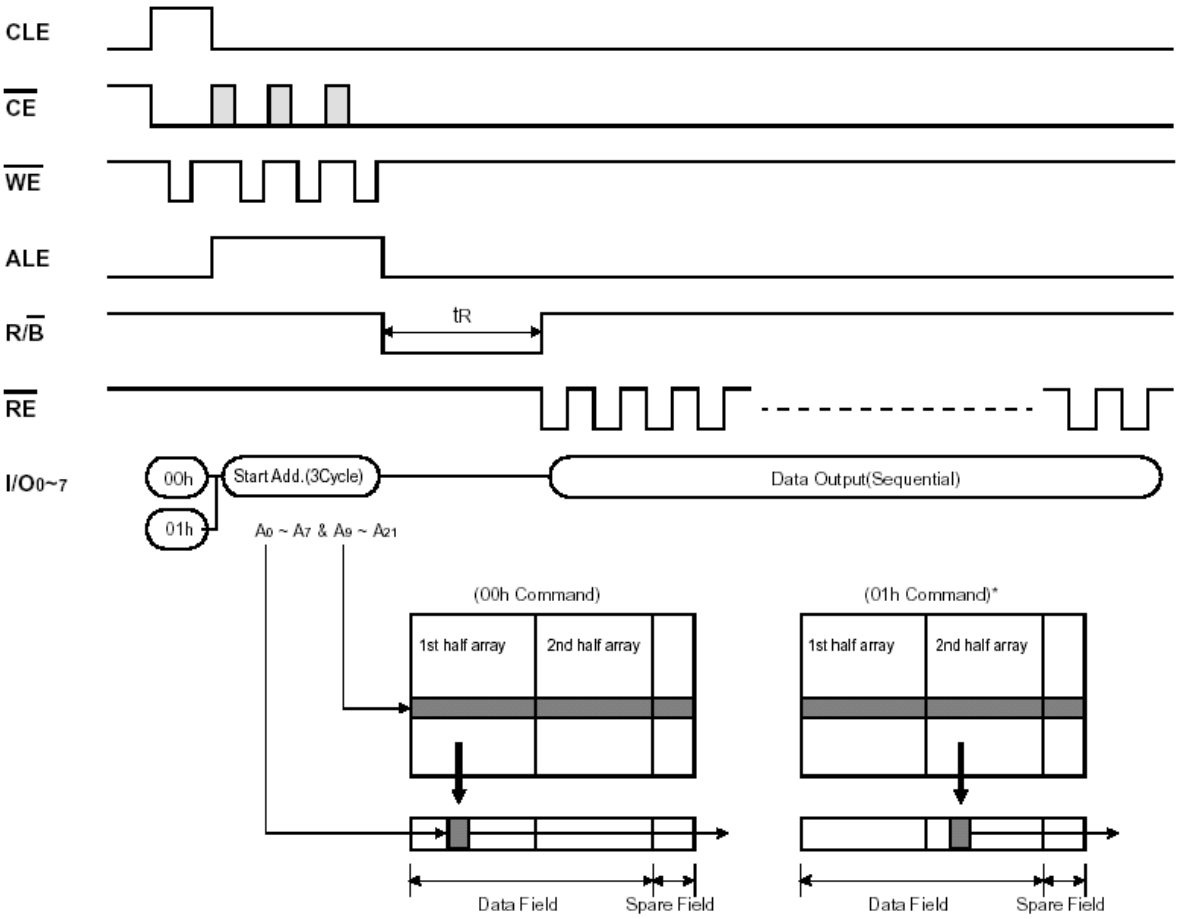
Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, serial page read and sequential read.

The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10 ms(t_R). The CPU can detect the completion of this data transfer(t_R) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out in 50 ns cycle time by sequentially pulsing $\overline{RE}$ with $\overline{CE}$ staying low. High to low transitions of the $\overline{RE}$ clock output the data starting from the selected column address up to the last column address(column 511 or 527 depending on state of $\overline{SE}$ pin).

After the data of last column address is clocked out, the next page is automatically selected for sequential read.

Waiting 10 µs again allows for reading of the selected page. The sequential read operation is terminated by bringing $\overline{CE}$ high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command with SE pin low. Toggling $\overline{SE}$ during operation is prohibited. Addresses A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command (00h/01h) is needed to move the pointer back to the main area. Figures 22 thru 25 show typical sequence and timings for each read operation.

FIGURE 22. READ1 OPERATION



* After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

FIGURE 23. READ2 OPERATION

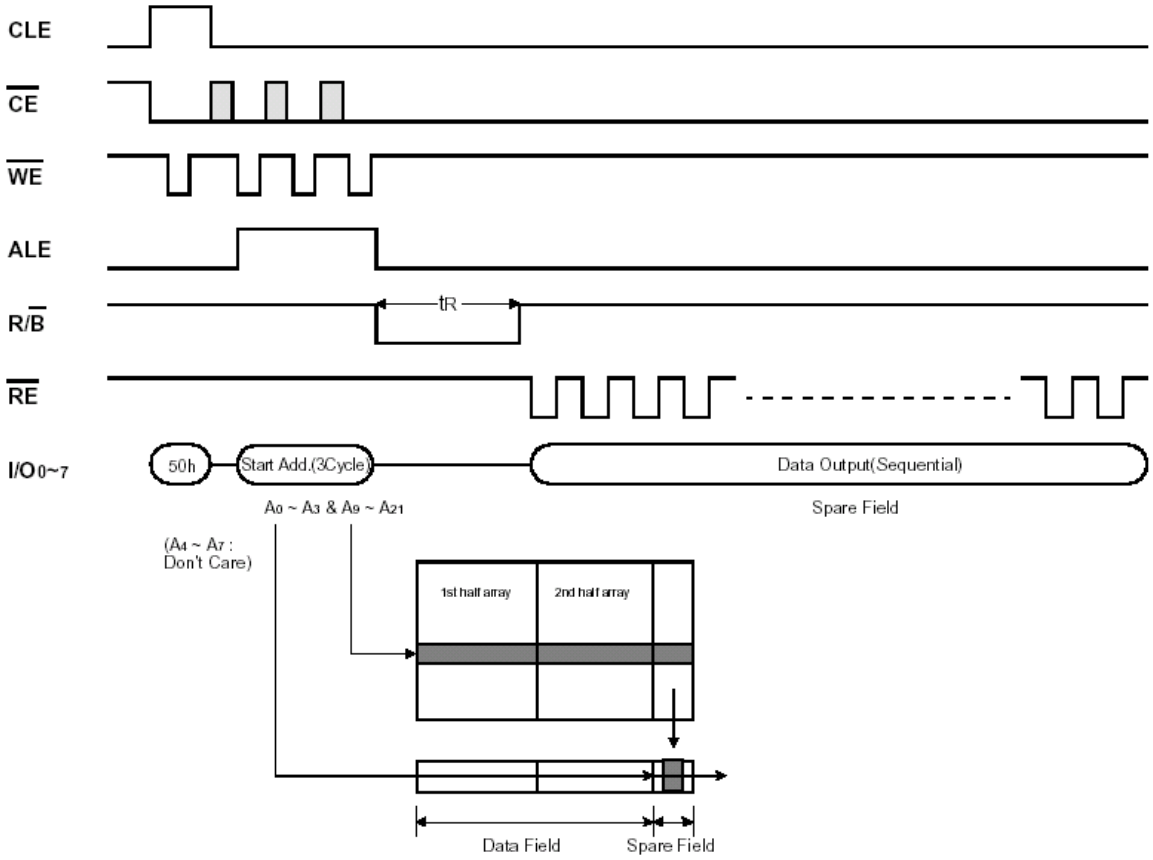


FIGURE 24. SEQUENTIAL ROW READ1 OPERATION

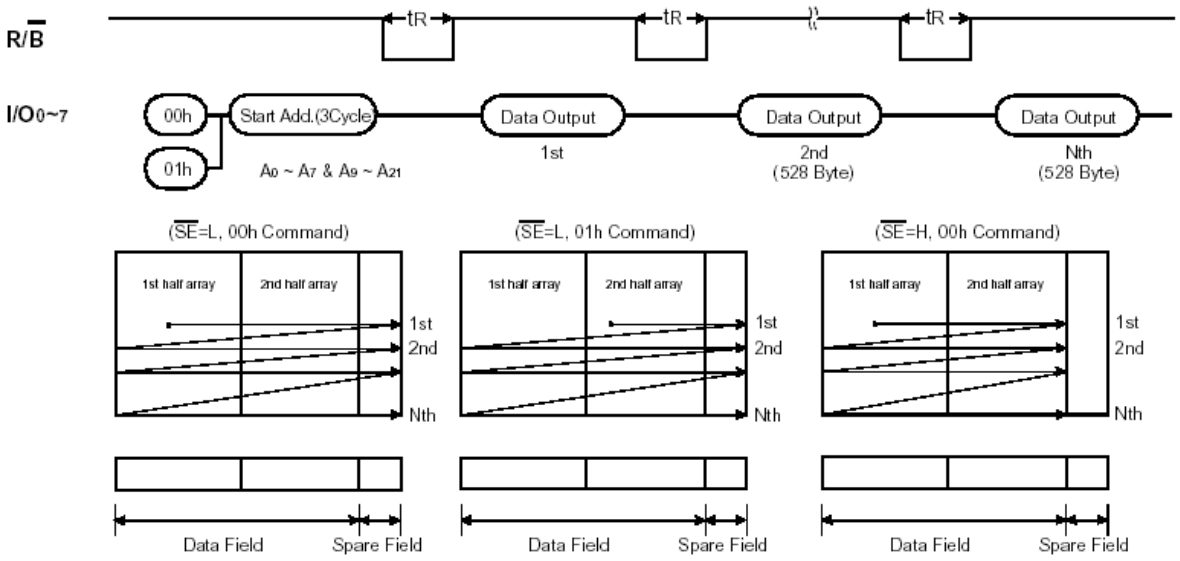
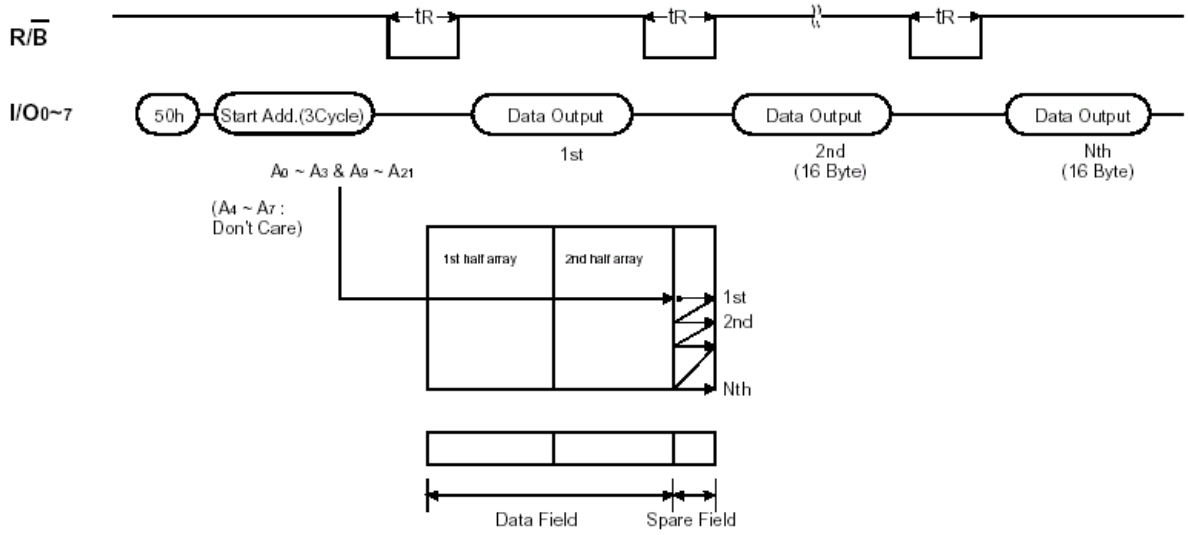


FIGURE 25. SEQUENTIAL READ2 OPERATION ($\overline{SE}$ = FIXED LOW)

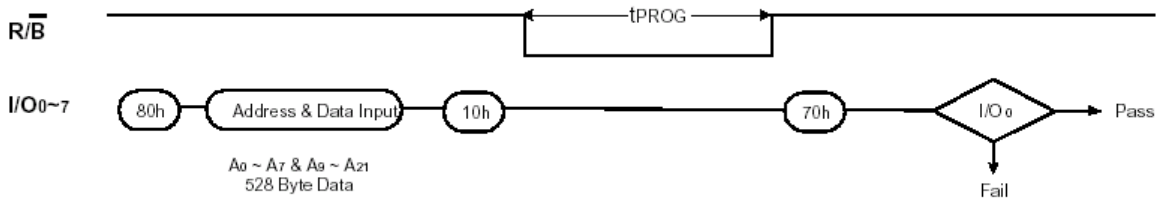


PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed ten. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array. About the pointer operation, please refer to the attached technical notes.The serial data loading period begins by inputting the Serial Data Input command (80H), followed by the three cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.

The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without perviously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The CPU can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O0) may be checked (Figure 26). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

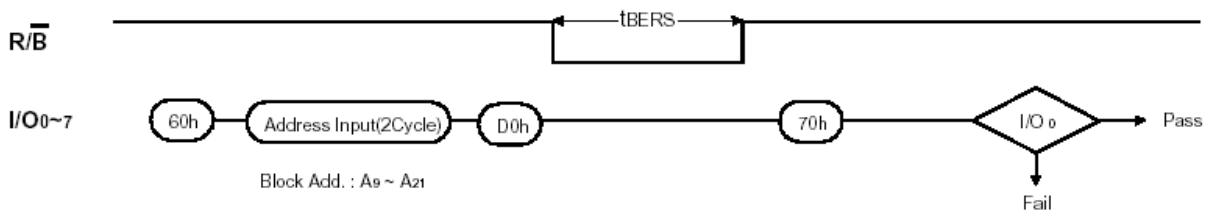
FIGURE 26. PROGRAM & READ STATUS OPERATION



BLOCK ERASE

The Erase operation can erase on a block (8K Byte) basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address A13 to A21 is valid while A9 to A12 is ignored. The addresses of the block to be erased to FFh. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit (I/O0) may be checked. Figure 27 details the sequence.

FIGURE 27. BLOCK ERASE OPERATION



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is complete, and whether the program or erase operation completed successfully. After writing 70h command to the command register, a read cycle outputs the contents of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 14 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h or 50h) should be given before sequential page read cycle.

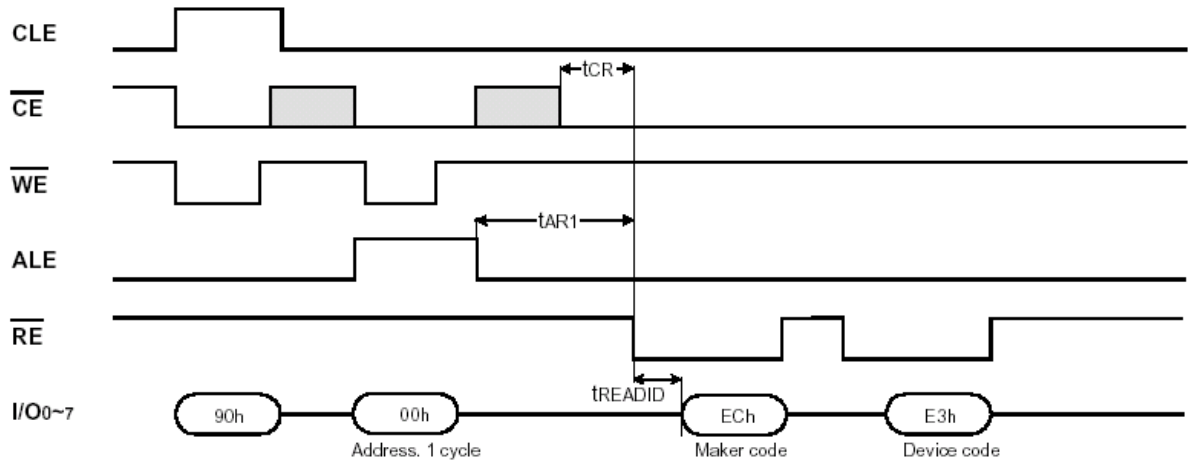
TABLE 14. READ STATUS REGISTER DEFINITION

I/O #	Status	Definition
I/O0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
I/O1	Reserved for Future Use	"0"
I/O2		"0"
I/O3		"0"
I/O4		"0"
I/O5		"0"
I/O6	Device Operation	"0" : Busy "1" : Ready
I/O7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code (E3h) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 28 shows the operation sequence.

FIGURE 28. READ ID OPERATION



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase modes, the reset operation will abort these operation. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. Internal address registers are cleared to "0"s and data registers to "1"s. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 15 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted to by the command register. The R/$\overline{B}$ pin transitions to low for t_{RST} after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure 29 below.

FIGURE 29. RESET OPERATION

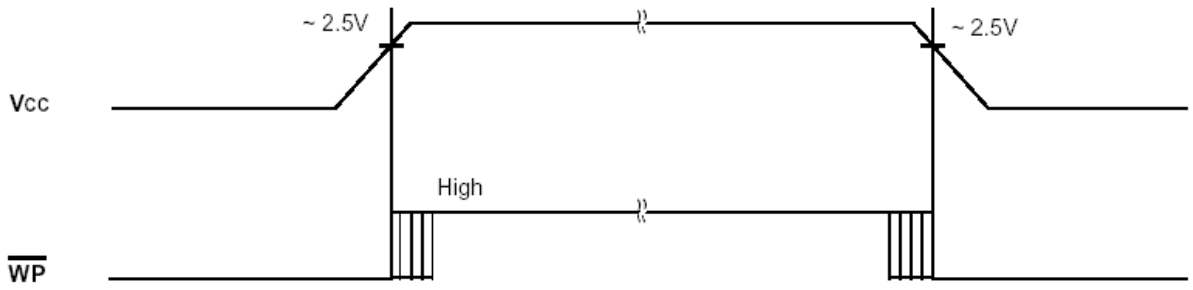
TABLE 15. DEVICE STATUS

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

DATA PROTECTION

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{CC} is below about 2V. WP pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down as shown in Figure 30. The two step command sequence for program/erase provides additional software protection.

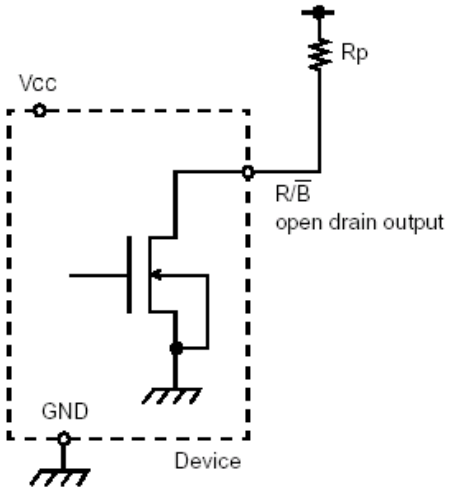
FIGURE 30. AC WAVEFORMS FOR POWER TRANSITION



READY/$\overline{\text{BUSY}}$

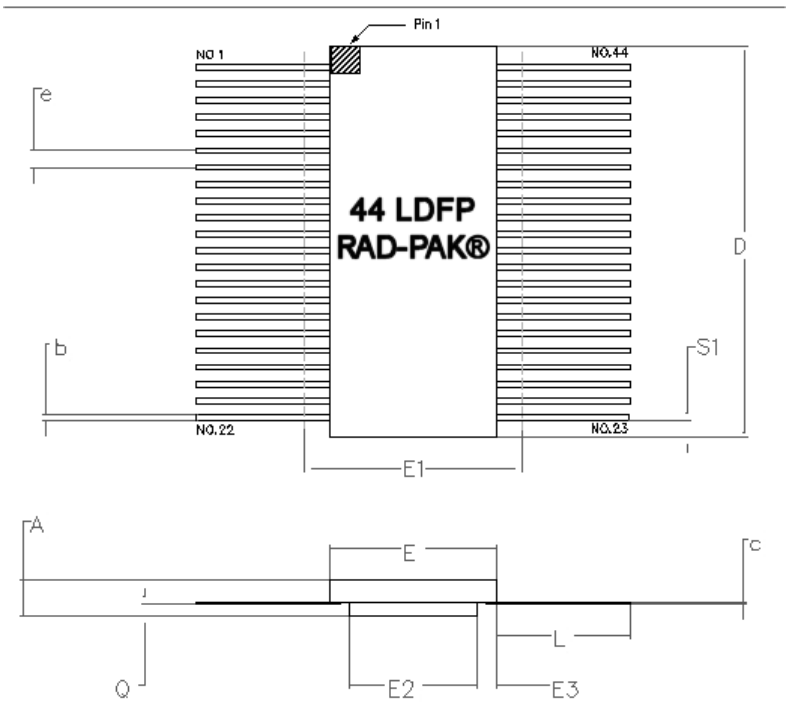
The device has a R/$\overline{\text{B}}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{\text{B}}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is begin after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{\text{B}}$ outputs to be Or-tied. An appropriate pull-up resister is required for proper operation and the value may be calculated by following equation.

FIGURE 31. READY/$\overline{\text{BUSY}}$



$$Rp = \frac{Vcc(Max.) - VoL(Max.)}{IoL + \Sigma IL} = \frac{3.2V}{8mA + \Sigma IL}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.



44 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.132	0.147	0.160
b	0.015	0.017	0.019
c	0.006	0.008	0.10
D	1.188	1.200	1.212
E	0.668	0.675	0.682
E1	--	--	0.705
E2	0.450	0.455	0.460
E3	0.098	0.110	0.122
e		0.050 BSC	
L	0.350	0.370	0.398
Q	0.022	0.027	0.032
S1	0.005	--	--
N		44	

Note: All dimensions in inches

Important Notice:

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The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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