PMC

Pm37LV512

512 Kbit (64K X 8) Dual-Voltage Multiple-Cycle-Programmable ROM

FEATURES

- **Low Voltage Operation**
  - Dual read V_{CC} ranges: 2.7 V to 3.6 V or 4.5 V to 5.5 V
  - Program/Erase voltage: V_{CC} - 2.7 V to 3.6 V and V_{PP} - 11.5 V to 12.5 V
- **High Performance Read**
  - 70 ns access time
- **Electrical Chip Erase and Byte Program Using EPROM Programmer**
  - Maximum 20 µs/byte programming
  - Maximum 100 ms chip erase
  - Do not require UV erase
- **Low Power Consumption**
  - Typical 5 mA active read current
  - Typical 18 µA CMOS standby current
- **Excellent Product Reliablity**
  - Guarantee minimum 1,000 program/erase cycles
  - Minimum 20 years data retention
- **JEDEC Standard Byte-wide Flash Memory Pin-out**
- **Industrial Standard Packaging**
  - 32-pin PLCC
  - 32-pin PDIP
  - 32-pin VSOP

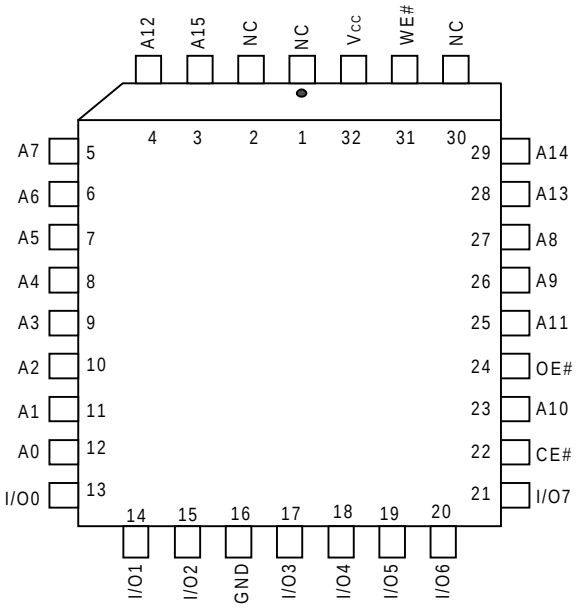
GENERAL DESCRIPTION

The Pm37LV512 is a 512 Kbit, Multiple-Cycle-Programmable Read-Only-Memory (MCP ROM) organized as 65,563 bytes of 8 bits each. The program and erase operation of device can be done on EPROM programmers by applying 3.0 Volt V_{CC} and 12.0 Volt V_{PP} to A9 and/or OE# pin. This eliminates the need of a UV-Source for erase operation such as EPROM device. The read operation of device can be in 2.7 Volt to 3.6 Volt or 4.5 Volt - 5.5 Volt range compatible to either 3.0 Volt or 5.0 Volt systems. The dual read operation ranges can greatly increase application flexibility for users.

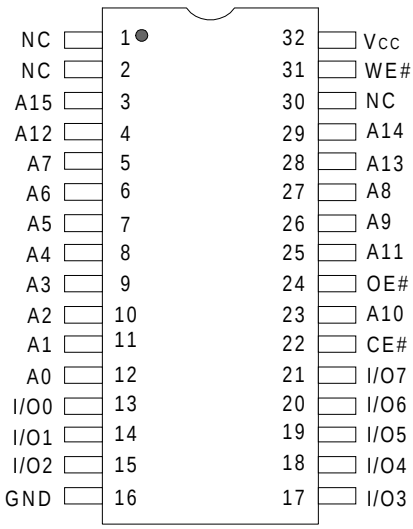
The device has a standard microprocessor interface as well as JEDEC single-power-supply Flash compatible pin-out. For applications that do not require in-system-programming (ISP) function for firmwire upgrade, the Pm37LV512 offers a direct cost reduction path for Flash memory, i.e. Pm39LV512, without modifying the schematic and board layout of system.

The Pm37LV512 is manufactured on PMC's advanced nonvolatile CMOS technology, P-FLASH™. The device is offered in 32-pin PLCC, VSOP and PDIP packages with access time of 70 ns.

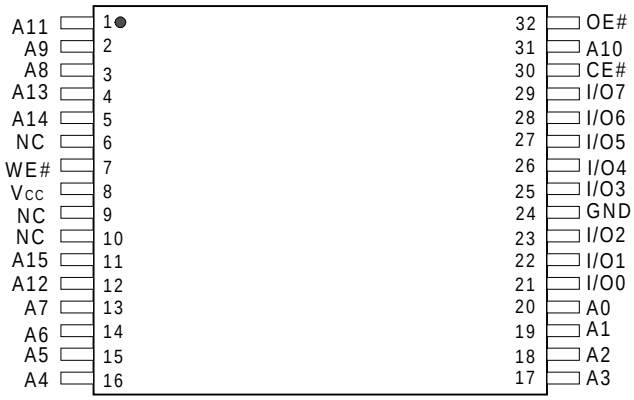
CONNECTION DIAGRAMS



32-Pin PLCC

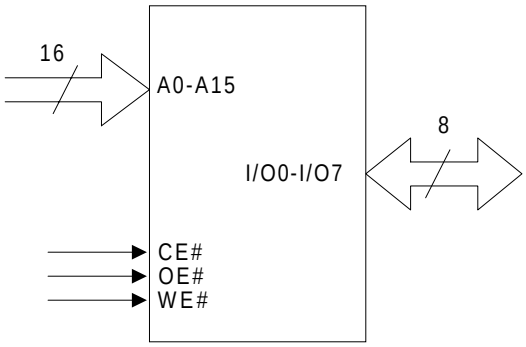


32-Pin PDIP

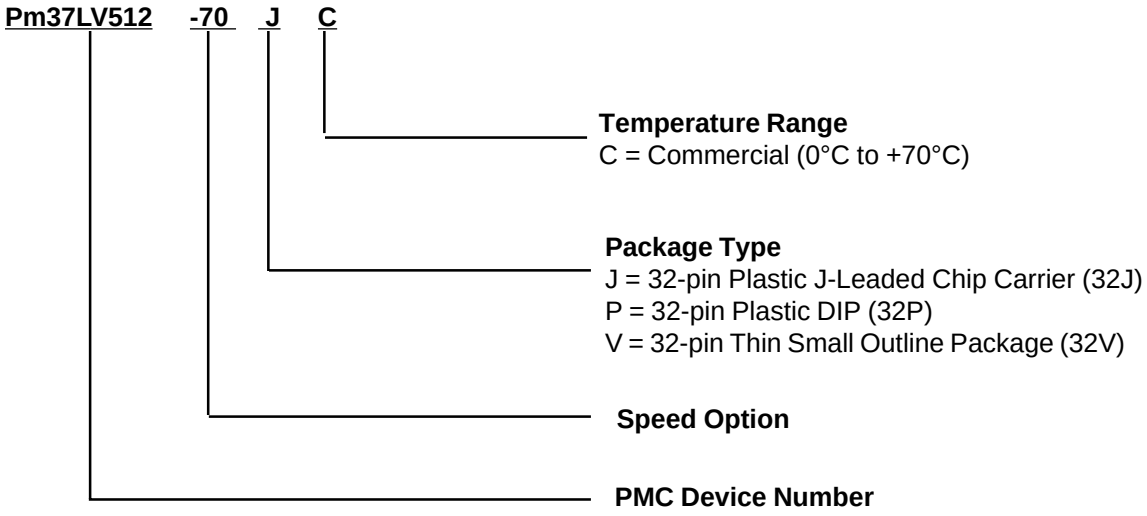


32-Pin VSOP

LOGIC SYMBOL



PRODUCT ORDERING INFORMATION

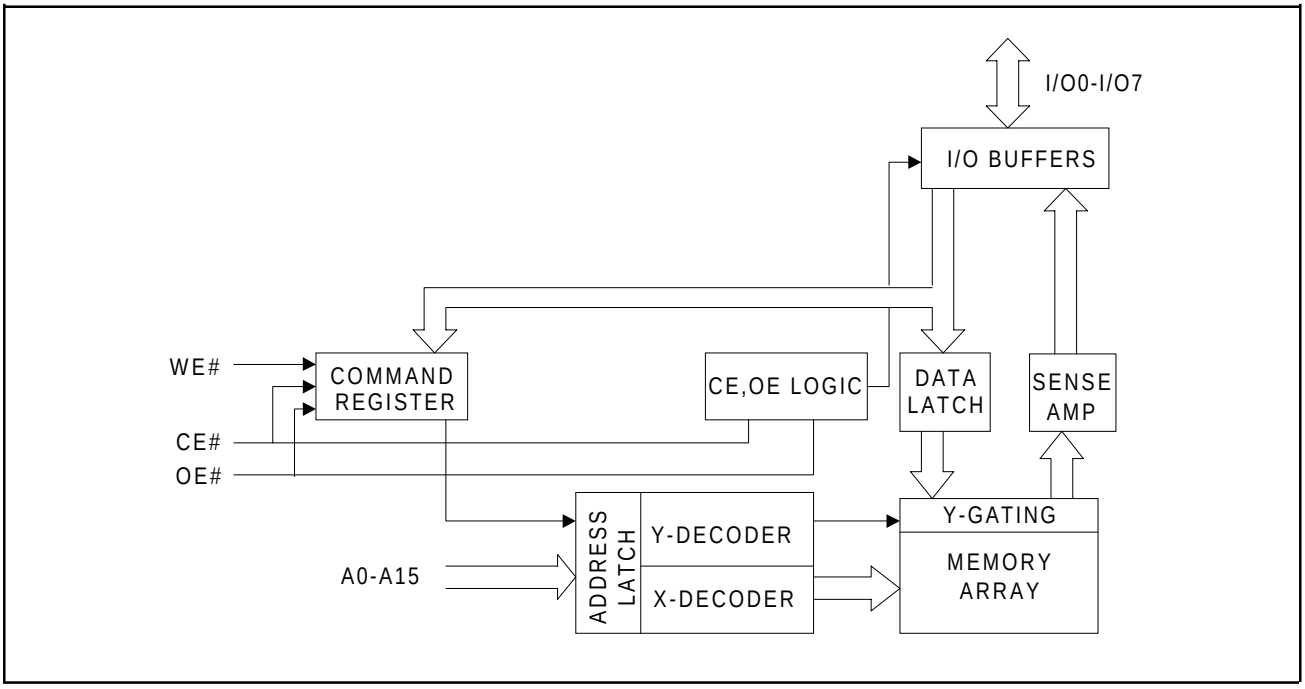


Part Number	t_{ACC} (ns)	Package	Temperature Range
Pm37LV512-70JC	70	32J	Commercial (0°C to + 70°C)
Pm37LV512-70PC		32P	Commercial (0°C to + 70°C)
Pm37LV512-70VC		32V	Commercial (0°C to + 70°C)

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
A0 - A15	INPUT	Address Inputs: For memory addresses input. Addresses are internally latched on the falling edge of WE# during a write cycle.
CE#	INPUT	Chip Enable: CE# goes low activates the device's internal circuitries for device operation. CE# goes high deselects the device and switches into standby mode to reduce the power consumption.
WE#	INPUT	Write Enable: Activate the device for write operation. WE# is active low.
OE#	INPUT	Output Enable: Control the device's output buffers during a read cycle. OE# is active low.
I/O0 - I/O7	INPUT/ OUTPUT	Data Inputs/Outputs: Input command/data during a write cycle or output data during a read cycle. The I/O pins float to tri-state when OE# are disabled.
V_{CC}		Device Power Supply
GND		Ground
NC		No Connection

BLOCK DIAGRAM



DEVICE OPERATION

READ OPERATION

The access of Pm37LV512 is similar as that of EPROM or Flash Memory. To obtain data at the outputs, three control functions must be satisfied:

• CE# is the chip enable and should be pulled low (V_{IL}).

• OE# is the output enable and should be pulled low (V_{IL}).

• WE# is the write enable and should remains high (V_{IH}).

BYTE PROGRAMMING

The Pm37LV512 is programmed by using an external EPROM programmer. The programming mode is activated by applying 12.0 Volt on OE# pin and V_{IL} on CE# pin. The byte program operation is completed by asserting WE# to low for 20 µs. A chip erase operation is required prior to program due to a data "0" can not be programmed back to a "1" and only erase operation can convert "0"s to "1"s. The entire chip can be programmed byte-by-byte by using the byte program algorithmm. Refer to Chart 1. Byte Programming Flowchart and Byte Program Operations AC Waveforms.

CHIP ERASE

The entire memory array can be erased through a chip erase operation on an external EPROM programmer. Pre-program the "1"s cells in the device is not required prior to chip erase operation. The chip erase operation is activated by applying 12.0 Volt to OE# and A9 pins while CE# pin is low. All other address and data pins are "don't care". Chip erase is completed by asserting WE# pin to low for 100 ms. The falling edge of WE# will start the chip erase operation. The device will return back to standby mode after the completion of chip erase. Refer to Chart 2. Chip Erase Flowchart and Chip Erase Operations AC Waveforms.

PRODUCT IDENTIFICATION

The hardware product identification mode can be used by an EPROM programmer to identify the device and manufacturer for selecting the right programming algorithm for the device. The product identification mode is activated by applying 12.0 Volt on A9 pin. For details, please see Bus Operation Modes in Table 1.

OPERATING MODES

Table 1. Bus Operation Modes

Mode	CE#	OE#	WE#	A_9	ADDRESS	I/O
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	A_{IN}	D_{OUT}
Chip-Erase	V_{IL}	V_H (1)	V_{IL}	V_H	X (2)	High Z
Byte-Program	V_{IL}	V_H	V_{IL}	A_{IN}	A_{IN}	D_{IN}
Program/Erase Inhibit	X	X	V_{IH}	X	X	High Z
	X	V_{IL} or V_{IH}	X	X	X	High Z/ D_{OUT}
Standby	V_{IH}	X	X	X	X	High Z
Output Disable	X	V_{IH}	X	X	X	High Z
Product Identification Hardware	V_{IL}	V_{IL}	V_{IH}	V_H	A2 - A15 = X, A1 = V_{IL}, A0 = V_{IL}	Manufacturer Code (3)
					A2 - A15 = X, A1 = V_{IL}, A0 = V_{IH}	Device Code (3)

Notes:
1. V_H = 12.0 V ± 0.5 V.
2. X can be V_{IL}, V_{IH} or addresses.
3. Manufacturer Code: 9Dh;
   Device Code: 9Bh

DEVICE OPERATIONS FLOWCHARTS

BYTE PROGRAMMING

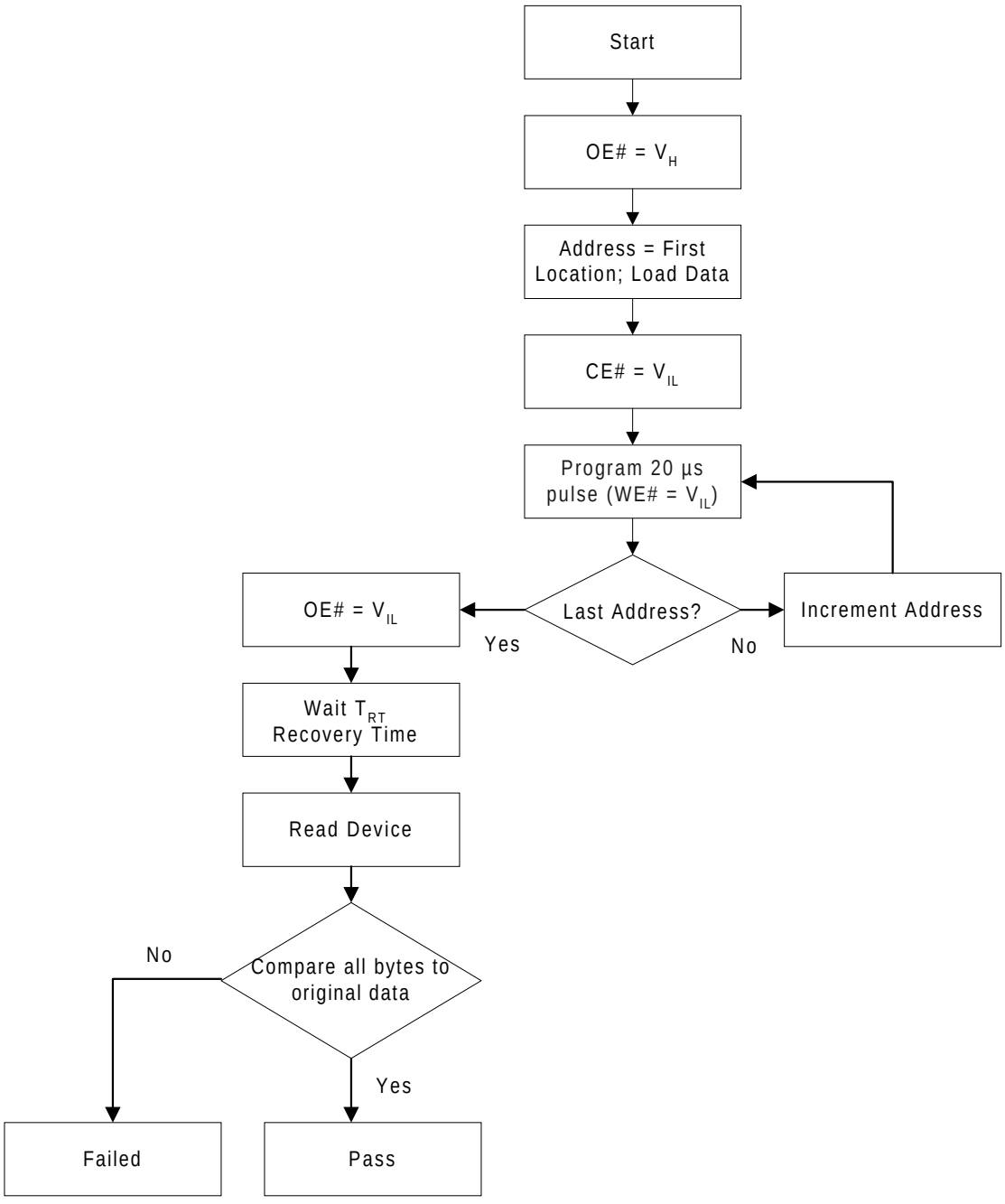


Chart 1. Byte Programming Flowchart

DEVICE OPERATIONS FLOWCHARTS (CONTINUED)

CHIP ERASE

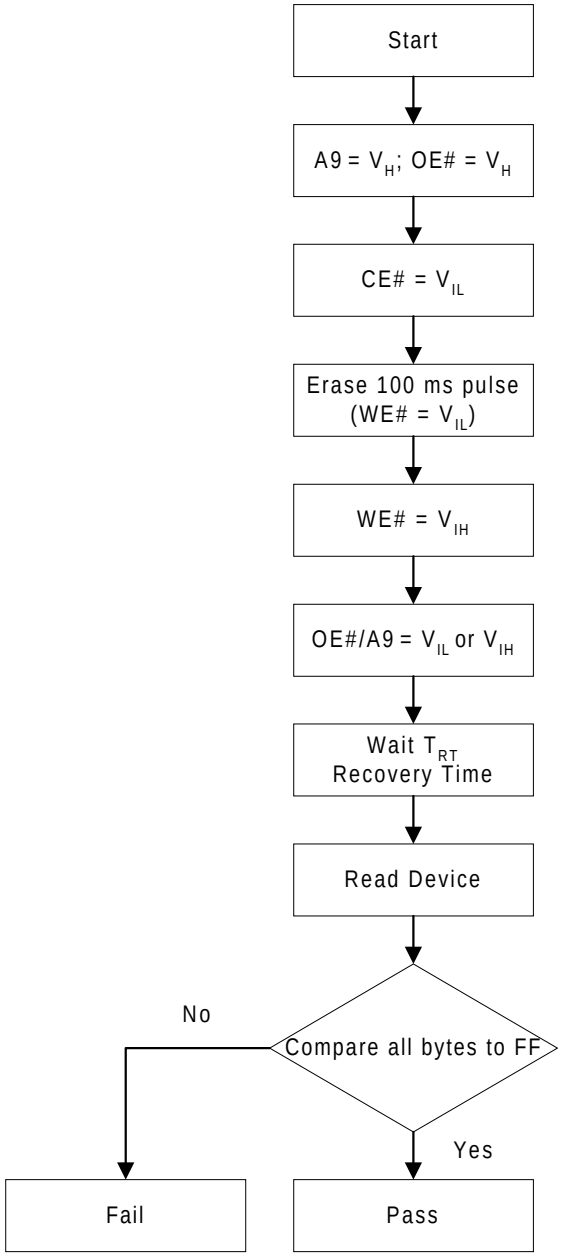


Chart 2. Chip Erase Flowchart

ABSOLUTE MAXIMUM RATINGS (1)

Temperature Under Bias	-65°C to +125°C
Storage Temperature	-65°C to +125°C
Surface Mount Lead Soldering Temperature	240°C 3 Seconds
Input Voltage with Respect to Ground on All Pins except OE# and A9 pin (2)	-0.5 V to V_{CC} + 0.5 V
Input Voltage with Respect to Ground on OE# and A9 pin (3)	-0.5 V to +13.0 V
All Output Voltage with Respect to Ground	-0.5 V to V_{CC} + 0.5 V
V_{CC} (2)	-0.5 V to +6.0 V

Notes:
1. Stresses under those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device or any other conditions under those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affected device reliability.
2. Maximum DC voltage on input or I/O pins are V_{CC} + 0.5 V. During voltage transitioning period, input or I/O pins may overshoot to V_{CC} + 2.0 V for a period of time up to 20 ns. Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitioning period, input or I/O pins may undershoot GND to -2.0 V for a period of time up to 20 ns.
3. Maximum DC voltage on OE# and A9 pin is +13.0 V. During voltage transitioning period, OE# and A9 pin may overshoot to +14.0 V for a period of time up to 20 ns. Minimum DC voltage on OE# and A9 pin is -0.5 V. During voltage transitioning period, OE# and A9 pin may undershoot GND to -2.0 V for a period of time up to 20 ns.

DC AND AC OPERATING RANGE

Part Number		**Pm37LV512**
Operating Temperature		0°C to 70°C
Program/Erase	V_{CC}	2.7 V - 3.6 V
	V_{PP}	11.5 V - 12.5 V
Read	V_{CC}	2.7 V - 3.6 V or 4.5 V - 5.5 V

DC CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}			1	µA
I_{SB1}	V_{CC} Standby Current CMOS	CE#, OE# = V_{CC} ± 0.3 V		18	100	µA
I_{SB2}	V_{CC} Standby Current TTL	CE# = V_{IH} to V_{CC}		0.01	3	mA
I_{CC1}	V_{CC} Active Read Current	f = 5 MHz; I_{OUT} = 0 mA		5	15	mA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA; V_{CC} = V_{CC} min			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA; V_{CC} = V_{CC} min	V_{CC} - 0.2			V

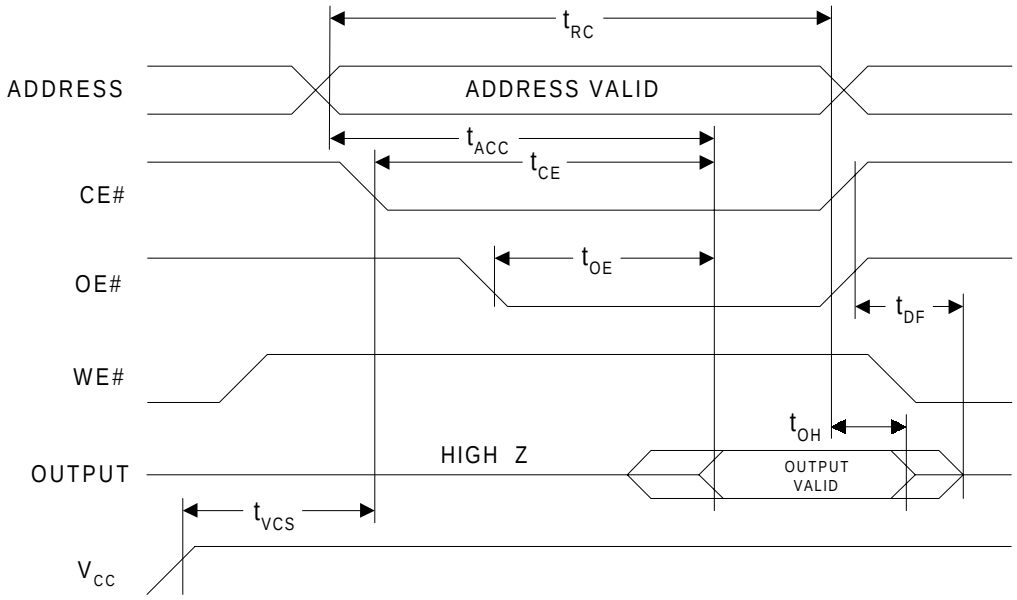
AC CHARACTERISTICS

READ OPERATIONS CHARACTERISTICS

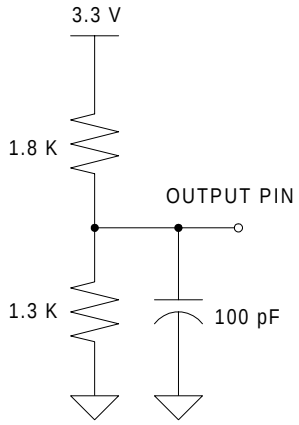
Symbol	Parameter	Pm37LV512-70		Units
		Min	Max	
t_{RC}	Read Cycle Time	70		ns
t_{ACC}	Address to Output Delay		70	ns
t_{CE}	CE# to Output Delay		70	ns
t_{OE}	OE# to Output Delay		35	ns
t_{DF}	CE# or OE# to Output High Z	0	20	ns
t_{OH}	Output Hold from OE#, CE# or Address, whichever occured first	0		ns
t_{VCS}	V_{CC} Set-up Time	50		µs

AC CHARACTERISTICS (CONTINUED)

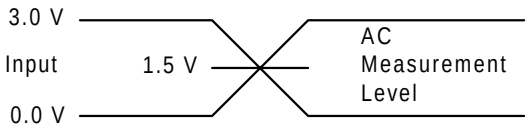
READ OPERATIONS AC WAVEFORMS



OUTPUT TEST LOAD



INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



PIN CAPACITANCE (f = 1 MHz, T = 25°C)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: These parameters are characterized but not 100% tested.

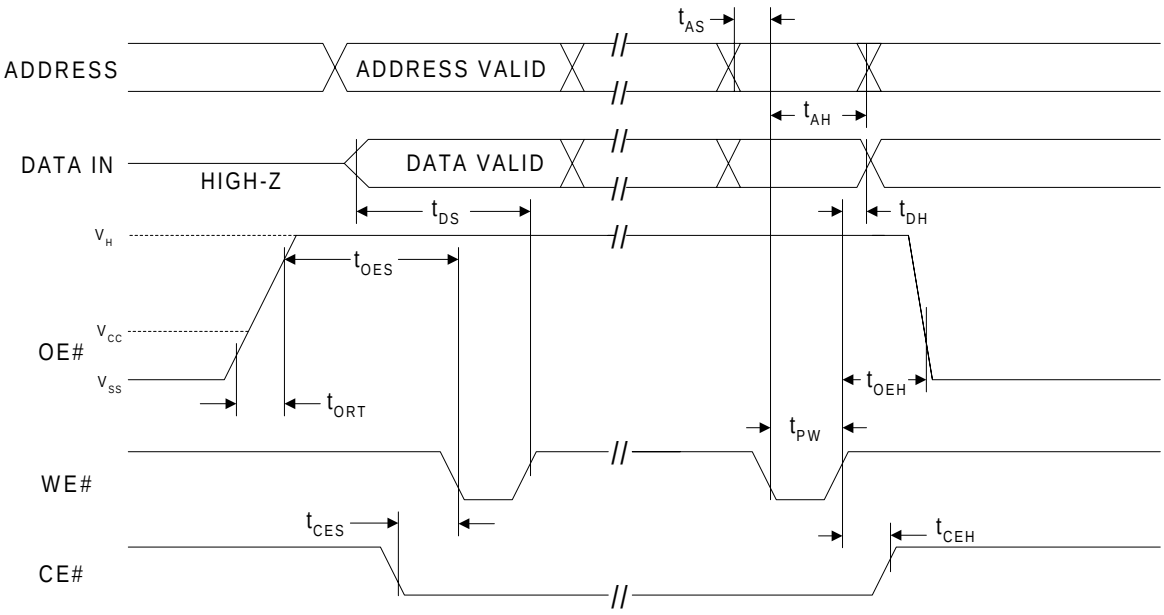
AC CHARACTERISTICS (CONTINUED)

WRITE (PROGRAM/ERASE) OPERATIONS CHARACTERISTICS

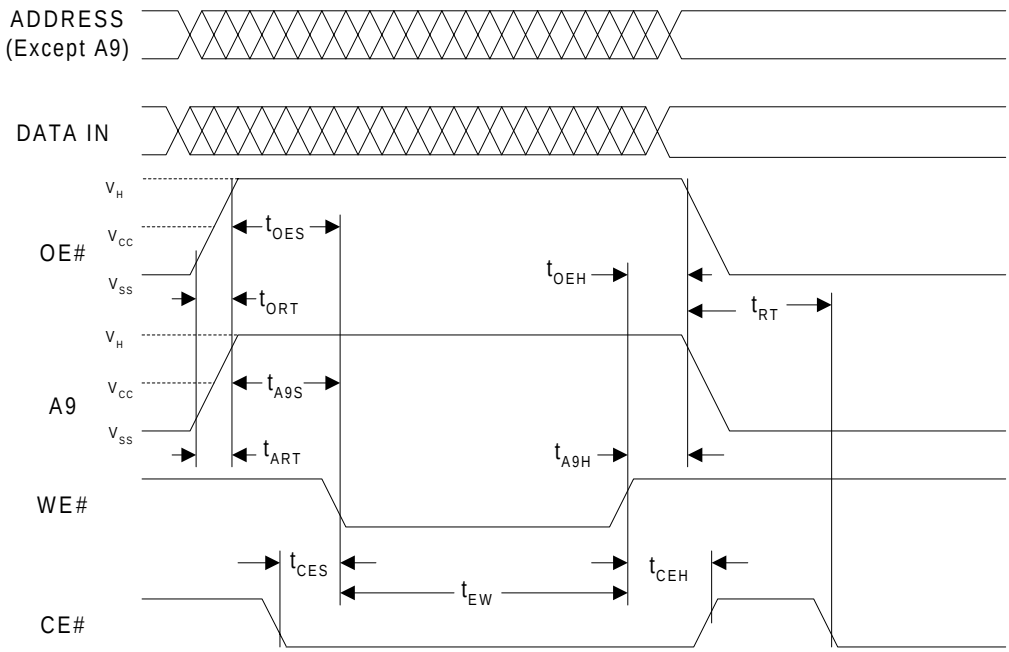
Symbol	Parameter	Pm37LV512-70		Units
		Min	Max	
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	30		ns
t_{CES}	CE# Set-up Time	0		ns
t_{CEH}	CE# Hold Time	0		ns
t_{DS}	Data Set-up Time	40		ns
t_{DH}	Data Hold Time	0		ns
t_{ORT}	OE# Rise Time for Program and Erase	1		ns
t_{OES}	OE# SetupTime for Program and Erase	1		ns
t_{OEH}	OE# Hold Time for Program and Erase	1		ns
t_{PW}	WE# Program Pulse Width		20	µs
t_{EW}	WE# Erase Pulse Width		100	ms
t_{RT}	OE#/A9 Recovery Time for Erase	1		ns
t_{ART}	A_9 Rise Time to 12V during Erase	1		ns
t_{A9S}	A_9 Setup Time during Erase	1		ms
t_{A9H}	A_9 Hold Time during Erase	1		ms

AC CHARACTERISTICS (CONTINUED)

BYTE PROGRAM OPERATIONS AC WAVEFORMS



CHIP ERASE OPERATIONS AC WAVEFORMS



AC CHARACTERISTICS (CONTINUED)

RELIABILITY CHARACTERISTICS

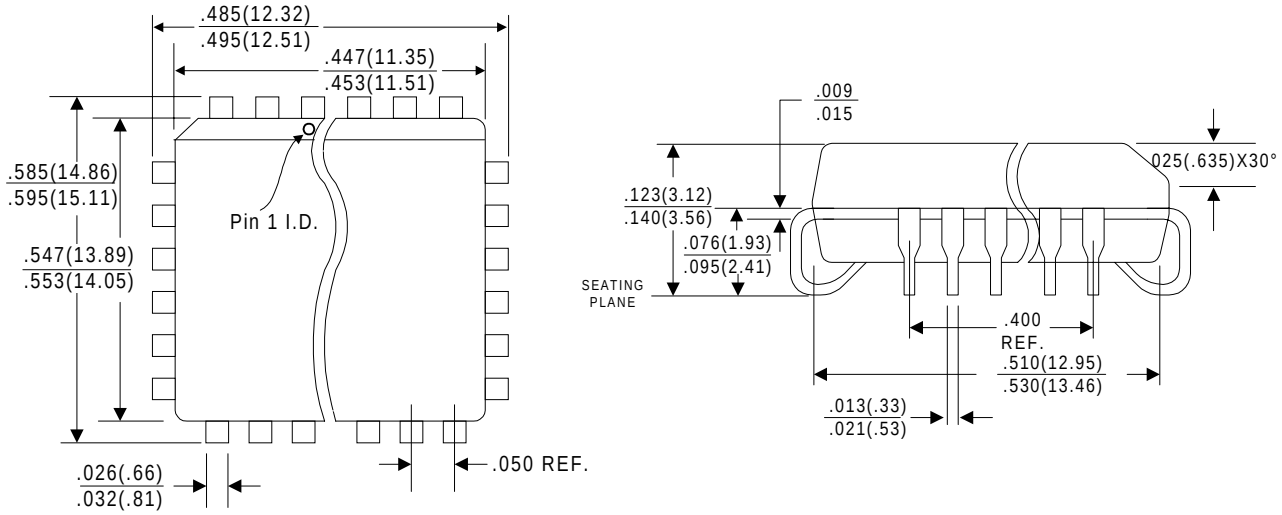
Parameter	Min	Unit	Test Method
Endurance	1,000	Cycles	JEDEC Standard A117
Data Retention	20	Years	JEDEC Standard A103
ESD - Human Body Model	2,000	Volts	JEDEC Standard A114
ESD - Machine Model	200	Volts	JEDEC Standard A115
Latch-Up	100 + I_{CC1}	mA	JEDEC Standard 78

Note: These parameters are characterized but not 100% tested.

PACKAGE TYPE INFORMATION

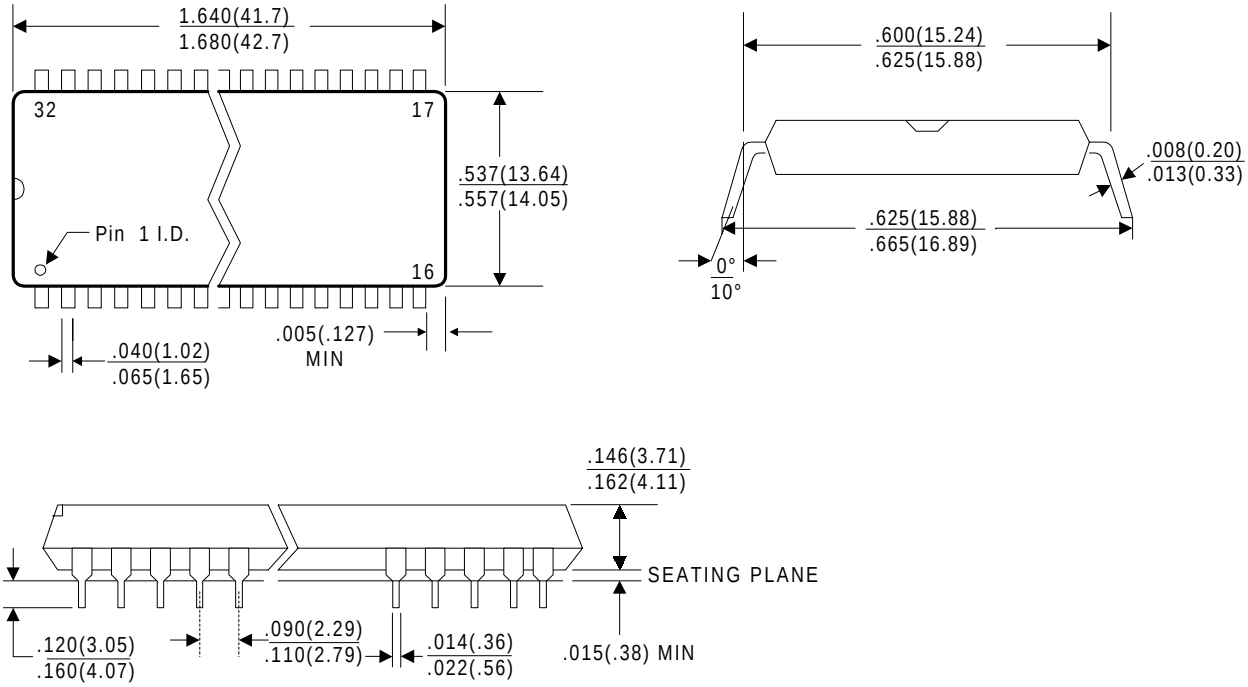
32J

32-Pin Plastic Leaded Chip Carrier Dimensions in Inches (Millimeters)



32P

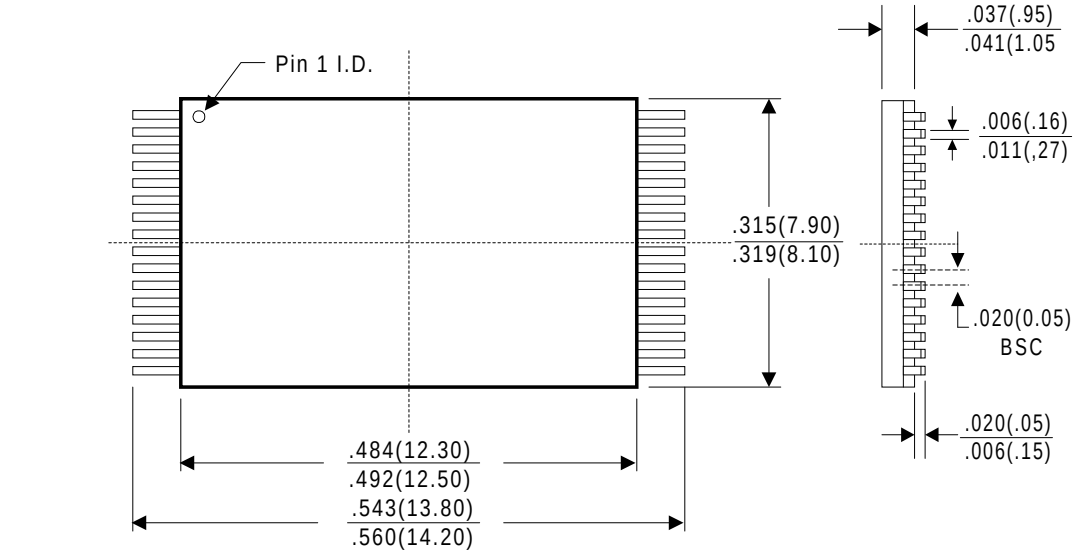
32-Pin Plastic DIP Dimensions in Inches (Millimeters)

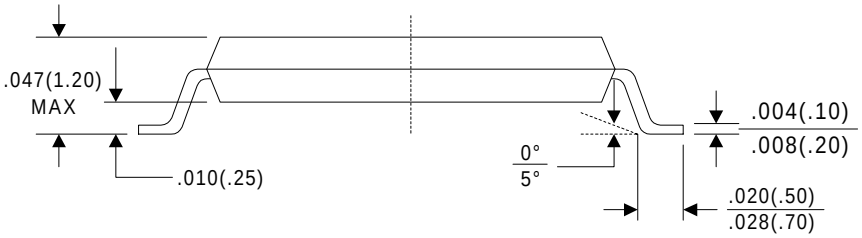


PACKAGE TYPE INFORMATION (CONTINUED)

32V

32-Pin Thin Small Outline Package (TSOP 8mm x 14mm)(Millimeters)





REVISION HISTORY

Date	Revision No.	Description of Changes	Page No.
March, 2002	1.0	New publication	All
May, 2002	1.1	Revised features and general description	1
		Removed 90 ns speed grade	3, 10, 12
		Revised bus operation modes	6
		Revised absolute maximum ratings	9
		Revised I_{SB1} specification	10
		Revised program/erase operation characteristics and waveforms	12, 13
June, 2002	1.2	Corrected the typo in 32-Pin PDIP pin connection	2
		Corrected the typo of T_{RT} recovery time in Byte Programming Flowchart	7
Dec. 2002	1.3	Added 32-Pin VSOP package spec.	1, 2, 3, 16