

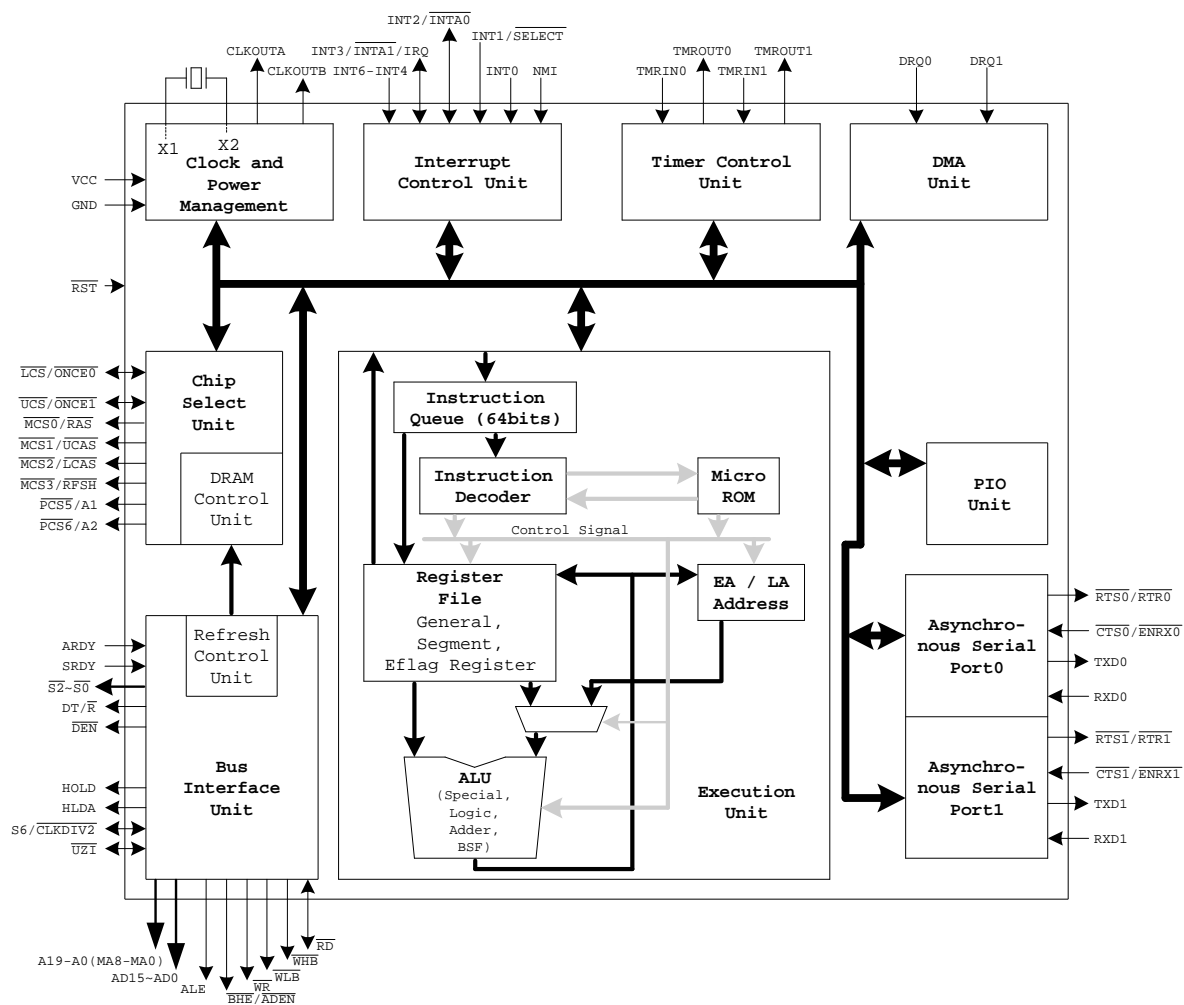
R1121
Brief Sheet
16 BIT RISC MICRO PROCESSOR

Specifications subject to change without notice, contact your sales representatives for the most update information.

1 Features

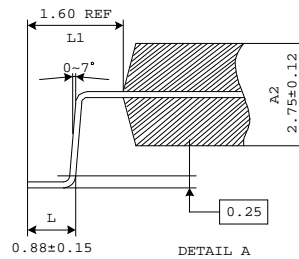
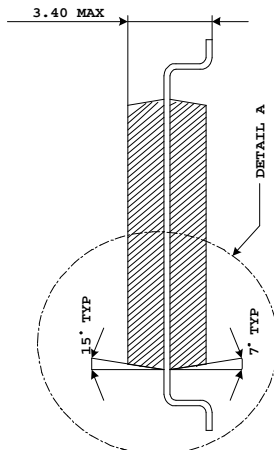
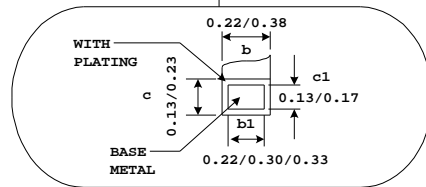
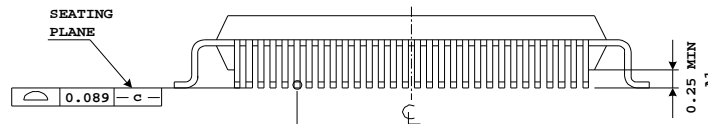
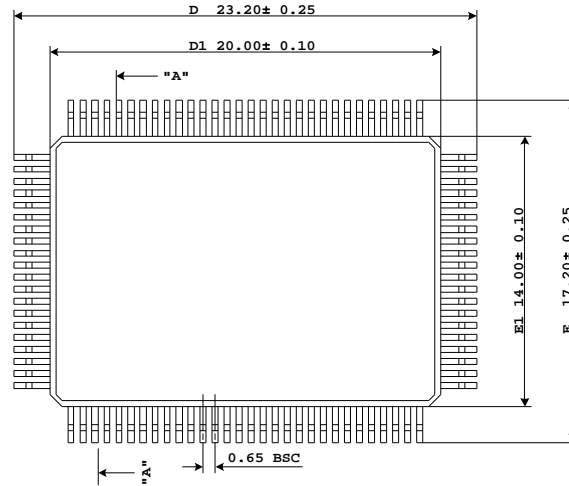
- I CPU Core
 - RDC's proprietary RISC architecture
 - Five-stages pipeline
 - Operation frequency: 80MHz,
 - Support CPU ID
 - Supports 32 PIO pins
 - Static Design & Synthesizable design
 - External bus, Internal bus and core in the same clock base
- I Bus interface
 - Multiplexed address and Data bus
 - With 8-bit or 16-bit boot ROM bus size
 - Supports direct address bus [A19 : A0]
 - 8-bit or 16-bit external bus dynamic access
- I ROM/RAM/DRAM Controller and Addressing Space
 - 1M byte memory address space
 - 64K byte I/O space
 - Support 64kx16, 128kx16, 256kx16 EDO or FP DRAM with auto-refresh control
- I Software
 - compatible with generic 80C186 microprocessor
- I Asynchronous Serial Channels
 - Support two Asynchronous serial channels with hardware handshaking signals.
- I Interrupt Controller
 - The interrupt controller with seven maskable external interrupts and one non-maskable external interrupt (NMI)
- I Two Independent DMA Channels
- I Integrate PLL(*1~*8)
- I Programmable Chip-select Logic
 - Programmable chip-select logic for Memory or I/O bus cycle decoder
- I Programmable wait-state generator
- I Counter/Timers
 - Three independent 16-bit timers and one independent programmable watchdog timer
- I Operating Voltage Range
 - Operation voltage: 3.3V
 - Input voltage: 2.5V ~ 5V
 - Out voltage: 3.3V
- I Package Type
 - 100 Pin PQFP & LQFP
- I A Green Product

2. Block Diagram



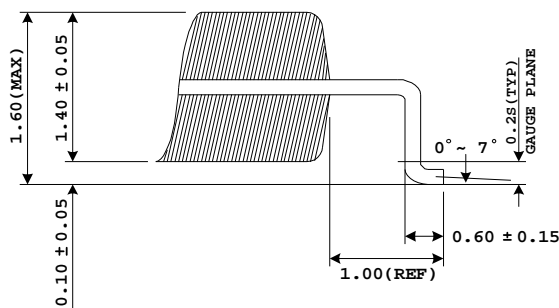
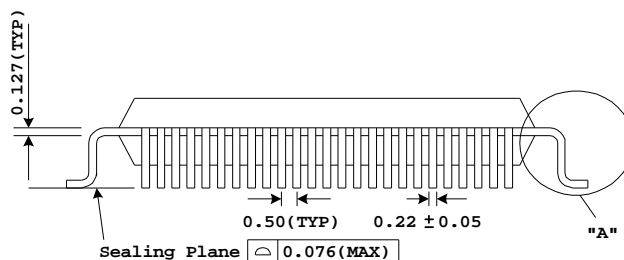
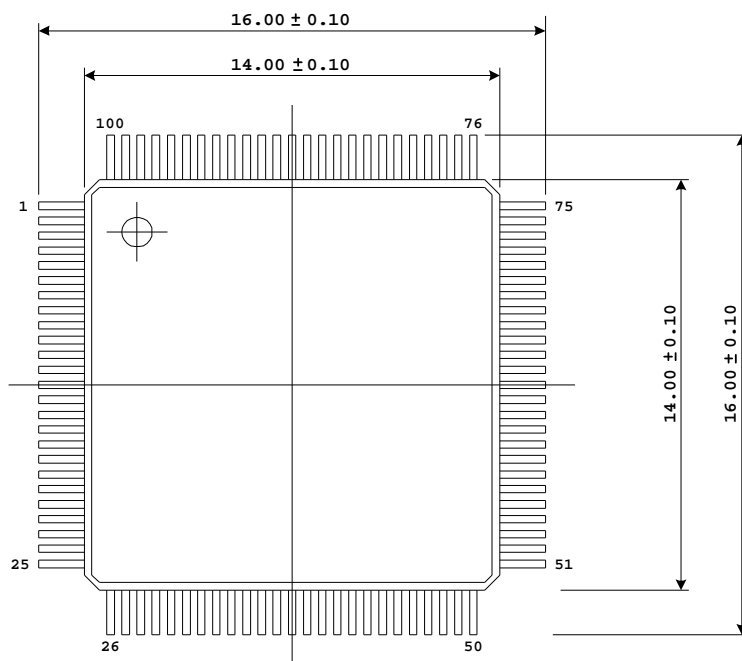
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3. Package Information
100 Pin PQFP



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100 Pin LQFP



UNIT : mm

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