

## 8K EPROM HCMOS MCUs WITH A/D CONVERTER

- Single chip microcontroller, 8K bytes of EPROM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulator or index pointers.
- 8/16 bit CORE with full feature DMA controller and powerful interrupt handler and a standard Serial Peripheral Interface (SPI) handling S-BUS/I<sup>2</sup>C Bus and IM BUS.
- Up to 8 external interrupts edge selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Timer/Watchdog for system integrity.
- Two 16 bit Multifunction Timer modules, each with an 8 bit Prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time and 8 bit ± 1/2 LSB resolution with Analog Watchdog on two channels.
- Full function Serial Communication Interface with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated with the Multifunction Timers and the Serial Communication Interface.
- Up to seven 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- 68-lead Window Ceramic Leaded Chip Carrier package for ST90E30.
- 48-pin Window Dual in Line Ceramic Multilayer package for ST90E31.
- 68-lead Plastic Leaded Chip Carrier package for ST90T30.
- 48-pin Dual in Line Plastic package for ST90T31

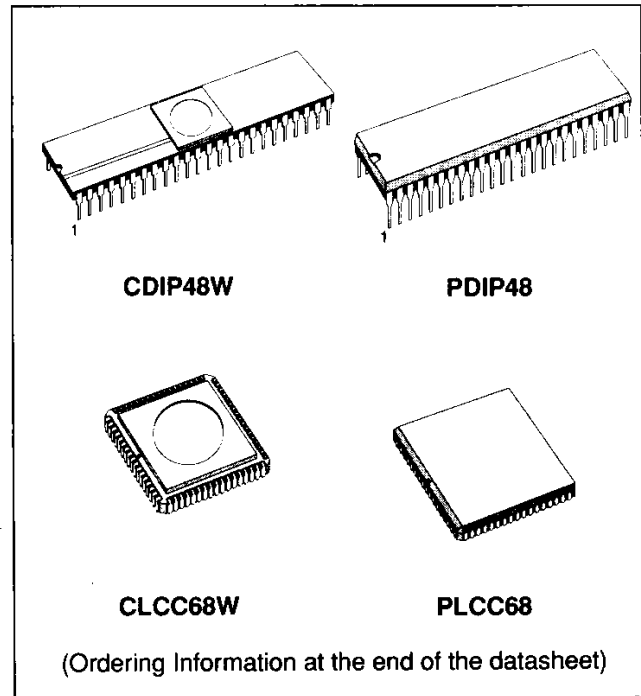


Figure 1. ST90E31, T31 Pin Configuration

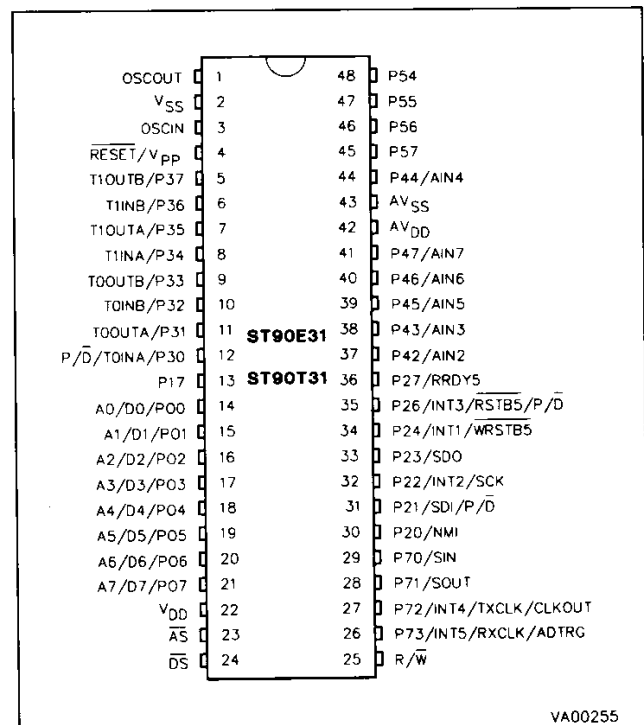


Figure 2. ST90E30,T30 Pin Configuration

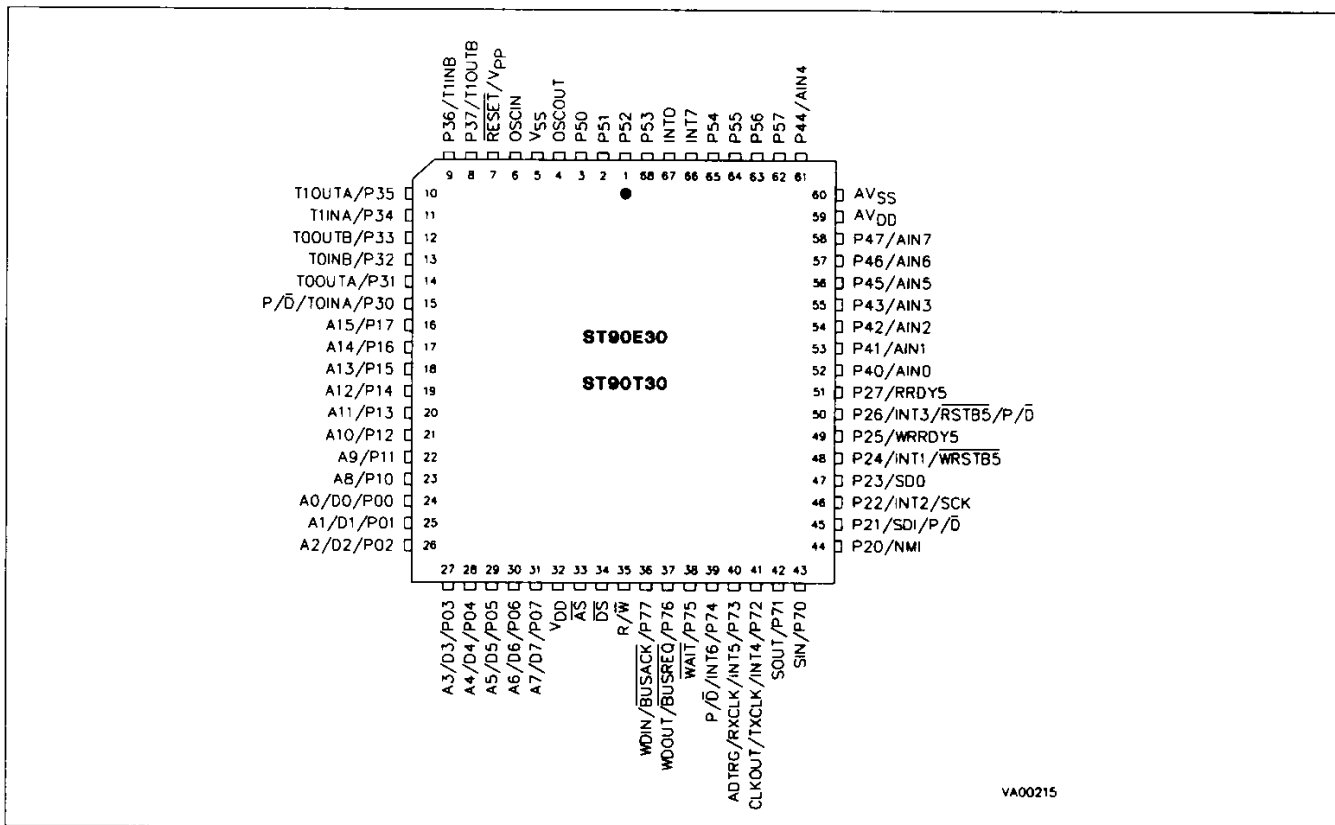
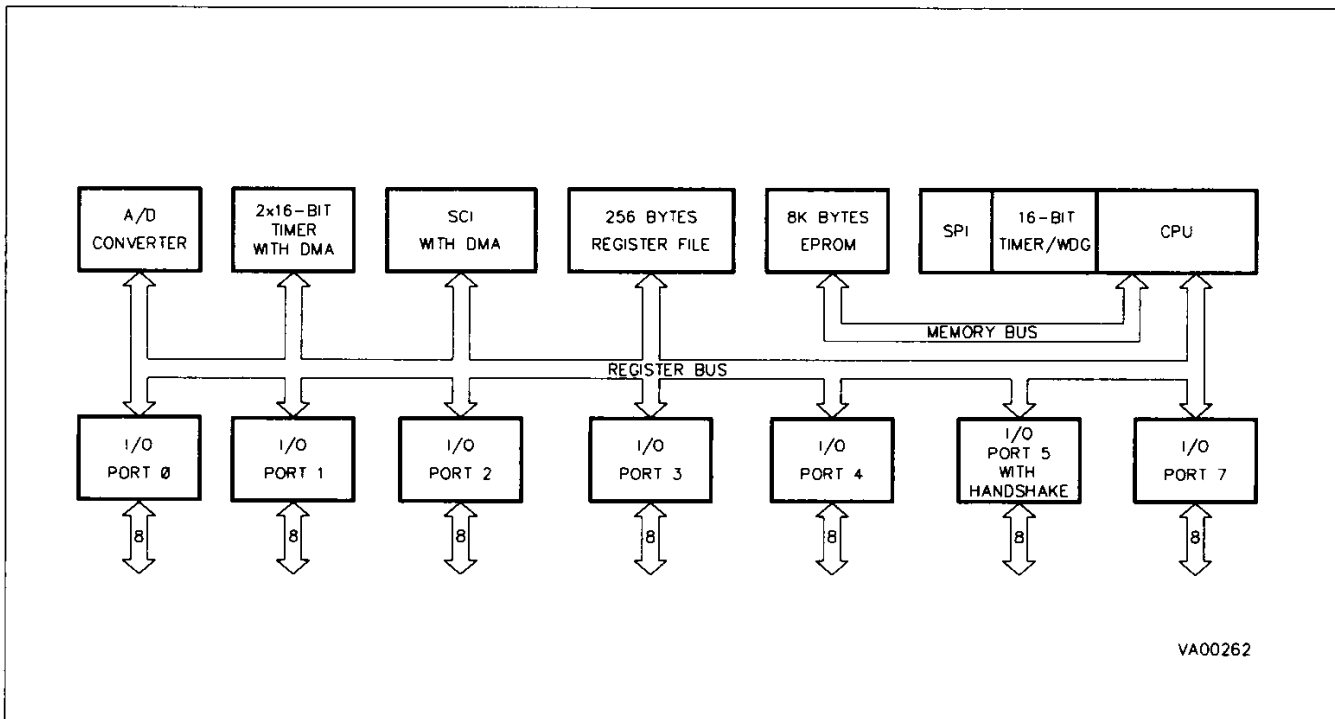


Figure 3. ST90E3X Block Diagram



## GENERAL DESCRIPTION

The ST90E30, ST90E31, ST90T30 and ST90T31 (following mentioned as ST90E3X) are EPROM members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

*THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9030 ROM-BASED DEVICE FOR FURTHER DETAILS.*

The EPROM ST90E3X may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 8K bytes of on-chip ROM, microcontrollers able to manage up to bytes of external memory, or as parallel processing elements in a system with other processors and peripheral controllers.

A key point of the ST90E3X architecture is related to its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90E3X is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I<sup>2</sup>C Bus and IM BUS Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E3X with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11 $\mu$ s conversion time and 8 bit  $\pm 1/2$  LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

## PIN DESCRIPTION

**$\overline{AS}$ .** *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of  $\overline{AS}$  indicates that address, Read/Write (R/W), and Data Memory signals are valid for program or data memory transfers. Under program control,  $\overline{AS}$  can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ( $\overline{DS}$ ) and R/W.

**$\overline{DS}$ .** *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of  $\overline{DS}$ . During a read cycle, Data In must be valid prior to the trailing edge of  $\overline{DS}$ . When the ST90E3X accesses on-chip memory,  $\overline{DS}$  is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1,  $\overline{AS}$  and R/W.

**R/W.** *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/W is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1,  $\overline{AS}$  and  $\overline{DS}$ .

**RESET/V<sub>PP</sub>.** *Reset (input, active low) or V<sub>PP</sub> (input).* The ST9 is initialised by the Reset signal. With the deactivation of RESET, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input V<sub>PP</sub>.

**OSCIN, OSCOUT.** *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

**AV<sub>DD</sub>.** Analog V<sub>DD</sub> of the Analog to Digital Converter.

**AV<sub>SS</sub>.** Analog V<sub>SS</sub> of the Analog to Digital Converter.

**V<sub>DD</sub>.** Main Power Supply Voltage (5V  $\pm$  10%).

**V<sub>SS</sub>.** Digital Circuit Ground.

**PIN DESCRIPTION** (Continued)

**P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P70-P77.** I/O Port Lines (Input/Output, TTL or CMOS compatible). 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate Functions (see next section).

**I/O Port Alternate Functions.** Each pin of the I/O ports of the ST90E3X may assume Alternative Functions as shown in the Pin Configuration Drawings. Due to Bonding options for the packages, some functions may not be present, Table 1 shows the Functions allocated to the I/O port pins and a summary of packages for which they are available.

**Table 1. ST90E3X I/O Port Alternate Function Summary**

| I/O PORT<br>Port. bit | Name   | Function | Alternate Function        | Pin Assignment |       |
|-----------------------|--------|----------|---------------------------|----------------|-------|
|                       |        |          |                           | 90E30          | 90E31 |
| P0.0                  | A0/D0  | I/O      | Address/Data bit 0 mux    | 24             | 14    |
| P0.1                  | A1/D1  | I/O      | Address/Data bit 1 mux    | 25             | 15    |
| P0.2                  | A2/D2  | I/O      | Address/Data bit 2 mux    | 26             | 16    |
| P0.3                  | A3/D3  | I/O      | Address/Data bit 3 mux    | 27             | 17    |
| P0.4                  | A4/D4  | I/O      | Address/Data bit 4 mux    | 28             | 18    |
| P0.5                  | A5/D5  | I/O      | Address/Data bit 5 mux    | 29             | 19    |
| P0.6                  | A6/D6  | I/O      | Address/Data bit 6 mux    | 30             | 20    |
| P0.7                  | A7/D7  | I/O      | Address/Data bit 7 mux    | 31             | 21    |
| P1.0                  | A8     | O        | Address bit 8             | 23             | –     |
| P1.1                  | A9     | O        | Address bit 9             | 22             | –     |
| P1.2                  | A10    | O        | Address bit 10            | 21             | –     |
| P1.3                  | A11    | O        | Address bit 11            | 20             | –     |
| P1.4                  | A12    | O        | Address bit 12            | 19             | –     |
| P1.5                  | A13    | O        | Address bit 13            | 18             | –     |
| P1.6                  | A14    | O        | Address bit 14            | 17             | –     |
| P1.7                  | A15    | O        | Address bit 15            | 16             | 13    |
| P2.0                  | NMI    | I        | Non-Maskable Interrupt    | 44             | 30    |
| P2.1                  | P/D    | O        | Program/Data Space Select | 45             | 31    |
| P2.1                  | SDI    | I        | SPI Serial Data Out       | 45             | 31    |
| P2.2                  | INT2   | I        | External Interrupt 2      | 46             | 32    |
| P2.2                  | SCK    | O        | SPI Serial Clock          | 46             | 32    |
| P2.3                  | SDO    | O        | SPI Serial Data In        | 47             | 33    |
| P2.4                  | INT1   | I        | External Interrupt 1      | 48             | 34    |
| P2.4                  | WRSTB5 | O        | Handshake Write Strobe P5 | 48             | 34    |
| P2.5                  | WRRDY5 | I        | Handshake Write Ready P5  | 49             | –     |
| P2.6                  | INT3   | I        | External Interrupt 3      | 50             | 35    |
| P2.6                  | RDSTB5 | I        | Handshake Read Strobe P5  | 50             | 35    |
| P2.6                  | P/D    | O        | Program/Data Space Select | 50             | 35    |
| P2.7                  | RDRDY5 | O        | Handshake Read Ready P5   | 51             | 36    |
| P3.0                  | T0INA  | I        | MF Timer 0 Input A        | 15             | 12    |
| P3.0                  | P/D    | O        | Program/Data Space Select | 15             | 12    |
| P3.1                  | T0OUTA | O        | MF Timer 0 Output A       | 14             | 11    |

## PIN DESCRIPTION (Continued)

Table 1. ST90E3X I/O Port Alternate Function Summary (Continued)

| I/O PORT<br>Port. bit | Name   | Function | Alternate Function         | Pin Assignment |       |
|-----------------------|--------|----------|----------------------------|----------------|-------|
|                       |        |          |                            | 90E30          | 90E31 |
| P3.2                  | T0INB  | I        | MF Timer 0 Input B         | 13             | 10    |
| P3.3                  | T0OUTB | O        | MF Timer 0 Output B        | 12             | 9     |
| P3.4                  | T1INA  | I        | MF Timer 1 Input A         | 11             | 8     |
| P3.5                  | T1OUTA | O        | MF Timer 1 Output A        | 10             | 7     |
| P3.6                  | T1INB  | I        | MF Timer 1 Input B         | 9              | 6     |
| P3.7                  | T1OUTB | O        | MF Timer 1 Output B        | 8              | 5     |
| P4.0                  | AIN0   | I        | A/D Analog Input 0         | 52             | –     |
| P4.1                  | AIN1   | I        | A/D Analog Input 1         | 53             | –     |
| P4.2                  | AIN2   | I        | A/D Analog Input 2         | 54             | 37    |
| P4.3                  | AIN3   | I        | A/D Analog Input 3         | 55             | 38    |
| P4.4                  | AIN4   | I        | A/D Analog Input 4         | 61             | 44    |
| P4.5                  | AIN5   | I        | A/D Analog Input 5         | 56             | 39    |
| P4.6                  | AIN6   | I        | A/D Analog Input 6         | 57             | 40    |
| P4.7                  | AIN7   | I        | A/D Analog Input 7         | 58             | 41    |
| P5.0                  |        | I/O      | I/O Handshake Port 5       | 3              | –     |
| P5.1                  |        | I/O      | I/O Handshake Port 5       | 2              | –     |
| P5.2                  |        | I/O      | I/O Handshake Port 5       | 1              | –     |
| P5.3                  |        | I/O      | I/O Handshake Port 5       | 68             | –     |
| P5.4                  |        | I/O      | I/O Handshake Port 5       | 65             | 48    |
| P5.5                  |        | I/O      | I/O Handshake Port 5       | 64             | 47    |
| P5.6                  |        | I/O      | I/O Handshake Port 5       | 63             | 46    |
| P5.7                  |        | I/O      | I/O Handshake Port 5       | 62             | 45    |
| P7.0                  | SIN    | I        | SCI Serial Input           | 43             | 29    |
| P7.1                  | SOUT   | O        | SCI Serial Output          | 42             | 28    |
| P7.2                  | INT4   | I        | External Interrupt 4       | 41             | 27    |
| P7.2                  | TXCLK  | I        | SCI Transmit Clock Input   | 41             | 27    |
| P7.2                  | CLKOUT | O        | SCI Byte Sync Clock Output | 41             | 27    |
| P7.3                  | INT5   | I        | External Interrupt 5       | 40             | 26    |
| P7.3                  | RXCLK  | I        | SCI Receive Clock Input    | 40             | 26    |
| P7.3                  | ADTRG  | I        | A/D Conversion Trigger     | 40             | 26    |
| P7.4                  | INT6   | I        | External Interrupt 6       | 39             | –     |
| P7.4                  | P/D    | O        | Program/Data Space Select  | 39             | –     |
| P7.5                  | WAIT   | I        | External Wait Input        | 38             | –     |
| P7.6                  | WDOUT  | O        | T/WD Output                | 37             | –     |
| P7.6                  | BUSREQ | I        | External Bus Request       | 37             | –     |
| P7.7                  | WDIN   | I        | T/WD Input                 | 36             | –     |
| P7.7                  | BUSACK | O        | External Bus Acknowledge   | 36             | –     |

**MEMORY**

The memory of the ST90E3X is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E3X 8K bytes of on-chip EPROM memory is selected at memory addresses 0 through 1FFFh (hexadecimal) in the Program Space, while the ST90T30 OTP version has the top 64 bytes of the program space reserved by SGS-THOMSON for testing purposes.

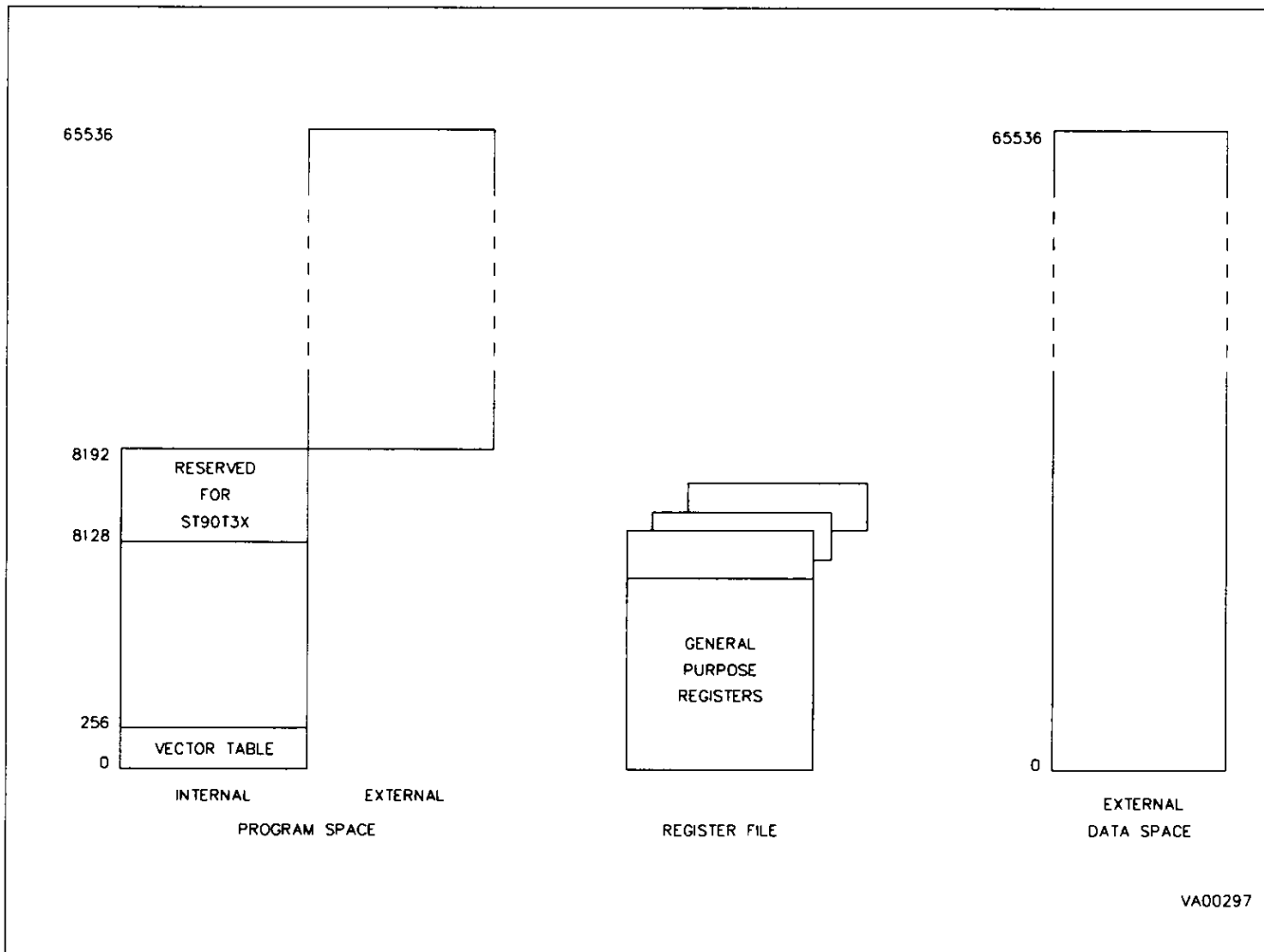
External memory may be addressed using the multiplexed address and data buses (Alternate

Functions of Port 0 and Port 1). At addresses greater than the first 8K of program space, the ST90E3X executes external memory cycles for instruction fetches. Data Memory may be decoded externally by using the P/D Alternate Function output. The on-chip general purpose (GP) Registers may be used as RAM memory for minimum chip count systems.

**EPROM PROGRAMMING**

The 8192 bytes of EPROM memory of the ST90E30 and ST90E31 (8128 for the ST90T3X) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

**Figure 4. Memory Spaces**



VA00297

**ABSOLUTE MAXIMUM RATINGS**

| Symbol                              | Parameter                            | Value   | Unit |
|-------------------------------------|--------------------------------------|---|------|
| V <sub>DD</sub>                     | Supply Voltage                       | - 0.3 to 7.0  | V    |
| AV <sub>DD</sub> , AV <sub>SS</sub> | Analog Supply Voltage                | V <sub>SS</sub> ≤ AV <sub>SS</sub> < AV <sub>DD</sub> ≤ V <sub>DD</sub> | V    |
| V <sub>I</sub>                      | Input Voltage                        | V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3                          | V    |
| V <sub>O</sub>                      | Output Voltage                       | V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3                          | V    |
| V <sub>PP</sub>                     | Input Voltage on V <sub>PP</sub> Pin | - 0.3 to 13.5   | V    |
| T <sub>STG</sub>                    | Storage Temperature                  | - 55 to + 150   | °C   |

**Note:** Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol            | Parameter                     | Value |      | Unit |
|-------------------|-------------------------------|-------|------|------|
|                   |                               | Min.  | Max. |      |
| T <sub>A</sub>    | Operating Temperature         | - 40  | 85   | °C   |
| V <sub>DD</sub>   | Operating Supply Voltage      | 4.5   | 5.5  | V    |
| f <sub>OSCE</sub> | External Oscillator Frequency |       | 24   | MHz  |
| f <sub>OSCI</sub> | Internal Oscillator Frequency |       | 12   | MHz  |

**DC ELECTRICAL CHARACTERISTICS**

(V<sub>DD</sub> = 5V ± 10% T<sub>A</sub> = - 40 °C to + 85°C, unless otherwise specified)

| Symbol            | Parameter              | Test Conditions                                      | Value                 |       |                       | Unit |
|-------------------|------------------------|--|-----------------------|-------|-----------------------|------|
|                   |                        |  | Min.                  | Typ.  | Max.                  |      |
| V <sub>IHCK</sub> | Clock Input High Level | External Clock                                       | 0.7 V <sub>DD</sub>   |       | V <sub>DD</sub> + 0.3 | V    |
| V <sub>ILCK</sub> | Clock Input Low Level  | External Clock                                       | - 0.3                 |       | 0.3 V <sub>DD</sub>   | V    |
| V <sub>IH</sub>   | Input High Level       | TTL  | 2.0                   |       | V <sub>DD</sub> + 0.3 | V    |
|                   |                        | CMOS   | 0.7 V <sub>DD</sub>   |       | V <sub>DD</sub> + 0.3 | V    |
| V <sub>IL</sub>   | Input Low Level        | TTL  | - 0.3                 |       | 0.8                   | V    |
|                   |                        | CMOS   | - 0.3                 |       | 0.3 V <sub>DD</sub>   | V    |
| V <sub>IHRS</sub> | Reset Input High Level |  | 0.7 V <sub>DD</sub>   |       | V <sub>DD</sub> + 0.3 | V    |
| V <sub>ILRS</sub> | Reset Input Low Level  |  | -0.3                  |       | 0.3 V <sub>DD</sub>   | V    |
| V <sub>HYRS</sub> | Reset Input Hysteresis |  | 0.3                   |       | 1.5                   | V    |
| V <sub>OH</sub>   | Output High Level      | Push Pull, I <sub>load</sub> = - 0.8mA               | V <sub>DD</sub> - 0.8 |       |                       | V    |
| V <sub>OL</sub>   | Output Low Level       | Push Pull or Open Drain, I <sub>load</sub> = - 1.6mA |                       |       | 0.4                   | V    |
| I <sub>WPU</sub>  | Weak Pull-up Current   | Bidirectional Weak Pull-up, V <sub>OL</sub> = 0V     | - 80                  | - 200 | - 420                 | μA   |

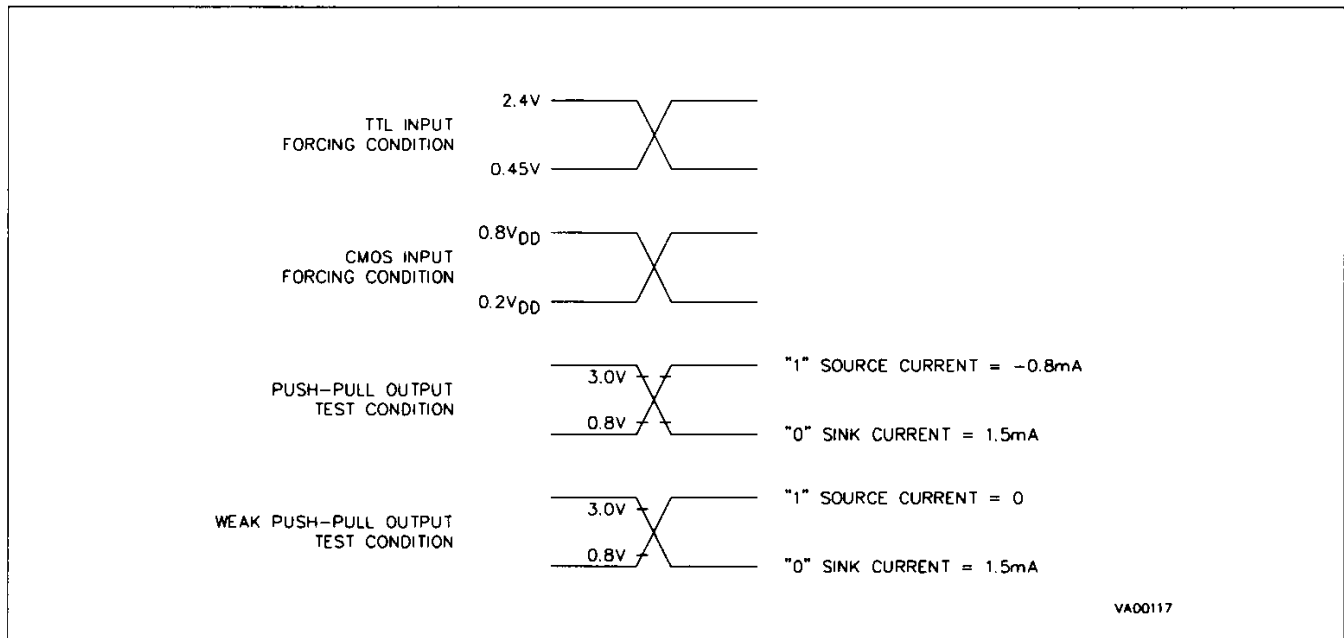


DC ELECTRICAL CHARACTERISTICS (continued)

| Symbol            | Parameter                                      | Test Conditions  | Value |       |       | Unit |
|-------------------|--|--|-------|-------|-------|------|
|                   |  |  | Min.  | Typ.  | Max.  |      |
| I <sub>APU</sub>  | Active Pull-up Current, for INT0 and INT7 only | V <sub>IN</sub> < 0.8V   | - 80  | - 200 | - 420 | μA   |
| I <sub>LKIO</sub> | I/O Pin Input Leakage                          | Input/Tri-State, 0V < V <sub>IN</sub> < V <sub>DD</sub>                | - 10  |       | + 10  | μA   |
| I <sub>LKRS</sub> | Reset Pin Input Leakage                        | 0V < V <sub>IN</sub> < V <sub>DD</sub>                                 | - 30  |       | + 30  | μA   |
| I <sub>LKAD</sub> | A/D Pin Input Leakage                          | Alternate Function, Open Drain, 0V < V <sub>IN</sub> < V <sub>DD</sub> | - 3   |       | + 3   | μA   |
| I <sub>LKAP</sub> | Active Pull-up Input Leakage                   | 0V < V <sub>IN</sub> < 0.8V  | - 10  |       | + 10  | μA   |
| I <sub>LKOS</sub> | OSCIN Pin Input Leakage                        | 0V < V <sub>IN</sub> < V <sub>DD</sub>                                 | - 10  |       | + 10  | μA   |
| I <sub>DD</sub>   | Run Mode Current                               | 24MHz, Note 1  |       | 32    | 70    | mA   |
|                   |  | 4MHz, Note 1   |       | 6     | 12    | mA   |
| I <sub>DP2</sub>  | Run Mode Current Prescale by 2                 | 24MHz, Note 1  |       | 19    | 40    | mA   |
|                   |  | 4MHz, Note 1   |       | 4     | 8     | mA   |
| I <sub>WFI</sub>  | WFI Mode Current                               | 24MHz, Note 1  |       | 9     | 18    | mA   |
|                   |  | 4MHz, Note 1   |       | 2.5   | 5     | mA   |
| I <sub>HALT</sub> | HALT Mode Current                              | 24MHz, Note 1  |       |       | 100   | μA   |
| V <sub>PP</sub>   | EPROM Programming Voltage                      |  | 12.2  | 12.5  | 12.8  | V    |
| I <sub>PP</sub>   | EPROM Programming Current                      |  |       |       | 30    | mA   |

Note: 1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS





## AC ELECTRICAL CHARACTERISTICS

## CLOCK TIMING TABLE

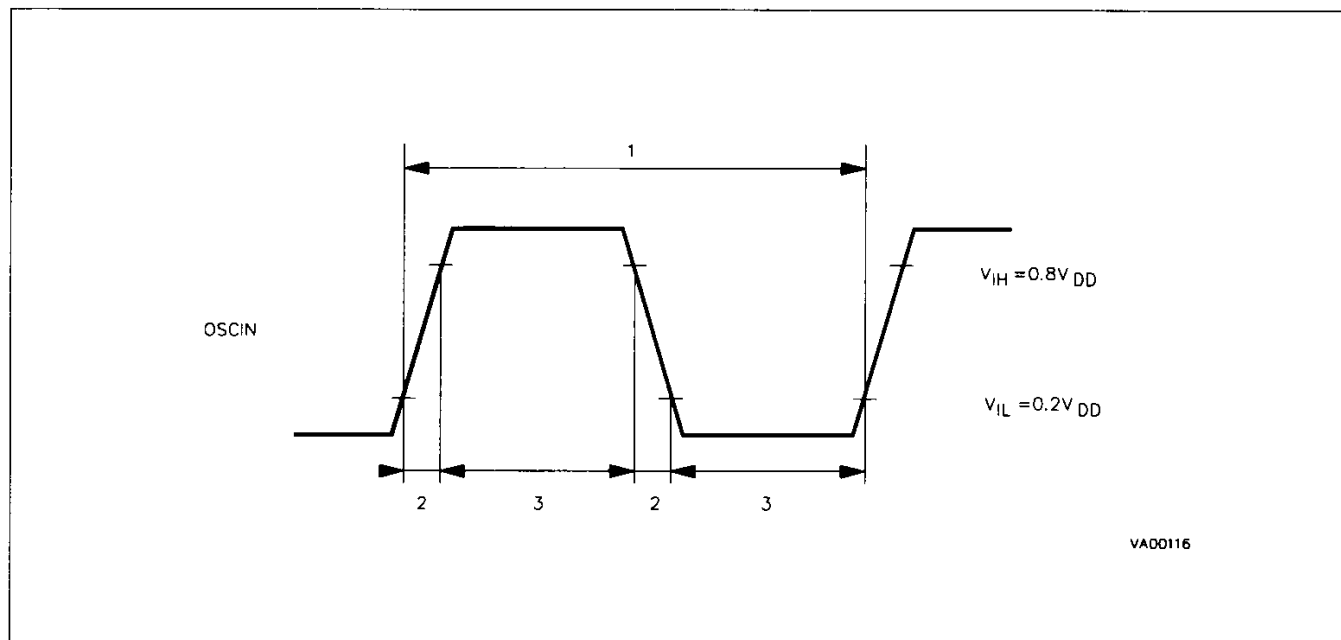
(V<sub>DD</sub> = 5V ± 10%, T<sub>A</sub> = - 40°C to + 85°C, unless otherwise specified)

| N° | Symbol     | Parameter                | Value |      | Unit | Note |
|----|------------|--------------------------|-------|------|------|------|
|    |            |                          | Min.  | Max. |      |      |
| 1  | TpC        | OSCIN Clock Period       | 41.5  |      | ns   | a    |
|    |            |                          | 83    |      | ns   | b    |
| 2  | TrC, TfC   | OSCIN Rise and Fall Time |       | 12   | ns   |      |
| 3  | TwCL, TwCH | OSCIN Low and High Width | 25    | 12   | ns   | a    |
|    |            |                          | 38    |      | ns   | b    |

## Notes:

- a. Clock divided by 2 internally (MODER.DIV2=1)  
b. Clock not divided by 2 internally (MODER.DIV2=0)

## CLOCK TIMING



**EXTERNAL BUS TIMING TABLE** ( $V_{DD} = 5V \pm 10\%$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $C_{load} = 50\text{pF}$ ,  $INTCLK = 12\text{MHz}$ , unless otherwise specified)

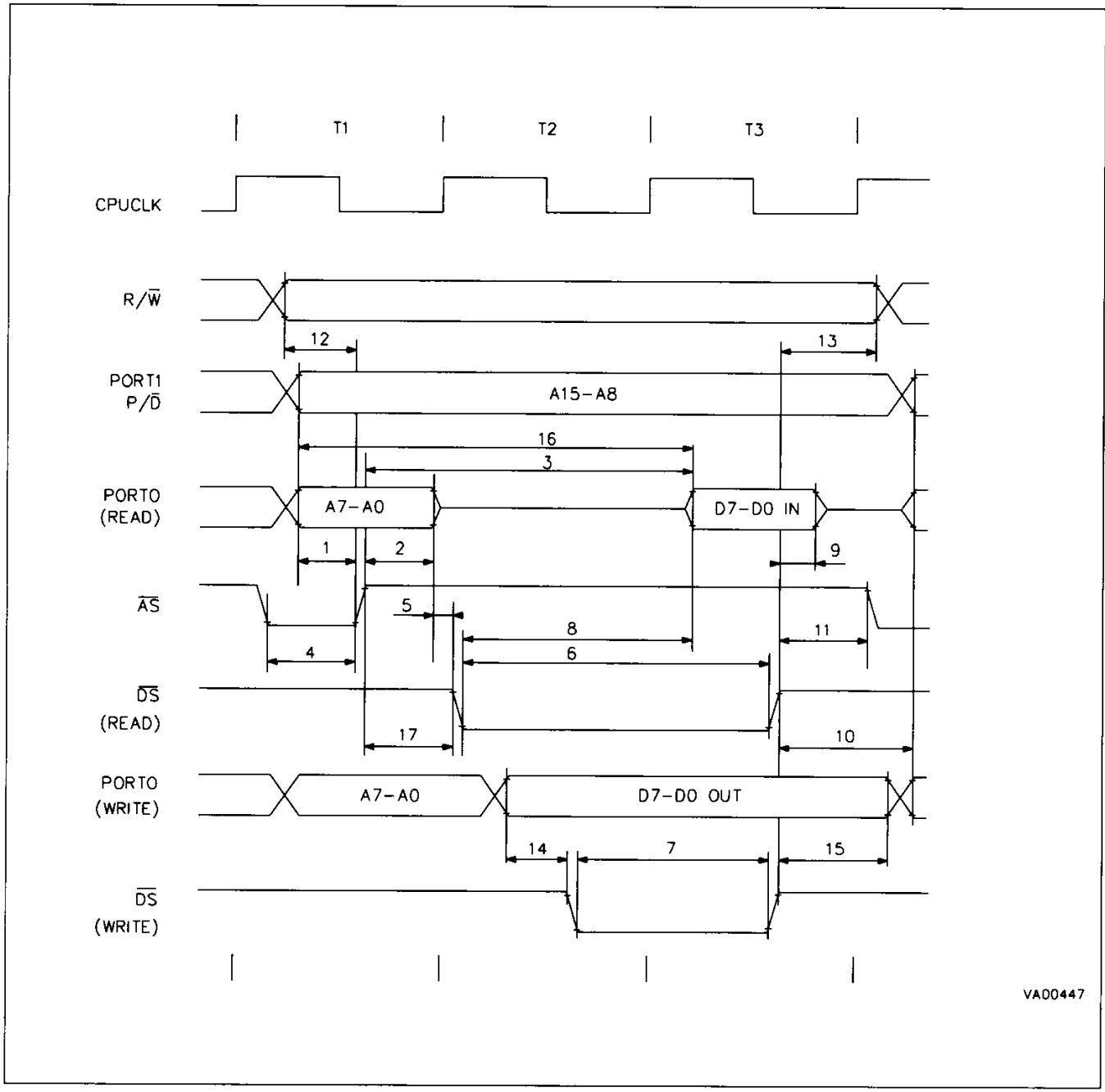
| N° | Symbol      | Parameter  | Value (Note)            |                                  |      |      | Unit |
|----|-------------|--|-------------------------|----------------------------------|------|------|------|
|    |             |  | OSCIN Divided By 2      | OSCIN Not Divided By 2           | Min. | Max. |      |
| 1  | TsA (AS)    | Address Set-up Time before $\overline{AS} \uparrow$          | $T_{pC} (2P+1) - 22$    | $T_{wCH} + P T_{pC} - 18$        | 20   |      | ns   |
| 2  | ThAS (A)    | Address Hold Time after $\overline{AS} \uparrow$             | $T_{pC} - 17$           | $T_{wCL} - 13$                   | 25   |      | ns   |
| 3  | TdAS (DR)   | $\overline{AS} \uparrow$ to Data Available (read)            | $T_{pC} (4P+2W+4) - 52$ | $T_{pC} (2P+W+2) - 51$           |      | 115  | ns   |
| 4  | TwAS        | $\overline{AS}$ Low Pulse Width                              | $T_{pC} (2P+1) - 7$     | $T_{wCH} + P T_{pC} - 3$         | 35   |      | ns   |
| 5  | TdAz (DS)   | Address Float to $\overline{DS} \downarrow$                  | 0                       | 0                                | 0    |      | ns   |
| 6  | TwDSR       | $\overline{DS}$ Low Pulse Width (read)                       | $T_{pC} (4P+2W+3) - 20$ | $T_{wCH} + T_{pC} (2P+W+1) - 16$ | 105  |      | ns   |
| 7  | TwDSW       | $\overline{DS}$ Low Pulse Width (write)                      | $T_{pC} (2P+2W+2) - 13$ | $T_{pC} (P+W+1) - 13$            | 70   |      | ns   |
| 8  | TdDSR (DR)  | $\overline{DS} \downarrow$ to Data Valid Delay (read)        | $T_{pC} (4P+2W-3) - 50$ | $T_{wCH} + T_{pC} (2P+W+1) - 46$ |      | 75   | ns   |
| 9  | ThDR (DS)   | Data to $\overline{DS} \uparrow$ Hold Time (read)            | 0                       | 0                                | 0    |      | ns   |
| 10 | TdDS (A)    | $\overline{DS} \uparrow$ to Address Active Delay             | $T_{pC} - 7$            | $T_{wCL} - 3$                    | 35   |      | ns   |
| 11 | TdDS (AS)   | $\overline{DS} \uparrow$ to $\overline{AS} \downarrow$ Delay | $T_{pC} - 18$           | $T_{wCL} - 14$                   | 24   |      | ns   |
| 12 | TsR/W (AS)  | R/W Set-up Time before $\overline{AS} \uparrow$              | $T_{pC} (2P+1) - 22$    | $T_{wCH} + P T_{pC} - 18$        | 20   |      | ns   |
| 13 | TdDSR (R/W) | $\overline{DS} \uparrow$ to R/W and Address Not Valid Delay  | $T_{pC} - 9$            | $T_{wCL} - 5$                    | 33   |      | ns   |
| 14 | TdDW (DSW)  | Write Data Valid to $\overline{DS} \downarrow$ Delay (write) | $T_{pC} (2P+1) - 32$    | $T_{wCH} + P T_{pC} - 28$        | 10   |      | ns   |
| 15 | ThDS (DW)   | Data Hold Time after $\overline{DS} \uparrow$ (write)        | $T_{pC} - 9$            | $T_{wCL} - 5$                    | 33   |      | ns   |
| 16 | TdA (DR)    | Address Valid to Data Valid Delay (read)                     | $T_{pC} (6P+2W+5) - 68$ | $T_{wCH} + T_{pC} (3P+W+2) - 64$ |      | 140  | ns   |
| 17 | TdAs (DS)   | $\overline{AS} \uparrow$ to $\overline{DS} \downarrow$ Delay | $T_{pC} - 18$           | $T_{wCL} - 14$                   | 24   |      | ns   |

**Note:** The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.  
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

**Legend:**

P = Clock Prescaling Value  
W = Wait Cycles  
 $T_{pC}$  = OSCIN Period  
 $T_{wCH}$  = High Level OSCIN half period  
 $T_{wCL}$  = Low Level OSCIN half period

EXTERNAL BUS TIMING



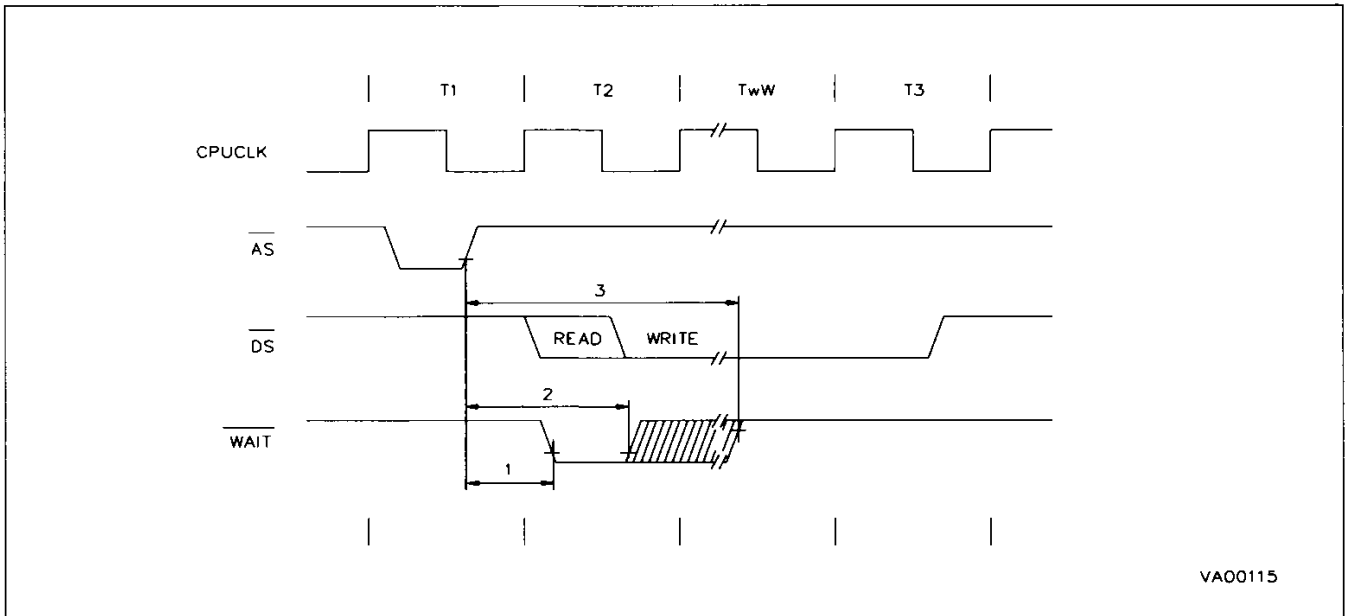
VA00447

**EXTERNAL WAIT TIMING TABLE** ( $V_{DD} = 5V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $C_{load} = 50pF$ ,  $INTCLK = 12MHz$ , Push-pull output configuration, unless otherwise specified)

| N° | Symbol      | Parameter                                      | Value (Note)       |                        |      |          | Unit |
|----|-------------|--|--------------------|------------------------|------|----------|------|
|    |             |  | OSCIN Divided By 2 | OSCIN Not Divided By 2 | Min. | Max.     |      |
| 1  | TdAS (WAIT) | AS $\uparrow$ to WAIT $\downarrow$ Delay       | $2(P+1)TpC - 29$   | $(P+1)TpC - 29$        |      | 40       | ns   |
| 2  | TdAS (WAIT) | AS $\uparrow$ to WAIT $\uparrow$ Minimum Delay | $2(P+W+1)TpC - 4$  | $(P+W+1)TpC - 4$       | 80   |          | ns   |
| 3  | TdAS (WAIT) | AS $\uparrow$ to WAIT $\uparrow$ Maximum Delay | $2(P+W+1)TpC - 29$ | $(P+W+1)TpC - 29$      |      | $83W+40$ | ns   |

**Note:** The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.  
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

**EXTERNAL WAIT TIMING**



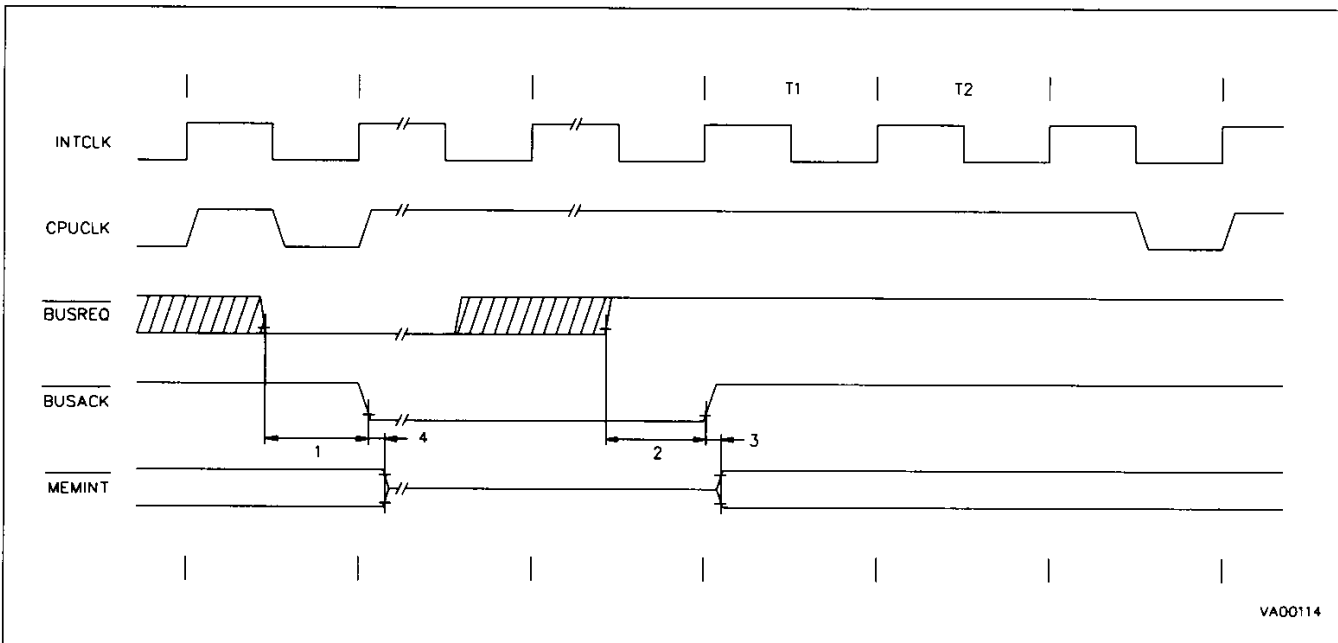
VA00115

**BUS REQUEST/ACKNOWLEDGE TIMING TABLE** ( $V_{DD} = 5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $C_{load} = 50\text{pF}$ ,  $\text{INTCLK} = 12\text{MHz}$ , Push-pull output configuration, unless otherwise specified)

| N° | Symbol        | Parameter               | Value (Note)         |                             |      |      | Unit |
|----|---------------|-------------------------|----------------------|-----------------------------|------|------|------|
|    |               |                         | OSCIN Divided By 2   | OSCIN Not Divided By 2      | Min. | Max. |      |
| 1  | TdBR (BACK)   | BREQ ↓ to BUSACK ↓      | $T_{pC}+8$           | $T_{wCL}+12$                | 50   |      | ns   |
|    |               |                         | $T_{pC}(6P+2W+7)+65$ | $T_{pC}(3P+W+3)+T_{wCL}+65$ |      | 360  | ns   |
| 2  | TdBR (BACK)   | BREQ ↑ to BUSACK ↑      | $3T_{pC}+60$         | $T_{pC}+T_{wCL}+60$         |      | 185  | ns   |
| 3  | TdBACK (BREL) | BUSACK ↓ to Bus Release | 20                   | 20                          |      | 20   | ns   |
| 4  | TdBACK (BACT) | BUSACK ↑ to Bus Active  | 20                   | 20                          |      | 20   | ns   |

**Note:** The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.  
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

### BUS REQUEST/ACKNOWLEDGE TIMING



**Note:** MEMINT = group of memory interface signals : AS, DS, R/W, P00-P07, P10-P17.

**HANDSHAKE TIMING TABLE** ( $V_{DD} = 5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $C_{load} = 50\text{pF}$ ,  $\text{INTCLK} = 12\text{MHz}$ , Push-pull output configuration, unless otherwise specified)

| N° | Symbol      | Parameter   | Value (Note)            |               |                               |                           | Min. | Max. | Unit |
|----|-------------|---|-------------------------|---------------|-------------------------------|---------------------------|------|------|------|
|    |             |   | OSCIN Divided By 2      |               | OSCIN Not Divided By 2        |                           |      |      |      |
|    |             |   | Min.                    | Max.          | Min.                          | Max.                      |      |      |      |
| 1  | TwRDY       | RDRDY, WRRDY Pulse Width in One Line Handshake                        | $2T_{pC} (P+W+1) - 18$  |               | $T_{pC} (P+W+1) - 18$         |                           | 65   |      | ns   |
| 2  | TwSTB       | RDSTB, WRSTB Pulse Width  | $2T_{pC} + 12$          |               | $T_{pC} + 12$                 |                           | 95   |      | ns   |
| 3  | TdST (RDY)  | RDSTB, or WRSTB $\uparrow$ to RDRDY or WRRDY $\downarrow$             |                         | $T_{pC} + 45$ |                               | $(T_{pC} - T_{wCL}) + 45$ |      | 87   | ns   |
| 4  | TsPD (RDY)  | Port Data to RDRDY $\uparrow$ Set-up Time                             | $(2P+2W+1) T_{pC} - 25$ |               | $T_{wCH} + (W+P) T_{pC} - 25$ |                           | 16   |      | ns   |
| 5  | TsPD (RDY)  | Port Data to WRRDY $\downarrow$ Set-up Time in One Line Handshake     | 43                      |               | 43                            |                           | 43   |      | ns   |
| 6  | ThPD (RDY)  | Port Data to WRRDY $\downarrow$ Hold Time in One Line Handshake       | 0                       |               | 0                             |                           | 0    |      | ns   |
| 7  | TsPD (STB)  | Port Data to WRSTB $\uparrow$ Set-up Time                             | 10                      |               | 10                            |                           | 10   |      | ns   |
| 8  | ThPD (STB)  | Port Data to WRSTB $\uparrow$ Hold Time                               | 25                      |               | 25                            |                           | 25   |      | ns   |
| 9  | TdSTB (PD)  | RDSTBD $\uparrow$ to Port Data Delay Time in Bidirectional Handshake  |                         | 35            |                               | 35                        |      | 35   | ns   |
| 10 | TdSTB (PHZ) | RDSTB $\uparrow$ to Port High-Z Delay Time in Bidirectional Handshake |                         | 25            |                               | 25                        |      | 25   | ns   |

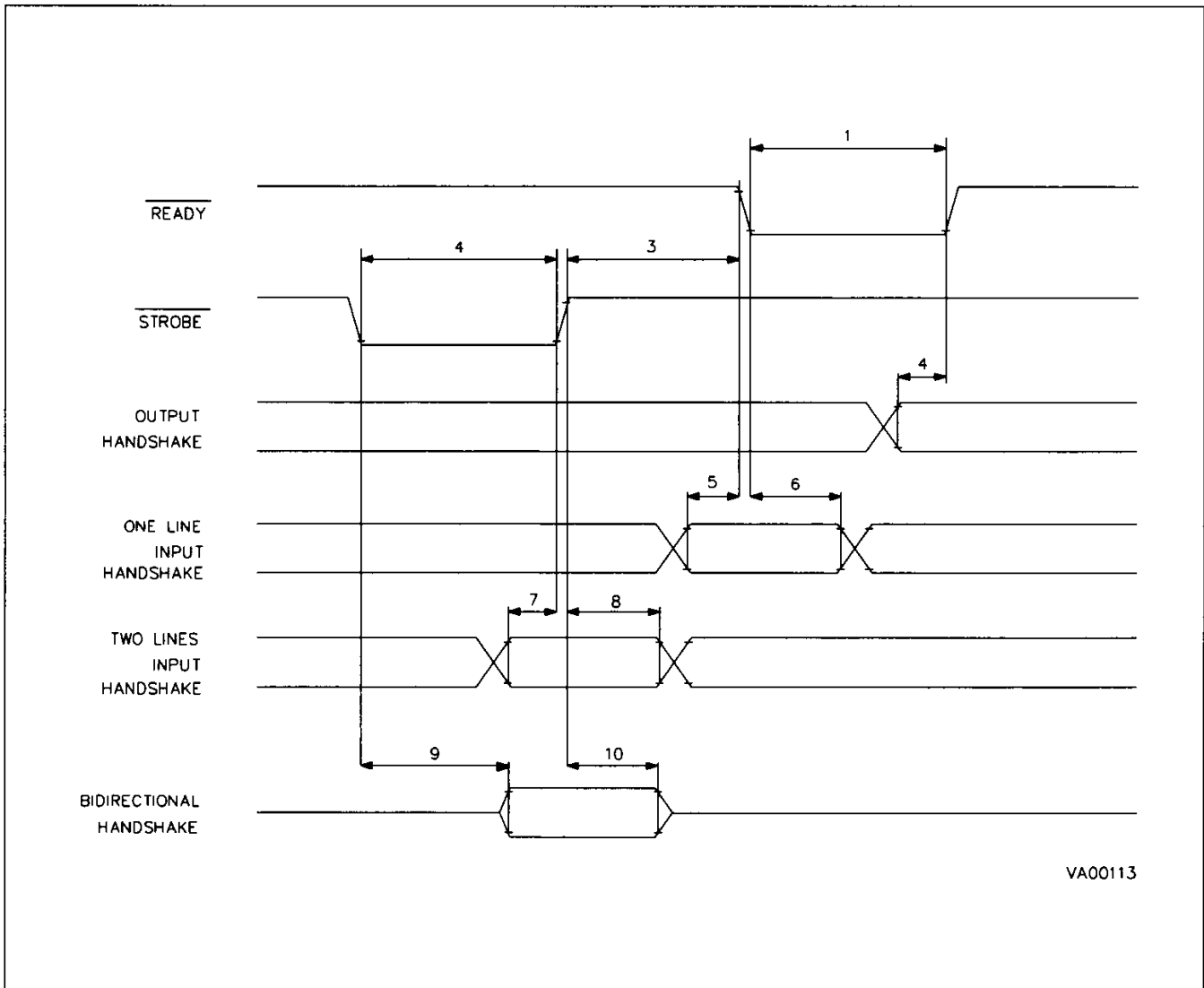
**Note:** The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted. The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

**Legend:**

P = Clock Prescaling Value (R235.4,3,2)

W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

## HANDSHAKE TIMING



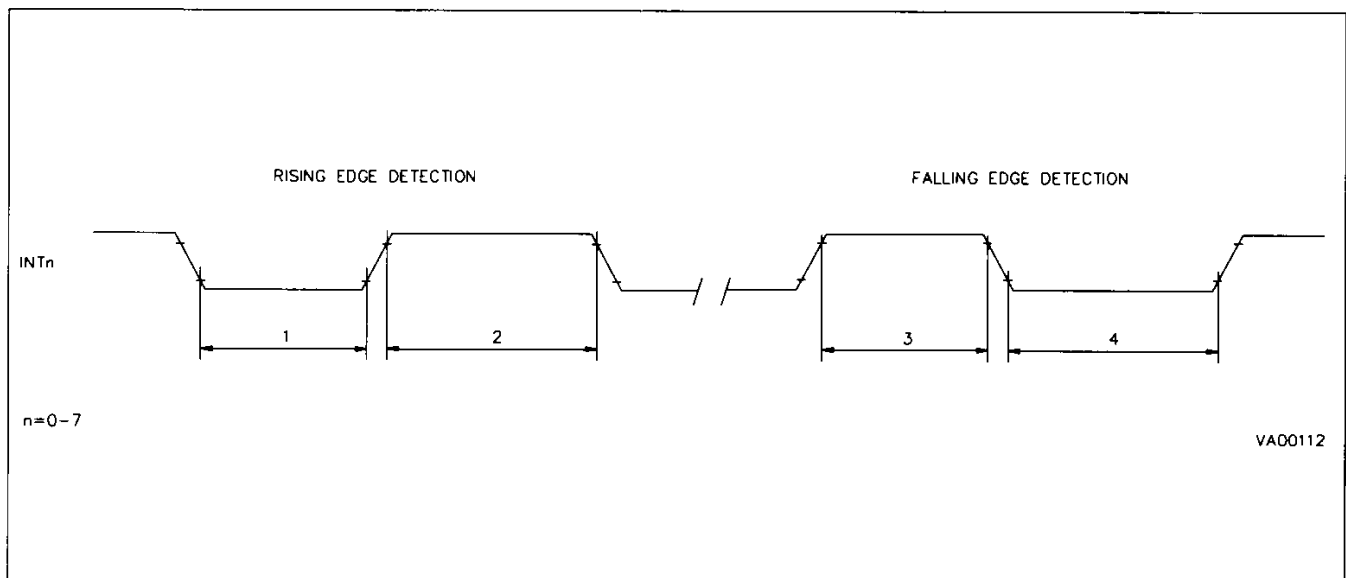


**EXTERNAL INTERRUPT TIMING TABLE** ( $V_{DD} = 5V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $C_{load} = 50pF$ ,  $INTCLK = 12MHz$ , Push-pull output configuration, unless otherwise specified)

| N° | Symbol | Parameter   | Value (Note)            |                             |      |      | Unit |
|----|--------|---|-------------------------|-----------------------------|------|------|------|
|    |        |   | OSCIN Divided By 2 Min. | OSCIN Not Divided By 2 Min. | Min. | Max. |      |
| 1  | TwLR   | Low Level Minimum Pulse Width in Rising Edge Mode   | $2T_{pC}+12$            | $T_{pC}+12$                 | 95   |      | ns   |
| 2  | TwHR   | High Level Minimum Pulse Width in Rising Edge Mode  | $2T_{pC}+12$            | $T_{pC}+12$                 | 95   |      | ns   |
| 3  | TwHF   | High Level Minimum Pulse Width in Falling Edge Mode | $2T_{pC}+12$            | $T_{pC}+12$                 | 95   |      | ns   |
| 4  | TwLF   | Low Level Minimum Pulse Width in Falling Edge Mode  | $2T_{pC}+12$            | $T_{pC}+12$                 | 95   |      | ns   |

**Note:** The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.  
 The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

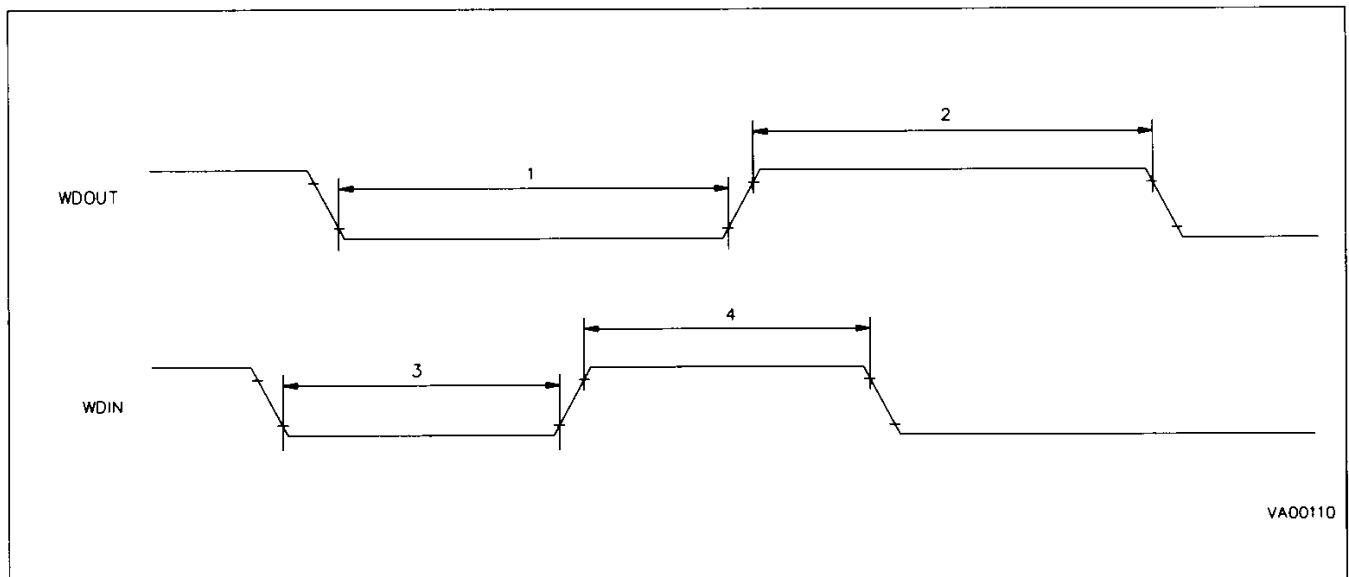
**EXTERNAL INTERRUPT TIMING**



**WATCHDOG TIMING TABLE** ( $V_{DD} = 5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $C_{load} = 50\text{pF}$ ,  $\text{INTCLK} = 12\text{MHz}$ , Output Alternate Function set as Push-pull)

| N° | Symbol      | Parameter              | Value |      | Unit |
|----|-------------|------------------------|-------|------|------|
|    |             |                        | Min.  | Max. |      |
| 1  | $T_{wWDOL}$ | WDOUT Low Pulse Width  | 620   |      | ns   |
| 2  | $T_{wWDOH}$ | WDOUT High Pulse Width | 620   |      | ns   |
| 3  | $T_{wWDIL}$ | WDIN Low Pulse Width   | 350   |      | ns   |
| 4  | $T_{wWDIH}$ | WDIN High Pulse Width  | 350   |      | ns   |

### WATCHDOG TIMING

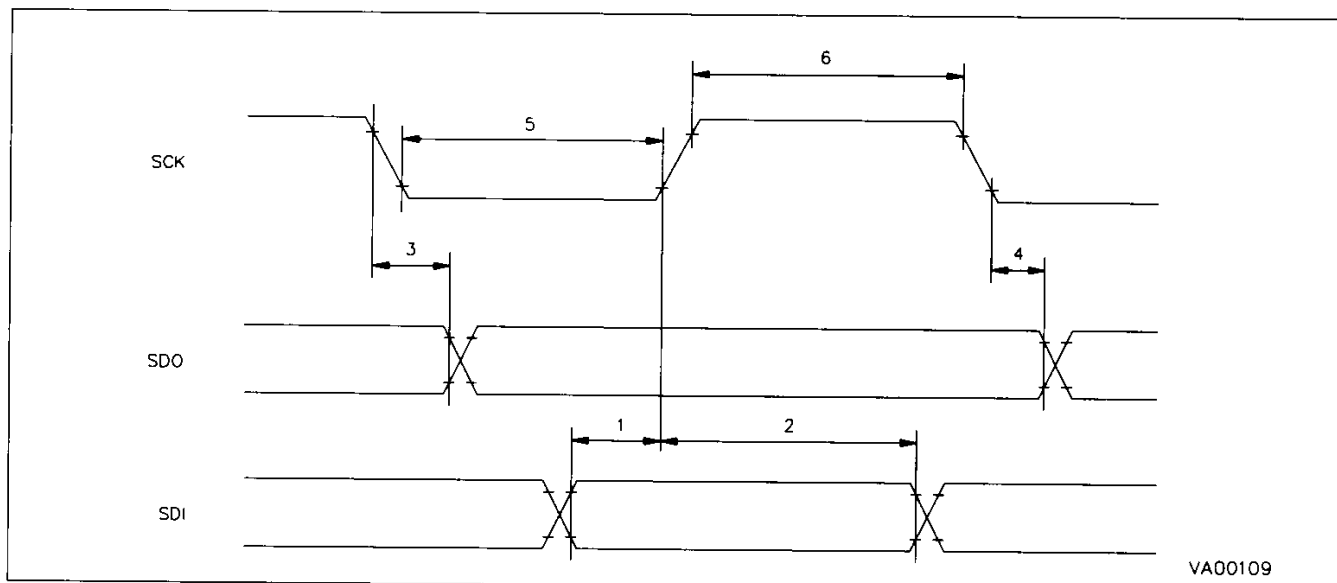


**SPI TIMING TABLE** ( $V_{DD} = 5V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $C_{load} = 50pF$ ,  $INTCLK = 12MHz$ , Output Alternate Function set as Push-pull)

| N° | Symbol   | Parameter                | Value              |      | Unit |
|----|----------|--------------------------|--------------------|------|------|
|    |          |                          | Min.               | Max. |      |
| 1  | TsDI     | Input Data Set-up Time   | 100                |      | ns   |
| 2  | ThDI (1) | Input Data Hold Time     | $1/2 T_{pC} + 100$ |      | ns   |
| 3  | TdOV     | SCK to Output Data Valid |                    | 100  | ns   |
| 4  | ThDO     | Output Data Hold Time    | -20                |      | ns   |
| 5  | TwSKL    | SCK Low Pulse Width      | 300                |      | ns   |
| 6  | TwSKH    | SCK High Pulse Width     | 300                |      | ns   |

Note: 1.  $T_{pC}$  is the Clock period.

**SPI TIMING**



PACKAGES MECHANICAL DATA

Figure 5. 48-Pin Window Dual In Line Ceramic Multilayer (D), 600-Mil Width

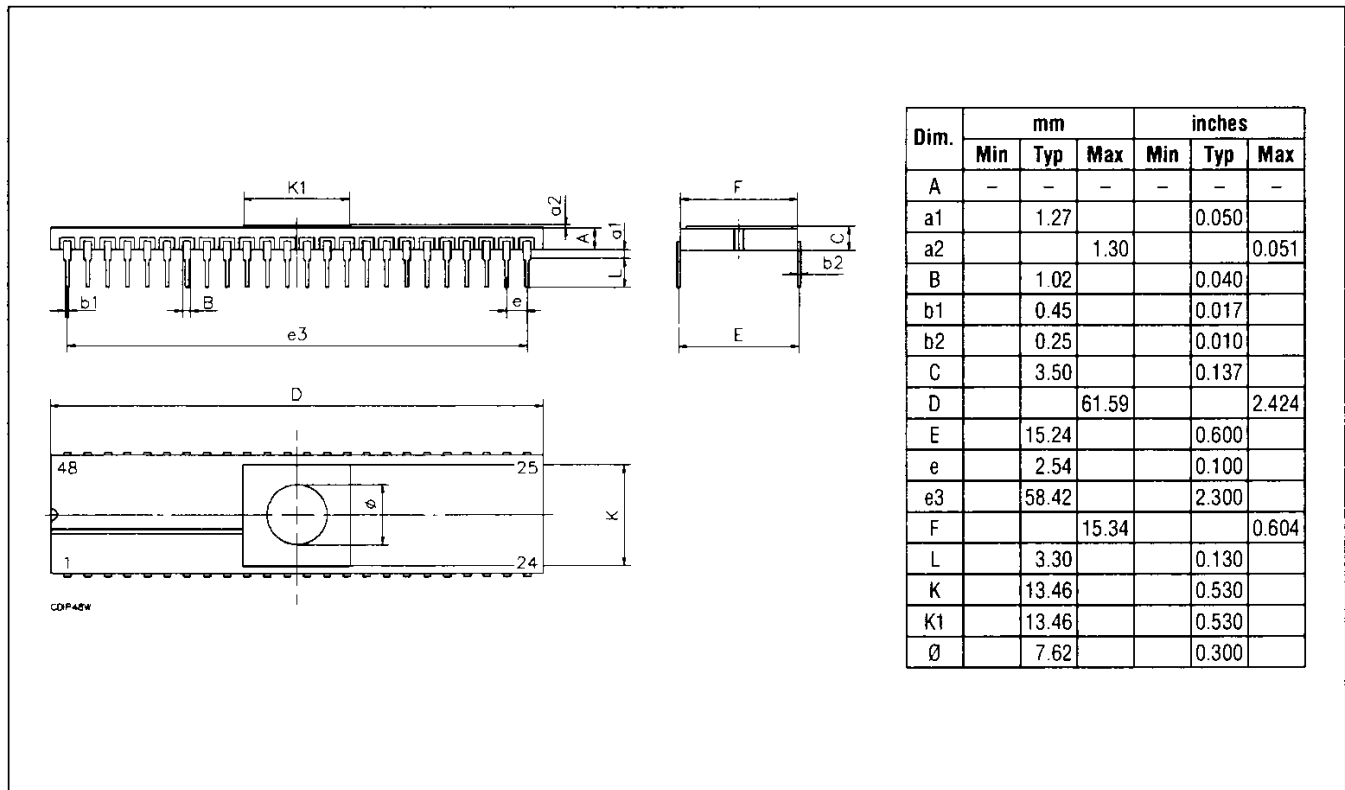
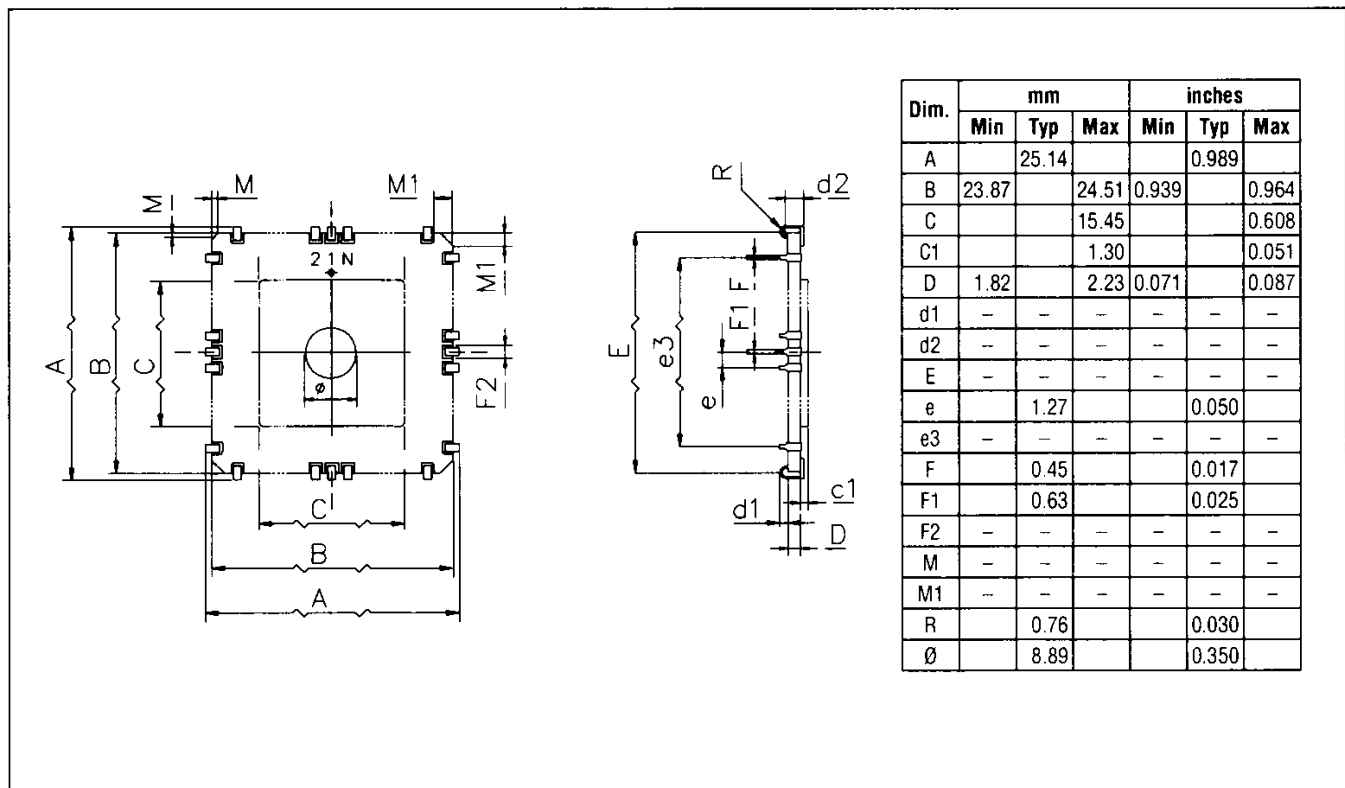


Figure 6. 68-Lead Window Ceramic Ledged Chip Carrier (L)



PACKAGES MECHANICAL DATA (continued)

Figure 7. 48-Pin Dual In Line Plastic (B), 600-Mil Width

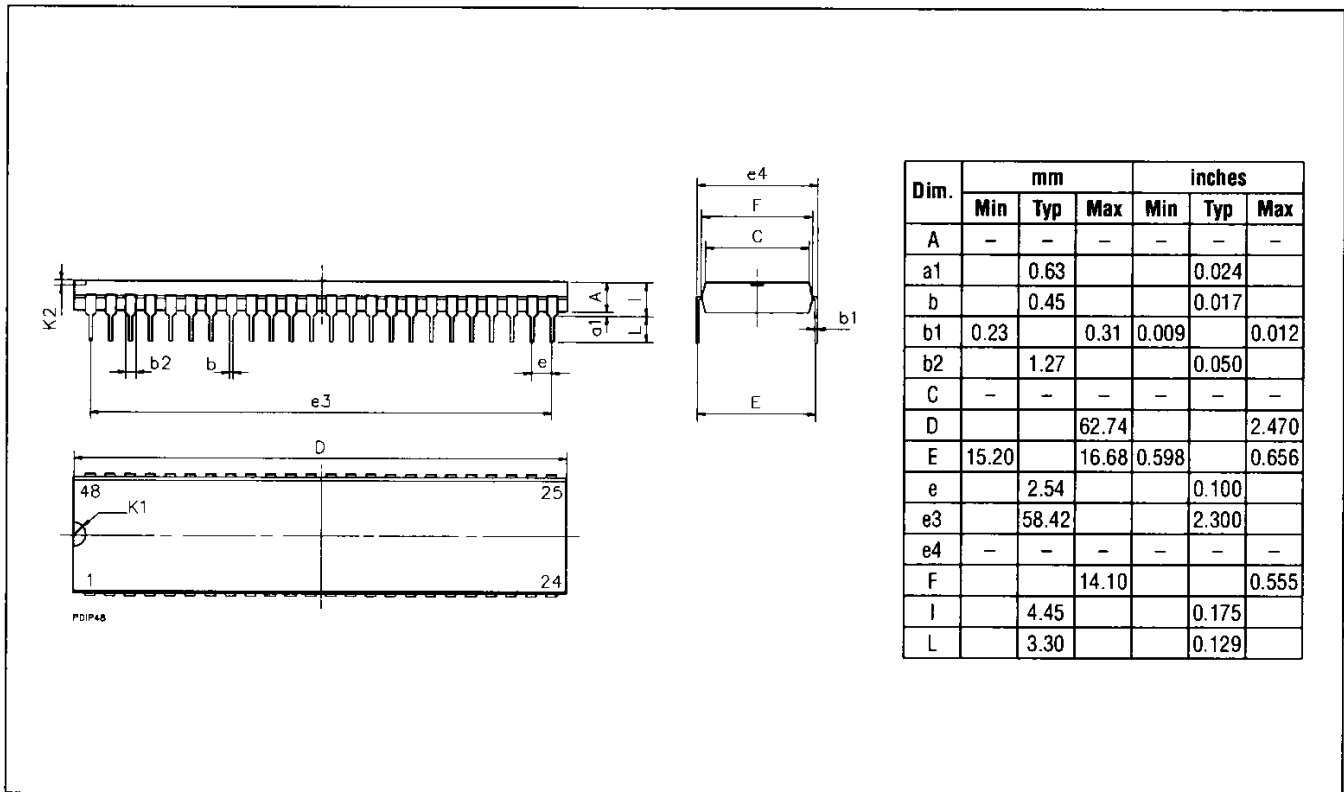
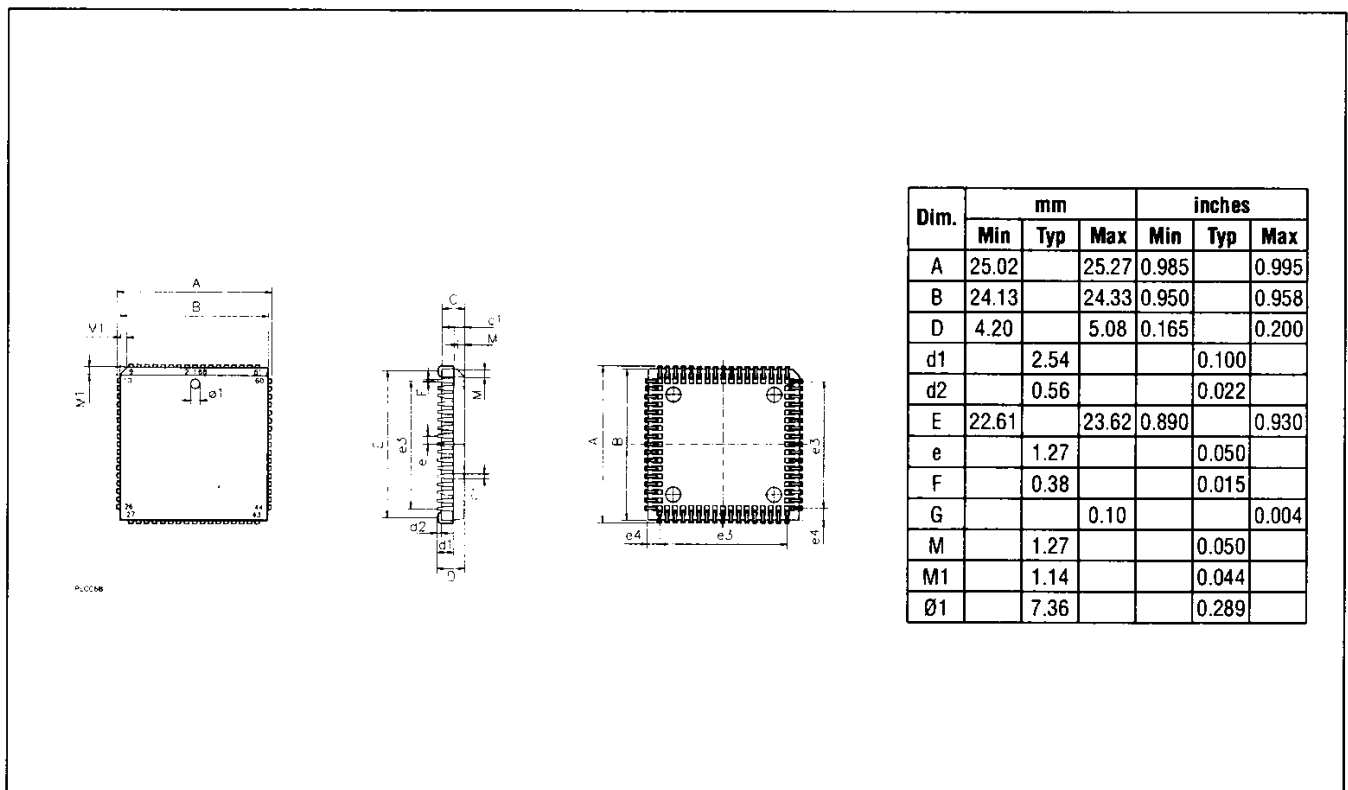


Figure 8. 68-Lead Plastic Leaded Chip Carrier (C)



## ORDERING INFORMATION

| Sales Type | Frequency | Temperature Range | Package |
|------------|-----------|-------------------|---------|
| ST90E30L6  | 24MHz     | - 40°C to + 85°C  | CLCC68W |
| ST90T30C6  | 24MHz     | - 40°C to + 85°C  | PLCC68  |
| ST90E31D6  | 24MHz     | - 40°C to + 85°C  | CDIP48W |
| ST90T31B6  | 24MHz     | - 40°C to + 85°C  | PDIP48  |
| ST90E30L1  | 24MHz     | 0°C to +70°C      | CLCC68W |
| ST90T30C1  | 24MHz     | 0°C to +70°C      | PLCC68  |
| ST90E31D1  | 24MHz     | 0°C to +70°C      | CDIP48W |
| ST90T31B1  | 24MHz     | 0°C to +70°C      | PDIP48  |