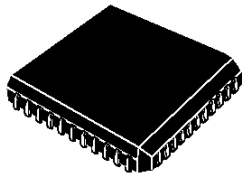
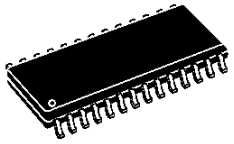
SGS-THOMSON MICROELECTRONICS

L6243
L6243D

VOICE COIL MOTOR DRIVER

- 12V/5V OPERATION
- PARKING FUNCTION FOR HARD DISK HEAD ACTUATOR
- OUTPUT CURRENT UP TO 2A DC, 2.5A PEAK
- LOW SATURATION VOLTAGE
- LOGIC AND POWER SUPPLY MONITOR
- LINEAR CONTROL
- THERMAL PROTECTION
- ENABLE FUNCTION
- CURRENT SENSE RESISTOR CONNECTIONS





PLCC44 **SO(24+2+2)**

ORDERING NUMBERS:

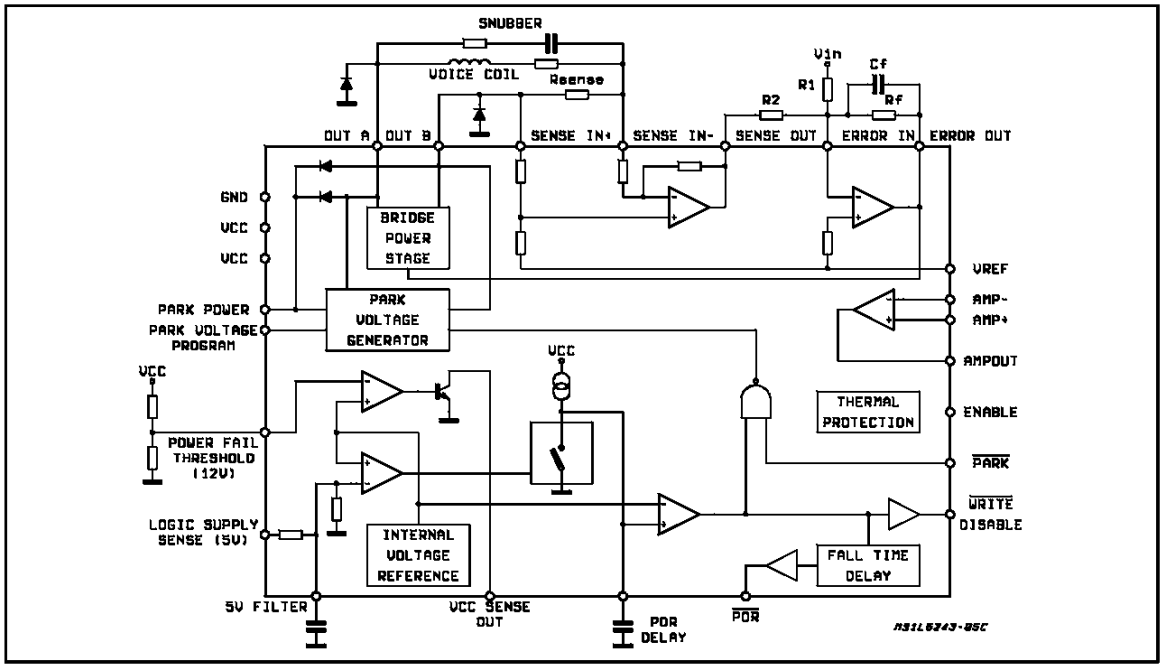
L6243 L6243D

DESCRIPTION

The L6243/D is a Bipolar IC developed for use in Hard Disk Head Actuator positioning applications. The Power Op-Amp Output Bridge, Differential Amplifier, and Error Amplifier, are controlled by TTL/CMOS, input compatible, Digital Logic, and an Analog Current Control Voltage. A simple RC compensation network, tied to the output of the Error Amp, will configure the system to work as a Transconductance Amplifier to drive a Voice Coil Motor in Linear Mode.

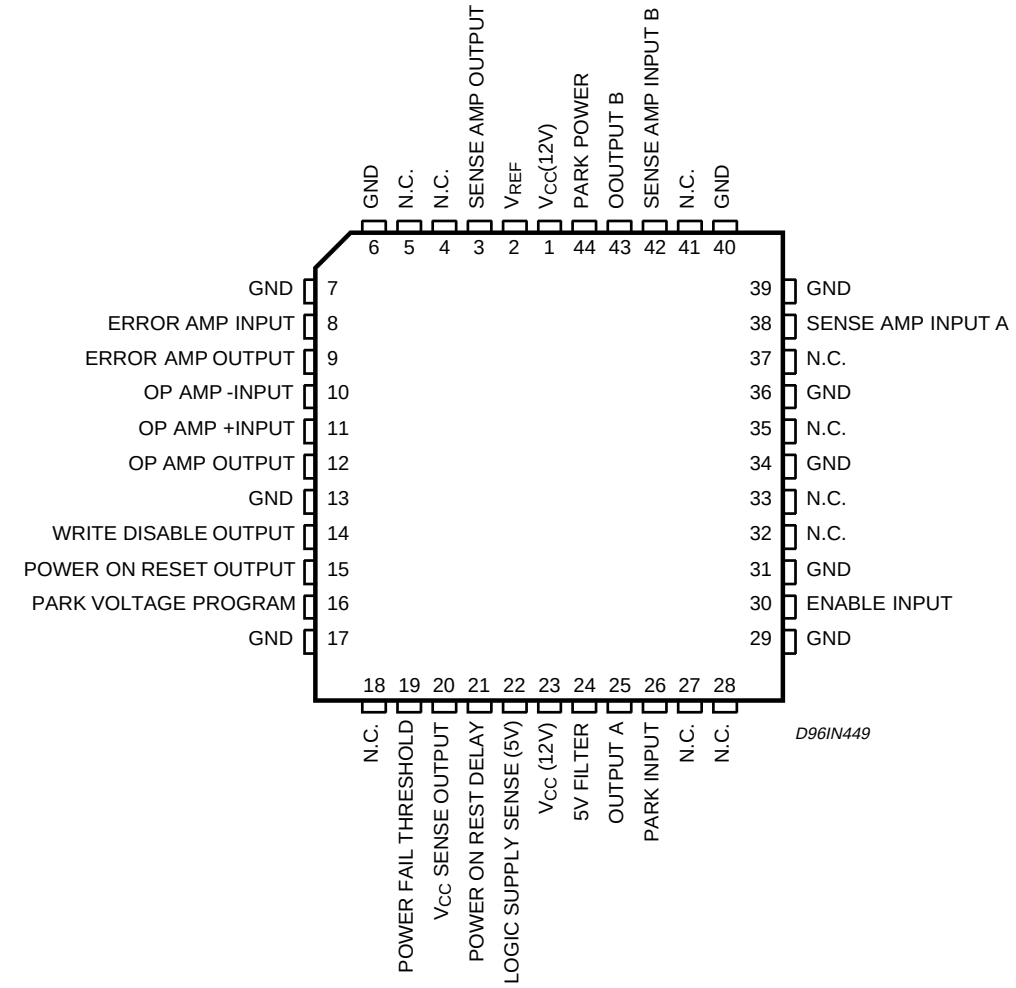
Additional features include Power On Reset Delay, Enable and Park, as well as a general purpose Operational Amplifier. A logic low at the Park input activates the parking function. Holding the Enable input low will disable the device by forcing the outputs into a tristate mode. Power Fail Monitors for the logic and power supplies initiate an automatic parking sequence during a power failure. A resistor programmed parking voltage enables a constant velocity head retract.

BLOCK DIAGRAM

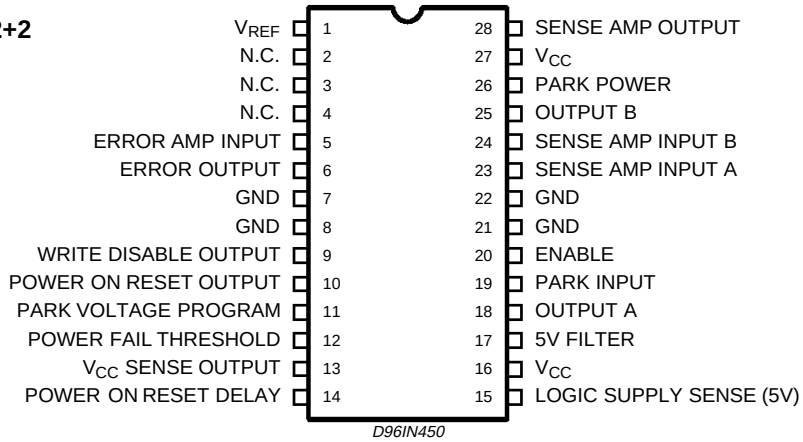


PIN CONNECTION (Top view)

PLCC-44



SO 24+2+2



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	18	V
V_{IN}	Input Voltage	0.3V to V_S	
V_{ID}	Differential Input Voltage	$\pm V_S$	
I_O	DC Output Current	2	A
I_p	Peak Output Current (non repetitive)	2.5	A
P_{tot}	Total Power Dissipation (T_{amb} = 70°C) for L6243 for L6243D	2 1.2	W W
T_{stg}	Storage and Junction Temperature	-55 to +150	°C

THERMAL DATA

Symbol	Description	L6243	L6243D	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction to pin	12	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to pin floating in air	62		°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to pin 16 cm^2 copper area on board heat sink	36	50	°C/W

PIN FUNCTIONS

Name	Function
V_{CC}	Power supply.
GND	Common Ground.
V_{ref}	Voltage Reference.
ENABLE	Input. Logic low will disable IC.
PARK POWER	Input Power supply for the parking circuit.
CURRENT SENSE OUT	Current sense operational amplifier output.
ERROR AMP IN	Error amplifier inverting input.
ERROR AMP OUT	Error amplifier output.
SENSE IN ±	Input for external sense resistors.
OUT A, B	Outputs of the two Power Operational Amplifiers Connections for Voice coil Motor.
PARK	External input for parking. Low will activate the park procedure.
PARK VOLTAGE PROGRAM	Input to set the park voltage.
POWER FAIL THRESHOLD	Supply monitor threshold setting.
LOGIC SUPPLY SENSE	Logic Supply Sense.
5V FILTER	Capacitor connection to filter the logic supply ripple.
V_{CC} SENSE OUT	Power supply failure monitor output.
POR	Power on reset output. Low will signal to the controller the failure of the logic supply.
POR DELAY	Capacitor connection to set the power on reset delay.
WRITE DISABLE	Output for write disable. Low will disable the writing mode.
AMP–	Inverting input of the additional op amp.
AMP+	Non-inverting input of the additional op amp.
AMPOUT	Output of the additional op amp.

ELECTRICAL CHARACTERISTICS (V_S = 12V, T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Range		4.5		13.2	V
I_d	Quiescent Drain Current			20		mA
T_j	Thermal Shutdown Junction Temperature			160		°C
ERROR AMPLIFIER						
I_b	Input Bias Current				1	µA
I_{OS}	Input Offset Current				300	nA
V_{OS}	Input Offset Voltage				5	mV
Gv	Large Signal Open Loop Voltage Gain		65			dB
GBW	Gain Bandwidth			3		MHz
G_{min}	Minimum Voltage Gain		5			
I_O+	Output Source Current			6		mA
I_{O-}	Output Sink Current			6		mA
SR	Slew-rate			2		V/µs
SENSE AMPLIFIER						
R_{IN}, V_{ref}	V_{ref} Input Impedance		9			KΩ
A_d	Differential Gain			8		V/V
SR	Slew-rate			1		V/µs
GBW	Gain Bandwidth Product			3		MHz
R_{in}	Sense Input Impedance		1.5			KΩ
CMRR	Common Mode Rejection Ratio		55			dB
POWER OP. AMP.						
G_V	Voltage Gain			26		dB
V_d	Total Output Voltage Drop	I_O = 250mA I_O = 500mA I_O = 1A I_O = 2A		450 750 1.15 2.30	 1.5 2.5	mV mV V V
V_{off}	Offset Voltage on Sense Resistor			5		mV
BW	Bandwidth on Resistive Load			100		KHz
GENERAL PURPOSE OP-AMP						
I_b	Input Bias Current				1	µA
I_{OS}	Input Offset Current				300	nA
V_{OS}	Input Offset Voltage				5	mV
G_V	Large Signal Open Loop Voltage Gain		65			dB
GBW	Gain Bandwidth Product			1		MHz
I_{O+}	Output Source Current			6		mA
I_{O-}	Output Sink Current			6		mA
SR	Slew Rate			1		V/µs

ELECTRICAL CHARACTERISTICS (continued)

MONITORS AND CONTROL CIRCUIT

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{t1}	Threshold Voltage at Logic Supply Sense		4.45	4.60	4.75	V
V_{t2}	Threshold Voltage at Power Fail Threshold Input		1.375	1.4	1.435	V
HV_{t1}	Hysteresis on V_{t1}			50		mV
HV_{t2}	Hysteresis on Vt2			15		mV
V_{ll}	Low Level Voltage	Write Disable = 2mA		250	500	mV
		Power on Reset = 2mA		250	500	mV
I_e	Enable Input Current	V_i = 2.4V			100	µA
		V_i = 0.4V			–200	µA
I_p	Input Current at Park	V_i = 2.4V			100	µA
		V_i = 0.4V			–200	µA
R_f	Equivalent Input Resistance at 5V Filter Input			6.9		KΩ
V_{enl}	Enable Low Input Voltage				0.8	V
V_{enh}	Enable High Input Voltage		2			V
V_{ph}	Parking Input High Voltage		2			V
V_{pl}	Parking Input Low Voltage				0.8	V
V_{pfl}	Power Fail Low Output Voltage	I_l = 2mA			0.5	V
I_{prog}	Parking Voltage Program Current			100		µA
I_{ch}	Power On Reset Delay Capacitor Charging			10		µA
T_d	Delay Between Write Disable and Power on Reset Falling Edges			4	10	µs

FUNCTIONAL DESCRIPTION

The VCM Driver is controlled via three control signals, ENABLE, POWER ON RESET, and WRITE DISABLE. An analog input voltage, ERROR AMP IN, controls the polarity and amplitude of the VCM driving current.

Refer to figure two. This diagram is a representation of the function of the VCM System. Note that the signals with the bars represent the "not true", or "non asserted" condition. From initial power up, the system is held in the Park Mode. Upon completion of the POWER UP RESET DELAY the machine moves to Tristate Mode or Run Mode, depending upon the condition of the ENABLE input. If ENABLE is asserted, the machine moves directly to Run Mode. If ENABLE is not asserted, the machine moves to Tristate Mode.

POWER ON RESET is an asynchronous output. Additionally it affects the internal logic as a hard wired reset and therefore if a supply failure occurs during Tristate or Run state, the machine moves directly back to the Park Mode. A WRITE DISABLE occurs a few to ten microseconds prior to the POWER ON RESET in order for the system to halt any read/write activity before a head retract begins.

While in Tristate Mode, the assertion of ENABLE will move the machine to the Run Mode. Run Mode will typically be the steady running state. The deassertion of the ENABLE signal causes the machine to move into Tristate. If it is desired to perform an active Parking function, the PARK input must be driven low by the external hardware, or the the VCM can be driven to the Park position via the ERROR AMP IN control voltage

FUNCTIONAL DESCRIPTION (continued)

Function	Description
V_{CC} input	This is the Power Supply input.
POWER FAIL THRESH	Input for the V_{CC} supply monitor. The Threshold can be externally set via a voltage divider.
V_{CC} SENSE OUT Output	TTL compatible signal indicating the V_{CC} supply has dropped below the POWER FAIL THRESHOLD.
LOGIC SUPPLY SENSE input	This input is used to monitor the Five Volt Logic Supply for the external control and other support IC's. The LOGIC SUPPLY SENSE operates independently of the 12V Power Supply. When a 5V supply failure is detected a POWER ON RESET is generated.
5V FILTER input	This pin allows for the application of filter circuitry in order to avoid false triggering.
PARK POWER input	This input is used during the Power Down/Power Fail Parking operation. When the supply goes down, a typical Spindle Driver Circuit automatically tristates its output stages. During this time the spindle motor spins freely and the stored energy is used to drive the VCM to the park position. The generated BEMF is rectified and filtered across an external PARKING CAPACITOR.
PROGRAMMABLE PARK VOLTAGE input	Used to set the voltage applied to the VCM during an Automatic Parking Operation.
PARK input	Logic signal asserted low, activates parking.
POWER ON RESET output	Indicates an error condition to the external control and support circuitry. A Logic Supply Fail condition automatically initiates a POWER ON RESET. Internal 30k Pullup to LSS.
POWER ON RESET DELAY input	The intent of this input is to provide a time delay at power up. During this time, the POWER ON RESET line will be asserted (low). A POWER ON RESET, will hold the system in the PARK mode. Once the delay has timed out, the POWER ON RESET will be removed to allow the external system to assume control. When applied in a Disk Drive Application, the POWER ON RESET DELAY will be required to have a minimum duration which will ensure that the Read/Write Heads can be fully parked.
WRITE DISABLE output	Becomes asserted a few microseconds prior to the assertion of POWER ON RESET. Internal 30k Pullup to LSS.
ENABLE input	This signal originates at the external controller and, when asserted, allows the VCM Drivers to operate. When deasserted the VCM Driver is forced into Tristate mode. During a POWER ON RESET condition however, the parking operation is automatic and takes priority over the ENABLE function. Only at the end of the POWER ON RESET DELAY will the ENABLE input become active. If active parking is desired, it will be accomplished under control of the V_{IN} signal, otherwise it is an automatic function at power down.
V_{REF} input	The reference voltage input is basically that voltage, at which the output current is zero.
ERROR AMP IN input	Inverting input of error amplifier. The non inverting one is internally tied to V_{ref}. Open collector output.
ERROR AMP OUT output	Error amplifier output pin.
OUTPUT A power output	Voice Coil power output.
OUTPUT B power output	Voice Coil power output.
SENSE AMP IN A/B signal input	Sense amplifier input pins. The sense resistor is connected across these pins.
SENSE AMP OUT signal output	Output pin of sense amplifier.
AMPOUT output	Output of an internal op-amp for general application.
AMP+ input	General purpose op-amp non inverting input.
AMP- input	General purpose op-amp inverting input.

BLOCK DESCRIPTION

OUTPUT STAGE

It consists of two Power Op Amps connected in bridge configuration.

CURRENT SENSE AMPLIFIER

Differential amplifier whose inputs are connected to the sense lines and whose output is accessible externally. Closing the loop will transform the differential voltage signal from the sense lines into a current signal for the Error Amplifier.

ERROR AMPLIFIER

Error amplifier which drives the output stage. The input and the output pins are accessible externally.

POWER SUPPLY MONITOR OPERATION

The circuit monitors the logic supply voltage input (typ 5V) and activates Power on Reset and Write Disable output when such a supply drops below the safe operating limit. After the logic supply voltage reaches its nominal value a delay capacitor has to be charged [Tdelay=3x10e5 x C sec] before Power on Reset and Write Disable outputs change from low to high level. Falling edges of Write Disable and Power on Reset are delayed (typ 4µs) in order to disable the writing on the disk before the Power on Reset is activated. An additional supervisor circuit is present in the IC with a programmable threshold, which is set by an external resistive divider. The TTL compatible output can be used separately or connected to Park input in order to park the head.

The V_{CC} sense output pin can also be connected to 5V filter input in order to implement a POWER ON RESET function sensitive both to 5V and V_{CC}.

PARKING CIRCUIT OPERATIONT

The voice coil driver is switched into the parking condition when Power on Reset output or Park input are low. In such a condition a fixed voltage is superimposed on the load and the value of such a voltage is set by connecting an external resistor between Park Voltage Program input and ground: (Vpark=Rext x Iref, Iref=100µA typ). Connecting ENABLE input to GND the driver will be disabled (outputs in high impedance mode).

THERMAL SHUTDOWN

It will disable the IC when the junction temperature exceeds the threshold value above which the device could be damaged.

Figure 1: Application Circuit (The pinout refers to the L6243)

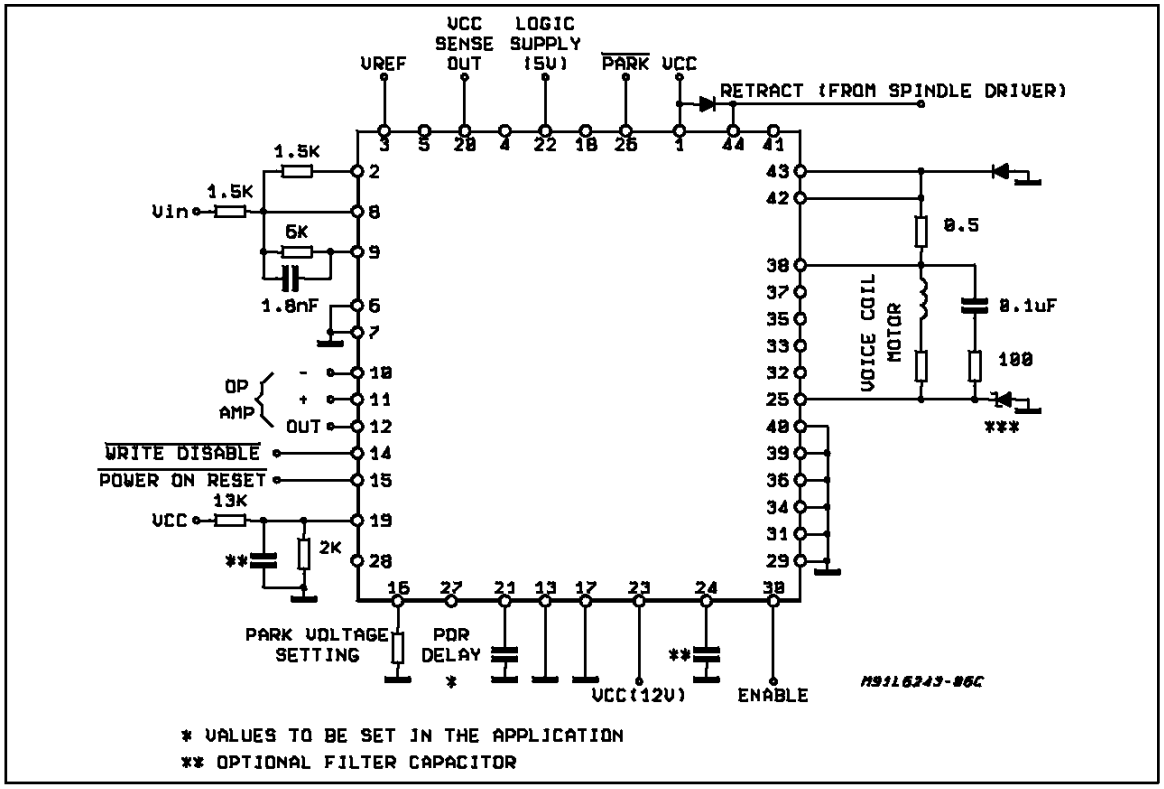
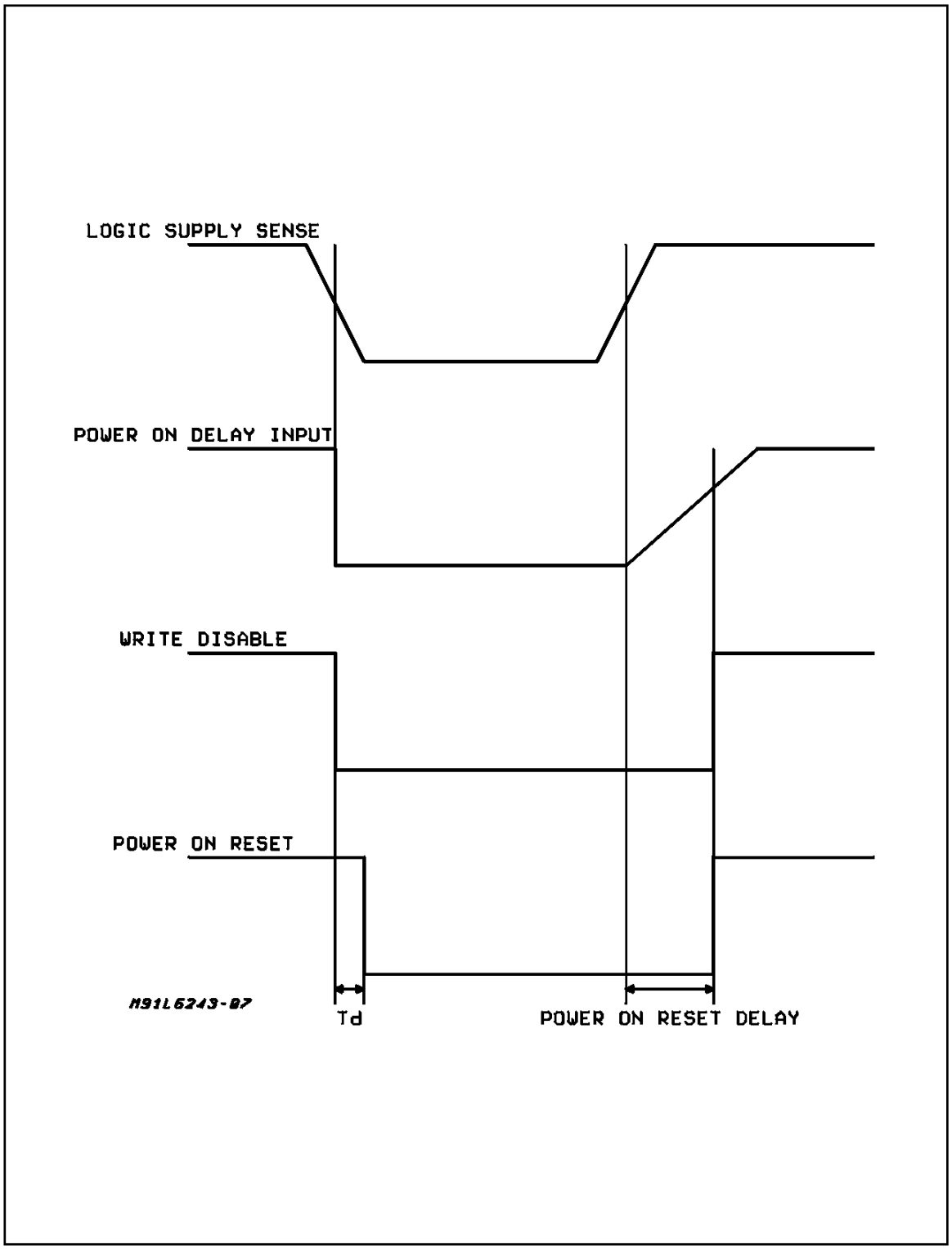


Figure 2: Waveforms



THERMAL CHARACTERISTICS

Figure 3: $R_{th\ (j\text{-}amb)}$ vs. Dissipated Power

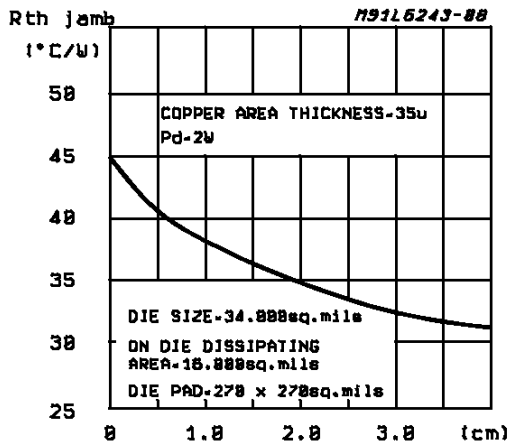
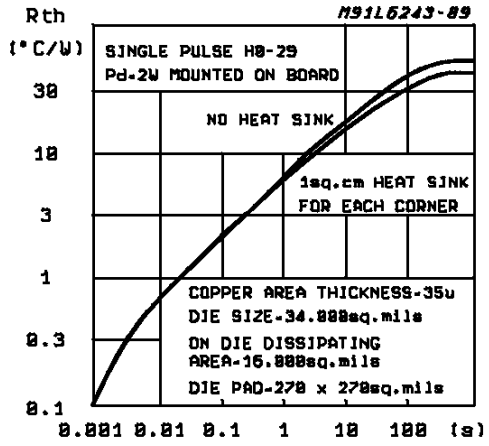
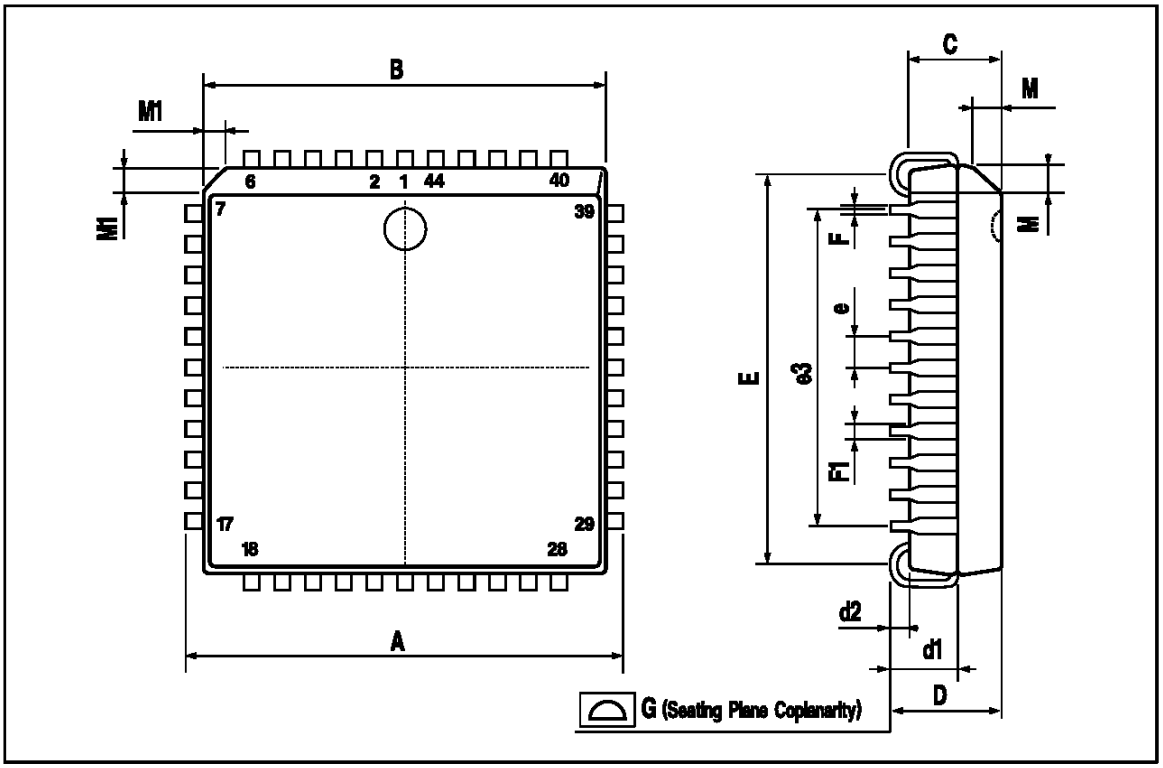


Figure 4: $R_{th\ (j\text{-}amb)}$ vs. Dissipated Power



PLCC44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	



SO28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)