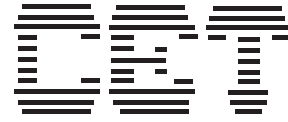


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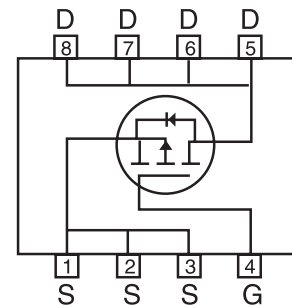
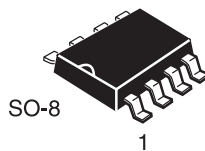
AUGUST 1999

P-Channel Enhancement Mode Field Effect Transistor

5

FEATURES

- -20V , -5.4A , $R_{DS(ON)}=65m\Omega$ @ $V_{GS}=-4.5V$.
 $R_{DS(ON)}=100m\Omega$ @ $V_{GS}=-2.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Surface Mount Package.



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous ^a @ $T_J=125^\circ\text{C}$ -Pulsed ^b	I_D	± 5.4	A
	I_{DM}	± 20	A
Drain-Source Diode Forward Current ^a	I_S	-2.6	A
Maximum Power Dissipation ^a	P_D	2.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ\text{C/W}$
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ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-16V, V _{GS} =0V			-1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±12V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS^b						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-0.6			V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-5.2A		45	65	mΩ
		V _{GS} =-2.5V, I _D =-4.5A		90	100	mΩ
On-State Drain Current	I _{D(ON)}	V _{DS} =-5V, V _{GS} =-4.5V	-20			A
Forward Transconductance	g _{FS}	V _{DS} =-9V, I _D =-5.1A		15		S
DYNAMIC CHARACTERISTICS^c						
Input Capacitance	C _{ISS}	V _{DS} =-10V, V _{GS} =0V f=1.0MHz		1530	1800	pF
Output Capacitance	C _{OSS}			480	1000	pF
Reverse Transfer Capacitance	C _{RSS}			130	500	pF
SWITCHING CHARACTERISTICS^c						
Turn-On Delay Time	t _{D(ON)}	V _D =-6V, I _D =-1A, V _{GEN} =-4.5V, R _{GEN} =6Ω		45	60	ns
Rise Time	t _r			75	100	ns
Turn-Off Delay Time	t _{D(OFF)}			135	180	ns
Fall Time	t _f			70	100	ns
Total Gate Charge	Q _g	V _{DS} =-6V, I _D =-5.1A, V _{GS} =-4.5V		19	60	nC
Gate-Source Charge	Q _{gs}			3		nC
Gate-Drain Charge	Q _{gd}			3.5		nC

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ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS^b						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = -2.6A$		-0.9	-1.2	V

Notes

- a. Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.
- b. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
- c. Guaranteed by design, not subject to production testing.

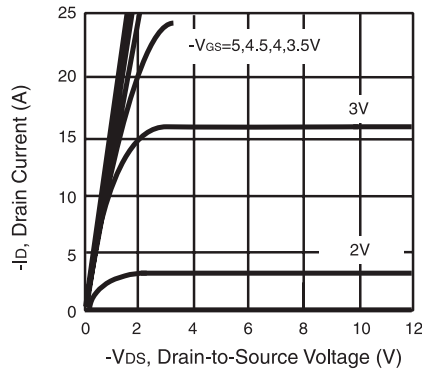


Figure 1. Output Characteristics

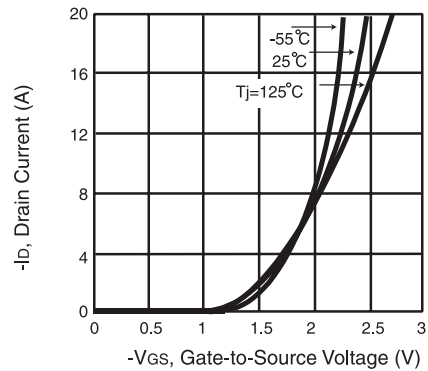


Figure 2. Transfer Characteristics

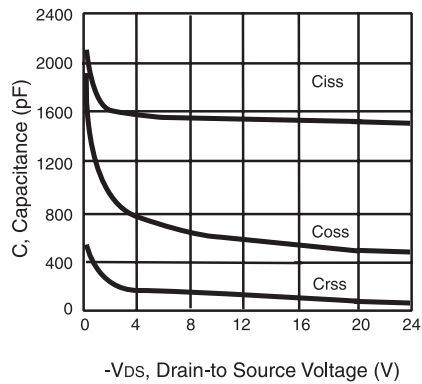


Figure 3. Capacitance

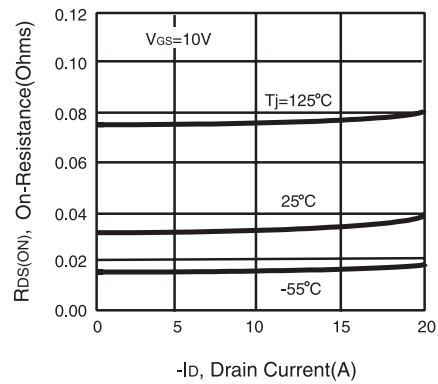


Figure 4. On-Resistance Variation with Drain Current and Temperature

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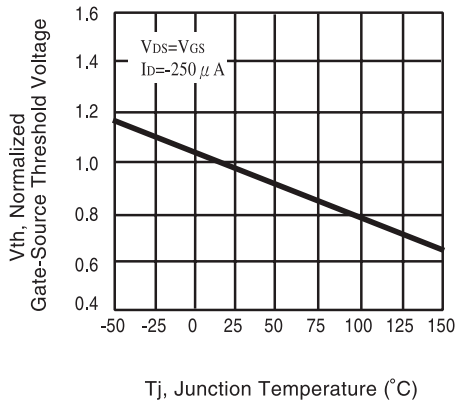


Figure 5. Gate Threshold Variation with Temperature

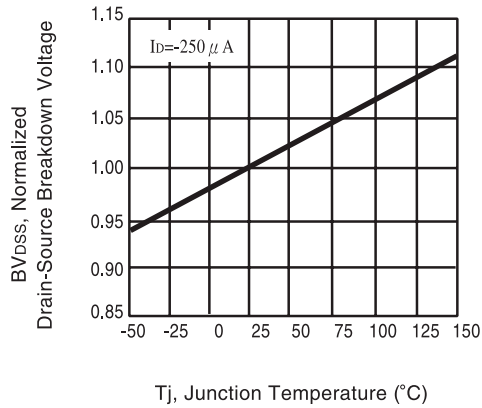


Figure 6. Breakdown Voltage Variation with Temperature

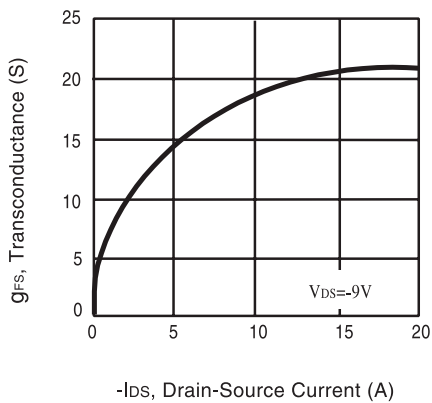


Figure 7. Transconductance Variation with Drain Current

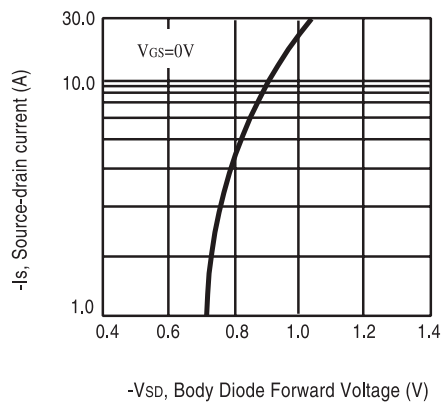


Figure 8. Body Diode Forward Voltage Variation with Source Current

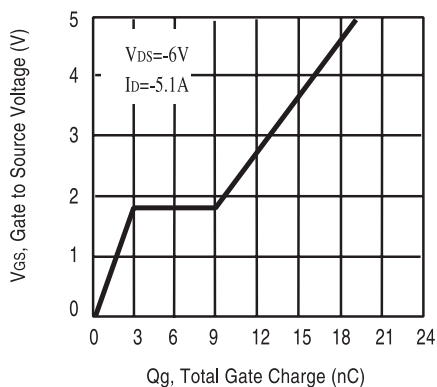


Figure 9. Gate Charge

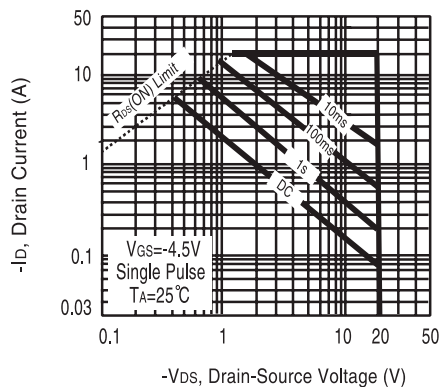


Figure 10. Maximum Safe Operating Area

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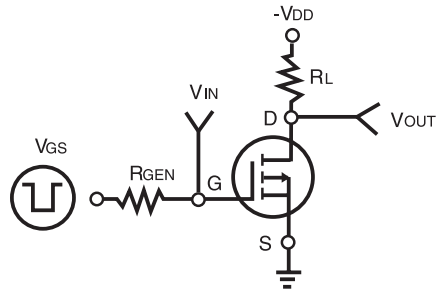


Figure 11. Switching Test Circuit

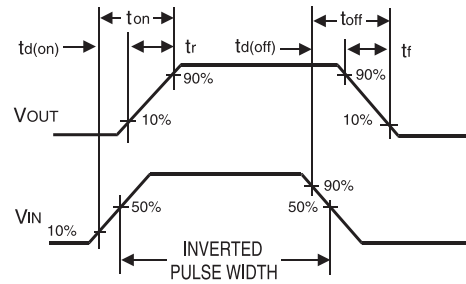


Figure 12. Switching Waveforms

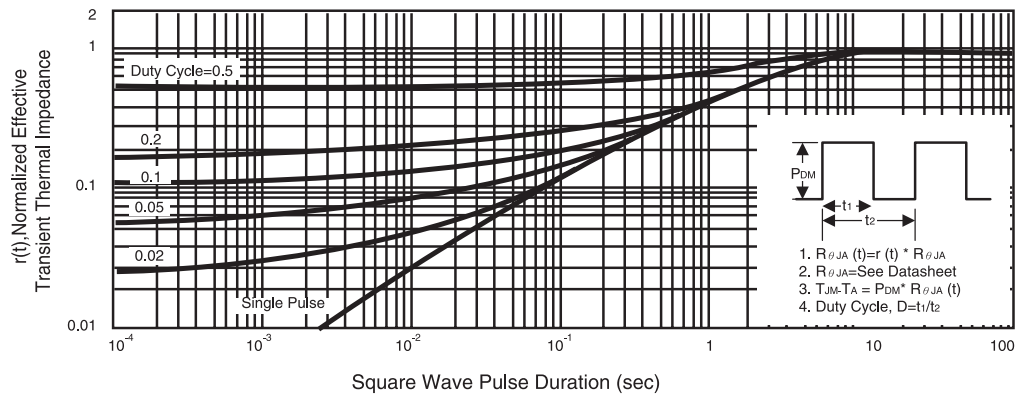


Figure 13. Normalized Thermal Transient Impedance Curve