

74ABT244

Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The ABT244 is an octal buffer and line driver with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

Features

- Non-inverting buffers
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

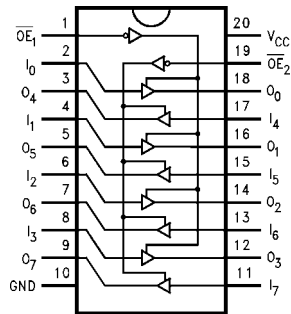
Ordering Code:

Order Number	Package Number	Package Description
74ABT244CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ABT244CSJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT244CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ABT244CMSAX_NL (Note 1)	MSA20	Pb-Free 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ABT244CMTc	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ABT244CMTcX_NL (Note 1)	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ABT244CPC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active LOW)
I_0-I_7	Inputs
O_0-O_7	Outputs

Truth Table

\overline{OE}_1	I_{0-3}	O_{0-3}	\overline{OE}_2	I_{4-7}	O_{4-7}
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Absolute Maximum Ratings(Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.5			V	Min	I _{OH} = -3 mA
		2.0			V	Min	I _{OH} = -32 mA
V _{OL}	Output LOW Voltage			0.55			I _{OL} = 64 mA
I _{IH}	Input HIGH Current			1	μA	Max	V _{IN} = 2.7V (Note 5)
				1			V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-1	μA	Max	V _{IN} = 0.5V (Note 5)
				-1			V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current			10	μA	0 - 5.5V	V _{OUT} = 2.7V; \overline{OE}_n = 2.0V
I _{OZL}	Output Leakage Current			-10	μA	0 - 5.5V	V _{OUT} = 0.5V; \overline{OE}_n = 2.0V
I _{OS}	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			50	μA	Max	\overline{OE}_n = V _{CC} , All Others at V _{CC} or Ground
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled		2.5	mA		V _I = V _{CC} - 2.1V
		Outputs 3-STATE		2.5	mA	Max	Enable Input V _I = V _{CC} - 2.1V
		Outputs 3-STATE		50	μA		Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or Ground
I _{CCD}	Dynamic I _{CC} (Note 5)	No Load		0.1	mA/ MHz	Max	Outputs OPEN \overline{OE}_n = GND, (Note 4) One Bit Toggling, 50% Duty Cycle

Note 4: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 5: Guaranteed, but not tested.

DC Electrical Characteristics

(SOIC package)

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		0.5	0.8	V	5.0	T _A = 25°C (Note 6)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-1.3	-0.8		V	5.0	T _A = 25°C (Note 6)
V _{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.7	3.1		V	5.0	T _A = 25°C (Note 8)
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.0	1.5		V	5.0	T _A = 25°C (Note 7)
V _{ILD}	Maximum LOW Level Dynamic Input Voltage		1.1	0.8	V	5.0	T _A = 25°C (Note 7)

Note 6: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 7: Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 8: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics

(SOIC and SSOP package)

Symbol	Parameter	T _A = +25°C V _{CC} = +5V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 4.5V–5.5V C _L = 50 pF		T _A = -40°C to +85°C V _{CC} = 4.5V–5.5V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	1.0	2.5	3.6	1.0	5.3	1.0	3.6	ns
t _{PHL}	Data to Outputs	1.0	2.3	3.6	1.0	5.0	1.0	3.6	
t _{PZH}	Output Enable	1.5	3.5	6.0	0.8	6.5	1.5	6.0	ns
t _{PZL}	Time	1.5	3.6	6.0	1.2	7.9	1.5	6.0	
t _{PHZ}	Output Disable	1.7	3.5	5.6	1.2	7.6	1.7	5.6	ns
t _{PLZ}	Time	1.7	3.3	5.6	1.0	7.9	1.7	5.6	

Extended AC Electrical Characteristics

(SOIC package)

Symbol	Parameter	T _A = -40°C to +85°C V _{CC} = 4.5V–5.5V C _L = 50 pF 8 Outputs Switching (Note 9)			T _A = -40°C to +85°C V _{CC} = 4.5V–5.5V C _L = 250 pF 1 Output Switching (Note 10)		T _A = -40°C to +85°C V _{CC} = 4.5V–5.5V C _L = 250 pF 8 Outputs Switching (Note 11)		Units
		Min	Typ	Max	Min	Max	Min	Max	
f _{TOGGLE}	Max Toggle Frequency		100						MHz
t _{PLH}	Propagation Delay	1.5		5.0	1.5	6.0	2.5	8.5	ns
t _{PHL}	Data to Outputs	1.5		5.0	1.5	6.0	2.5	8.5	
t _{PZH}	Output Enable Time	1.5		6.5	2.5	7.5	2.5	10.0	ns
t _{PZL}	Time	1.5		6.5	2.5	7.5	2.5	12.0	
t _{PHZ}	Output Disable Time	1.0		5.6	(Note 12)		(Note 12)		ns
t _{PLZ}	Time	1.0		5.6	(Note 12)		(Note 12)		

Note 9: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

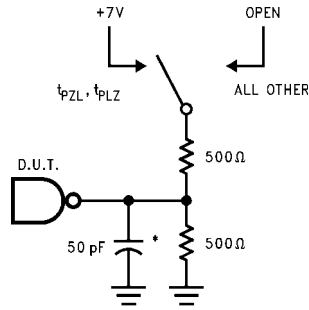
Note 10: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 11: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 12: The 3-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

Skew				
Symbol	Parameter	$T_A = -40^\circ\text{C to }+85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 15)	$T_A = -40^\circ\text{C to }+85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 16)	Units
		Max	Max	
t_{OSHL} (Note 13)	Pin to Pin Skew HL Transitions	0.8	1.8	ns
t_{OSLH} (Note 13)	Pin to Pin Skew LH Transitions	0.8	1.8	ns
t_{PS} (Note 17)	Duty Cycle LH-HL Skew	1.0	2.5	ns
t_{OST} (Note 13)	Pin to Pin Skew LH/HL Transitions	1.0	2.5	ns
t_{PV} (Note 14)	Device to Device Skew LH/HL Transitions	1.5	3.0	ns
<p>Note 13: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). The specification is guaranteed but not tested.</p> <p>Note 14: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.</p> <p>Note 15: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)</p> <p>Note 16: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p>Note 17: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.</p>				
Capacitance				
Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 18)	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$
<p>Note 18: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883, Method 3012.</p>				

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

AC Waveforms

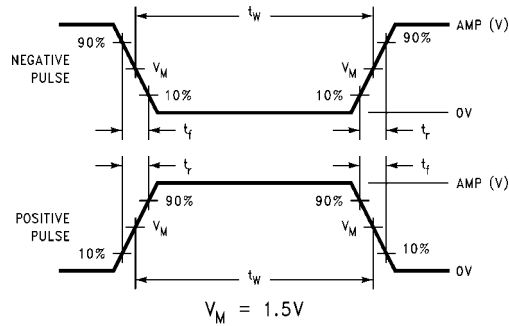


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

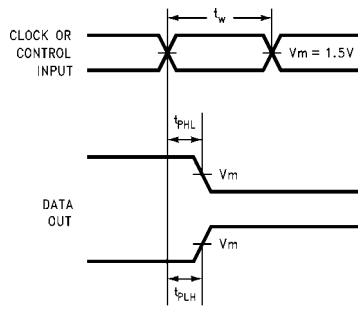


FIGURE 4. Propagation Delay, Pulse Width Waveforms

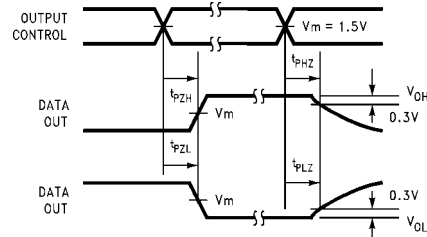


FIGURE 5. 3-STATE Output HIGH and LOW Enable and Disable Times

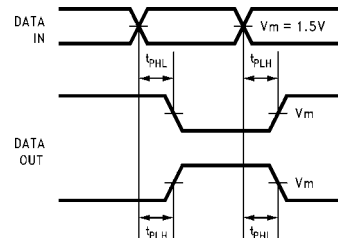


FIGURE 6. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

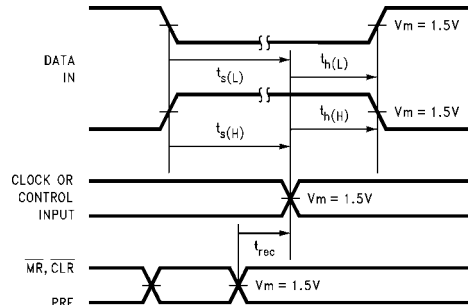
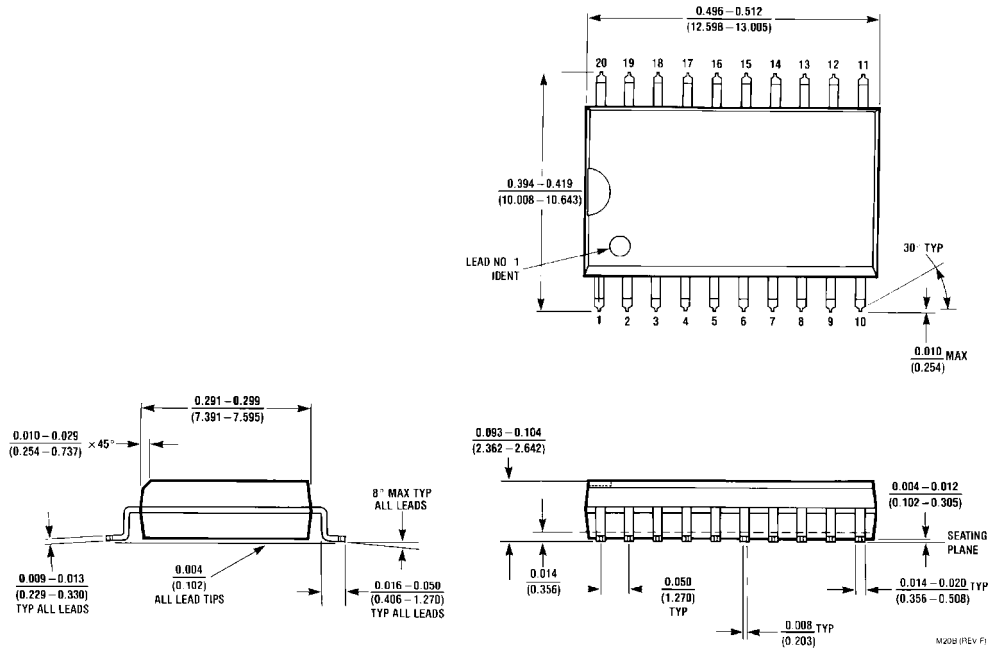


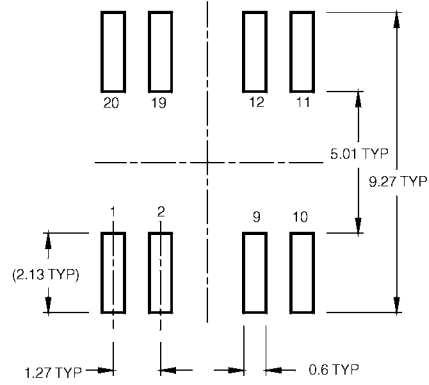
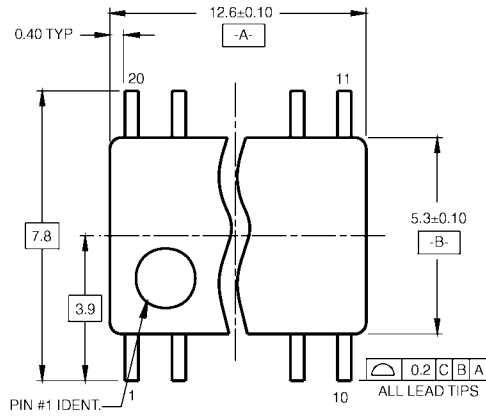
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

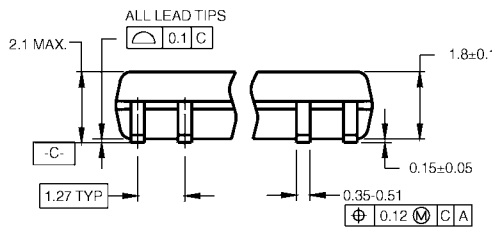


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

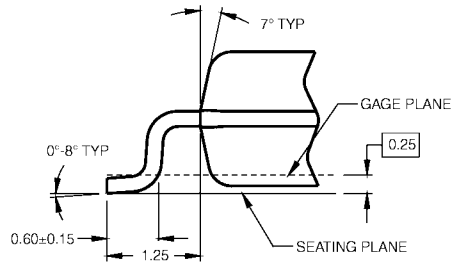
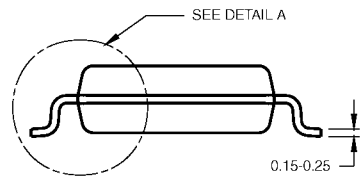
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

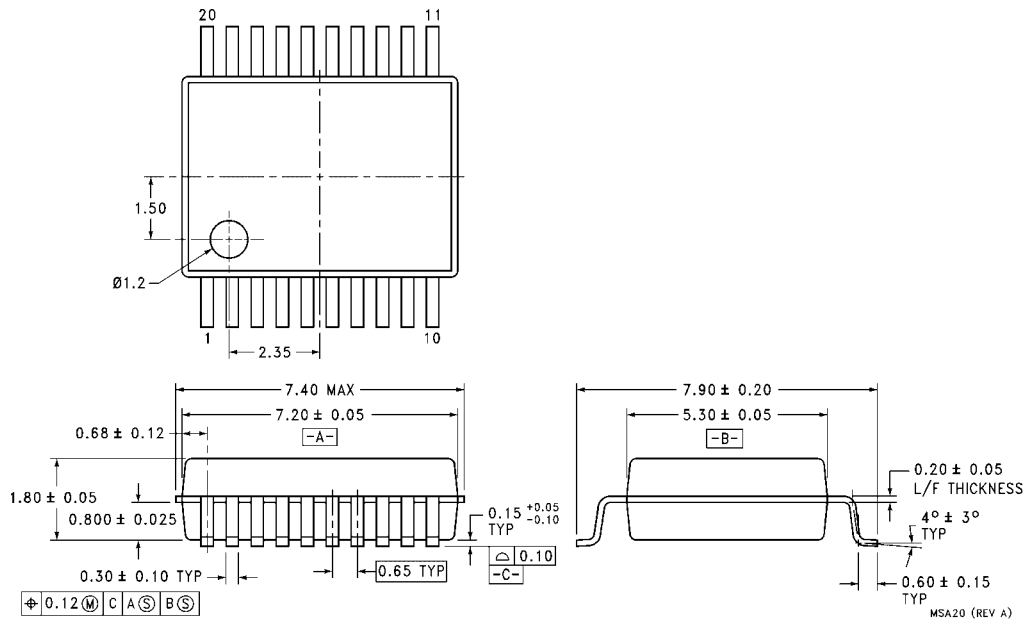
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

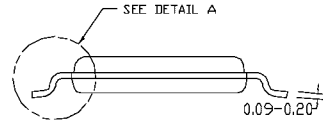
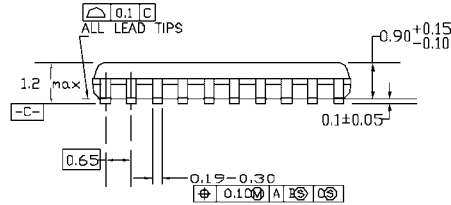
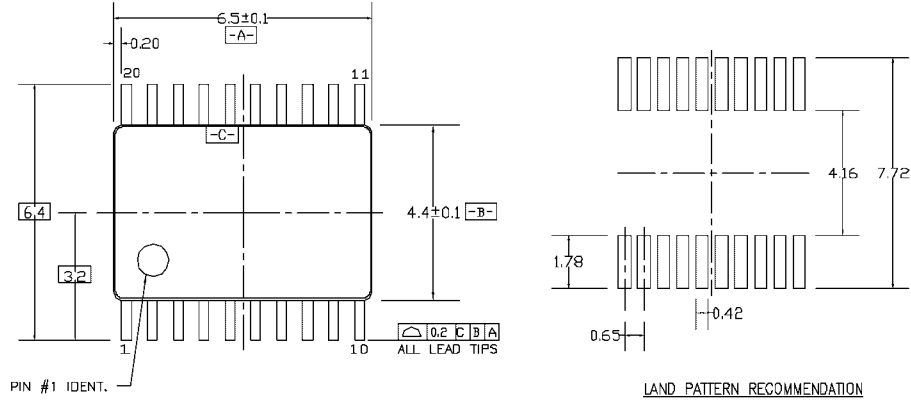
Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

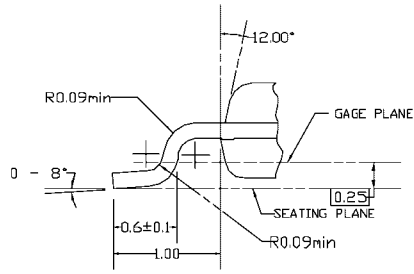


**20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
 Package Number MSA20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

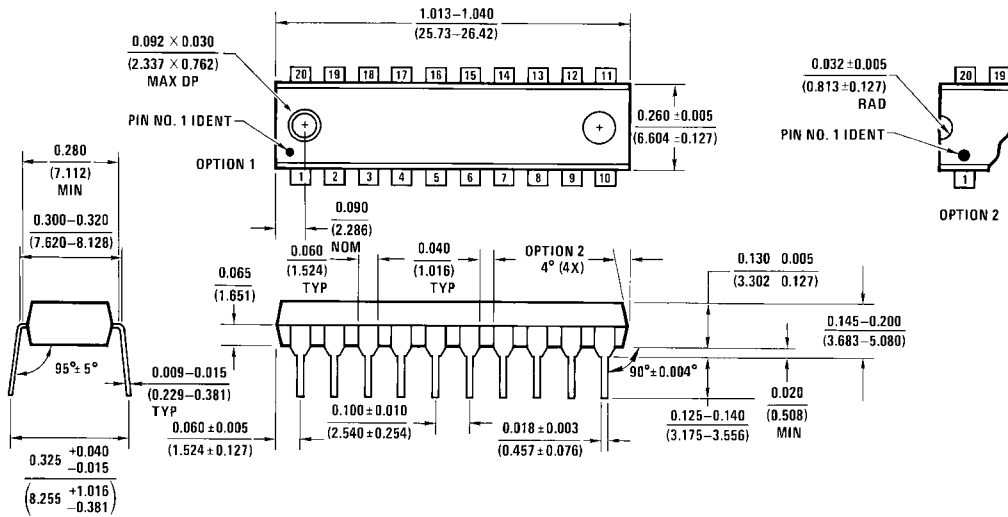
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com