

MN6577F, MN6577H

Low Power 10-Bit 3-Volt CMOS A/D Converters for Image Processing

Overview

The MN6577F and MN6577H are high-speed 10-bit CMOS analog-to-digital converters for image processing applications.

They use a half flash structure based on chopper comparators to achieve both high speed and low power consumption, and operate on a single 3 volt power supply.

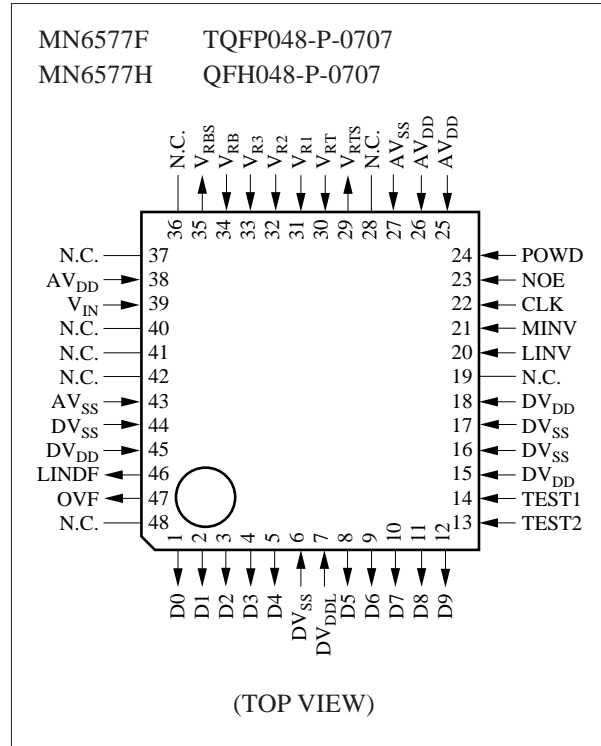
Features

- Maximum conversion rate: 15 MSPS (min.)
- Linearity error: ± 1.3 LSB (typ.)
- Differential linearity error: ± 0.5 LSB (typ.)
- Power supply voltage: 3.0 V
- Power consumption: 40 mW (typ.) ($f_{CLK}=15$ MHz)

Applications

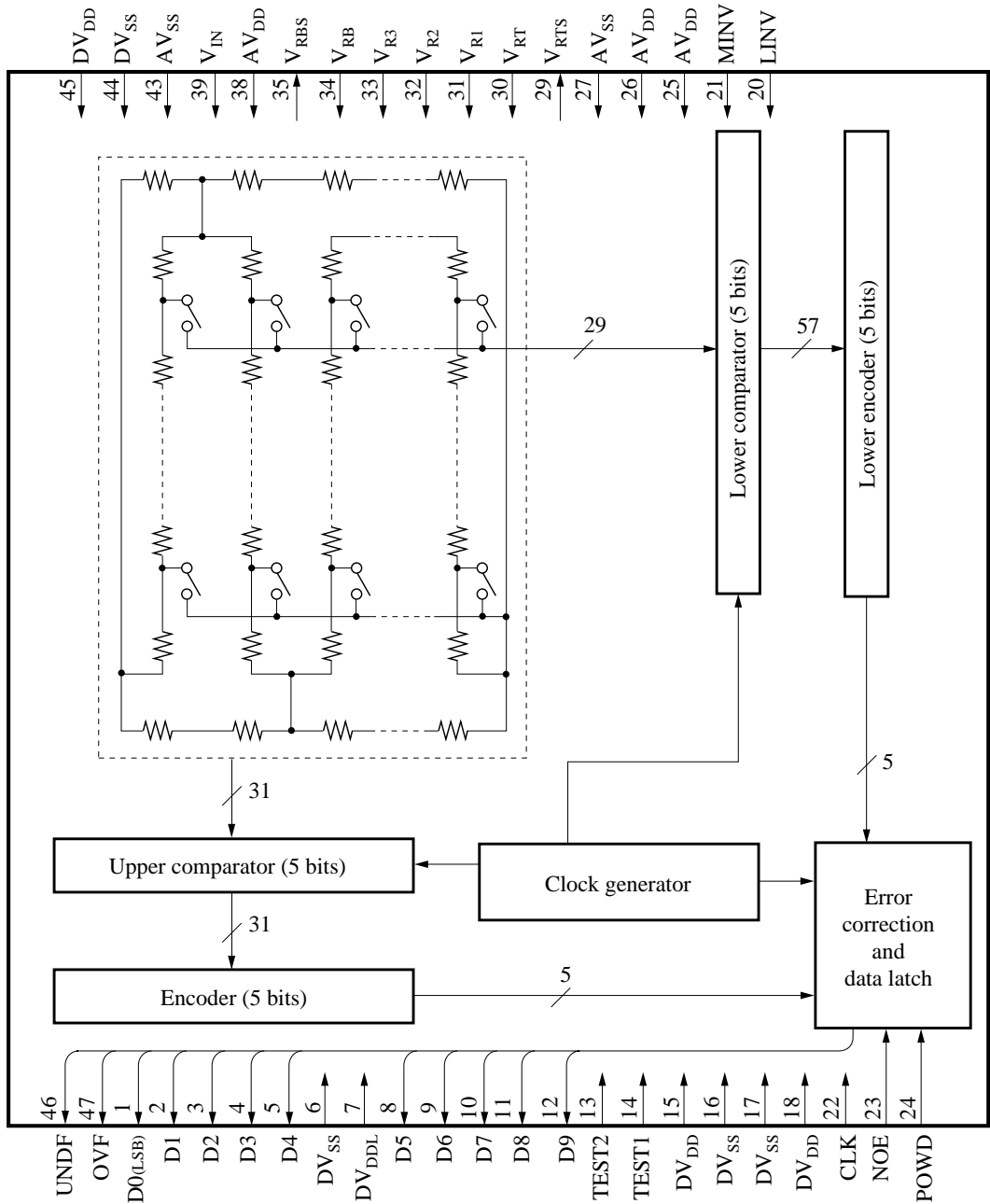
- Digital television
- Digital video equipment
- Digital image processing equipment

Pin Assignment



■ Block Diagram

(Pins 19, 28, 36, 37, 40, 41, 42, and 48 are no connection pins.)



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	D0	Digital code output (LSB)
2	D1	Digital code output
3	D2	Digital code output
4	D3	Digital code output
5	D4	Digital code output
6	DV _{SS}	Ground for digital circuits
7	DV _{DD}	Power supply for digital circuits
8	D5	Digital code output
9	D6	Digital code output
10	D7	Digital code output
11	D8	Digital code output
12	D9	Digital code output (MSB)
13	TEST2	Test mode selection pin
14	TEST1	Test mode selection pin
15	DV _{DD}	Power supply for digital circuits
16	DV _{SS}	Ground for digital circuits
17	DV _{SS}	Ground for digital circuits
18	DV _{DD}	Power supply for digital circuits
19	N.C.	No connection
20	LINV	Output inversion pin
21	MINV	Output inversion pin
22	CLK	Sampling clock
23	NOE	Digital output enable pin
24	POWD	Power down mode selection pin
25	AV _{DD}	Power supply for analog circuits
26	AV _{DD}	Power supply for analog circuits
27	AV _{SS}	Ground for analog circuits
28	N.C.	No connection
29	V _{RTS}	Reference voltage power supply (TOP)
30	V _{RT}	Reference voltage input (TOP)
31	V _{R1}	Intermediate reference voltage
32	V _{R2}	Intermediate reference voltage
33	V _{R3}	Intermediate reference voltage
34	V _{RB}	Reference voltage input (BOTTOM)
35	V _{RBS}	Reference voltage power supply (BOTTOM)
36	N.C.	No connection
37	N.C.	No connection
38	AV _{DD}	Power supply for analog circuits
39	V _{IN}	Analog signal input
40	N.C.	No connection

■ Pin Description (continued)

Pin No.	Symbol	Function Description
41	N.C.	No connection
42	N.C.	No connection
43	AV _{SS}	Ground for analog circuits
44	DV _{SS}	Ground for digital circuits
45	DV _{DD}	Power supply for digital circuits
46	UNDF	Underflow output
47	OVF	Overflow output
48	N.C.	No connection

■ Absolute Maximum Ratings $T_a=25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Power supply voltage	V _{DD}	- 0.3 to +7.0	V
Input voltage	V _I	- 0.3 to V _{DD} +0.3	V
Output voltage	V _O	- 0.3 to V _{DD} +0.3	V
Operating ambient temperature	T _{opr}	-20 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C

■ Recommended Operating Conditions $V_{DD}=AV_{DD}=DV_{DD}=3.0\text{V}$, $V_{SS}=AV_{SS}=DV_{SS}=0\text{V}$, $T_a=25^\circ\text{C}$

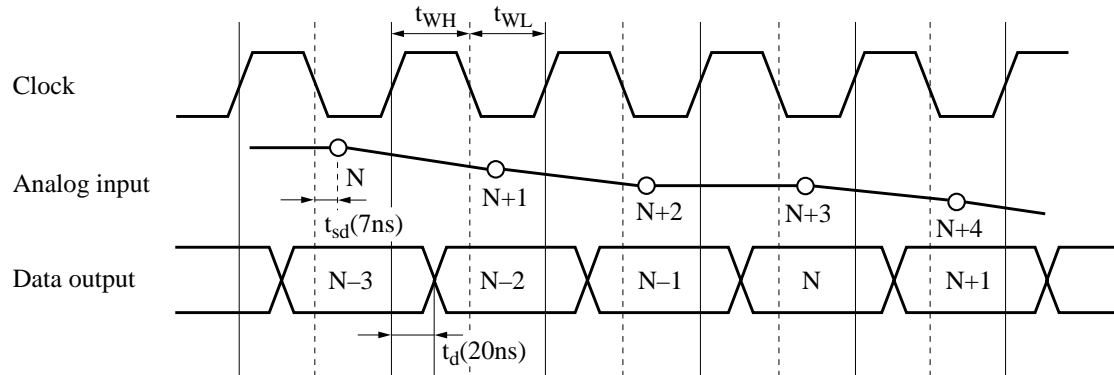
Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V _{DD}	2.85	3.00	3.30	V
Digital input voltage	"H" level	V _{IH}	2.4	V _{DD}	V
	"L" level	V _{IL}	V _{SS}	0.8	V
Reference voltage	"H" level	V _{RT}	2.0	V _{DD}	V
	"L" level	V _{RB}	V _{SS}	1.0	V
Clock	"H" level pulse width	t _{WH}	30		ns
	"L" level pulse width	t _{WL}	30		ns
Analog input voltage	V _{AIN}	V _{SS}		V _{DD}	V

■ Electrical Characteristics $V_{DD}=AV_{DD}=DV_{DD}=3.0\text{V}$, $AV_{SS}=DV_{SS}=0\text{V}$, $T_a=25^\circ\text{C}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Power consumption	P _C	F _C =15MSPS (not including reference current)		39	72	mW
Resolution	RES			10		bit
Linearity error	E _L	f _{CLK} =15MSPS		±1.3	±2.5	LSB
Differential linearity error	E _D	V _{RT} =3.0V V _{BB} =1.0V		±0.5	±1.0	LSB
Maximum conversion rate	F _{C(max.)}		15			MSPS
Clock frequency	f _{CLK}		1		15	MHz
Analog input dynamic range	D _R		2		V _{RT} - V _{RB}	V
Output current	"H" level	I _{OH}	V _{OH} =V _{DD} -0.8V		-1.5	mA
	"L" level	I _{OL}	V _{OL} =0.4V	1.5		mA
Output delay time	t _d	C _L =20pF	10	20	40	ns
Analog input capacitance	C _I			18		pF
Sampling delay	t _{sd}			7		ns

■ Timing Chart

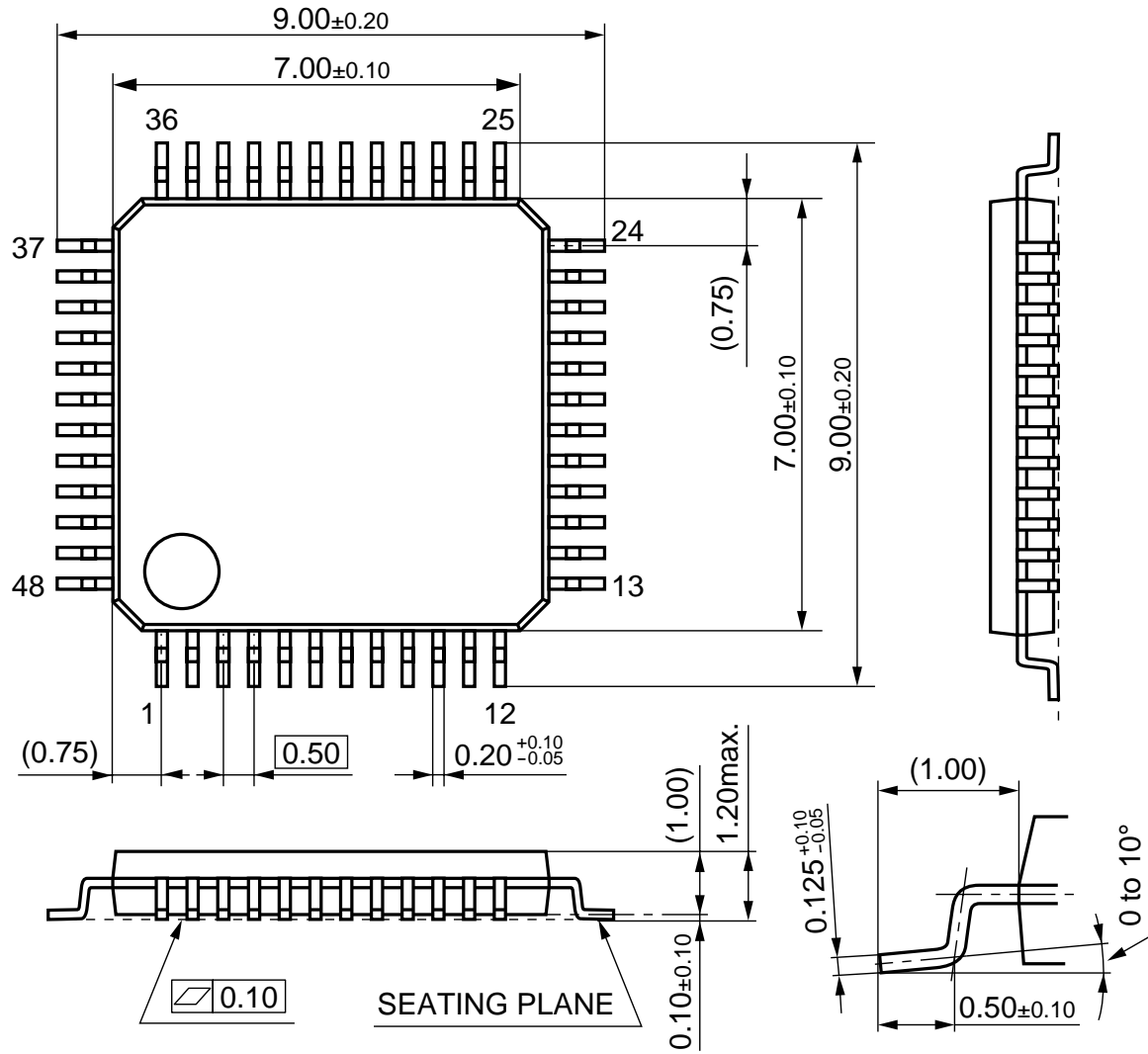
The chip samples the analog input at the falling edge of the clock signal and provides the corresponding digital output 2.5 clock cycles later at the rising edge of the clock signal.



Note: The circles indicate analog signal sampling points.

■ Package Dimensions (Unit:mm)

- MN6577F TQFP048-P-0707



■ Package Dimensions (Unit:mm)(continued)

● MN6577H QFH048-P-0707

