



EMIF02-MIC02F2

IPAD™

2 LINES EMI FILTER INCLUDING ESD PROTECTION

MAIN PRODUCT CHARACTERISTICS:

Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers, printers and MCU Boards

DESCRIPTION

The EMIF02-MIC02 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF02 flip chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.

BENEFITS

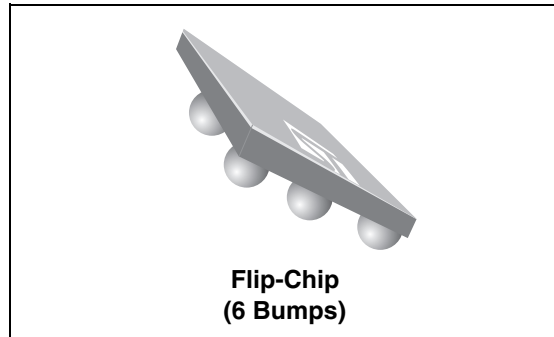
- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead free package
- Very low PCB space consuming: 1.07mm x 1.57mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2

Level 4 on input pins 15kV (air discharge)
8kV (contact discharge)

Level 1 on output pins 2kV (air discharge)
2kV (contact discharge)



Flip-Chip
(6 Bumps)

Table 1: Order Code

Part Number	Marking
EMIF02-MIC02F2	FJ

Figure 1: Pin Configuration (Ball side)

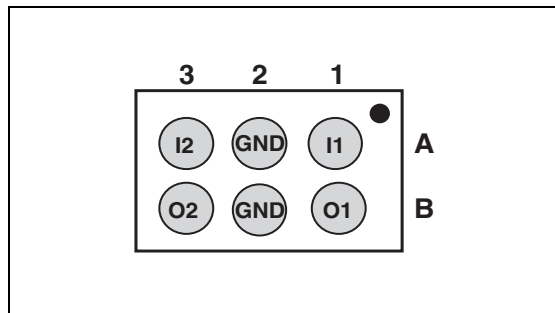
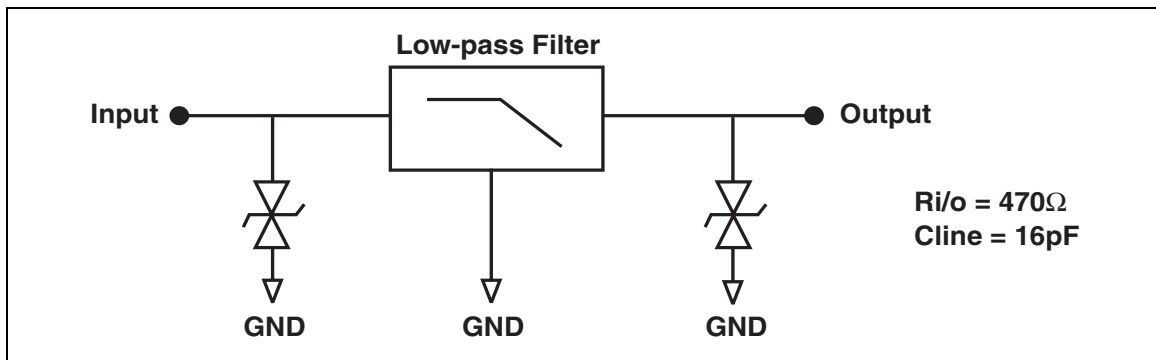


Figure 2: Basic Cell Configuration



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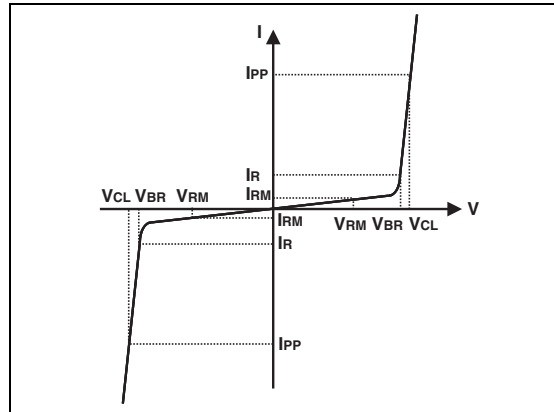
EMIF02-MIC02F2

Table 2: Absolute Ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 3: Electrical Characteristics ($T_{amb} = 25^\circ\text{C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1 \text{ mA}$	14	16		V
I_{RM}	$V_{RM} = 12\text{V}$ per line			500	nA
$R_{I/O}$		423	470	517	Ω
C_{line}	@ 0V		16		pF

Figure 3: S21 (dB) attenuation measurement and Aplac simulation

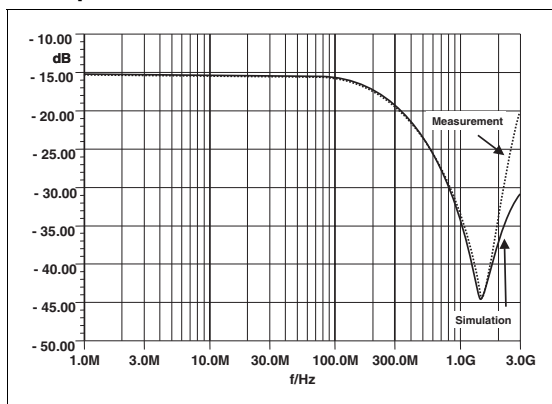


Figure 4: Analog crosstalk measurements

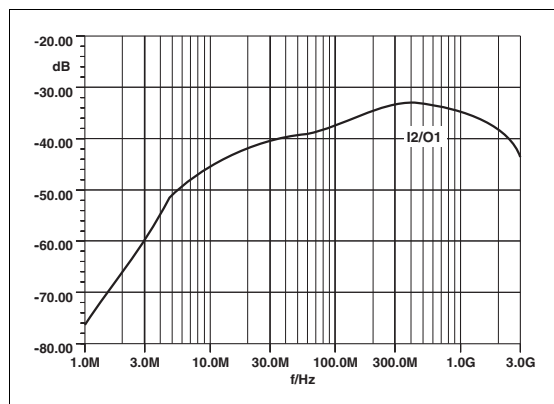


Figure 5: Digital crosstalk measurement

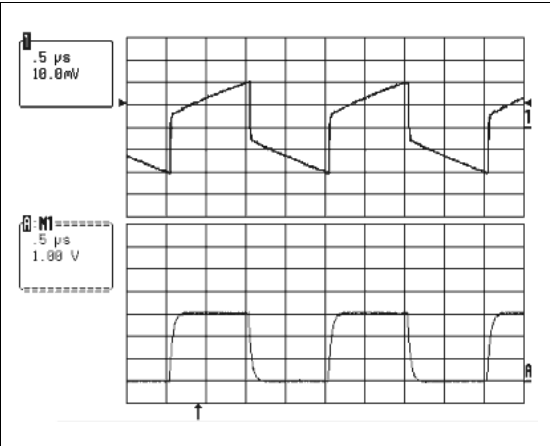


Figure 6: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout)

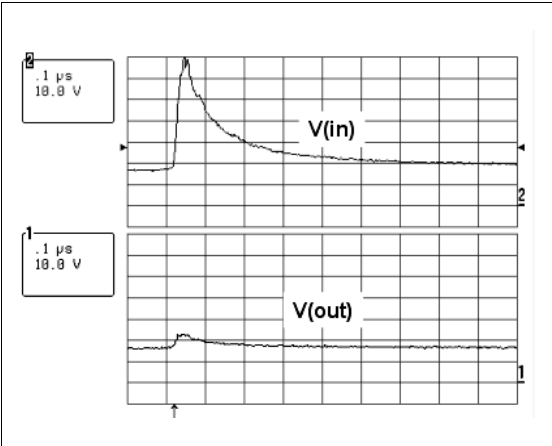


Figure 7: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout)

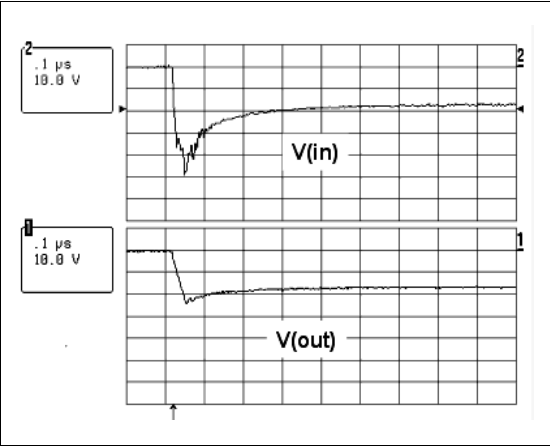


Figure 8: Line capacitance versus applied voltage

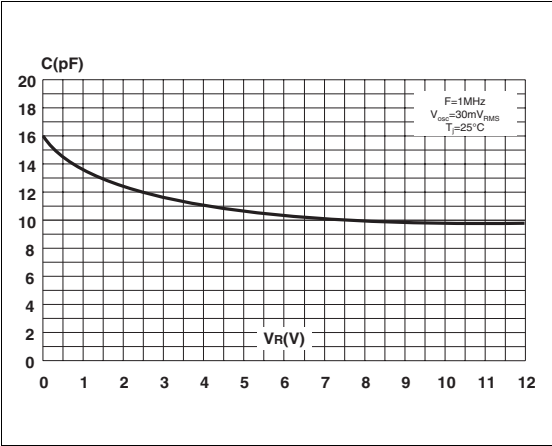


Figure 9: Aplac model

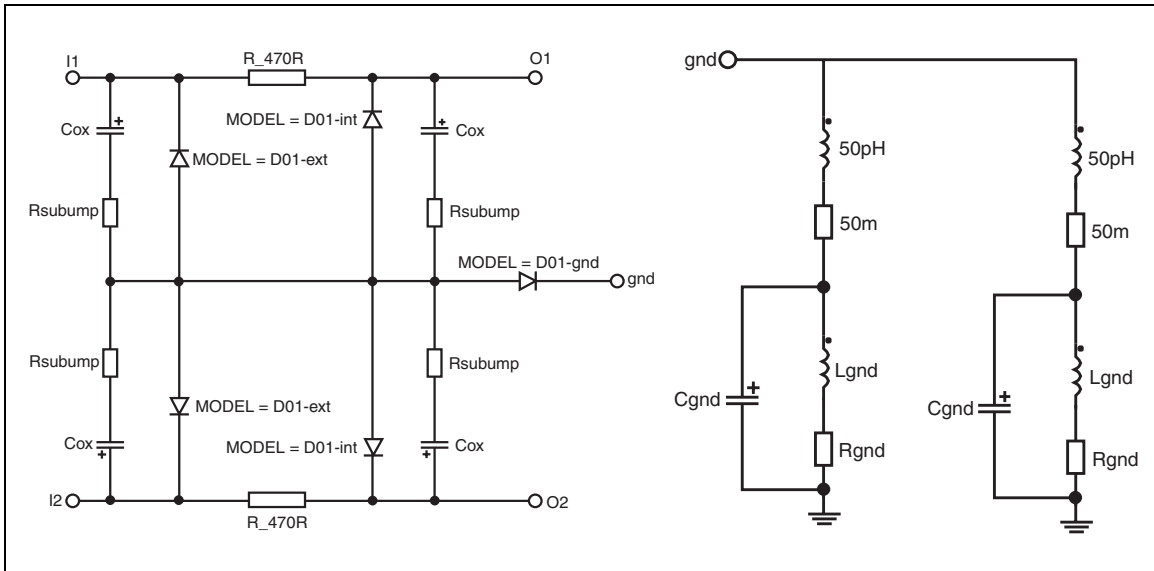


Figure 10: Aplac parameters

Model D01-ext	Model D01-int	Model D01-gnd	Ls 400pH
BV = 7	BV = 7	BV = 7	Rs 100m
CJO = Cz_ext	CJO = Cz_int	CJO = Cz_gnd	R_470R 482.6
IBV = 1u	IBV = 1u	IBV = 1u	Cz_ext 8.73pF
IKF = 1000	IKF = 1000	IKF = 1000	Rs_ext 850m
IS = 10f	IS = 10f	IS = 10f	Cz_int 2.9pF
ISR = 100p	ISR = 100p	ISR = 100p	Rs_int 850m
N = 1	N = 1	N = 1	Cz_gnd 215.61pF
M = 0.3333	M = 0.3333	M = 0.3333	Rs_gnd 470m
RS = Rs_ext	RS = Rs_int	RS = Rs_gnd	Rgnd 10m
VJ = 0.6	VJ = 0.6	VJ = 0.6	Lgnd 48pH
TT = 50n	TT = 50n	TT = 50n	Cgnd 0.15pF
			Cox 3.05pF
			Rsubump 200m

Figure 11: Ordering Information Scheme

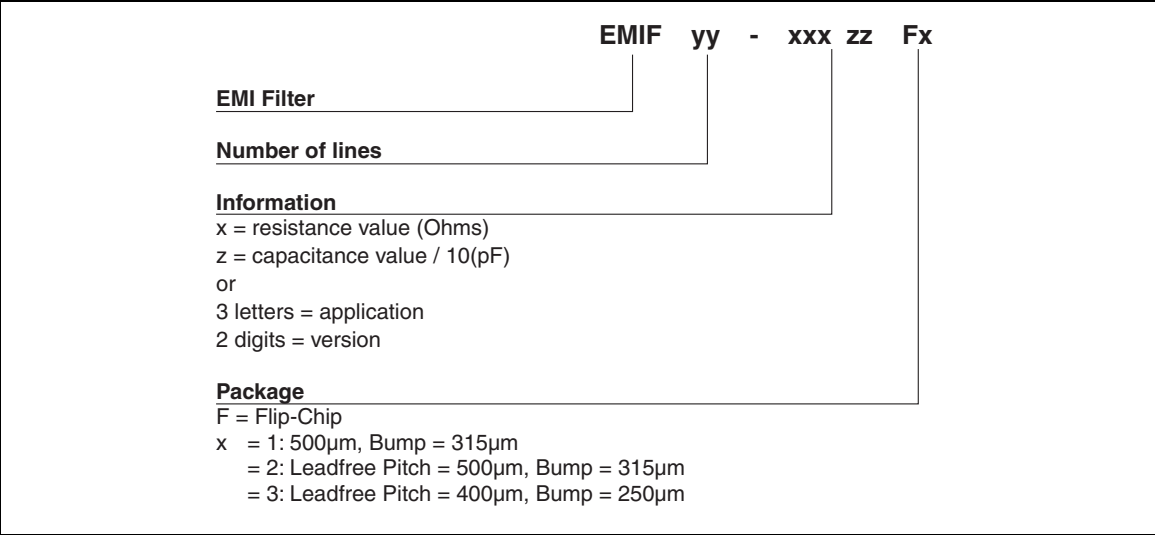


Figure 12: FLIP-CHIP Package Mechanical Data

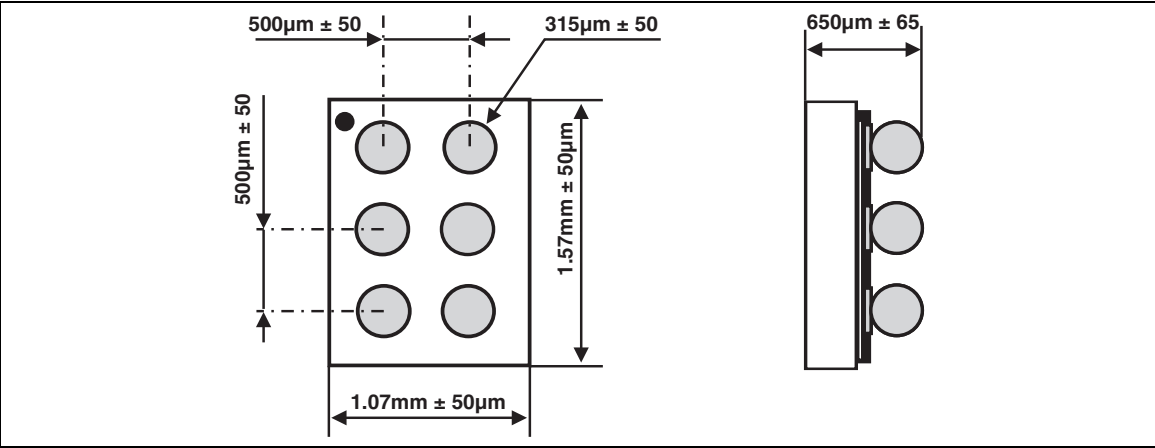


Figure 13: Foot print recommendations

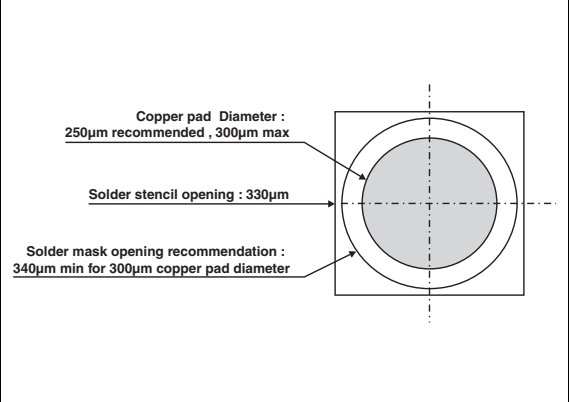


Figure 14: Marking

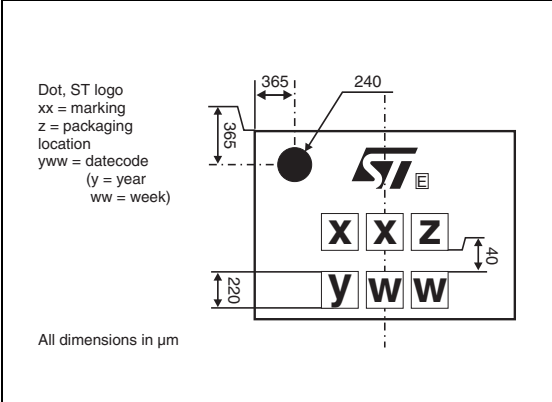


Figure 15: FLIP-CHIP Tape and Reel Specification

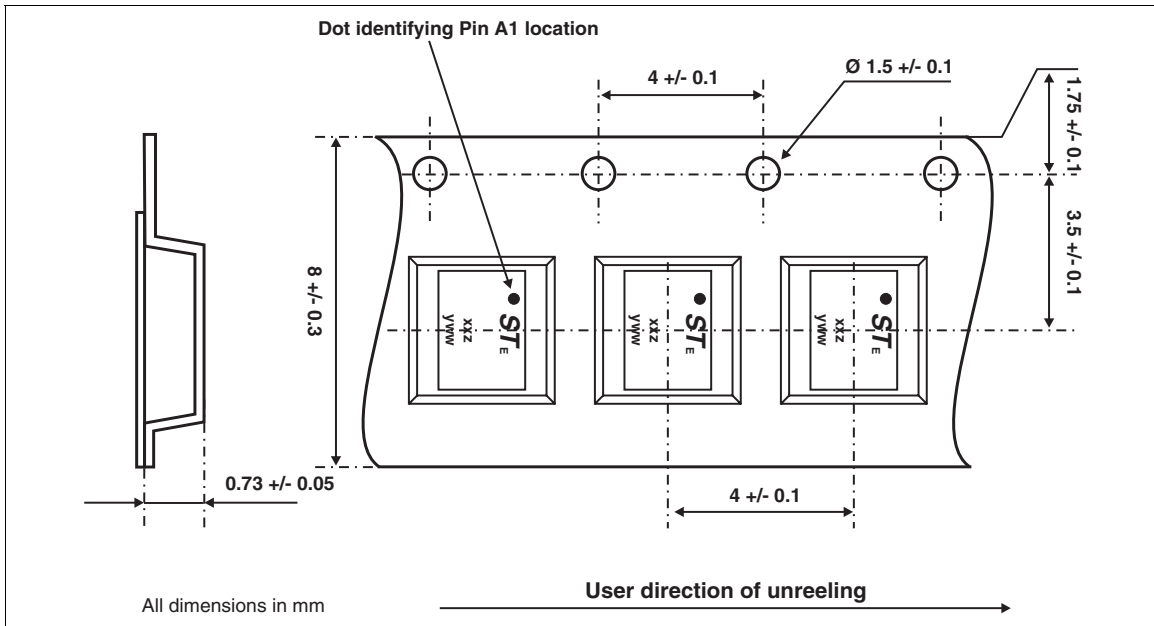


Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-MIC02F2	FJ	Flip-Chip	2.3 mg	5000	Tape & reel 7"

Note: More informations are available in the application notes:
 AN1235: "Flip-Chip: Package description and recommendations for use"
 AN1751: "EMI Filters: Recommendations and measurements"

Table 5: Revision History

Date	Revision	Description of Changes
12-Oct-2004	1	First issue

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