
HD66206

(80-Channel Column/Common Driver for Middle- or Large-sized Liquid Crystal Panel)

HITACHI

Rev 0.2
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Description

The HD66206 is an 80-channel LCD driver, which is used for liquid crystal dot matrix display. This product can drive various types of liquid crystal displays, from small-sized to monochrome VGA-sized displays. Since this product can function as a column and a common driver, an LCD panel can be configured only with this product.

Features

- Logic power supply voltage: 2.7 to 5.5V
- Display duty: 1/16 (1/5 bias) to 1/240
- 80 liquid crystal display drive circuits
- Liquid crystal display drive voltage: 6 to 28V
- Data transfer speed
 - 8 MHz max (at 5-V operation)
 - 6.5 MHz max (at 3-V operation)
- Chip enable signal automatic generation
- Standby function
- Controllers that can be used with
 - HD64645/HD64646 (LCTC series)
 - HD66841 (LVIC series)
- Packages
 - TFP-100B
 - No package (bare chip)
- CMOS process

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Ordering information

Type name	Package
HD66206TE	TFP-100B
HCD66206	Bare chip

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Pin Arrangement

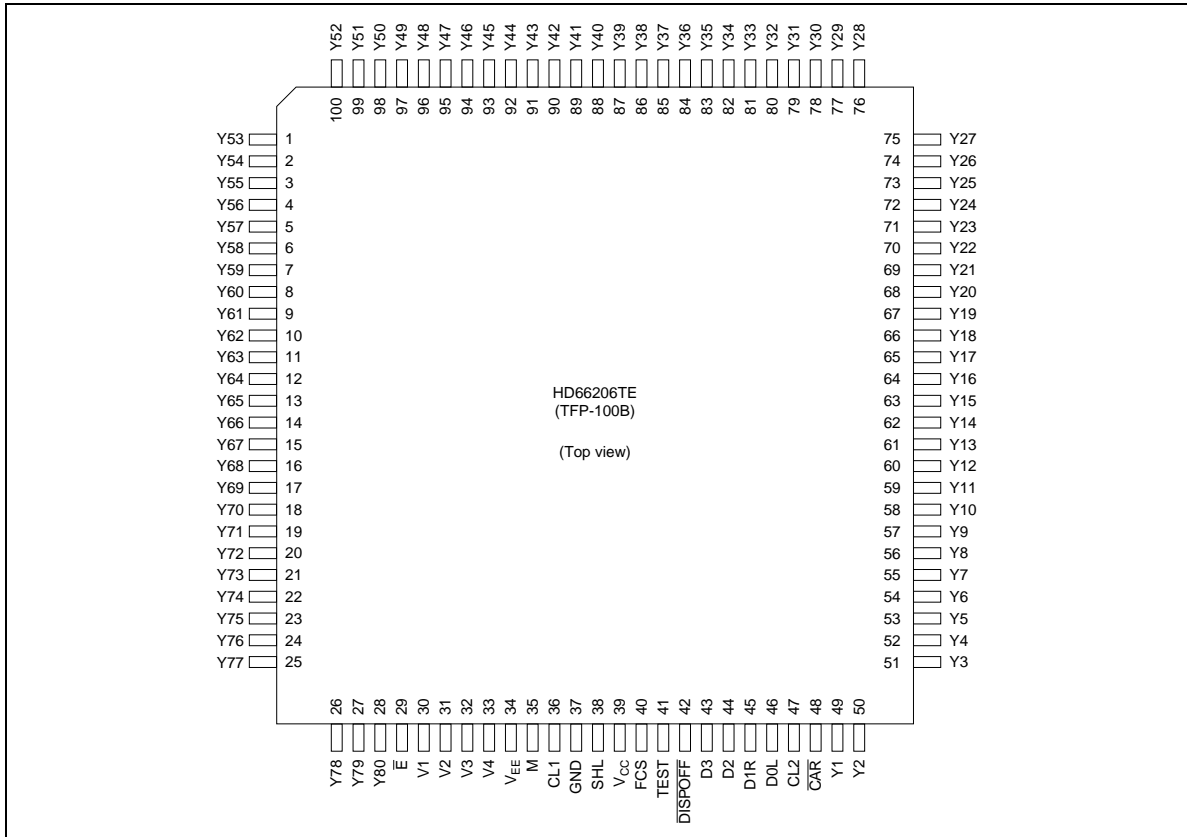


Figure 1 Pin Arrangement (HD66206TE)

Block Diagram

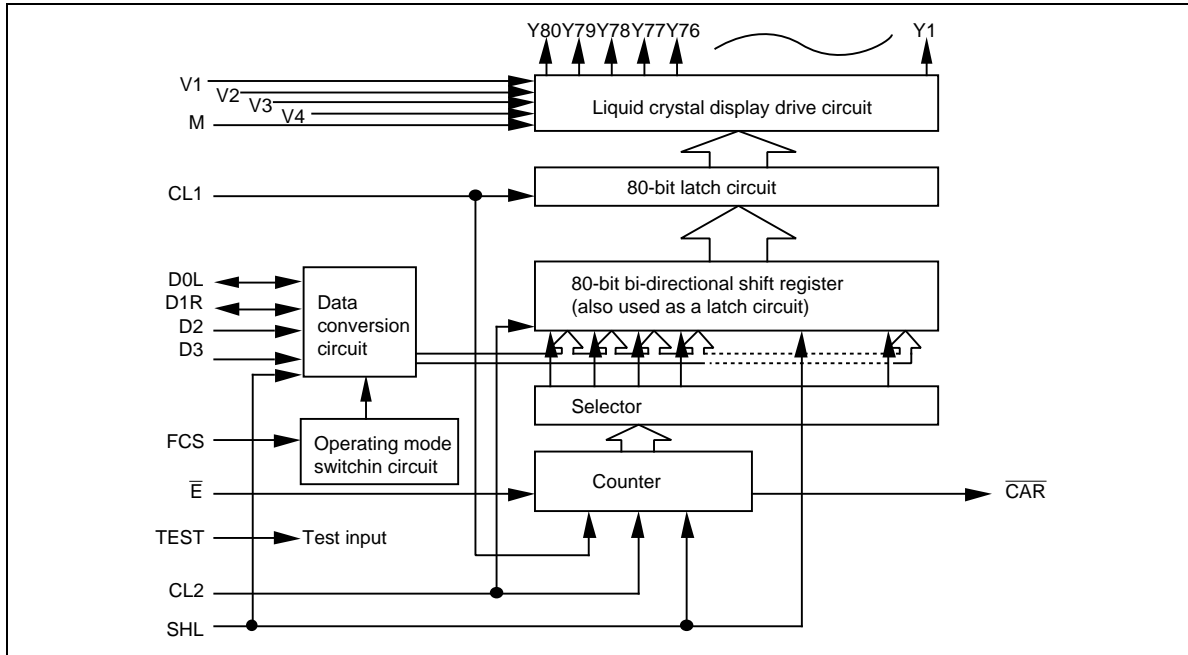


Figure 2 Block Diagram

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Block Functions

Liquid crystal display drive circuit

Generates one of four levels V1 to V4 to the output pin to drive the liquid crystal display according to the combination of data of the 80-bit latch circuit and the M signal.

80-bit latch circuit

Latches data of the 80-bit bi-directional shift register (also used as a latch circuit) at the falling edge of CL1, and transmits it to the liquid crystal display drive circuit.

80-bit bi-directional shift register (also used as a latch circuit)

When FCS is low, this register functions as an 80-bit shift register. At this time, D0L and D1R are used as data input/output pins. When FCS is high, this register functions as a 20×4 -bit unit latch circuit. At this time, data that is input in parallel to data input pin D0L, D1R, D2 and D3 is converted to 4-bit data, and then is latched to this register according to the latch signal generated by the selector.

Data conversion circuit

When FCS is low, D0L and D1R are used as data input/output pins. When FCS is high, D0L, D1R, D2, and D3 are input data.

Selector

Decodes output data from the counter and generates a latch signal. Functions when latching data at serial-latch operation (when FCS is high). At this time, after 80 bits of data Y1 to Y80 are completely latched, the operation of the selector terminates. Even if input data changes, data in the latch circuit is maintained.

Operating mode switching circuit

Switches common driver operation (when FCS is low) and column driver operation (when FCS is high).

Pin Function
Table 1 Pin Functions

Classification	Symbol	Pin No.	Pin Name	Input/ Output	Function
Power supply	V_{CC}	39	V_{CC}	—	V_{CC} -GND: Logic power supply
	GND	37	GND		V_{CC} - V_{EE} : Power supply for driving the liquid crystal display.
	V_{EE}	34	V_{EE}		
	V1	30	V1	Input	Power supply voltage for liquid crystal display drive level. See Figure 3.
	V2	31	V2		
V3	32	V3			
V4	33	V4			
Control signal	CL1	36	Clock 1	Input	Column driver data latch signal. Data is latched at the falling edge of this signal. Set this signal low in common driver operation.
	CL2	47	Clock 2	Input	In column driver operation, used as a display data latch signal. In common driver operation, used as a line selection data shift signal. In both operations, this signal is valid at its falling edge.
	M	35	M	Input	AC conversion signal for liquid crystal display drive output.
	SHL	38	Shift left	Input	Control signal for inverting data output destination. 1. In column driver operation See Figure 4. 2. In common driver operation SR1, SR2, SR3, ..., SR80 correspond to Y1, Y2, Y3, ..., Y80 outputs. When SHL is low, data is input to D0L pin and output from D1R pin. D2 and D3 are set low. When SHL is high, the relationships between D0L and D1R are reverse. See Table 2.
	\bar{E}	29	Enable	Input	When FCS is high, data latch starts by setting the \bar{E} signal low. When FCS is low, set the \bar{E} signal high. The relationships between the \bar{E} signal, the FCS signal, data latch operation, and driver function are as show in Table 3

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Table 1 Pin Function (cont)

Classification	Symbol	Pin No.	Pin Name	Input/ Output	Function
Control signal	$\overline{\text{CAR}}$	48	Carry	Output	When FCS is high, a chip enable signal is transferred to the next IC from this pin. Connect this pin to $\overline{\text{E}}$ of the next IC. When FCS is low, open this pin.
	$\overline{\text{DISPOFF}}$	42	Display off	Input	When this signal is low, liquid crystal display drive output is set at V1 level and liquid crystal display is turned off. At this time, internal display data is not affected. When this signal is high, the operation returns to the normal status.
	D0L D1L	46 45	Data0 (L) Data1 (R)	Input/ output	In column driver operation, input display data to D0L, D1R, D2, and D3 pins. In common driver operation, when SHL is high, D0L and D1R pins are display data output and input pins, respectively, and vice versa when SHL is low. At this time, set D2 and D3 low.
	D2 D3	44 43	Data2 Data3	Input	When display data is high, liquid crystal display drive output is selection level and the display is on, and when display data is low, they are non-selection level and off, respectively.
	FCS	40	Function select	Input	Control signal to select each operating mode. When the FCS pin is high, the operating mode is column driver, and when it is low, the operation mode is common driver.
	TEST	41	TEST	Input	Test pin. Set this pin low.
Liquid crystal display drive output	Y1 to Y80	49 to 100 1 to 28	Y1 to Y80	Output	Liquid crystal display drive output. One of four levels V1 to V4 is output according to the combination of the M signal and display data. See Figures 5 and 6.

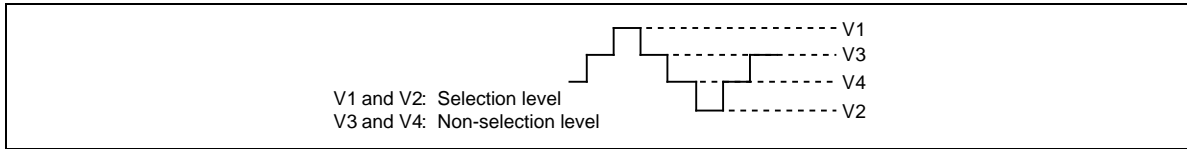


Figure 3 Liquid Crystal Display Drive Level

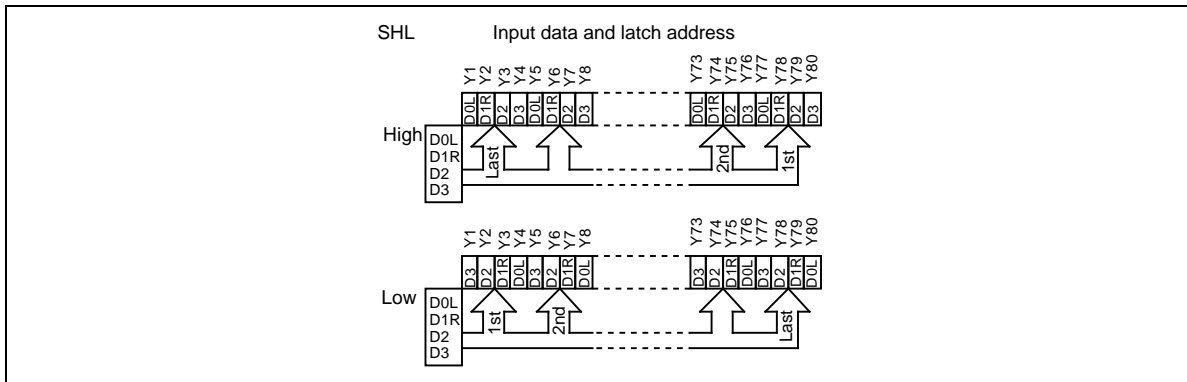


Figure 4 Column Driver Operating Mode

Table 2 Common Driver Operation

SHL	Shift Register Shift Direction				Common Signal Scan Direction		
Low	D0L	SR	SR	SR	D1R	Y1	Y80
		1	2	80			
High	D1R	SR	SR	SR	D0L	Y80	Y1
		80	79	1			

Table 3 Relationship between FCS, \bar{E} , Data Latch Operation, and Driver Function

FCS	\bar{E}	Data Latch Operation	Driver Function
High	Low	Enabled	Column driver
	High	Disabled	
Low	High	—	Common driver

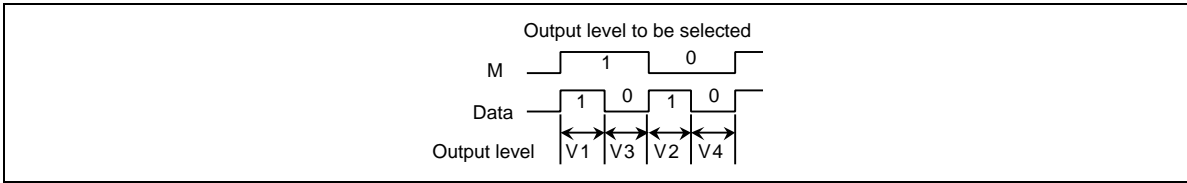


Figure 5 Liquid Crystal Display Drive Output in Column Driver Operation

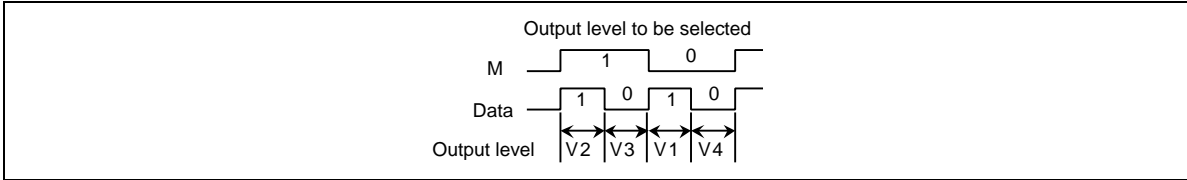


Figure 6 Liquid Crystal Display Drive Output in Common Driver Operation

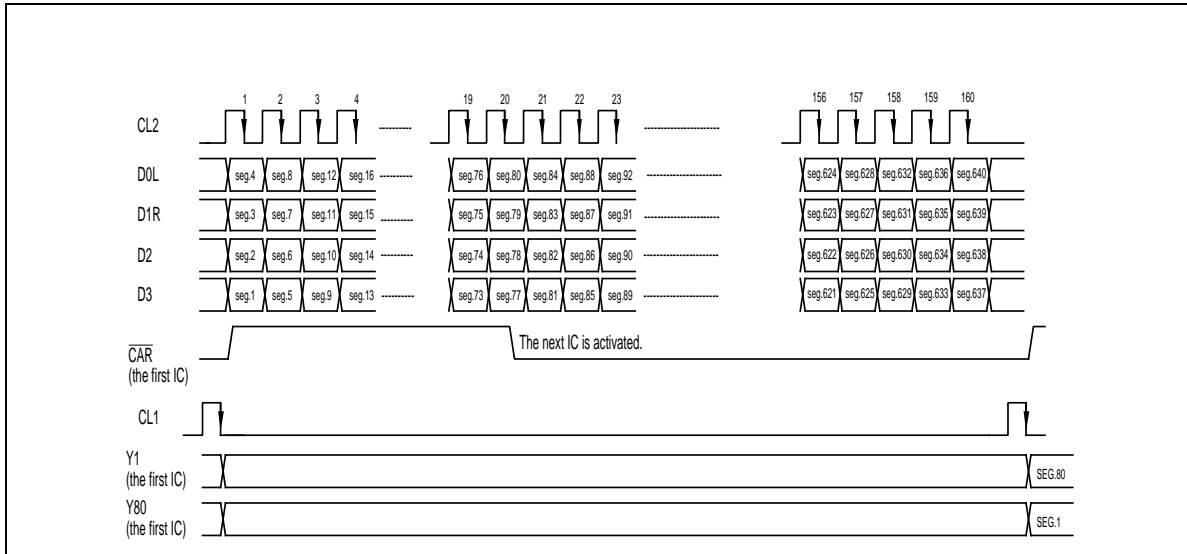


Figure 8 Timing Charts for Application Example in Column Driver Operation

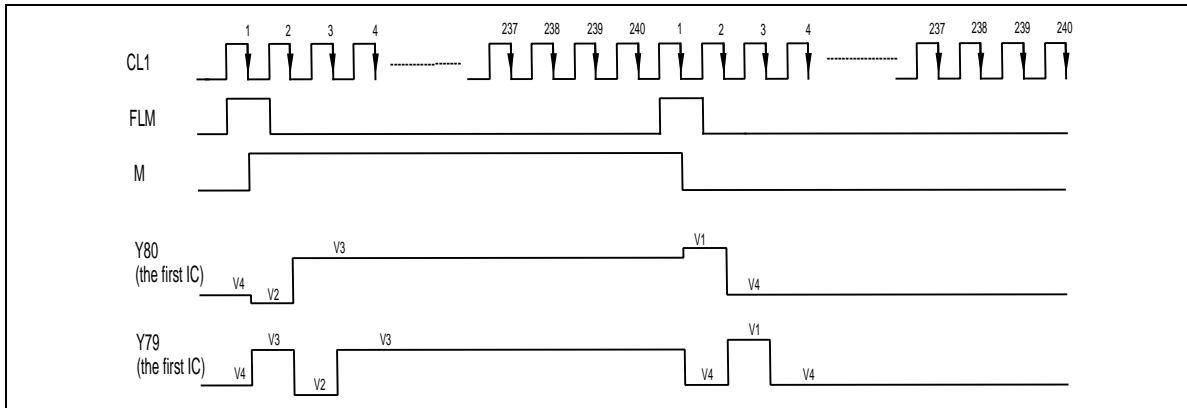


Figure 9 Timing Charts for Application Example in Common Driver Operation

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Note
Power supply voltage	Logic circuit	V_{CC}	-0.3 to +7.0	V	1
	Liquid crystal display drive circuit	V_{EE}	$V_{CC} - 30.0$ to $V_{CC} + 0.3$	V	
Input voltage (1)		VT1	-0.3 to $V_{CC} + 0.3$	V	1 and 2
Input voltage (2)		VT2	$V_{EE} - 0.3$ to $V_{CC} + 0.3$	V	1 and 3
Operating temperature		T_{opr}	-20 to +75	°C	
Storage temperature		T_{stg}	-55 to +125	°C	

- Notes:
1. Measured relative to GND (0V).
 2. Applies to CL1, CL2, M, SHL, \bar{E} , D0L, D1R, D2, D3, FCS, TEST, and $\overline{DISPOFF}$ pins.
 3. Applies to V1 to V4 pins.
 4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.

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Electrical Characteristics

DC Characteristics 1 ($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $V_{CC} - V_{EE} = 6$ to $28V$, and $T_a = -20$ to 75 °C, unless otherwise stated)

Item	Symbol	Applicable Pin	Min.	Typ.	Max.	Unit	Conditions	Note
Input high level voltage	V_{IH}	CL1, CL2, M, SHL, \bar{E} , D0L, D1R, D2,	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage	V_{IL}	D3, FCS, TEST, and $\overline{DISPOFF}$	0	—	$0.3 \times V_{CC}$	V		
Output high level voltage	V_{OH}	\overline{CAR} , D0L, D1R	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -0.4$ mA	
Output low level voltage	V_{OL}	\overline{CAR} , D0L, D1R	—	—	0.4	V	$I_{OL} = 0.4$ mA	
Vi-Yj on resistance	R_{ON1}	Y1 to Y80, V1 to V4	—	—	2.0	k Ω	$I_{ON} = 100$ μ A $V_{CC} - V_{EE} = 28V$	1 and 5
	R_{ON2}		—	—	4.0	k Ω		1 and 4
Input leakage current (1)	I_{IL1}	CL1, CL2, M, SHL, \bar{E} , D0L, D1R, D2, D3, FCS, TEST, and $\overline{DISPOFF}$	-5	—	5	μ A	$V_{IN} = V_{CC}$ to GND	
Input leakage current (2)	I_{IL2}	V1 to V4	-25	—	25	μ A	$V_{IN} = V_{CC}$ to V_{EE}	
Consumption current (1)	I_{GND1}	—	—	—	3.0	mA	$f_{CL2} = 8.0$ MHz $f_{CL1} = 50$ kHz $f_M = 2.3$ kHz	2 and 4
Consumption current (2)	I_{ST}	—	—	—	200	μ A	$V_{CC} = 5V$ $V_{CC} - V_{EE} = 28V$	2 to 4
Consumption current (3)	I_{EE1}	—	—	—	500	μ A	Checker data FCS = high	2 and 4
Consumption current (4)	I_{GND2}	—	—	—	100	μ A	$f_{CL1} = 50$ kHz $f_M = 2.3$ kHz	2 and 5
Consumption current (5)	I_{EE2}	—	—	—	500	μ A	$V_{CC} = 5V$ $V_{CC} - V_{EE} = 28V$ FCS = low	2 and 5

DC Characteristics 2 ($V_{CC} = 2.7$ to $4.5V$, $GND = 0V$, $V_{CC} - V_{EE} = 6$ to $28V$, and $T_a = -20$ to $75\text{ }^\circ\text{C}$, unless otherwise stated)

Item	Symbol	Applicable pin	Min.	Typ.	Max.	Unit	Conditions	Note
Input high level voltage	V_{IH}	CL1, CL2, M, SHL, \bar{E} , D0L, D1R, D2,	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage	V_{IL}	D3, FCS, TEST, and $\overline{DISPOFF}$	0	—	$0.2 \times V_{CC}$	V		
Output high level voltage	V_{OH}	\overline{CAR} , D0L, and D1R	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -0.4\text{ mA}$	
Output low level voltage	V_{OL}	\overline{CAR} , D0L, and D1R	—	—	0.4	V	$I_{OL} = 0.4\text{ mA}$	
Vi-Yj on resistance	R_{ON1}	Y1 to Y80, and V1 to V4	—	—	2.0	k Ω	$I_{ON} = 100\text{ }\mu\text{A}$ $V_{CC} - V_{EE} = 2\text{ }8V$	1 and 5
	R_{ON2}		—	—	4.0	k Ω		1 and 4
Input leakage current (1)	I_{IL1}	CL1, CL2, M, SHL, \bar{E} , D0L, D1R, D2, D3, FCS, TEST, and $\overline{DISPOFF}$	-5	—	5	μA	$V_{IN} = V_{CC}$ to GND	
Input leakage current (2)	I_{IL2}	V1 to V4	-25	—	25	μA	$V_{IN} = V_{CC}$ to V_{EE}	
Consumption current (1)	I_{GND1}	—	—	—	1.5	mA	$f_{CL2} = 6.5\text{ MHz}$ $f_{CL1} = 40.6\text{ kHz}$ $f_M = 1.8\text{ kHz}$	2 and 4
Consumption current (2)	I_{ST}	—	—	—	100	μA	$V_{CC} = 3.0V$ $V_{CC} - V_{EE} = 28V$	2 to 4
Consumption current (3)	I_{EE1}	—	—	—	500	μA	Checker data FCS = high	2 and 4
Consumption current (4)	I_{GND2}	—	—	—	50	μA	$f_{CL1} = 40.6\text{ kHz}$ $f_M = 1.8\text{ kHz}$	2 and 5
Consumption current (5)	I_{EE2}	—	—	—	500	μA	$V_{CC} = 3.0V$ $V_{CC} - V_{EE} = 28V$ FCS = low	2 and 5

Notes: 1. Indicates the resistance between one pin from Y1 to Y80 and another pin from the V pins V1 to V4, when a load current is applied to the Y pin; defined under the following conditions:

In column driver operation

$$V1 \text{ and } V3 = V_{CC} - 2/10 (V_{CC} - V_{EE})$$

$$V4 \text{ and } V2 = V_{EE} + 2/10 (V_{CC} - V_{EE})$$

In common driver operation

$$V1 \text{ and } V3 = V_{CC} - 2/10 (V_{CC} - V_{EE})$$

$$V4 \text{ and } V2 = V_{EE} + 2/10 (V_{CC} - V_{EE})$$

V1 and V3 should be near the V_{CC} level, and V4 and V2 should be near the V_{EE} level. All these voltage pairs should be separated by less than ΔV , which is the range within which R_{ON} , the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage $V_{CC} - V_{EE}$. See Figure 10.

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2. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND, respectively.
3. $V_{CC} - GND$ current at standby (\bar{E} input = high)
4. Applies to column driver operation.
5. Applies to common driver operation.

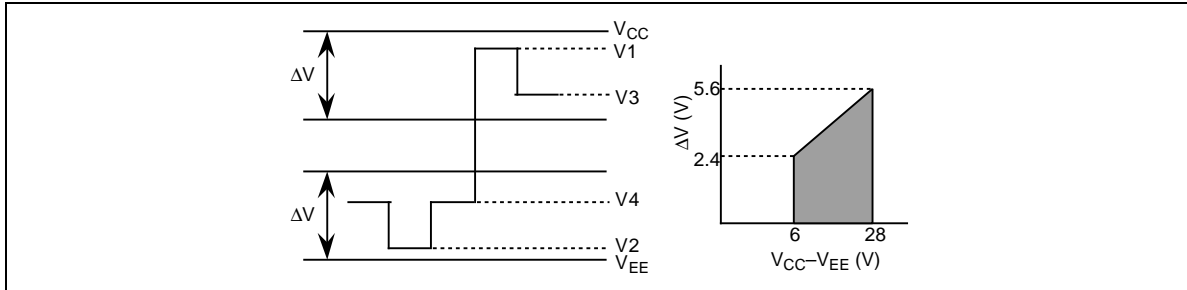


Figure 10 Relationship between Driver Output Waveform and Level Voltages

Pin Configuration

Each pin configuration is shown below.

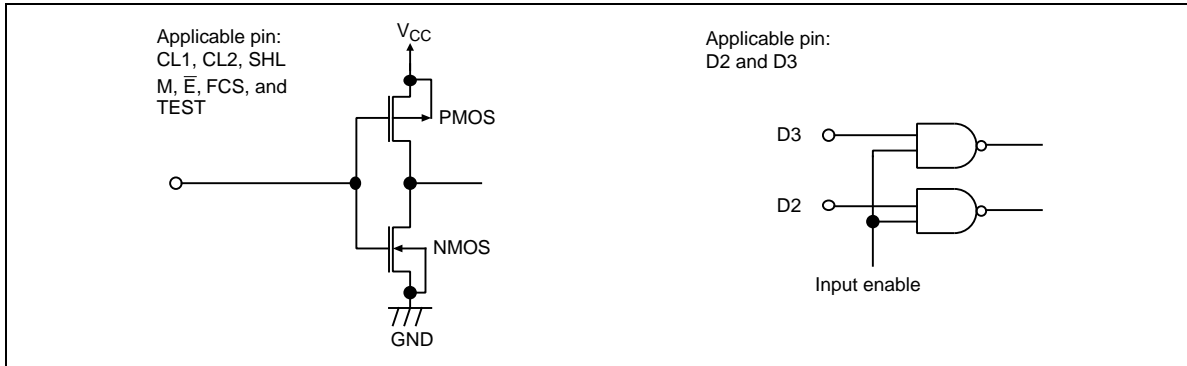


Figure 11 Input Pin Configuration

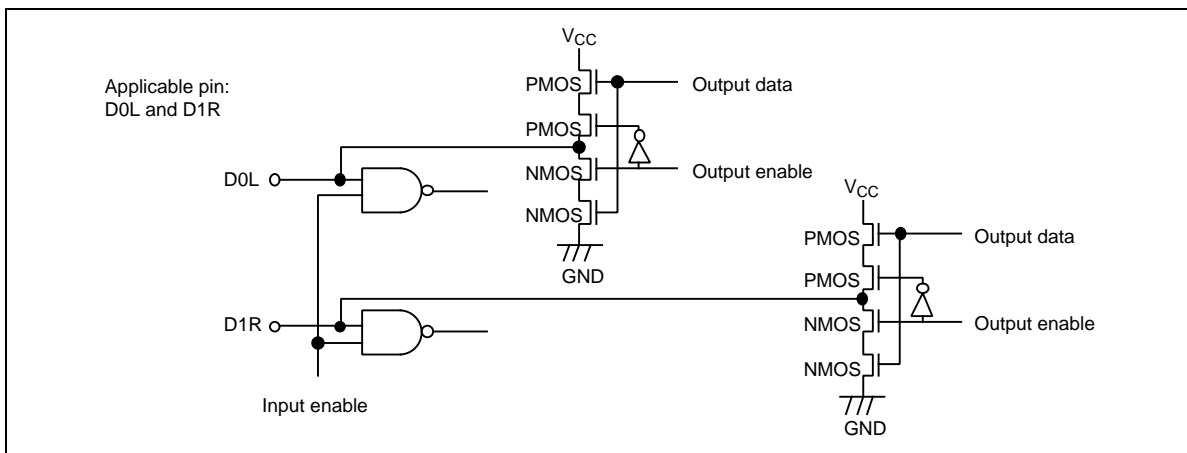


Figure 12 Input/Output Pin Configuration

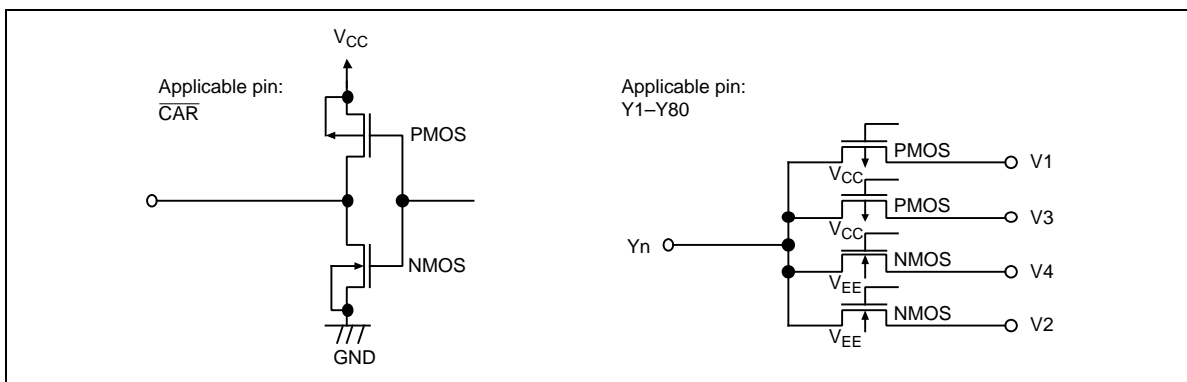


Figure 13 Output Pin Configuration

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AC Characteristics 1 (In Column Driver Operation) ($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $V_{CC} - V_{EE} = 6$ to $28V$, and $T_a = -20$ to $+75$ ° C, unless otherwise stated)

Item	Symbol	Applicable Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	125	—	ns	
Clock high level width	t_{CWH}	CL2 and CL1	40	—	ns	
Clock low level width	t_{CWL}	CL2	40	—	ns	
Clock setup time	t_{SCL}	CL1 and CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1 and CL2	80	—	ns	
Clock rise time	t_r	CL1 and CL2	—	1	ns	1
Clock fall time	t_f	CL1 and CL2	—	1	ns	1
Data setup time	t_{DS}	D0L, D1R, D2, D3, and CL2	20	—	ns	
Data hold time	t_{DH}	D0L, D1R, D2, D3, and CL2	20	—	ns	
Enable setup time	t_{ESU}	\bar{E} and CL2	20	—	ns	
Carry output delay time	t_{CAR}	$\bar{C}AR$ and CL2	—	70	ns	2
M phase difference	t_{CM}	M and CL1	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

AC Characteristics 2 (In Column Driver Operation) ($V_{CC} = 2.7$ to $4.5V$, $GND = 0V$, $V_{CC} - V_{EE} = 6$ to $28V$, and $T_a = -20$ to $+75$ ° C, unless otherwise stated)

Item	Symbol	Applicable pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	152	—	ns	
Clock high level width	t_{CWH}	CL2 and CL1	65	—	ns	
Clock low level width	t_{CWL}	CL2	65	—	ns	
Clock setup time	t_{SCL}	CL1 and CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1 and CL2	120	—	ns	
Clock rise time	t_r	CL1 and CL2	—	1	ns	1
Clock fall time	t_f	CL1 and CL2	—	1	ns	1
Data setup time	t_{DS}	D0L, D1R, D2, D3, and CL2	50	—	ns	
Data hold time	t_{DH}	D0L, D1R, D2, D3, and CL2	50	—	ns	
Enable setup time	t_{ESU}	\bar{E} and CL2	30	—	ns	
Carry output delay time	t_{CAR}	$\bar{C}AR$ and CL2	—	100	ns	2
M phase difference	t_{CM}	M and CL1	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

Notes: 1. Clock rise time (t_r) and clock fall time (t_f) must satisfy the following conditions:

$$t_r \text{ and } t_f < (t_{CYC} - t_{CWH} - t_{CWL})/2$$

$$t_r \text{ and } t_f \leq 50$$

2. Defined by connecting the load circuit shown in Figure 14.

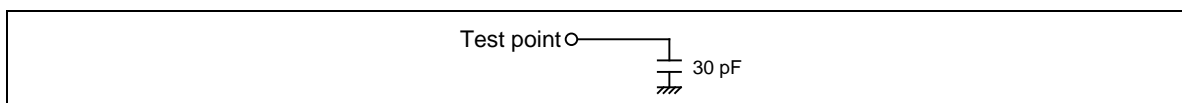


Figure 14 Load Circuit

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AC Characteristics 3 (In Common Driver Operation) ($V_{CC} = 2.7$ to $5.5V$, $GND = 0V$, $V_{CC} - V_{EE} = 6$ to $28V$, and $T_a = -20$ to $+75$ ° C, unless otherwise stated)

Item	Symbol	Applicable Pins	Min.	Max.	Unit	Note
Clock cycle time	t_{CYC}	CL2	10	—	μs	
Clock high level width	t_{CWH}	CL2	80	—	ns	
Clock low level width	t_{CWL}	CL2	1.0	—	μs	
Clock rise time	t_r	CL2	—	30	ns	
Clock fall time	t_f	CL2	—	30	ns	
Data setup time	t_{DS}	D0L, D1R, and CL2	100	—	ns	
Data hold time	t_{DH}	D0L, D1R, and CL2	100	—	ns	
Data output delay time	t_{DD}	D0L, D1R, and CL2	—	7.0	μs	1

Note: Defined by connecting the load circuit shown in Figure 15.

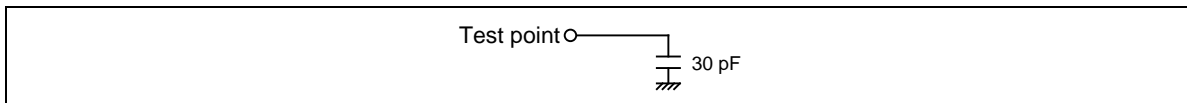


Figure 15 Load Circuit

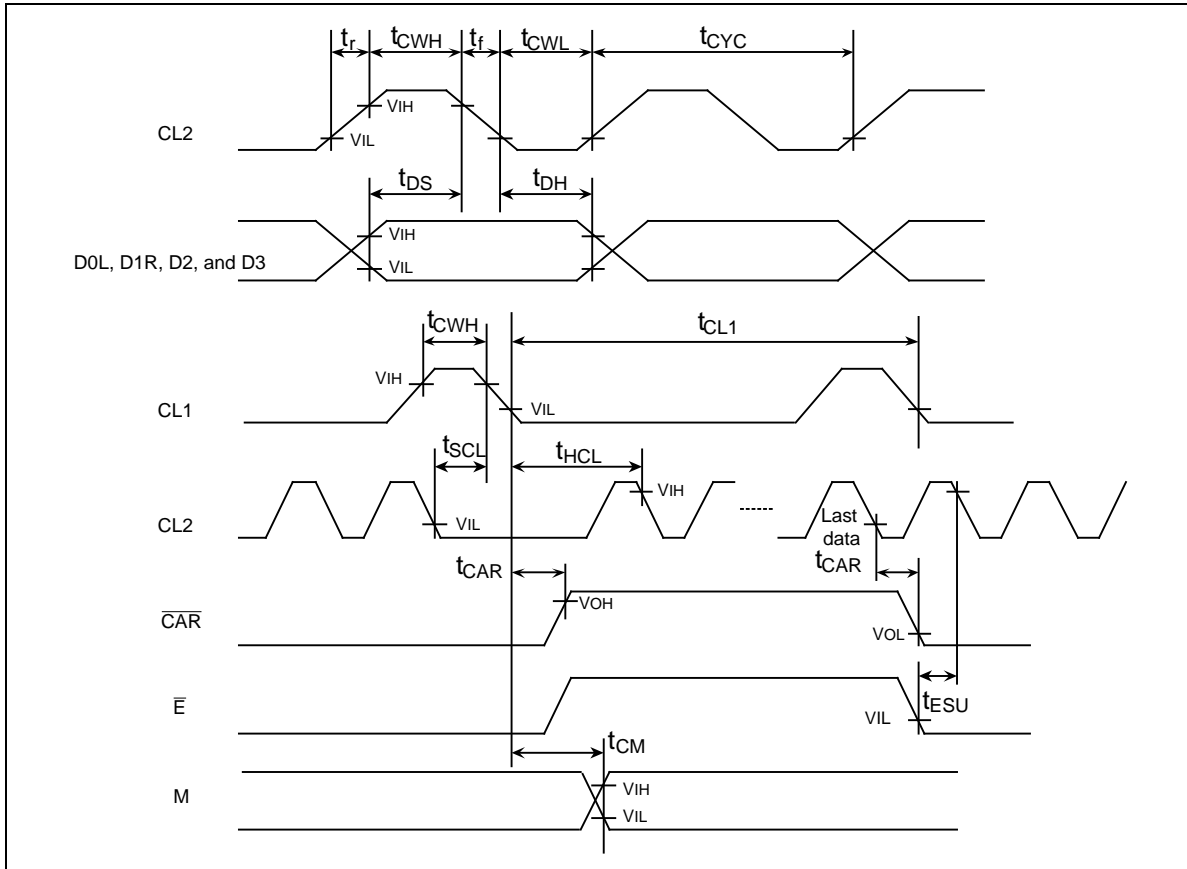


Figure 16 Common Driver Operation Timing

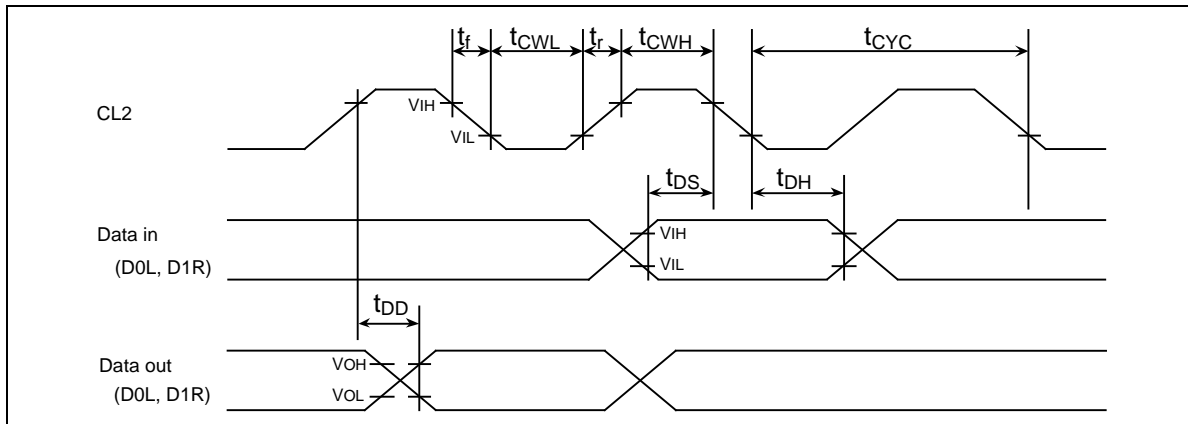


Figure 17 Common Driver Operation Timing