HD66204

(Dot Matrix Liquid Crystal Graphic Display Column Driver with 80-Channel Outputs)

Description

The HD66204F/HD66204FL/HD66204TF/HD66204TFL, the column driver for a large liquid crystal graphic display, features as many as 80 LCD outputs powered by 80 internal LCD drive circuits. This device latches 4-bit parallel data sent from an LCD controller, and generates LCD drive signals. In standby mode provided by its internal standby function, only one drive circuit operates, lowering power dissipation. The HD66204 has a complete line-up: the HD66204F, a standard device powered by 5 V ± 10%; the HD66204FL, a 2.7–5.5 V, low power dissipation device suitable for battery-driven portable equipment such as "notebook" personal computers and palm-top personal computers; and the HD66204TF and HD66204TFL, thin package devices powered by 5 V ± 10% and 2.7–5.5 V, respectively.

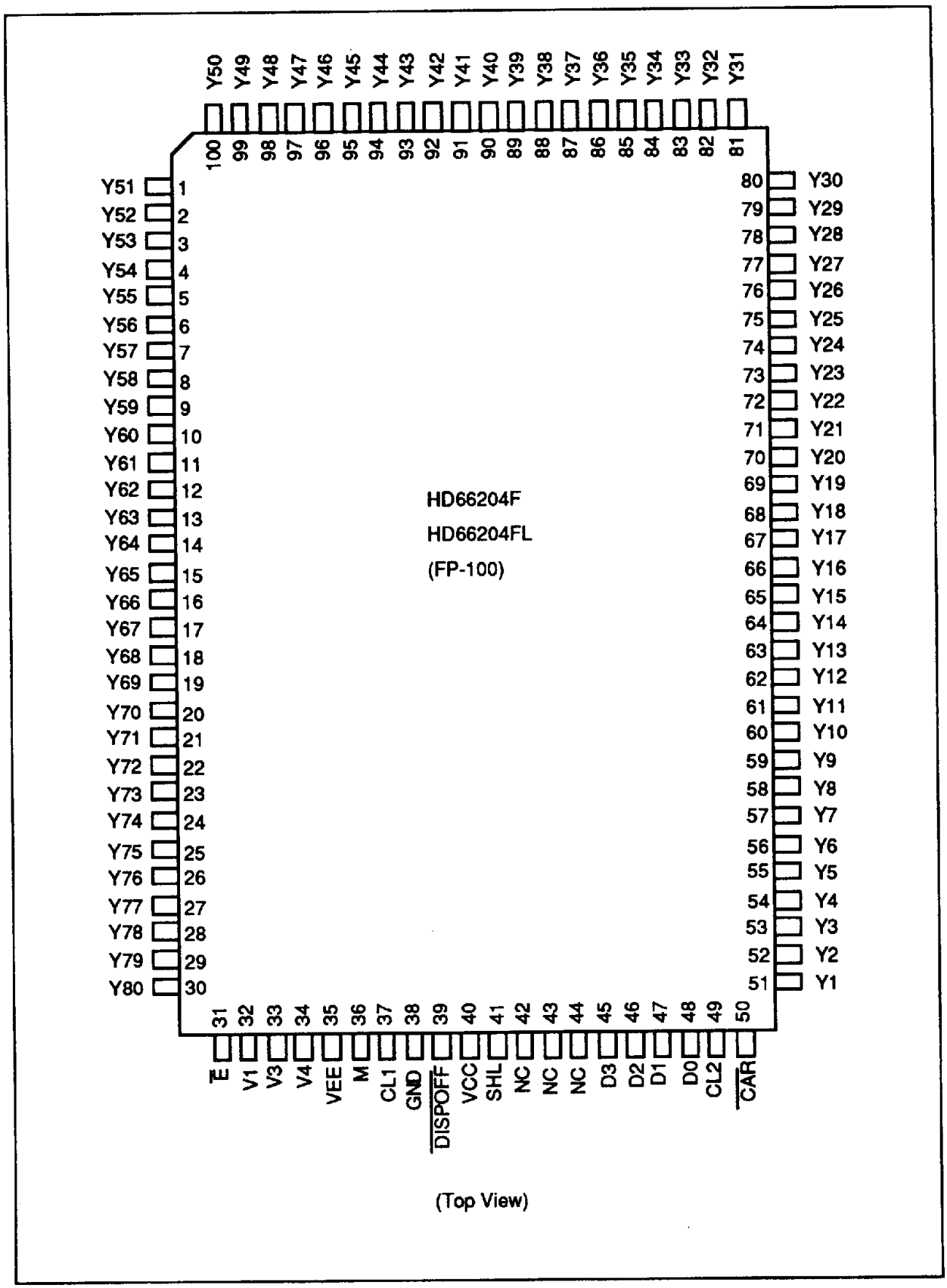
Features

- Duty cycle: 1/64 to 1/240
- High voltage
  - — LCD drive: 10–28 V
- High clock speed
  - — 8 MHz max under 5-V operation (HD66204F/HD66204TF)
  - — 4 MHz max under 3-V operation (HD66204FL/HD66204TFL)
- Display off function
- Internal automatic chip enable signal generator
- Various LCD controller interfaces
  - — LCTC series: HD63645, HD64645, HD64646
  - — LVIC series: HD66840, HD66841
  - — CLINE: HD66850

Ordering Information

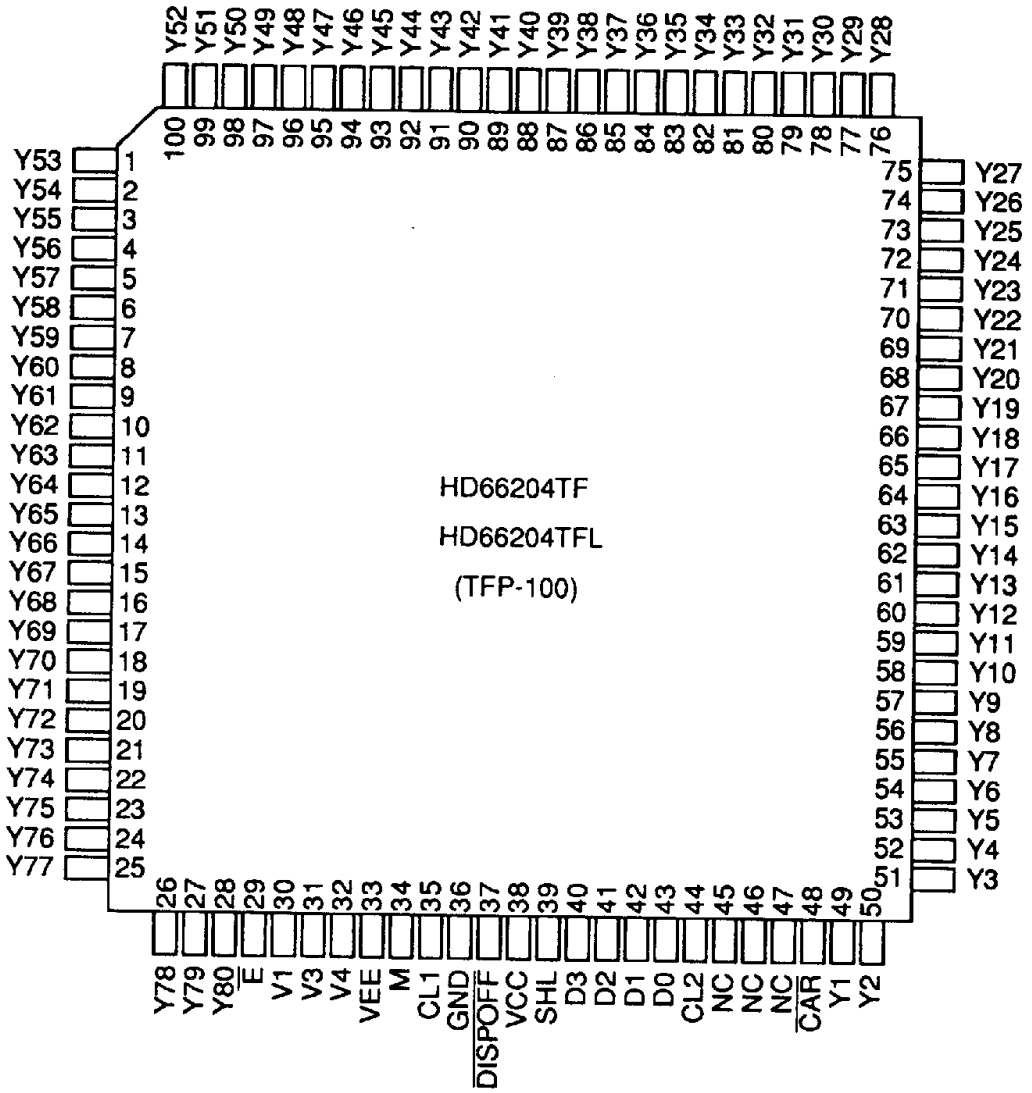
Type No.	Voltage Range	Package
HD66204F	5 V ± 10%	100-pin plastic QFP (FP-100)
HD66204TF	5 V ± 10%	100-pin thin plastic QFP (TFP-100)
HCD66204	5 V ± 10%	Chip
HD66204FL	2.7–5.5 V	100-pin plastic QFP (FP-100)
HD66204TFL	2.7–5.5 V	100-pin thin plastic QFP (TFP-100)
HCD66204L	2.7–5.5 V	Chip

Pin Arrangement



(Top View)

HITACHI



(Top View)

Pin Description

Symbol	Pin No. (FP-100/TFP-100)	Pin Name	Input/Output	Classification
V_{CC}	40/38	V_{CC}	—	Power supply
GND	38/36	GND	—	Power supply
V_{EE}	35/33	V_{EE}	—	Power supply
V1	32/30	V1	Input	Power supply
V3	33/31	V3	Input	Power supply
V4	34/32	V4	Input	Power supply
CL1	37/35	Clock 1	Input	Control signal
CL2	49/44	Clock 2	Input	Control signal
M	36/34	M	Input	Control signal
D_0–D_3	48–45/43–40	Data 0–data 3	Input	Control signal
SHL	41/39	Shift left	Input	Control signal
$\overline{E}$	31/29	Enable	Input	Control signal
$\overline{CAR}$	50/48	Carry	Output	Control signal
$\overline{DISPOFF}$	39/37	Display off	Input	Control signal
Y_1–Y_{80}	51–100, 1–30/49–100, 1–28	Y1–Y80	Output	LCD drive output
NC	42, 43, 44/45, 46, 47	No connection	—	—

Pin Functions

Power Supply

V_{CC}, V_{EE}, GND: V_{CC}–GND supplies power to the internal logic circuits. V_{CC}–V_{EE} supplies power to the LCD drive circuits.

V1, V3, V4: Supply different levels of power to drive the LCD. V1 and V_{EE} are selected levels, and V3 and V4 are non-selected levels. See figure 1.

Control Signal

CL1: Inputs display data latch pulses for the line data latch circuit. The line data latch circuit latches display data input from the 4-bit latch circuit, and outputs LCD drive signals corresponding to the latched data, both at the falling edge of each CL1 pulse.

CL2: Inputs display data latch pulses for the 4-bit latch circuit. The 4-bit latch circuit latches display data input via D_0–D_3 at the falling edge of each CL2 pulse.

M: Changes LCD drive outputs to AC.

D_0–D_3: Input display data. High-voltage level of data corresponds to a selected level and turns an LCD pixel on, and low-voltage level data corresponds to a non-selected level and turns an LCD pixel off.

SHL: Shifts the destinations of display data output. See figure 2.

$\overline{E}$: A low $\overline{E}$ enables the chip, and a high $\overline{E}$ disables the chip.

$\overline{CAR}$: Outputs the $\overline{E}$ signal to the next HD66204 if HD66204s are connected in cascade.

$\overline{DISPOFF}$: A low $\overline{DISP}$ sets LCD drive outputs Y_1–Y_{80} to V1 level.

LCD Drive Output

Y_1–Y_{80}: Each Y outputs one of the four voltage levels V1, V3, V4, or V_{EE}, depending on a combination of the M signal and display data levels. See figure 3.

NC: Must be open.

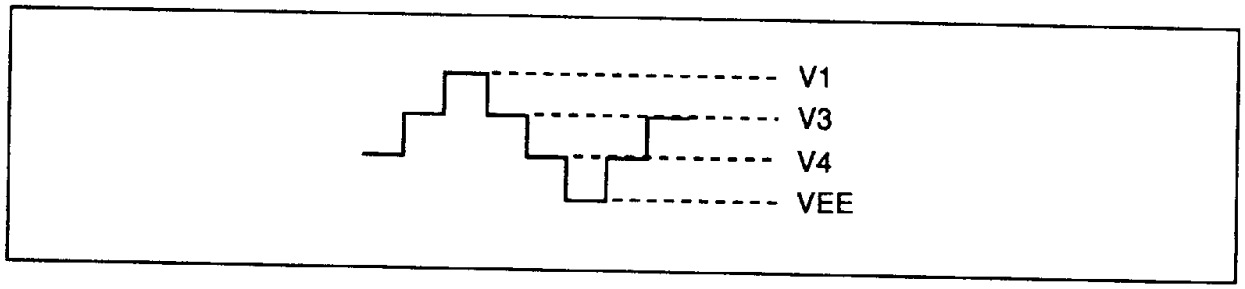


Figure 1 Different Power Supply Voltage Levels for LCD Drive Circuits

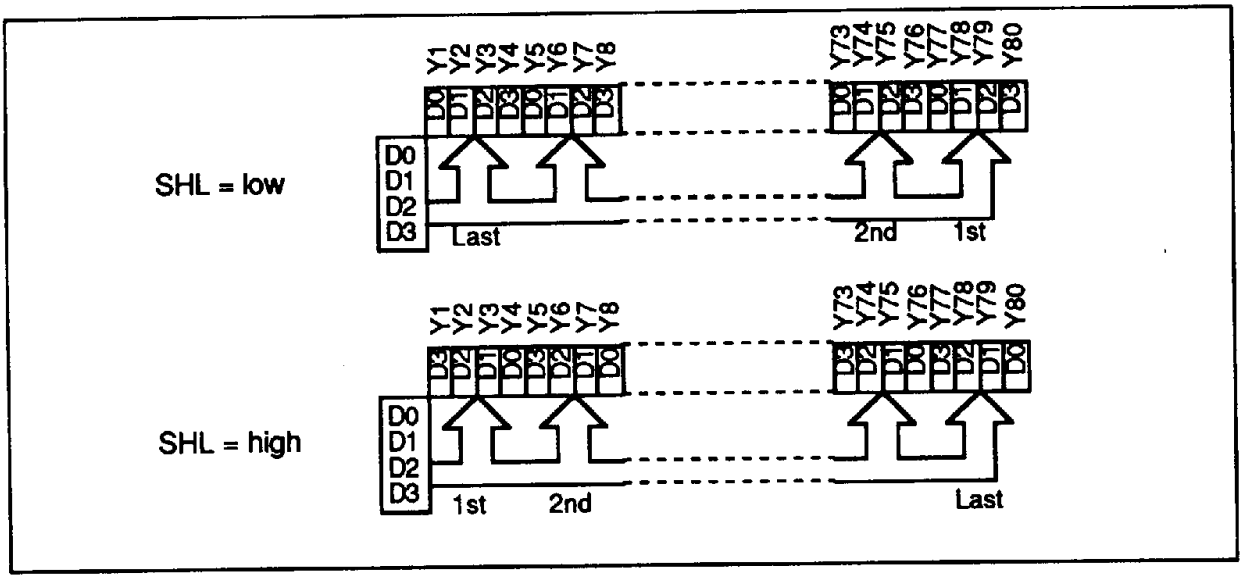


Figure 2 Selection of Destinations of Display Data Output

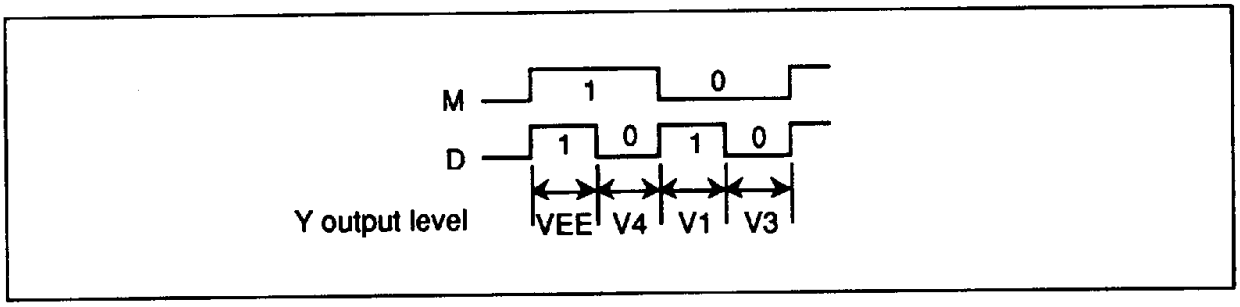


Figure 3 Selection of LCD Drive Output Level

Block Functions

LCD Drive Circuit

Controller: The controller generates the latch signal at the falling edge of each CL2 pulse for the 4-bit latch circuit.

4-Bit Latch Circuit

The 4-bit latch circuit latches 4-bit parallel data input via the D_0 to D_3 pins at the timing generated by the control circuit.

Line Data Latch Circuit

The 80-bit line data latch circuit latches data input from the 4-bit latch circuit, and outputs the latched data to the level shifter, both at the falling edge of each clock 1 (CL1) pulse.

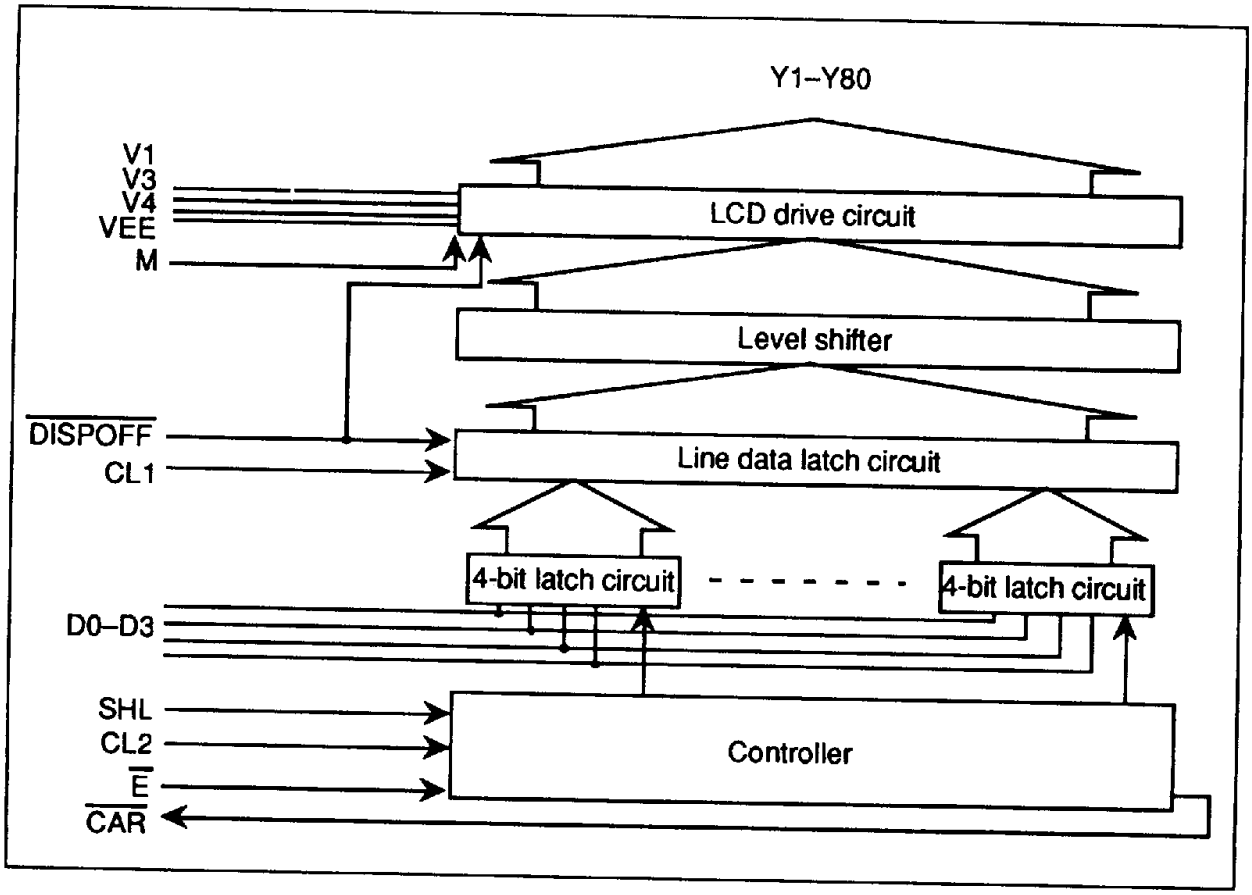
Level Shifter

The level shifter changes 5-V signals into high-voltage signals for the LCD drive circuit.

LCD Drive Circuit

The 80-bit LCD drive circuit generates four voltage levels V1, V3, V4, and VEE, for driving an LCD panel. One of the four levels is output to the corresponding Y pin, depending on a combination of the M signal and the data in the line data latch circuit.

Block Diagram



Comparison of the HD66204 with the HD61104

Item	HD66204	HD61104
Clock speed	8.0 MHz max.	3.5 MHz max.
Display off function	Provided	Not provided
LCD drive voltage range	10–28 V	10–26 V
Relation between SHL and LCD output destinations	See figure 4	See figure 4
Relation between LCD output levels, M, and data	See figure 5	See figure 5
LCD drive V pins	V1, V3, V4 (V2 level is the same as VEE level)	V1, V2, V3, V4

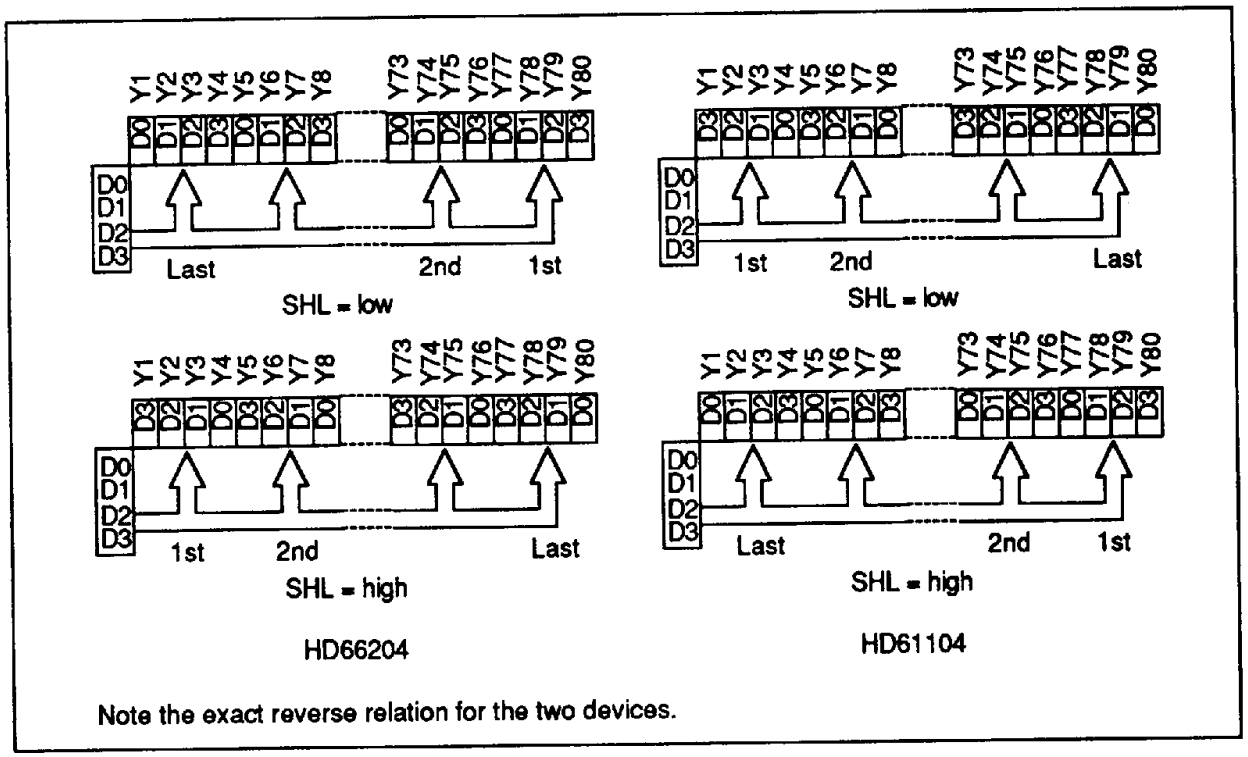


Figure 4 Relation between SHL and LCD Output Destinations for the HD66204 and HD61104

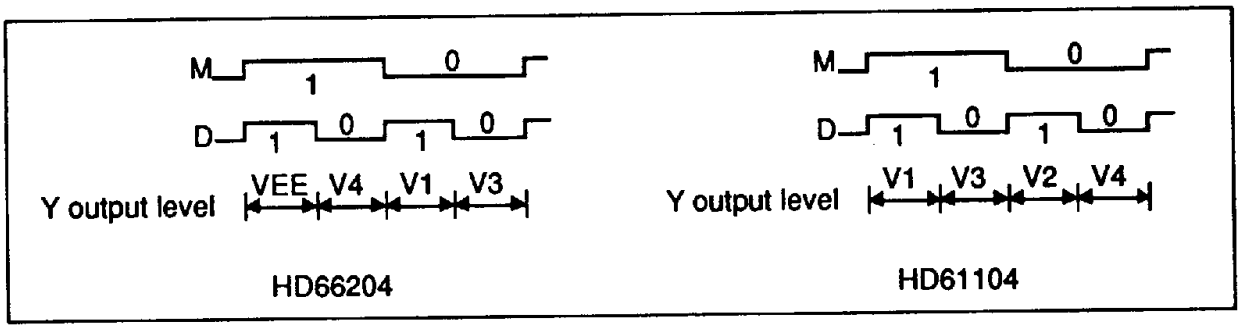
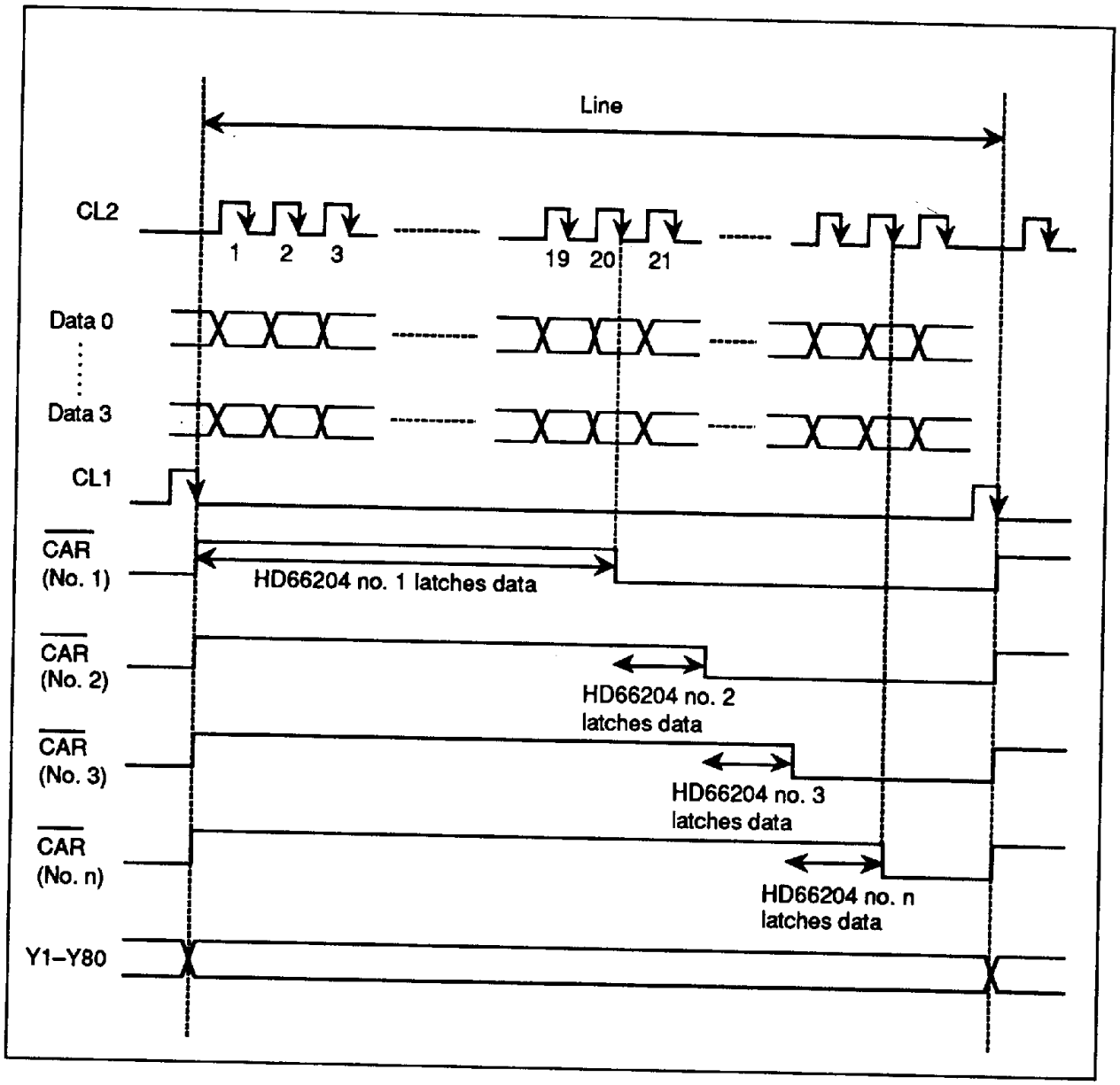
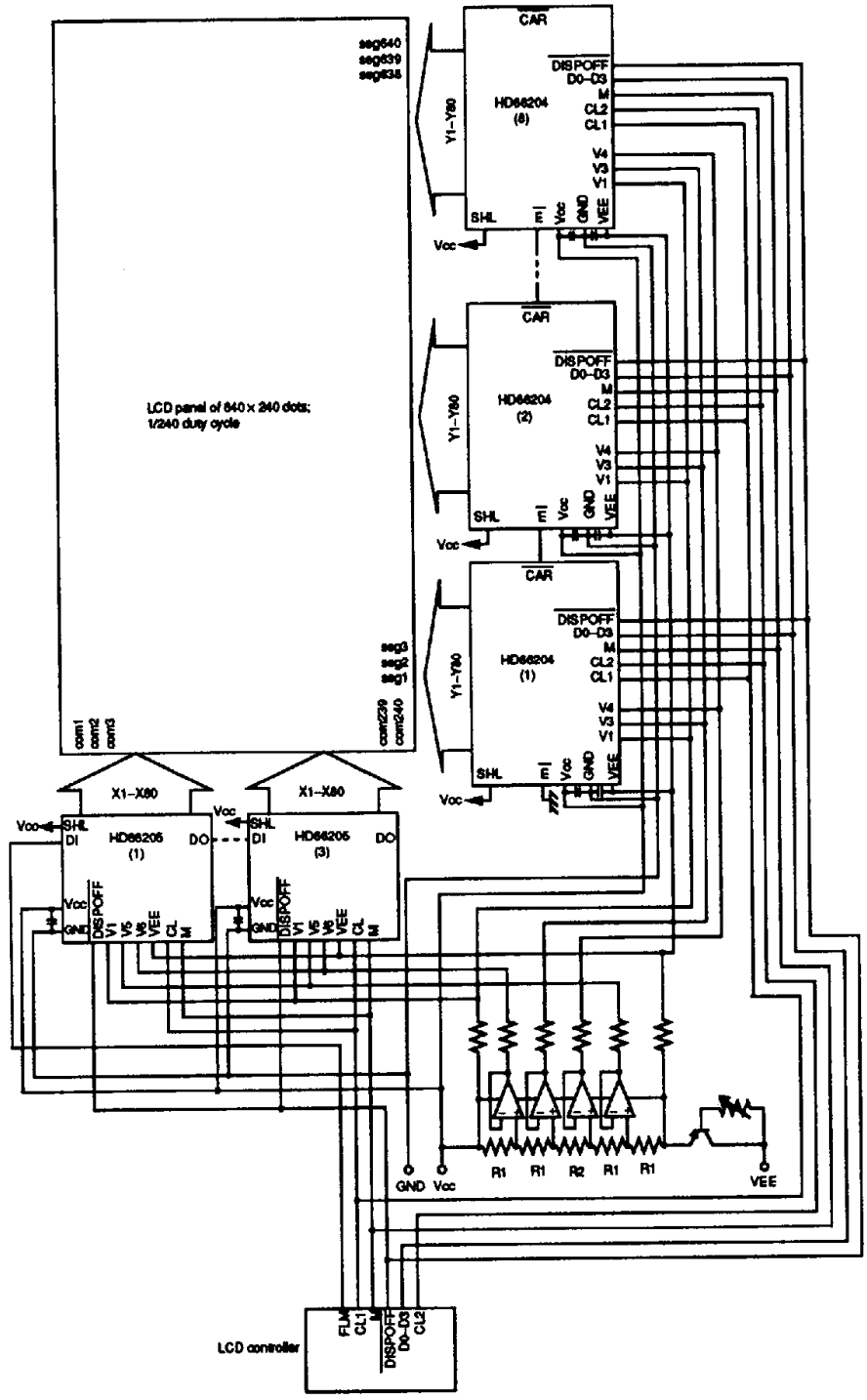


Figure 5 Relation between LCD Output Levels, M, and Data for the HD66204 and HD61104

Operation Timing



Application Example



Notes:
1. The resistances of R1 and R2 depend on the type of the LCD panel used. For example, for an LCD panel with a 1/15 bias, R1 and R2 must be 3 kΩ and 33 kΩ, respectively. That is, R1/(4 • R1 + R2) should be 1/15.
2. To stabilize the power supply, place two 0.1-μF capacitors near each LCD driver: one between the V_{CC} and GND pins, and the other between the V_{CC} and V_{EE} pins.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	−0.3 to +7.0	V	1
Power supply voltage for LCD drive circuits	V_{EE}	V_{CC} − 30.0 to V_{CC} + 0.3	V	
Input voltage 1	V_{T1}	−0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{EE} − 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−55 to +125	°C	

Notes: 1. The reference point is GND (0 V).

2. Applies to pins CL1, CL2, M, SHL, $\overline{E}$, D_0–D_3, $\overline{DISPOFF}$.
3. Applies to pins V1, V3, and V4.
4. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its electrical characteristics in order to prevent malfunctioning or degradation of reliability.

Electrical Characteristics

DC Characteristics for the HD66204F/HD66204TF (V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} − V_{EE} = 10 to 28 V, and Ta = −20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Typ.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	0.7 × V_{CC}	—	V	V		
Input low voltage	V_{IL}	1	0	—	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} − 0.4	—	—	V	I_{OH} = −0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	−1.0	—	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	−25	—	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	3.0	mA	f_{CL2} = 8.0 MHz f_{CL1} = 20 kHz V_{CC} − V_{EE} = 28 V	2
Current consumption 2	I_{EE}	—	—	150	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	—	200	µA	Same as above	2, 3

Pins and notes on next page.

DC Characteristics for the HD66204FL/HD66204TFL (V_{CC} = 2.7 to 5.5 V, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Condition	Notes
Input high voltage	V_{IH}	1	0.7 × V_{CC}	V_{CC}	V		
Input low voltage	V_{IL}	1	0	0.3 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Yj on resistance	R_{ON}	3	—	4.0	kΩ	I_{ON} = 100 µA	1
Input leakage current 1	I_{IL1}	1	–1.0	1.0	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	25	µA	V_{IN} = V_{CC} to V_{EE}	
Current consumption 1	I_{GND}	—	—	1.0	mA	f_{CL2} = 4.0 MHz f_{CL1} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V $V_{CC} - V_{EE}$ = 28 V Checker-board pattern	2
Current consumption 2	I_{EE}	—	—	500	µA	Same as above	2
Current consumption 3	I_{ST}	—	—	50	µA	Same as above	2, 3

Pins: 1. $\overline{CL1}$, $\overline{CL2}$, M, SHL, E, D_0–D_3, DISPOFF

2. $\overline{CAR}$
3. Y_1–Y_{80}, V1, V3, V4
4. V1, V3, V4

Notes: 1. Indicates the resistance between one pin from Y_1–Y_{80} and another pin from V1, V3, V4, and V_{EE}, when load current is applied to the Y pin; defined under the following conditions.

V_{CC} – GND = 28 V

V1, V3 = $V_{CC} - \{2/10(V_{CC} - V_{EE})\}$

V4 = $V_{EE} + \{2/10(V_{CC} - V_{EE})\}$

V1 and V3 should be near V_{CC} level, and V4 should be near V_{EE} level (figure 6). All voltage must be within ΔV. ΔV is the range within which R_{ON}, the LCD drive circuits' output impedance, is stable. Note that ΔV depends on power supply voltage V_{CC}–V_{EE} (figure 7).

2. Input and output current is excluded. When a CMOS input is floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held to V_{CC} and GND levels, respectively.

3. Applies to standby mode.

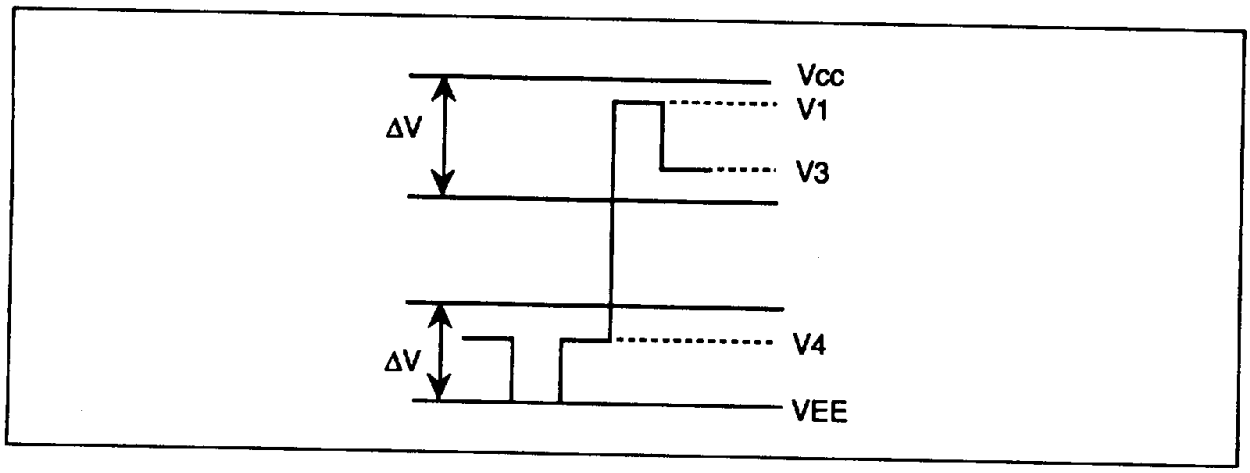


Figure 6 Relation between Driver Output Waveform and Level Voltages

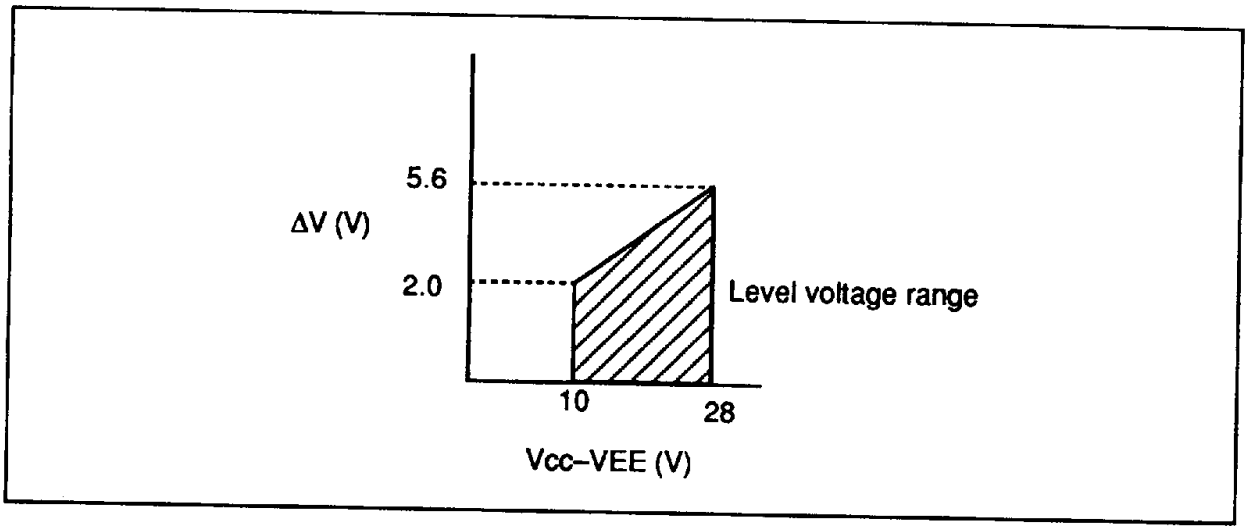


Figure 7 Relation between $V_{CC} - V_{EE}$ and ΔV

AC Characteristics for the HD66204F/HD66204TF (V_{CC} = 5 V ± 10%, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Notes
Clock cycle time	t_{CYC}	CL2	125	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	45	—	ns	
Clock low-level width	t_{CWL}	CL2	45	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	Note 1	ns	1
Clock fall time	t_f	CL1, CL2	—	Note 1	ns	1
Data setup time	t_{DS}	D_0–D_3, CL2	20	—	ns	
Data hold time	t_{DH}	D_0–D_3, CL2	20	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	30	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	80	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

AC Characteristics for the HD66204FL/HD66204TFL (V_{CC} = 2.7 to 5.5V, GND = 0 V, and Ta = –20 to +75°C, unless otherwise noted.)

Item	Symbol	Pins	Min.	Max.	Unit	Notes
Clock cycle time	t_{CYC}	CL2	250	—	ns	
Clock high-level width 1	t_{CWH}	CL1, CL2	95	—	ns	
Clock low-level width	t_{CWL}	CL2	95	—	ns	
Clock setup time	t_{SCL}	CL1, CL2	80	—	ns	
Clock hold time	t_{HCL}	CL1, CL2	80	—	ns	
Clock rise time	t_r	CL1, CL2	—	Note 1	ns	1
Clock fall time	t_f	CL1, CL2	—	Note 1	ns	1
Data setup time	t_{DS}	D_0–D_3, CL2	50	—	ns	
Data hold time	t_{DH}	D_0–D_3, CL2	50	—	ns	
Enable ($\overline{E}$) setup time	t_{ESU}	$\overline{E}$, CL2	65	—	ns	
Carry ($\overline{CAR}$) output delay time	t_{CAR}	$\overline{CAR}$, CL2	—	155	ns	2
M phase difference time	t_{CM}	M, CL2	—	300	ns	
CL1 cycle time	t_{CL1}	CL1	$t_{CYC} \times 50$	—	ns	

Notes: 1. t_r, $t_f < (t_{CYC} - t_{CWH} - t_{CWL})/2$ and t_r, $t_f \leq 50$ ns

2. The load circuit shown in figure 8 is connected.

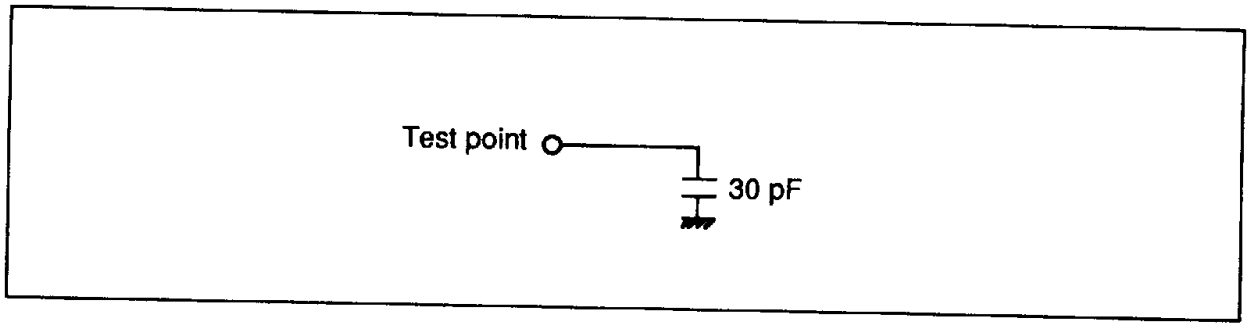


Figure 8 Load Circuit

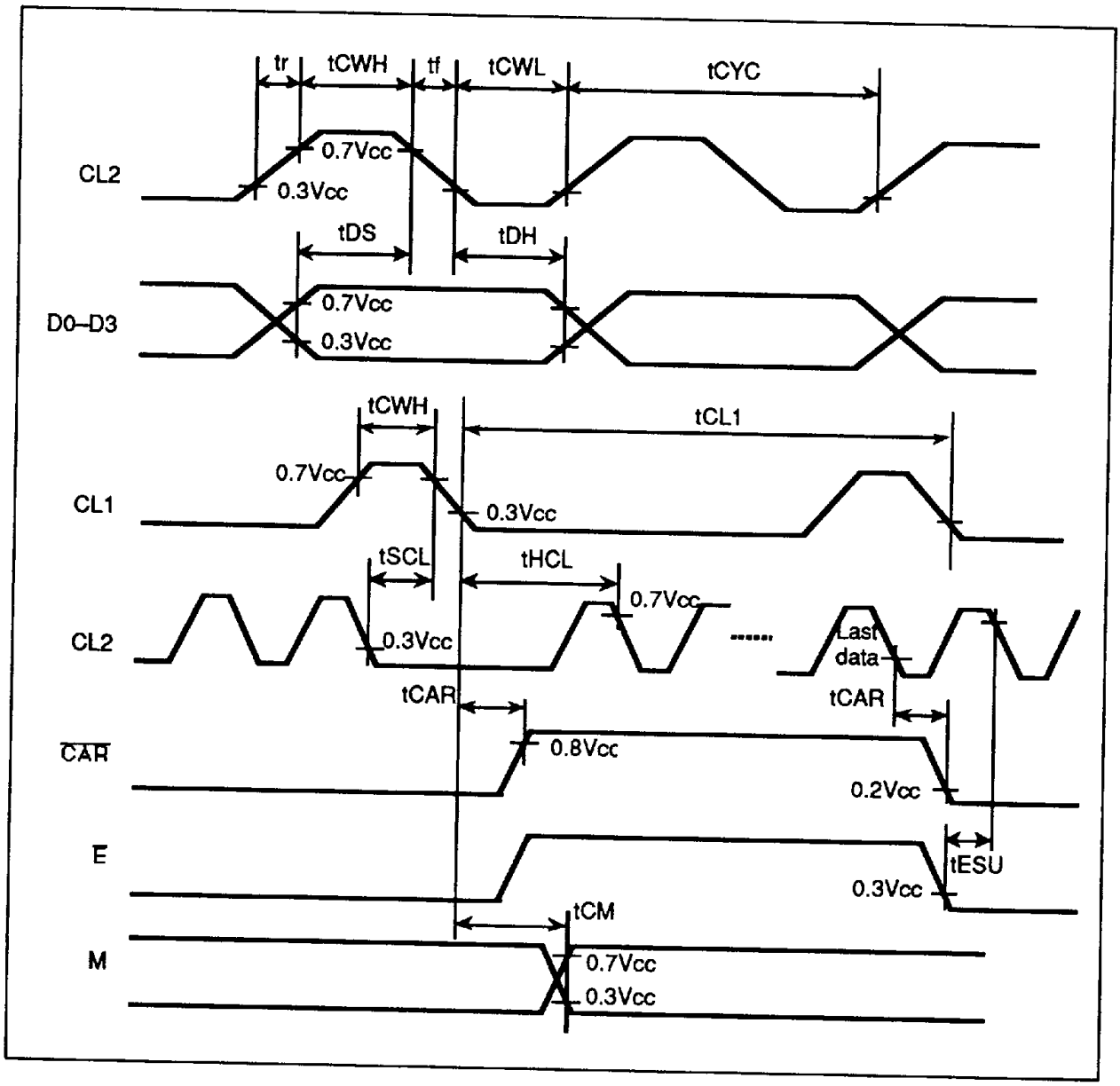


Figure 9 LCD Controller Interface Timing