HD66108

(RAM-Provided 165-Channel LCD Driver for Liquid Crystal Dot Matrix Graphics)

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Description

The HD66108T under control of an 8-bit MPU can drive a dot matrix graphic LCD (liquid-crystal display) employing bit-mapped display with support of an 8-bit MPU.

Use of the HD66108T enables a simple LCD system to be configured with only a small number of chips, since it has all the functions required for driving the display.

The HD66108T also enables highly-flexible display selection due to the bit-mapped method, in which one bit of data in a display RAM turns one dot of an LCD panel on or off. A single HD66108T can display a maximum of 100 × 65 dots by using its on-chip 165 × 65-bit RAM. Also, by using several HD66108T's, a display can be further expanded.

The HD66108T employs the CMOS process and TCP package. Thus, if used together with an MPU, it can provide the means for a battery-driven pocket-size graphic display device utilizing the low current consumption of LCDs.

Features

- Four types of LCD driving circuit configurations can be selected:

Configuration Type	No. of Column Outputs	No. of Row Outputs
Column outputs only	165	0
Row outputs from the left and right sides	100	65 (from left: 32, from right: 33)
Row outputs from the right side 1	100	65
Row outputs from the right side 2	132	33

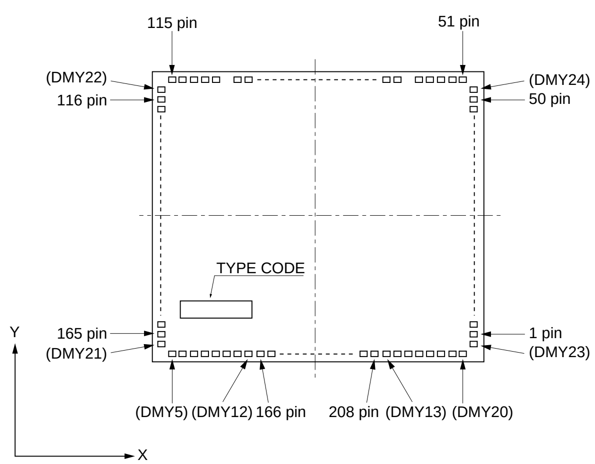
- Seven types of multiplexing duty ratios can be selected: 1/32, 1/34, 1/36, 1/48, 1/50, 1/64, 1/66
  Notes: The maximum number of row outputs is 65.
- Built-in bit-mapped display RAM: 10 kbits (165 × 65 bits)
- The word length of display data can be selected according to the character font: 8-bit or 6-bit
- A standby operation is available
- The display can be extended through a multi-chip operation
- A built-in CR oscillator
- An 80-system CPU interface: ø = 4 MHz
- Power supply voltage for operation: 2.7V to 6.0V
- LCD driving voltage: 6.0V to 15.0V
- Low current consumption: 400 µA max (at fOSC = 500 kHz, fOSC is external clock frequency)
- Package: 208-pin TCP (Tape-Carrier-Package)

Ordering Information

Type No.	Package	
HD66108T00	208 pin TCP	(Quad)
HD66108TA0		(Double side)
HD66108TB0		(Double side & folding TCP)
HCD66108BP		(Chip with bump)

Note: The details of TCP pattern are shown in "The Information of TCP."

HD66108 Pad Arrangement



Chip size (X × Y) : 8.30 × 6.02 mm
Coordinate : Pad Center
Origin : Chip Center
Pad size (X × Y) : 70 × 70 µm² (Bump size)

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HD66108 Pad Location Coordinates

Pin No.	Pad Name	Coordinate X	Coordinate Y	Pin No.	Pad Name	Coordinate X	Coordinate Y	Pin No.	Pad Name	Coordinate X	Coordinate Y	Pin No.	Pad Name	Coordinate X	Coordinate Y
	(DMY23)	4040	–2550	34	X33	4040	850	67	Y66	1600	2900	101	X100	–1800	2900
1	X0	↓	–2450	35	X34	↓	950	68	X67	1500	↓	102	X101	–1900	↓
2	X1	↓	–2350	36	X35	↓	1050	69	X68	1400	↓	103	X102	–2000	↓
3	X2	↓	–2250	37	X36	↓	1150	70	X69	1300	↓	104	X103	–2100	↓
4	X3	↓	–2150	38	X37	↓	1250	71	X70	1200	↓	105	X104	–2200	↓
5	X4	↓	–2050	39	X38	↓	1350	72	X71	1100	↓	106	X105	–2300	↓
6	X5	↓	–1950	40	X39	↓	1450	73	X72	1000	↓	107	X106	–2400	↓
7	X6	↓	–1850	41	X40	↓	1550	74	X73	900	↓	108	X107	–2500	↓
8	X7	↓	–1750	42	X41	↓	1650	75	X74	800	↓	109	X108	–2600	↓
9	X8	↓	–1650	43	X42	↓	1750	76	X75	700	↓	110	X109	–2700	↓
10	X9	↓	–1550	44	X43	↓	1850	77	X76	600	↓	111	X110	–3300	↓
11	X10	↓	–1450	45	X44	↓	1950	78	X77	500	↓	112	X111	–3400	↓
12	X11	↓	–1350	46	X45	↓	2050	79	X78	400	↓	113	X112	–3500	↓
13	X12	↓	–1250	47	X46	↓	2150	80	X79	300	↓	114	X113	–3600	↓
14	X13	↓	–1150	48	X47	↓	2250	81	X80	200	↓	115	X114	–3700	2900
15	X14	↓	–1050	49	X48	↓	2350	82	X81	100	↓		(DMY24)	–4040	2550
16	X15	↓	–950	50	X49	↓	2450	83	X82	0	↓	116	X115	↓	2450
17	X16	↓	–850		(DMY24)	4040	2550	84	X83	–100	↓	117	X116	↓	2350
18	X17	↓	–750	51	X50	3700	2900	85	X84	–200	↓	118	X117	↓	2250
19	X18	↓	–650	52	X51	3600	↓	86	X85	–300	↓	119	X118	↓	2150
20	X19	↓	–550	53	X52	3500	↓	87	X86	–400	↓	120	X119	↓	2050
21	X20	↓	–450	54	X53	3400	↓	88	X87	–500	↓	121	X120	↓	1950
22	X21	↓	–350	55	X54	3300	↓	89	X88	–600	↓	122	X121	↓	1850
23	X22	↓	–250	56	X55	2700	↓	90	X89	–700	↓	123	X122	↓	1750
24	X23	↓	–150	57	X56	2600	↓	91	X90	–800	↓	124	X123	↓	1650
25	X24	↓	–50	58	X57	2500	↓	92	X91	–900	↓	125	X124	↓	1550
26	X25	↓	50	59	X58	2400	↓	93	X92	–1000	↓	126	X125	↓	1450
27	X26	↓	150	60	X59	2300	↓	94	X93	–1100	↓	127	X126	↓	1350
28	X27	↓	250	61	X60	2200	↓	95	X94	–1200	↓	128	X127	↓	1250
29	X28	↓	350	62	X61	2100	↓	96	X95	–1300	↓	129	X128	↓	1150
30	X29	↓	450	63	X62	2000	↓	97	X96	–1400	↓	130	X129	↓	1050
31	X30	↓	550	64	X63	1900	↓	98	X97	–1500	↓	131	X130	↓	950
32	X31	↓	650	65	X64	1800	↓	99	X98	–1600	↓	132	X131	↓	850
33	X32	4040	750	66	X65	1700	2900	100	X99	–1700	2900	133	X132	↓	750

Note: The pin marked by * must be hold V_{CC}.

Pin No.	Pad Name	Coordinate X	Y
134	X133	–4040	650
135	X134	↓	550
136	X135	↓	450
137	X136	↓	350
138	X137	↓	250
139	X138	↓	150
140	X139	↓	50
141	X140	↓	–50
142	X141	↓	–150
143	X142	↓	–250
144	X143	↓	–350
145	X144	↓	–450
146	X145	↓	–550
147	X146	↓	–650
148	X147	↓	–750
149	X148	↓	–850
150	X149	↓	–950
151	X150	↓	–1050
152	X151	↓	–1150
153	X152	↓	–1250
154	X153	↓	–1350
155	X154	↓	–1450
156	X155	↓	–1550
157	X156	↓	–1650
158	X157	↓	–1750
159	X158	↓	–1850
160	X159	↓	–1950
161	X160	↓	–2050
162	X161	↓	–2150
163	X162	↓	–2250
164	X163	↓	–2350
165	X164	↓	–2450
	(DMY21)	–4040	–2550
*	(DMY5)	–3750	–2900

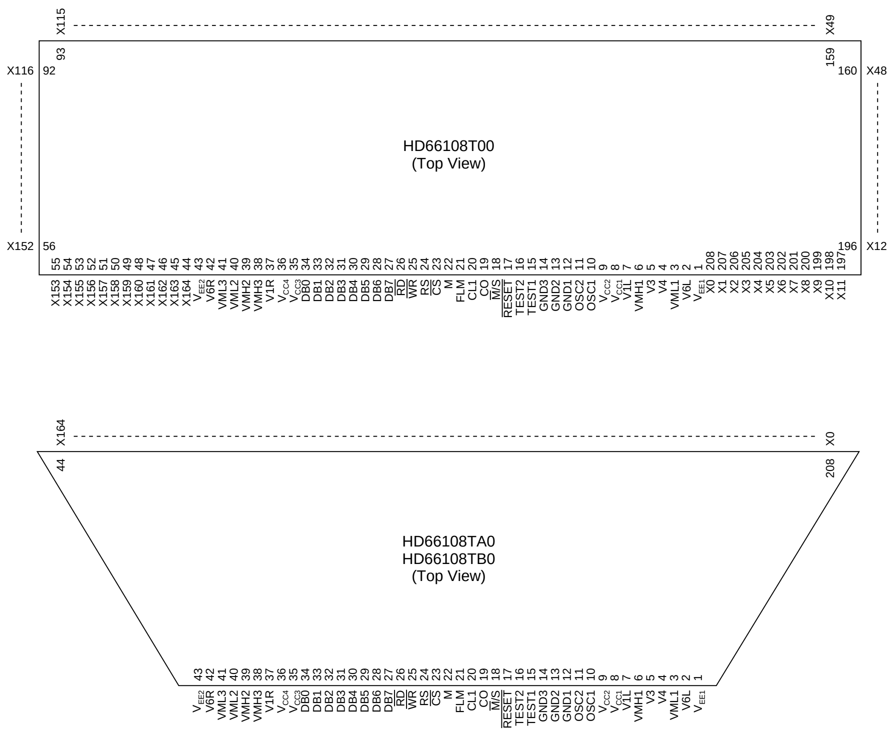
Pin No.	Pad Name	Coordinate X	Y
*	(DMY6)	–3650	–2900
*	(DMY7)	–3550	↓
*	(DMY8)	–3450	↓
*	(DMY9)	–3350	↓
*	(DMY10)	–3250	↓
*	(DMY11)	–3150	↓
*	(DMY12)	–3050	–2900
166	V_{EE2}	–2920	–2872
167	VGR	–2820	↓
168	VML3	–2720	↓
169	VML2	–2620	↓
170	VMH2	–2520	↓
171	VMH3	–2420	↓
172	VIR	–2320	↓
173	V_{CC4}	–2210	–2872
174	V_{CC3}	–2110	–2850
	(V_{CCA})	–2010	↓
175	DB0	–1860	↓
176	DB1	–1660	↓
177	DB2	–1460	↓
178	DB3	–1260	↓
179	DB4	–1060	↓
180	DB5	–860	↓
181	DB6	–660	↓
182	DB7	–460	↓
183	$\overline{RD}$	–285	↓
184	$\overline{WR}$	–155	↓
185	RS	–25	–
186	$\overline{CS}$	105	↓
187	M	250	↓
188	FLM	440	↓
189	CL1	580	↓
190	CO	755	↓
191	MS	900	–2850

Pin No.	Pad Name	Coordinate X	Y
192	$\overline{RESET}$	1030	–2850
193	TEST2	1160	↓
194	TEST1	1290	↓
195	BND3	1400	↓
196	GND2	1500	↓
197	GND1	1600	↓
	(GNDA)	1700	↓
198	OSC2	1815	↓
199	OSC1	1995	↓
200	V_{CC2}	2105	–2850
201	V_{CC1}	2205	–2882
202	VIL	2320	↓
203	VMH1	2420	↓
204	V3	2520	↓
205	V4	2620	↓
206	VML1	2720	↓
207	V6L	2820	↓
208	V_{EE1}	2920	–2882
*	(DMY13)	3050	–2900
*	(DMY14)	3150	↓
*	(DMY15)	3250	↓
*	(DMY16)	3350	↓
*	(DMY17)	3450	↓
*	(DMY18)	3550	↓
*	(DMY19)	3650	↓
*	(DMY20)	3750	–2900

(Unit : µm)

Note: The pin marked by * must be hold V_{CC}.

Pin Arrangement



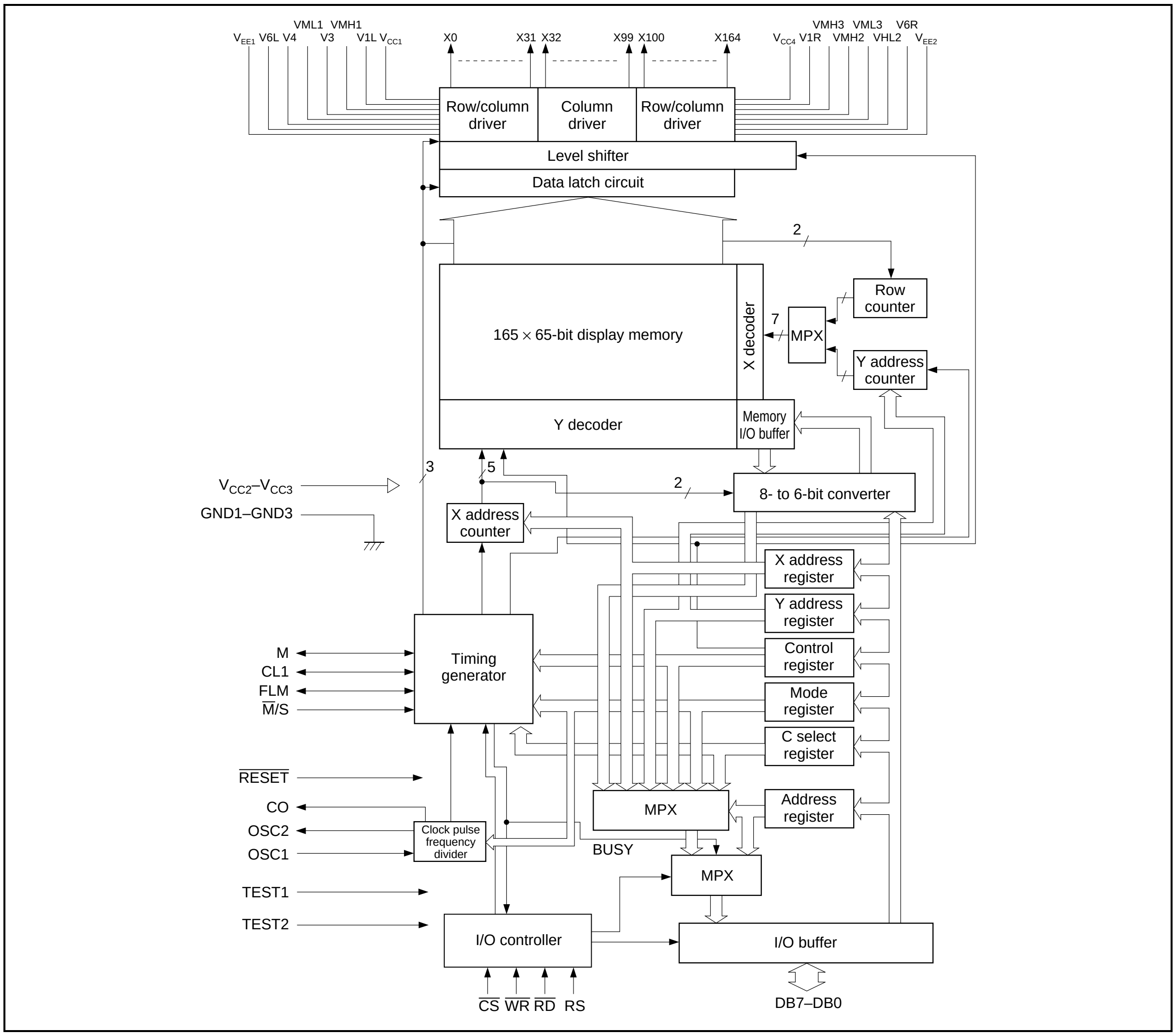
Note : These figures of TCP are not drawn to a scale.

Pin Description

Classification	No. of Pins	Symbol	I/O	No.of Pins	Function
Power supply	8, 9, 35, 36	V_{CC1}–V_{CC4}	—	4	Connect these pins to V_{CC}.
	12 to 14	GND1–GND3	—	3	Ground these pins.
	1, 43	V_{EE1}, V_{EE2}	—	2	These pins supply power to the LCD driving circuits and should usually be set to the V6 level.
	2, 7 37, 42 4, 5 6, 39, 38 3, 40, 41	V6L, V1L, V1R, V6R, V4, V3, VMH1–VMH3, VML1–VML3	—	12	Apply an LCD driving voltage V1 to V6 to these pins.
CPU interface	23	$\overline{CS}$	I	1	Input a chip select signal via this pin. A CPU can access the HD66108T's internal registers only while the $\overline{CS}$ signal is low.
	25	$\overline{WR}$	I	1	Input a write enable signal via this pin.
	26	$\overline{RD}$	I	1	Input a read enable signal via this pin.
	24	RS	I	1	Input a register select signal via this pin.
	27 to 34	DB7–DB0	I/O	8	Data is transferred between the HD66108T and a CPU via these pins.
LCD driving output	44 to 208	X164–X0	O	165	These pins output LCD driving signals. The X0–X31 and X100–X164 pins are column/row common pins and output row driving signals when so programmed. X32–X99 pins are column pins.
LCD interface	21	FLM	I/O	1	This pin outputs a first line marker when the HD66108T is a master chip and inputs the signal when the chip is a slave chip.
	20	CL1	I/O	1	This pin outputs latch clock pulses of display data when the chip is a master chip and inputs clock CL1 pulses when the chip is a slave chip.
	22	M	I/O	1	This pin outputs or inputs an M signal, which converts LCD driving outputs to AC; it outputs the signal when the HD66108T is a master chip and inputs the signal when the chip is a slave chip.

Classification	No.of Pins	Symbol	I/O	No.of Pins	Function
Control signals	10	OSC1	I	1	Input system clock pulses via this pin.
	11	OSC2	O	1	This pin outputs clock pulses generated by the internal CR oscillator.
	19	CO	O	1	This pin outputs the same clock pulses as the system clock pulses. Connect with the OSC1 pin of a slave chip.
	18	$\overline{\text{M}}$/S	I	1	This pin specifies master/slave. Set this pin low when the HD66108T is a master chip and set high when the chip is a slave chip; must not be changed after power-on.
	17	$\overline{\text{RESET}}$	I	1	Input a reset signal via this pin. Setting this pin low initializes the HD66108T.
	15, 16	TEST1, TEST2	I	2	These pins input a test signal and must be set low.

Internal Block Diagram



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Register List

CS	RS	Reg. No. 2	1	0	Reg. Symbol	Register Name	Read/ Write	Data Bit Assignment 7	6	5	4	3	2	1	0	Busy Time	Notes
1	—	—	—	—	—	Invalid	—									—	1
0	0	—	—	—	AR	Address	R	Busy	STBY	DISP			Register No.			None	
							W										
0	1	0	0	0	DRAM	Display memory	R	D7	D6	D5	D4	D3	D2	D1	D0	8 clocks max	2
							W										3
0	1	0	0	1	XAR	X address	R				XAD					None	
							W									1.5 clocks max	
0	1	0	1	0	YAR	Y address	R		YAD							None	
							W									1.5 clocks max	
0	1	0	1	1	FCR	Control	R	INC	WLS	PON	ROS		DUTY			None	
							W										
0	1	1	0	0	MDR	Mode	R				FFS			DWS		None	
							W										
0	1	1	0	1	CSR	C select	R			EOR	CLN					None	
							W										
0	1	1	1	0	—	Invalid	—									—	
0	1	1	1	1	—	Invalid	—									—	

Notes:
1. Shaded bits are invalid. Writing 1 or 0 to invalid bits does not affect LSI operation. Reading these bits returns 0.
2. DRAM is not actually a register but can be handled as one.
3. Setting the WLS bit of control register to 1 invalidates D7 and D6 bits of the display memory register.
4. DRAM must not be written to or read from until a time period of t_{CL1} has elapsed rewriting the DUTY bit of FCR or the FFS bit of MDR. t_{CL1} can be obtained from the following equation; in general, a time period of 1 ms or greater is sufficient if the frame frequency is 60–90 Hz.

$$t_{CL1} = \frac{D2}{Ni \cdot f_{CLK}(kHz)} (ms) \text{ .... Equation}$$

D2 (duty correction value): 192 (duty = 1/32, 1/34, or 1/36)
128 (duty = 1/48 or 1/50)
96 (duty = 1/64 or 1/66)

Ni (frequency-division ratio specified by the mode register's FFS bits):
2, 1, 1/2, 1/3, 1/4, 1/6, or 1/8
Refer to "6. Clock and Frame Frequency."

f_{CLK}: Input clock frequency (kHz)

System Description

The HD66108T can assign a maximum of 65 out of 165 channels to row outputs for LCD driving. It also incorporates a timing generator and display memory, which are necessary to drive an LCD.

If connected to an MPU and supplied with LCD driving voltage, one HD66108T chip can be used to configure an LCD system with a 100 × 65 dot panel (Figure 1). In this case, clock pulses should be supplied by the internal CR oscillator or the MPU.

Using LCD expansion signals CL1, FLM and M enables the display size to be expanded. In this case, LCD expansion signal pins output corresponding signals when pin $\overline{M}$/S is set low for master mode and conversely input corresponding signals when pin $\overline{M}$/S is set high for slave mode; LCD expansion signal pins of both master chip and slave chips must be mutually connected. Figure 2 shows a basic system configuration using two HD66108T chips.

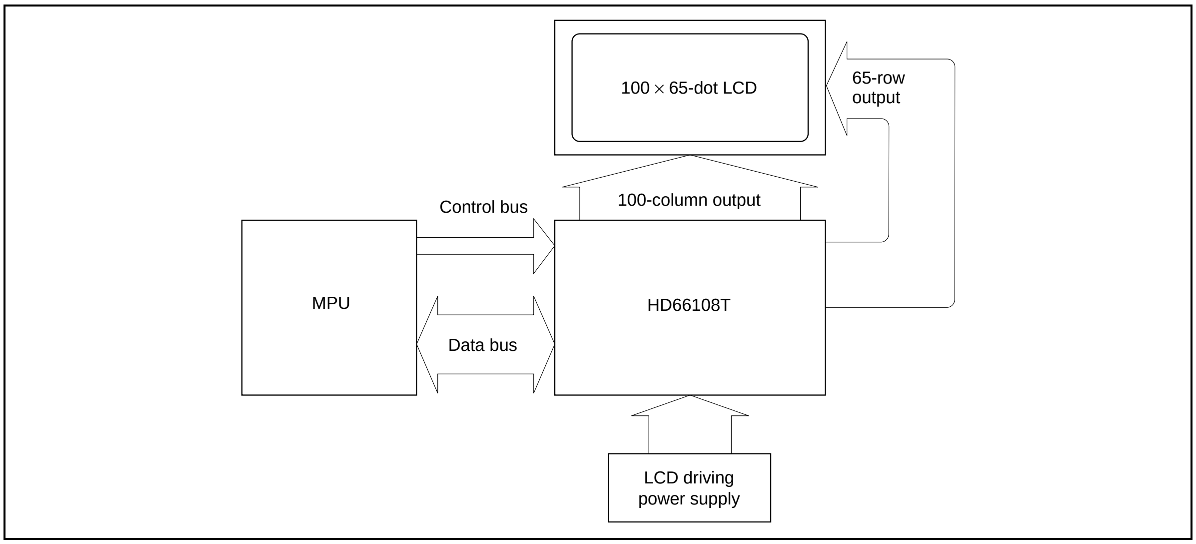


Figure 1 Basic System Configuration (1)

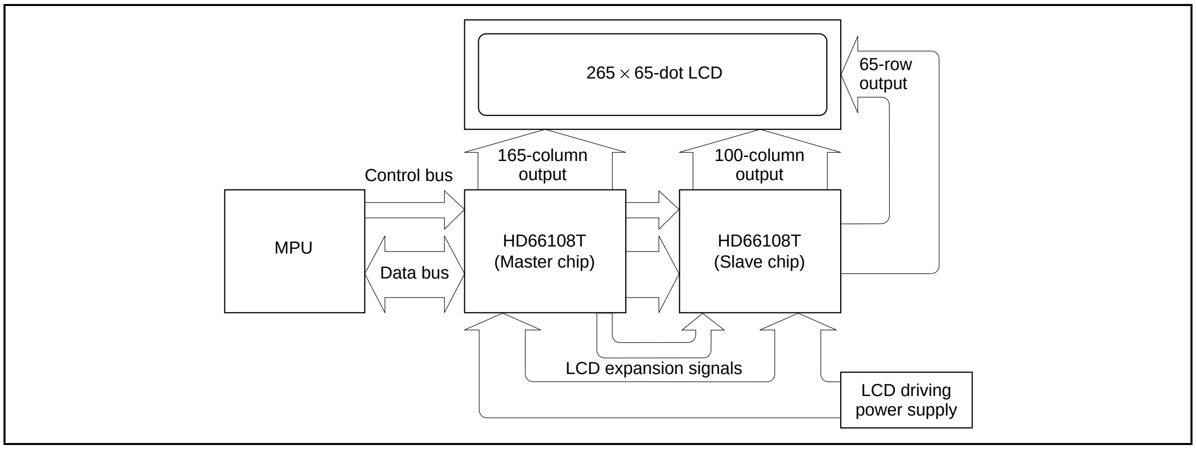


Figure 2 Basic System Configuration (2)

Functional Description

1. Display Size Programming

A variety of display sizes can be programmed by changing the system configuration and internal register settings.

(1) System Configuration Using One HD66108T Chip

When the 65-row-output mode is selected by internal register settings, a maximum of 100 dots in the X direction can be displayed (Figure 3 (a)). Display size in the Y direction can be selected from 32, 34, 36, 48, 50, 64, and 65 dots according to display duty setting. Note that Y direction settings does not affect those in the X direction (100 dots).

When the 33-row-output mode is selected by internal register settings, a maximum of 132 dots in the X direction can be displayed (Figure 3 (b)).

Table 1 shows the relationship between display sizes and the control register's (FCR) ROS and DUTY bits. ROS and DUTY bit settings determine the function of X pins. For more details, refer to "4.1 Row Output Pin Selection."

(2) System Configuration Using One HD66108T Chip and One HD61203 Chip as Row Driver

A maximum of 64 dots in the Y direction and 165 dots in the X direction can be displayed. 48 or 64 dots in the Y direction can be selected by HD61203 pin settings (Figure 3 (c)).

(3) System Configuration Using Two or more HD66108T Chips

X direction size can be expanded by 165 dots per chip. Figure 3 (d) shows a 265 × 65-dot display. Y direction size can be expanded up to 130 dots with 2 chips; a 100 × 130-dot display provided by 2 chips is shown in Figure 3 (e).

Table 1 Relationship between Display Size and Register Settings (No. of Dots)

ROS Bit Setting (X0–X164 Pin Function)	Duty Bit Setting (Multiplexing Duty Ratio)						
	1/32	1/34	1/36	1/48	1/50	1/64	1/66
165-column-output	Specified by a row driver						
65-row-output from the right side	X: 100 Y: 32	X: 100 Y: 34	X:100 Y: 36	X: 100 Y: 48	X: 100 Y: 50	X: 100 Y: 64	X:100 Y: 65
65-row-output from the left and right sides	X: 100 Y: 32	X: 100 Y: 34	X:100 Y: 36	X: 100 Y: 48	X: 100 Y: 50	X: 100 Y: 64	X:100 Y: 65
33-row-output from the right side	X: 132 Y: 32	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33	X: 132 Y: 33

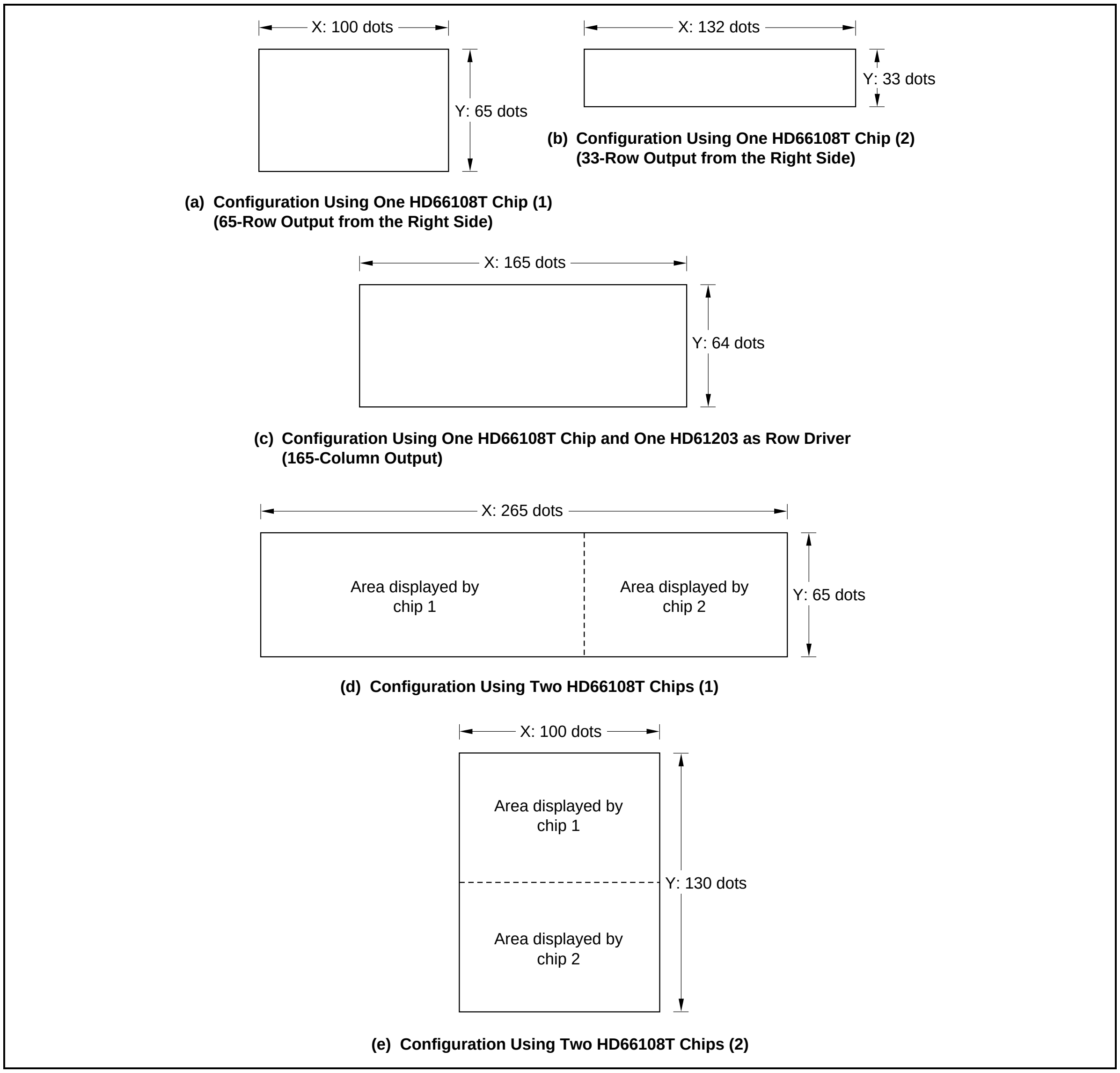


Figure 3 Relationship between System Configurations and Display Sizes

2. Display Memory Construction and Word Length Setting

The HD66108T has a bit-mapped display memory of 165 × 65 bits. As shown in Figure 4, data from the MPU is stored in the display memory, with the MSB (most significant bit) on the left and the LSB (least significant bit) on the right.

The sections on the LCD panel corresponding to the display memory bits in which 1's are written will be displayed as on (black).

Display area size of the internal RAM is determined by control register (FCR) settings (refer to Table 1).

The start address in the Y direction for the display area is always Y0, independent of the register setting. In contrast, the start address in the X direction is X0 in the modes for 165-column-output, 65-row-output from the right side, and 33-row-output from the right side, and is X32 in the 65-row-output mode from the left and right sides.

Each display area contains the number of dots shown in Table 1, beginning from each start address.

For more detail, refer to "4.2 Row Output Data Setting," Figures 15 to 19.

In the display memory, one X address is assigned to each word of 8 or 6 bits long in X direction. (Either 8 or 6 bits can be selected as word length of display data.) Similarly, one Y address is assigned to each row in Y direction.

Accordingly, X address 20 in the case of 8-bit word and X address 27 in the case of 6-bit word have 5 and 3 bits of display data, respectively. Nevertheless, data is also stored here with the MSB on the left (Figure 5).

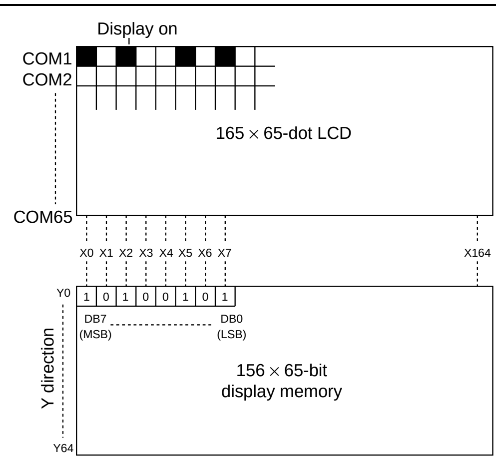


Figure 4 Relationship between Memory Construction and Display

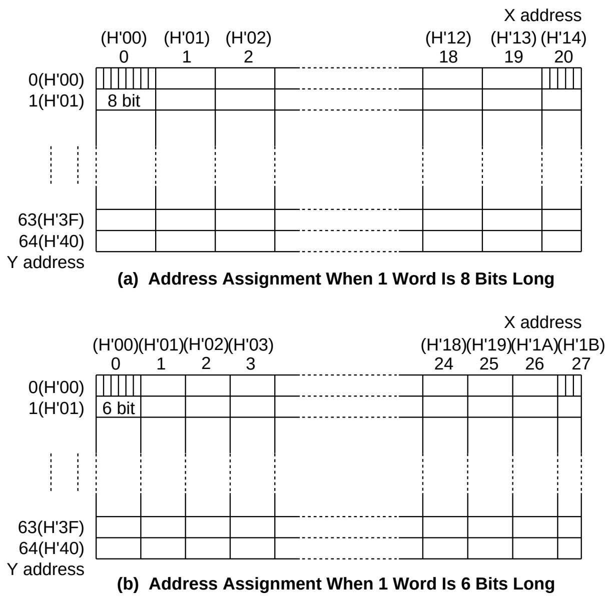


Figure 5 Display Memory Addresses

3. Display Data Write

3.1 Display Memory and Data Register Accesses

(1) Access

Figure 6 shows the relationship between the address register (AR) and internal registers and display memory in the HD66108T. Display memory shall be referred to as a data register since it can be handled as other registers.

To access a data register, the register address assigned to the desired register must be written into the address register's Register No. bits. The MPU will access only that register until the register address is updated.

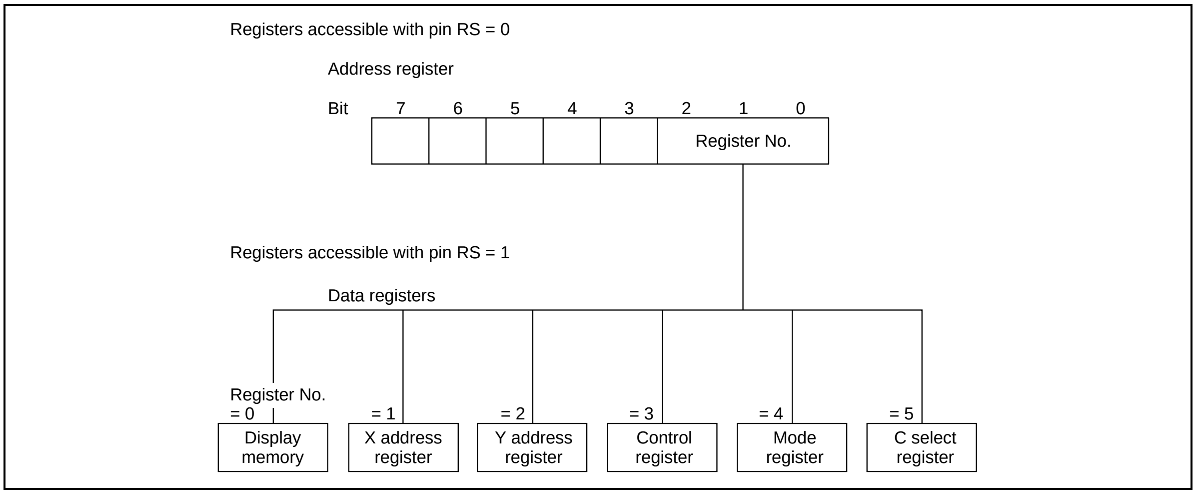


Figure 6 Relationship between Address Register and Register No.

(2) Busy Check

A busy time period appears after display memory read/write or X or Y address register write, since post-access processing is performed synchronously with internal clock pulses. Updating data in registers other than the address register is disabled during this time. Subsequent data must be input after confirming ready mode by reading the address register. The busy time period is a maximum of 8 clock pulses after display memory read/write and a maximum of 1.5 clock pulses after X or Y address register write (Figure 7).

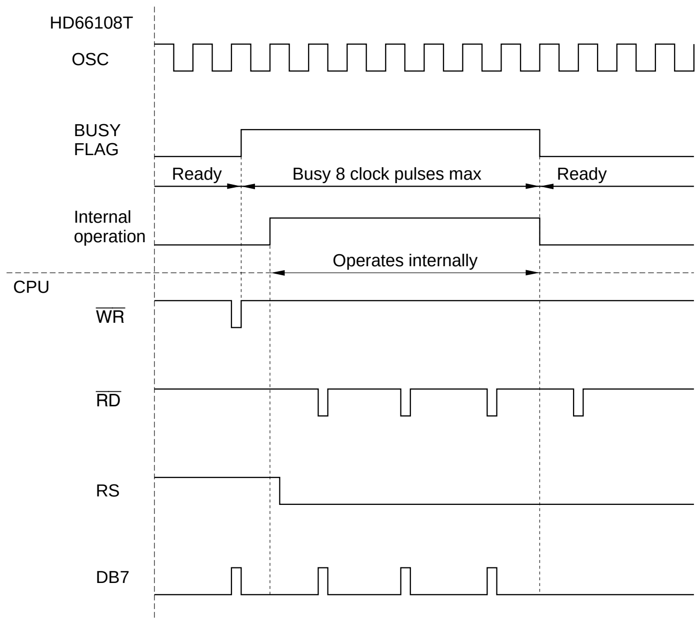


Figure 7 Relationship between Clock Pulses and Busy Time (Updating Display Data)

(3) Dummy Read

When reading out display data, the data which is read out immediately after setting the X and Y addresses is invalid. Valid data can be read out after one dummy read, which is performed after setting the X and Y addresses desired (Figure 8).

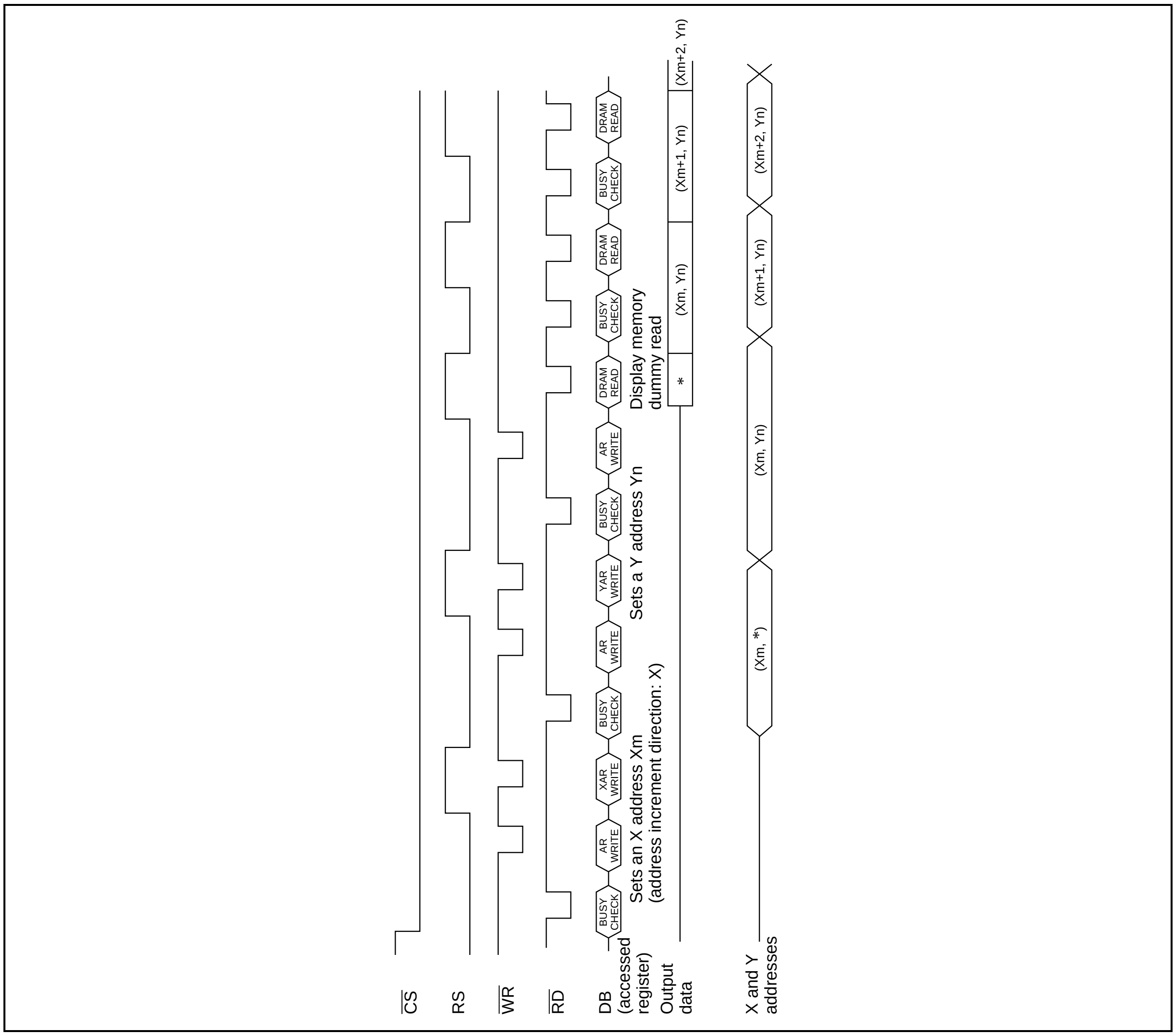


Figure 8 Display Memory Reading

(4) Limitations on Access

As shown in Figure 9, the display memory must not be rewritten until a time period of t_{CL1} or longer has elapsed after rewriting the control register's DUTY bits or the mode register's FFS bits. However, display memory and registers other than the control register and mode register can be accessed even during this time period. t_{CL1} can be obtained from the following equation. If using an LSI with a frame frequency of 60 Hz or greater, a time period of 1 ms should be sufficient.

$$t_{CL1} = \frac{D2}{Ni \cdot f_{CLK}(kHz)} \text{ (ms) ...... Equation 1}$$

D2 (duty correction value):

192 (duty = 1/32, 1/34, or 1/36)

128 (duty = 1/48 or 1/50)

96 (duty = 1/64 or 1/66)

Ni (frequency-division ratio specified by the mode register's FFS bits):

2, 1, 1/2, 1/3, 1/4, 1/6, or 1/8

f_{CLK}: Input clock frequency (kHz)

3.2 X and Y address Counter Auto-Incrementing Function

As described in "2. Display Memory Construction and Word Length Setting," the HD66108T display memory has X and Y addresses. Internal X address counter and Y address counter both employ an auto-incrementing function. After display data is read or written, the X or Y address is incremented according to the address increment direction selected by internal register.

Although X addresses up to 20 are valid when 8 bits make up one word (up to 27 when 6 bits make up one word), the X address counter can count up to 31 since it is a 5-bit free counter. Similarly, although Y addresses up to 64 are valid, the Y address counter can count up to 127. Consequently, X or Y address must be reset at an appropriate point as shown in Figure 10.

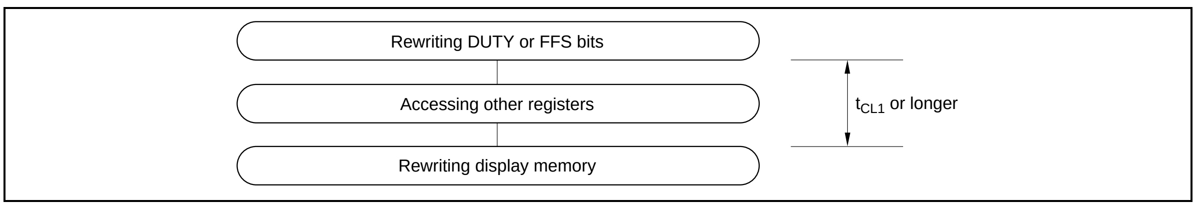


Figure 9 Rewriting Display Memory after Rewriting Registers

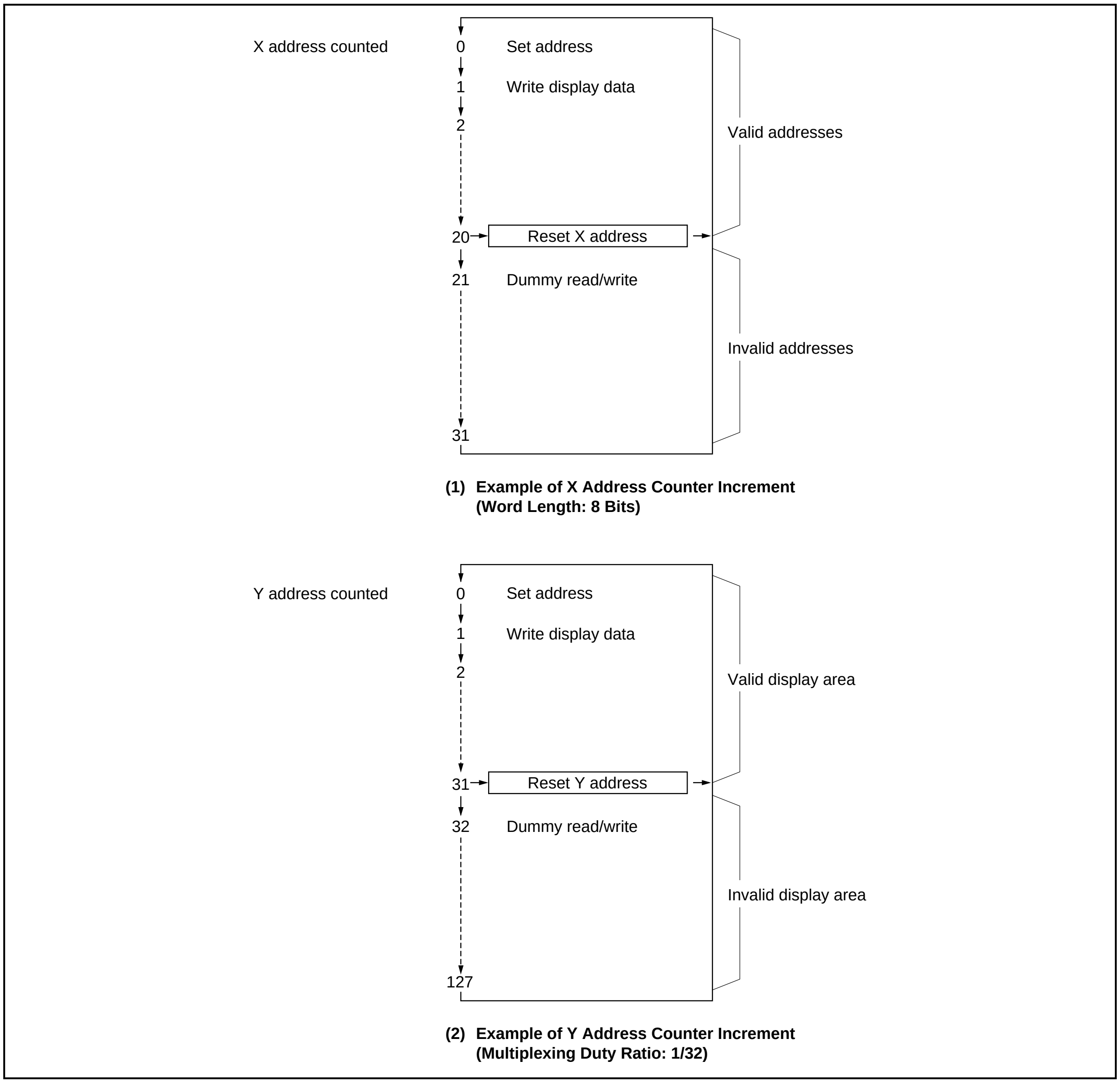


Figure 10 X/Y Address Counter Increment

4. Selection for LCD Driving Circuit Configuration

4.1 Row Output Pin Selection

The HD66108T can assign a maximum of 65 pins for row outputs among the 165 pins named X0–X164. The X0–X164 pins can be classified into four blocks labelled A, B, C, and D (Figure 11 (a)). Blocks A, C, and D consist of row/column common pins and block B consists of column pins only. The output function of the LCD driving pins and the combination of blocks can be selected by internal registers.

Figure 11 shows an example of 165-column-output mode. This configuration is useful when using more than one HD66108T chip or using the HD66108T as a slave chip of the HD61203U.

Figure 12 shows an example of 65-row-output mode from the right side. Blocks A and B are used for column output and blocks C and D (X100–X164 pins) for row output. This configuration offers an easy way of connecting row output lines in the case of using one or more HD66108T chips.

Figure 13 shows an example of 65-row-output mode from the left and right sides. 32 pins of X0–X31 and 33 pins of X132–X164 are used for row output here. This configuration offers an easy way of connecting row output lines in the case of using only one HD66108T chip.

Figure 14 shows an example of 33-row-output mode from the right side. Block D, i.e., X132–X164 pins, is used for row outputs. This configuration provides a means for assigning many pins to column outputs when 1/32 or 1/34 multiplexing duty ratio is desired.

In all modes, it is row data and multiplexing duty ratio that determine which pins are actually used among the pins assigned to row output. Y values shown in Table 1 indicate the numbers of pins that are actually used. Pins not used must be left disconnected.

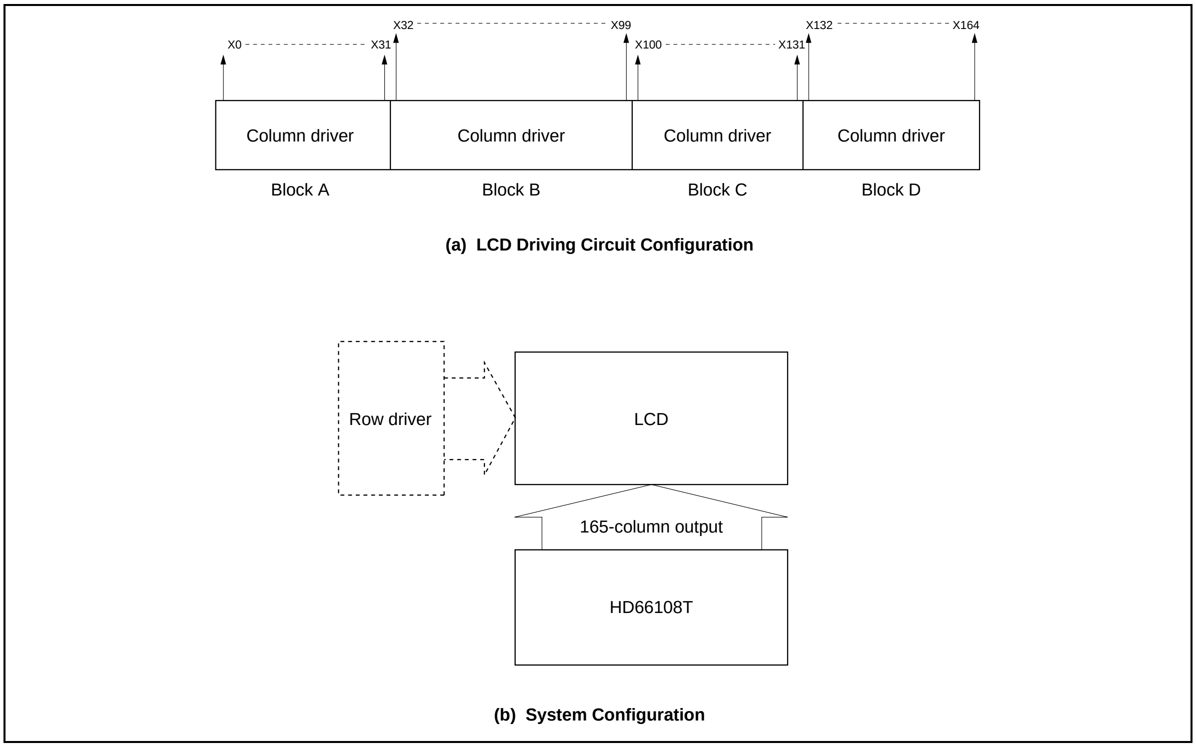


Figure 11 165-Column-Output Mode

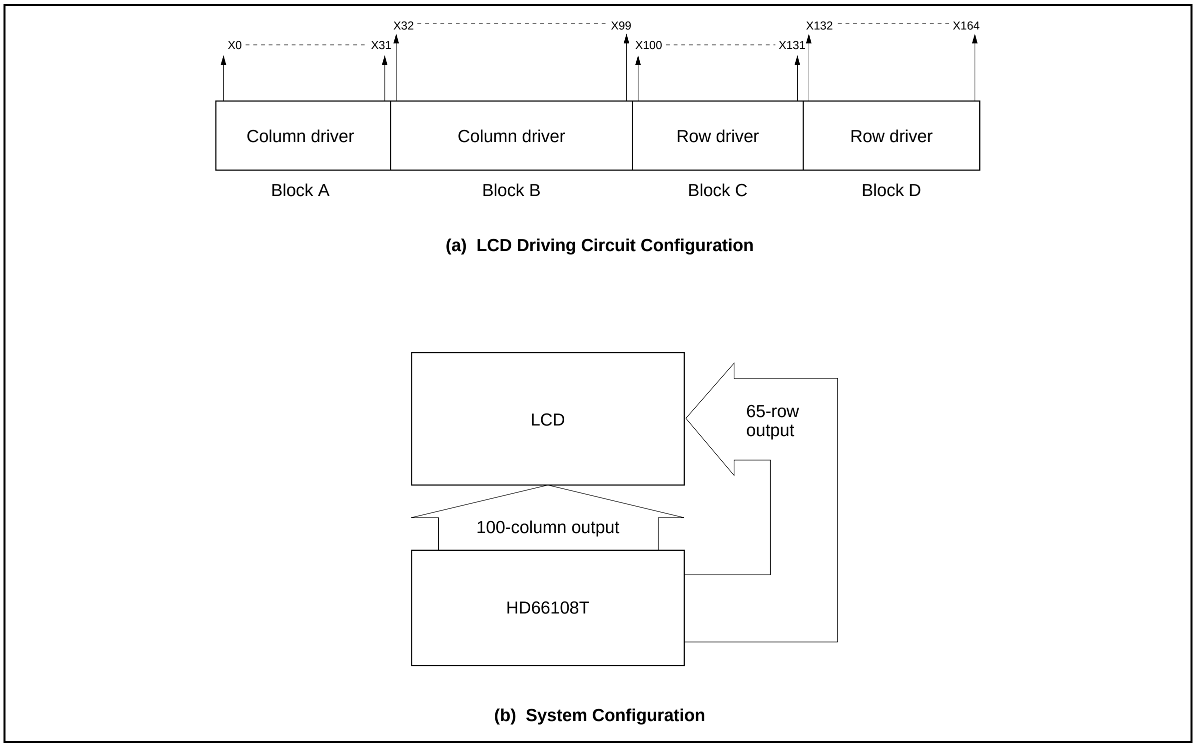
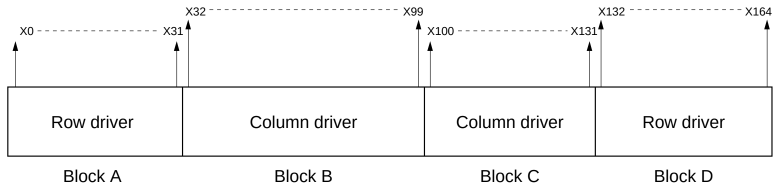
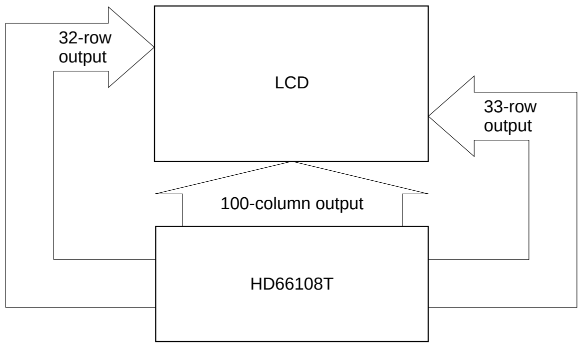


Figure 12 65-Row-Output Mode from the Right Side



(a) LCD Driving Circuit Configuration



(b) System Configuration

Figure 13 65-Row-Output Mode from the Left and Right Sides

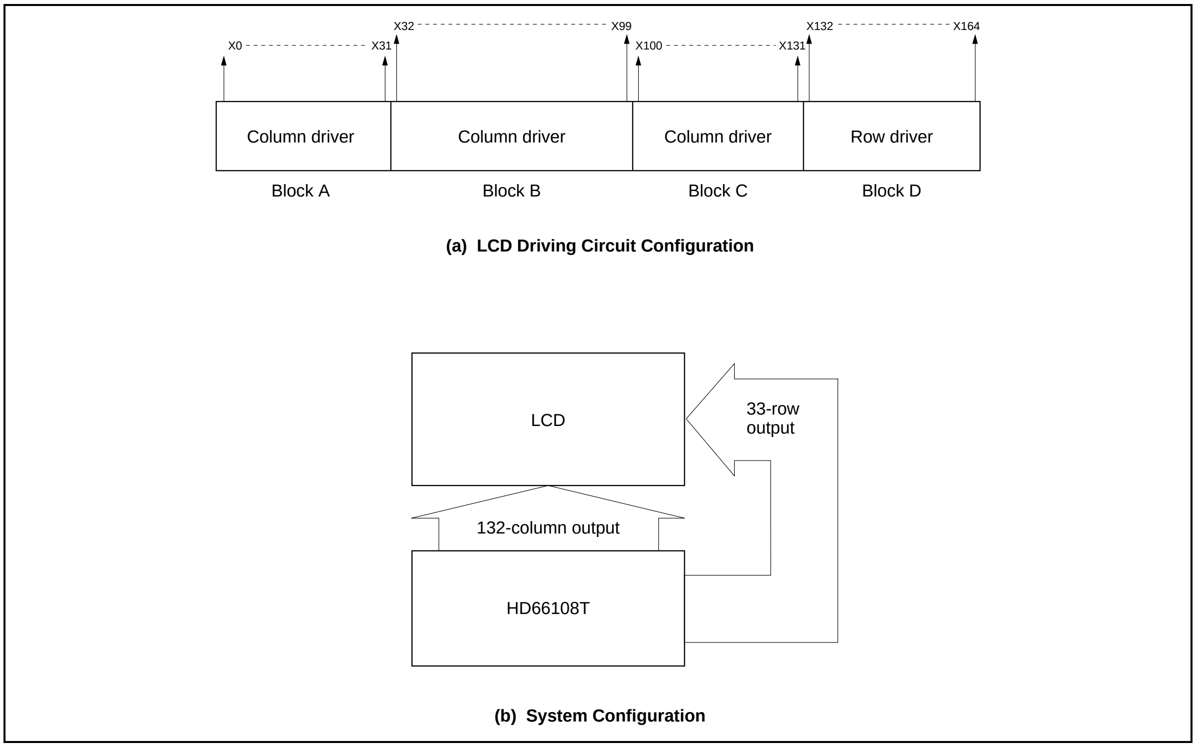


Figure 14 33-Row-Output-Mode from the Right Side

4.2 Row Output Data Setting

If certain LCD driving output pins are assigned to row output, data must be written to display memory for row output. The specific area to which this data must be written depends on the row-output mode and the procedure of writing row data to the display memory (0 or 1 to which bits?) depends on which X pin drives which line of the LCD. Row data area is determined by the control register's (FCR) ROS and DUTY bits and is identical to the protected area, which will be described below. (165-column-output mode has no protected area, thus requiring no row data to be written (Figure 15).)

Procedure of writing row data to the display memory is as follows. First, 1 must be written to the bit at the intersection between line Yj and line (column) Xi (column). Line Yj is filled with data to be displayed on the first line of the LCD and line Xi is connected to pin Xn, which drives the first line of the LCD. Following this, 0s must be written to the remaining bits on line Yj in the row data area. This rule applies to subsequent lines on the LCD.

Table 2 shows the relationship between FCR settings and protected areas.

Figure 16 shows the relationship between row data and display. Here the mode is 65-row output from the right side. Display data on Y0 is displayed on the first line of the LCD and data on Y64 is displayed on the 65th line of the LCD. If X164 is connected to the first line of the LCD and X100 is connected to the 65th line of the LCD, 1s must be written to the bits on the diagonal line between coordinates (X164, Y0) and (X100, Y64) and 0s to the remaining bits. Row data protect function must be turned off before writing row data and be turned on after writing row data. Turning on the row data protect function disables read/write of display memory area corresponding to the row output pins, i.e., prevents row data from being destroyed. In Figure 16, display memory area corresponding to pins X100 to X164 is protected.

Figures 17 to 19 show examples of row data settings. Some multiplexing duty ratios result in invalid display areas. Although an invalid display area can be read from or written to, it will not be displayed.

Table 2 Relationship between FCR Settings and Protected Areas

Control Register (FCR)					
	ROS				
PON	4	3	Mode	LCD Driving Signal Output Pins Connected to Protected Area of Display Memory	Figures
1	0	0	165-column	No area protected	15
1	0	1	65-row (R)	X100–X164	16, 19
1	1	0	65-row (L/R)	X0–X31 and X132–X164	17
1	1	1	33-row (R)	X132–X164	18

65-row (R) : 65-row-output mode from the right side
65-row (L/R): 65-row-output mode from the left and right sides
33-row (R): 33-row-output mode from the right side

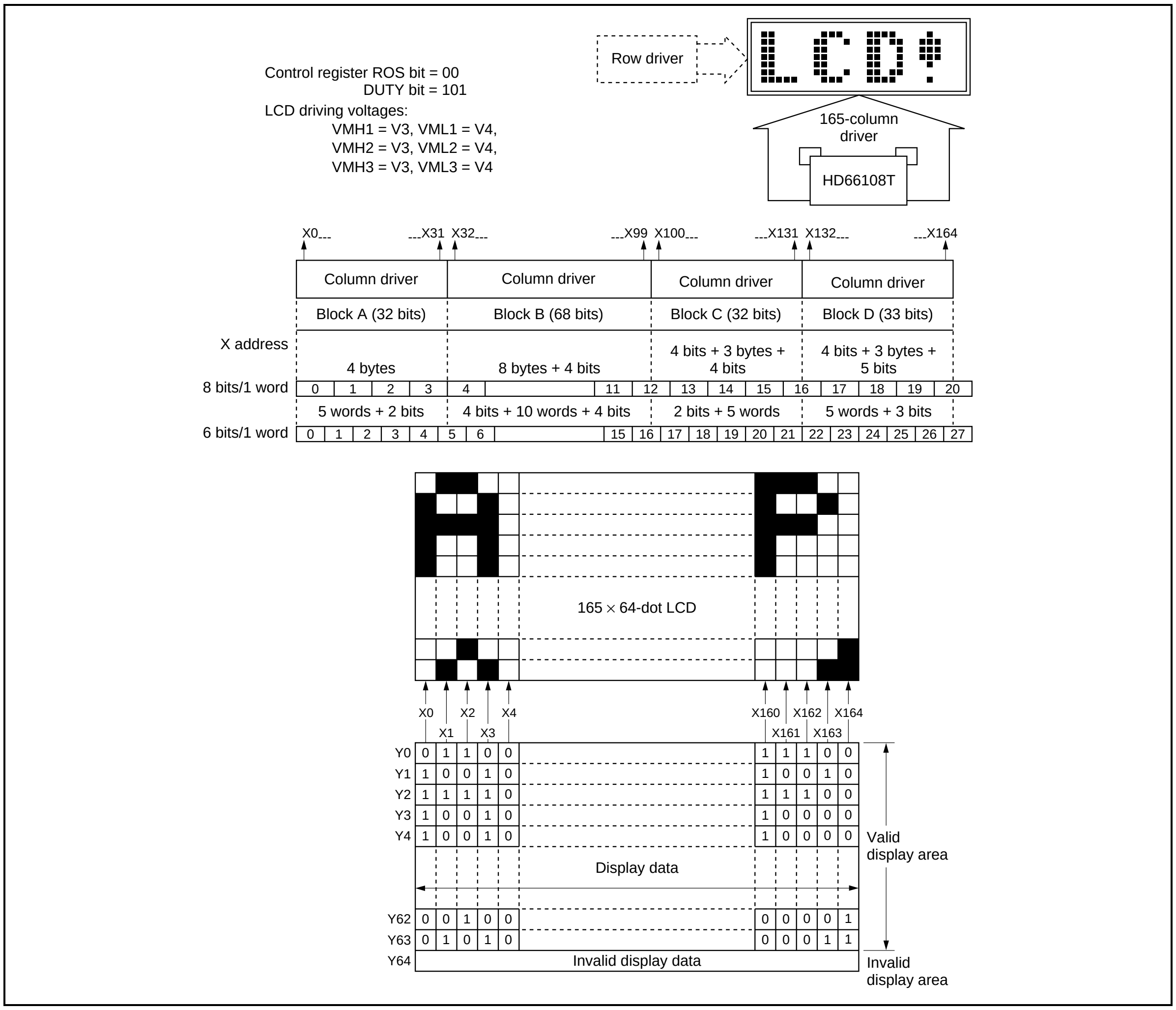


Figure 15 Relationship between Row Data and Display (165-Column Output, 1/64 Multiplexing Duty Ratio)

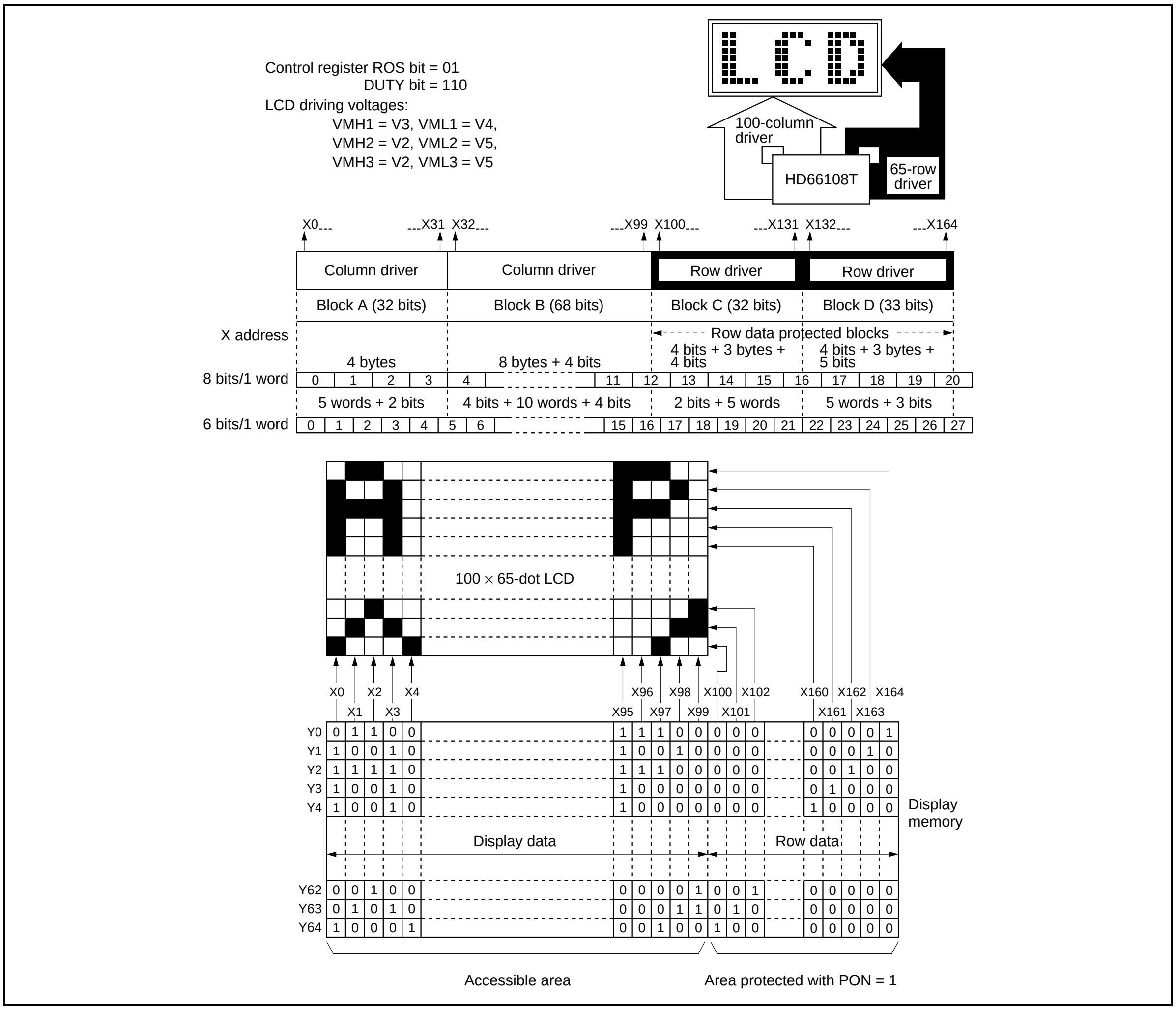


Figure 16 Relationship between Row Data and Display (65-Row Output from the Right Side, 1/66 Multiplexing Duty Ratio)

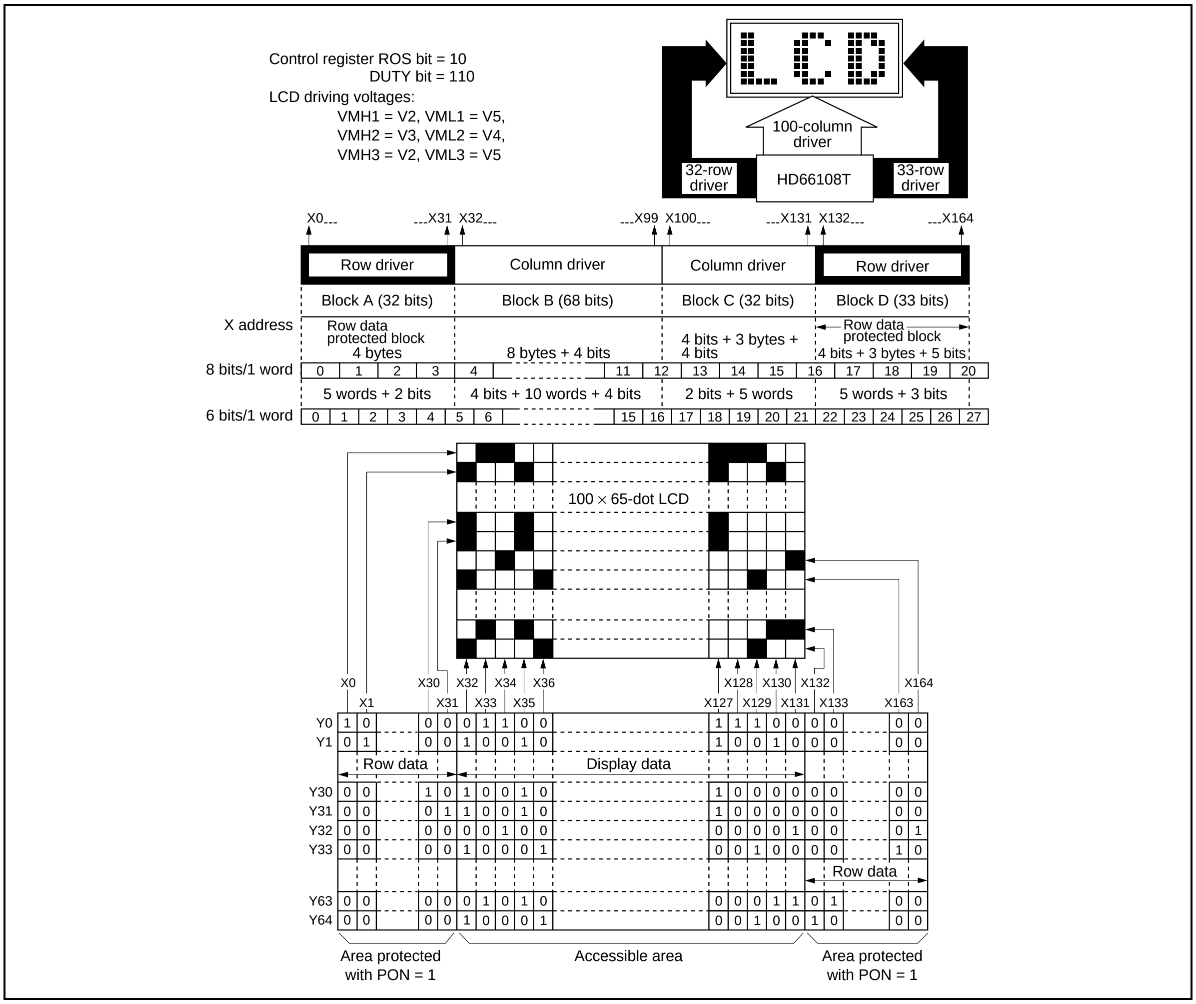


Figure 17 Relationship between Row Data and Display (65-Row Output from the Left and Right Sides, 1/66 Multiplexing Duty Ratio)

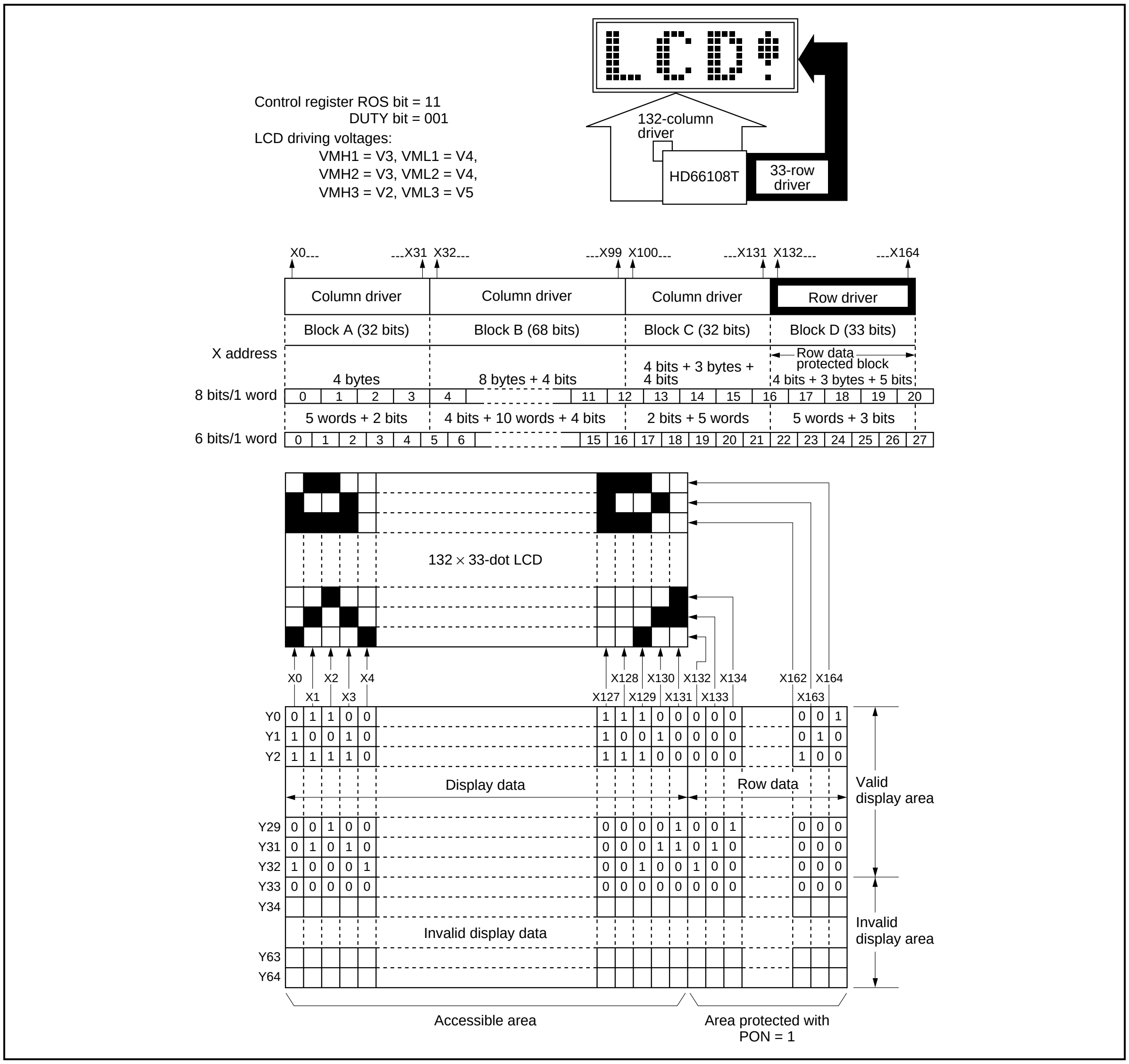


Figure 18 Relationship between Row Data and Display (33-Row Output from the Right Side, 1/34 Multiplexing Duty Ratio)

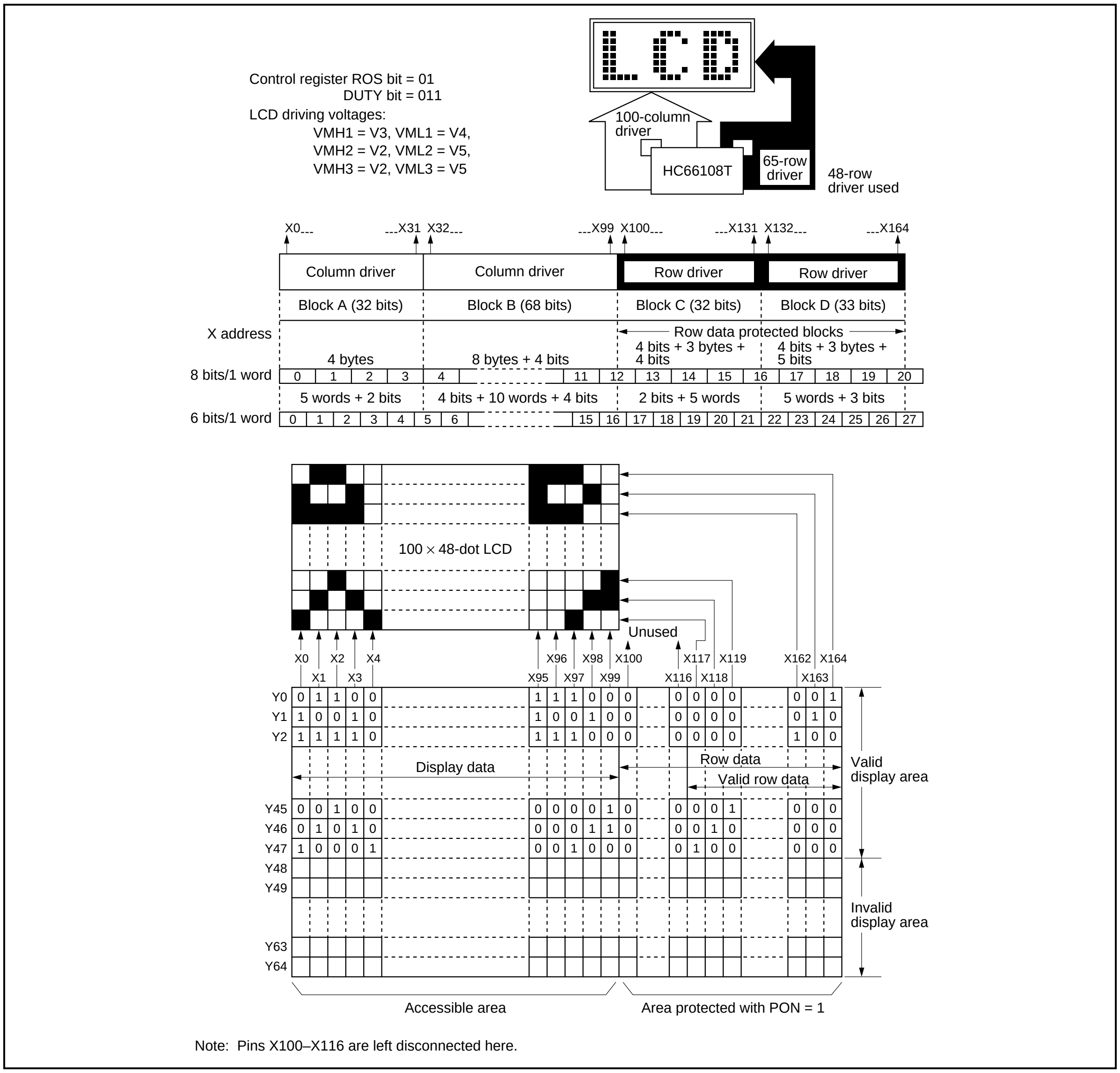


Figure 19 Relationship between Row Data and Display (65-Row Output from the Right Side, 1/48 Multiplexing Duty Ratio)

4.3 LCD Driving Voltage Setting

There are 6 levels of LCD driving voltages ranging from V1 to V6; V1 is the highest and V6 is the lowest. As shown in Figure 20, column output waveform is made up of a combination of V1, V3, V4, and V6 while row output waveform is made up of V1, V2, V5, and V6. This means that V1 and V6 are common to both waveforms while mid-voltages are different.

To accommodate this situation, each block of the HD66108T is provided with power supply pins for mid-voltages as shown in Figure 21. Each pair of V1R and V1L and V6R and V6L are internally connected and must be applied the same level of voltage. Block B is fixed for column output and must be applied V3 and V4 as mid-voltages. The other blocks must be applied different levels of voltages according to the function of their LCD driving output pins; if the LCD driving output pins are set for row output, VMHn and VMLn must be applied V2 and V5, respectively, while they must be applied V3 and V4, respectively, if the pins are set for column output (n = 1 to 3).

Table 3 Relationship between FCR Settings and LCD Driving Voltages

Control Register (FCR)			LCD Driving Voltage Pins									
ROS4	ROS3	Mode	VIR/VIL	V3	V4	VMH1	VML1	VMH2	VML2	VMH3	VML3	V6R/V6L
0	0	165-column	V1	V3	V4	V3	V4	V3	V4	V3	V4	V6
0	1	65-row (R)	V1	V3	V4	V3	V4	V2	V5	V2	V5	V6
1	0	65-row (L/R)	V1	V3	V4	V2	V5	V3	V4	V2	V5	V6
1	1	33-row (R)	V1	V3	V4	V3	V4	V3	V4	V2	V5	V6

65-row (R): 65-row-output mode from the right side

65-row (L/R): 65-row-output mode from the left and right sides

33-row (R): 33-row-output mode from the right side

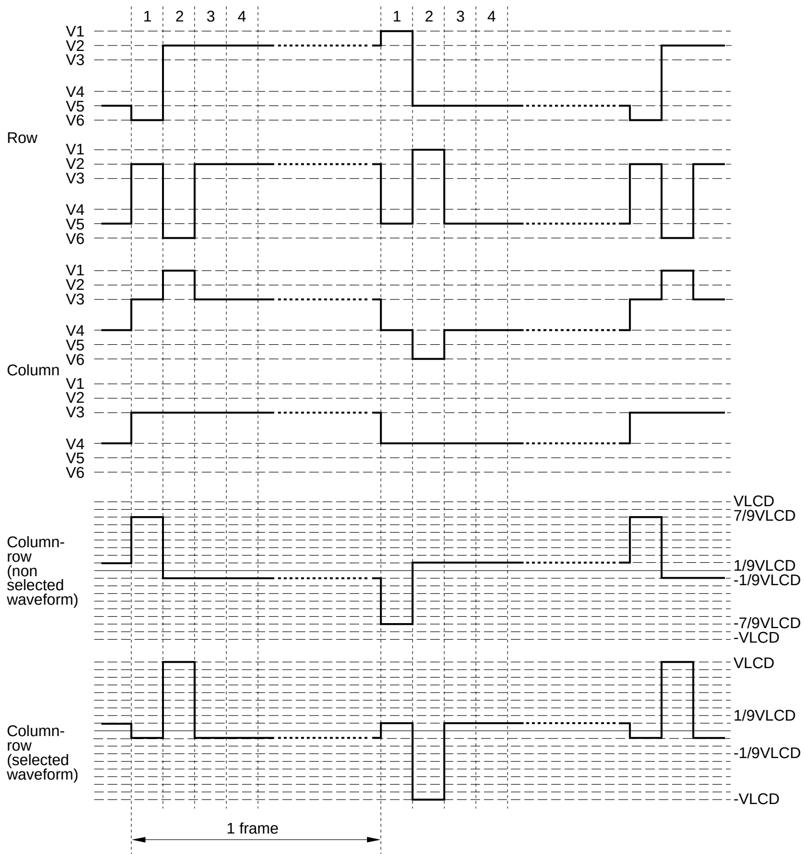


Figure 20 LCD Driving Voltage Waveforms

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5. Multiplexing Duty Ratio and LCD Driving Waveform Settings

A multiplexing duty ratio and LCD driving waveform can be selected via internal registers.

A multiplexing duty ratio of 1/32, 1/34, 1/36, 1/48, 1/50, 1/64, or 1/66 can be selected according to the LCD panel used. However, since there are only 65 row-output pins, only 65 lines will be displayed even if 1/66 multiplexing duty ratio is selected.

There are three types of LCD driving waveforms, as shown in Figure 22: A-type waveform, B-type waveform, and C-type waveform.

The A-type waveform is called per-half-line inversion. Here, the waveforms of M signal and CL1 signal are the same and alternate every LCD line.

The B-type waveform is called per-frame inversion; in this case, the M signal inverts its polarity every frame so as to alternate every two LCD frames. This is the most common type.

The C-type waveform is called per-n-line inversion and inverts its polarity every n lines (n can be set as needed within 1 to 31 via the internal registers). The C-type waveform combines the advantages of the A- and B-types of waveforms. However, some lines will not be alternated depending on the multiplexing duty ratio and n. To avoid this, another C-type waveform is available which is generated from the EOR of the C-type waveform M signal mentioned above and the B-type waveform M signal. Since the relationship between n and display quality usually depends on the LCD panel, n must be determined by observing actual display results.

The B-type waveform should be used if the LCD panel specifies no particular type of waveform. However, in some cases, the C-type waveform may create a better display.

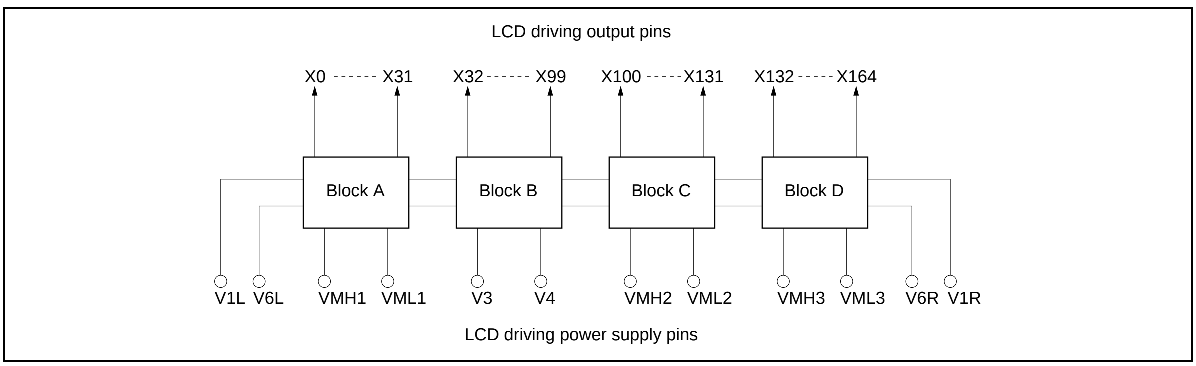


Figure 21 Relationship between Blocks and LCD Driving Voltages

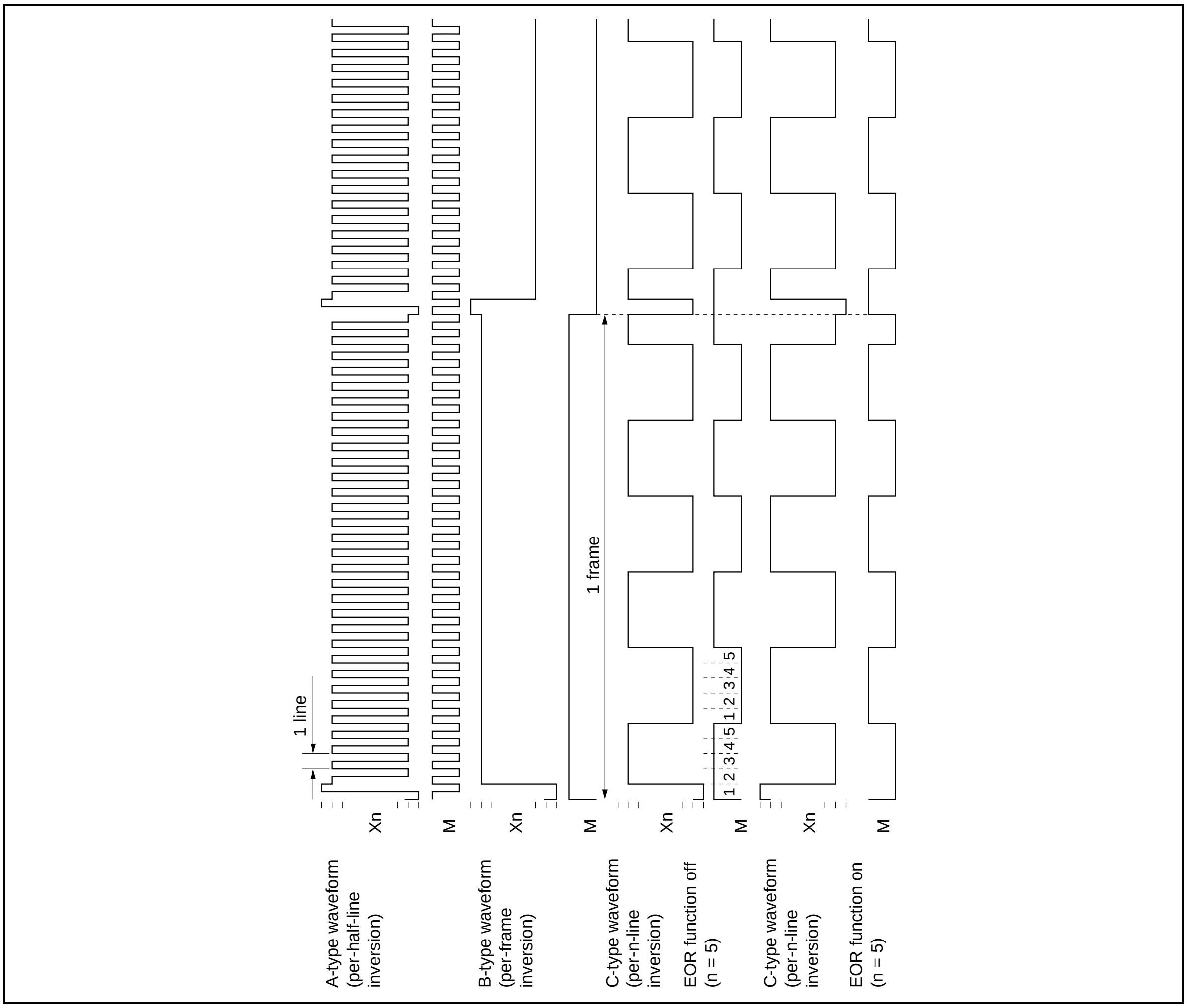


Figure 22 LCD Driving Waveforms (Row Output with a 1/32 Multiplexing Duty Ratio)

6. Clock and Frame Frequency

An input clock with a 200-kHz to 4-MH frequency can be used for the HD66108T. Note that raising clock frequency increases current consumption although it reduces busy time and enables high-speed operations. An optimum system clock frequency should thus be selected within 200 kHz to 4 MHz.

The clock frequency driving the LCD panel (= frame frequency) is usually 70 Hz to 90 Hz. Accordingly, the HD66108T is so designed that the frequency-division ratio of the input clock can be selected. The HD66108T generates around 80-Hz LCD frame frequency if the frequency-division ratio is 1. The frequency-division ratio can be obtained from the following equation.

$$Ni = \frac{f_F}{f_{CLK}} \times \frac{500}{80} \times D1$$

Ni: Frequency-division ratio
f_F: Frame frequency required for the LCD panel (Hz)
f_{CLK}: Input clock frequency (kHz)
D1: Duty correction value 1
D1 = 1 when multiplexing duty ratio is 1/32, 1/48 or 1/64
D1 = 32/34 when multiplexing duty ratio is 1/34
D1 = 32/36 when multiplexing duty ratio is 1/36
D1 = 48/50 when multiplexing duty ratio is 1/50
D1 = 64/66 when multiplexing duty ratio is 1/66

The frequency-division ratio nearest the value obtained from the above equation must be selected; selectable frequency-division ratios by internal registers are 2, 1, 1/2, 1/3, 1/4, 1/6, and 1/8.

7. Display Off Function

The HD66108T has a display off function which turns off display by rewriting the contents of the internal register. This prevents random display at power-on until display memory is initialized.

8. Standby Function

The HD66108T has a standby function providing low-power dissipation. Writing a 1 to bit 6 of the address register starts up the standby function.

The LCD driving voltages, ranking from V1 to V6, must be set to V_{CC} to prevent DC voltage from being applied to an LCD panel during standby state.

The HD66108T operates as follows in standby mode.

(1) Stops oscillation and external clock input

(2) Resets all registers to 0's except the STBY bit

Here, note that the display memory will not preserve data if the standby function is turned on; the display memory as well as registers must be set again after the standby function is terminated. V1 to V6 terminals must be connected to V_{CC} to prevent DC voltage being supplied during stand by.

Table 4 shows the standby status of pins and Table 5 shows the status of registers after standby function termination.

Writing a 0 to bit 6 of the address register terminates the standby function. Writing values into the DISP and Register No. bits at this time is ignored; these bits need to be set after the standby function has been completely terminated.

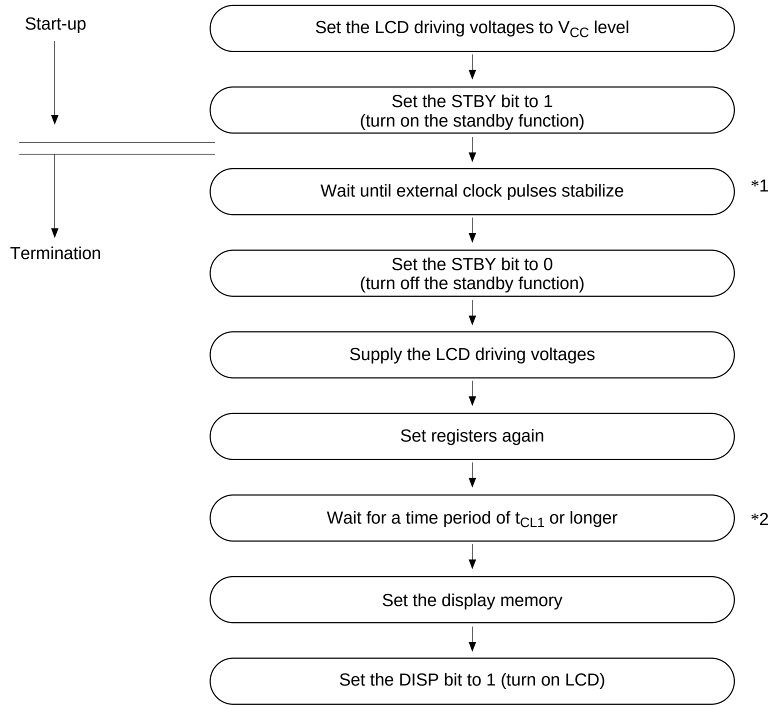
Figure 23 shows the flow for start-up and termination of the standby function and related operations.

Table 4 Standby Status of Pins

Pin	Status
OSC2	High
CO	Low
CL1	Low (master chip) or high-impedance (slave chip)
FLM	Low (master chip) or high-impedance (slave chip)
M	Low (master chip) or high-impedance (slave chip)
Xn	V4 (column output pins)
Xn'	V5 (row output pins)

Table 5 Register Status after Standby Function Termination

Register Name	Status after Standby Function Termination
Address register	Reset to 0's except for the STBY bit
X address register	Reset to 0's
Y address register	Reset to 0's
Control register	Reset to 0's
Mode register	Reset to 0's
C select register	Reset to 0's
Display memory	Data not preserved



Notes: 1. Not necessary in the case of using internal oscillation.
2. Refer to equation 1 (Section 3.1).

Figure 23 Start-Up and Termination of Standby Function and Related Operations

9. Multi-Chip Operation

Using multiple HD66108T chips (= multi-chip operation) provides the means for extending the number of display dots. Note the following items when using the multi-chip operation.

(1) The master chip and the slave chips must be determined; the $\overline{M}$/S pin of the master chip must be set low and the $\overline{M}$/S pin of the slave chips must be set high.

(2) All the HD66108T chips will be slave chips if HD61203 or its equivalent is used as a row driver.

(3) The master chip supplies the FLM, CL1, and M signals to the slave chips via the corresponding pins, which synchronizes the slave chips with the master chip.

(4) Since a master chip outputs synchronization signals, all data registers must be set.

(5) The following bits for slave chips must always be set:

INC, WLS, PON, and ROS (control register) FFS (mode register)

It is not necessary to set the control register's DUTY bits, the mode register's DWS bits, or the C select register. For other registers' settings, refer to Table 6.

(6) All chips must be set to LCD off in order to turn off the display.

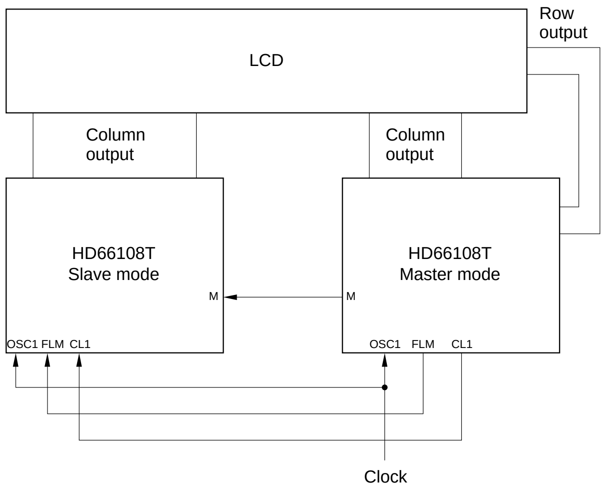
(7) The standby function of slave chips must be started up first while that of the master chip must be terminated first.

Figure 24 to 26 show the connections of the synchronization signals for different system configurations and Table 6 lists the differences between master mode and slave mode.

Table 6 Comparison between Master and Slave Mode

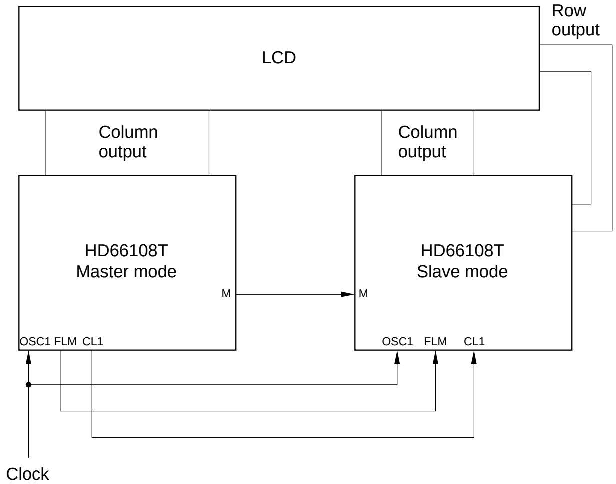
Item		Master Mode	Slave Mode
Pin:	$\overline{M}$/S	Must be set low	Must be set high
	OSC1, OSC2	Oscillation is possible	Oscillation is possible
	CO	= OSC1	= OCS1
	FLM, CL1, M	Output signals	Input signals
Register:	AR	Valid	Valid
	XAR	Valid	Valid
	YAR	Valid	Valid
	FCR	Valid	Valid except for the DUTY bits
	MDR	Valid	Valid except for the DWS bits
	CSR	Valid (only if the DWS bits are set for the C-type waveform)	Invalid

Notes: Valid: Needs to be set
Invalid: Needs not be set



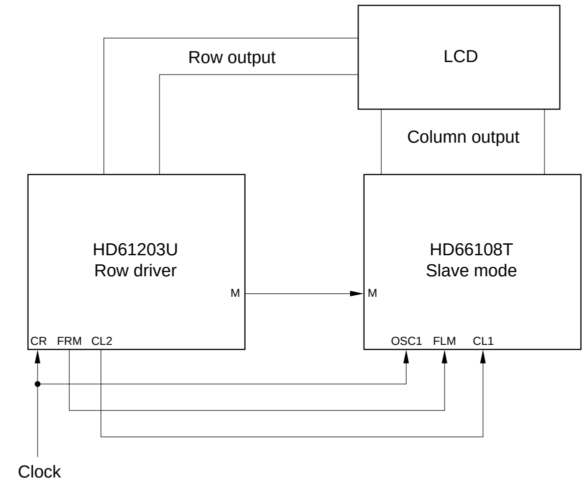
Note: Clock pulses for the slave chip can be supplied from the master chip's CO pin.

Figure 24 Configuration Using Two HD66108T Chips (1)



Note: Clock pulses for the slave chip can be supplied from the master chip CO pin.

Figure 25 Configuration Using Two HD66108T Chips (2)



Notes: 1. The slave chip can oscillate CR clock pulses. In this case, the clock pulses must be supplied to the HD61203U from the HD66108T's CO pin.
2. The HD61203U's control pins must be set in accordance with the type of RAMs.

Figure 26 Configuration Using One HD66108T Chip with Another Row Driver (HD61203U)

Internal Registers

All HD66108T's registers can be read from and written into. However, the BUSY FLAG and invalid bits cannot be written to and reading invalid bits or registers returns 0's.

1. Address Register (AR) (Accessed with RS = 0)

This register (Figure 27) contains Register No. bits, BUSY FLAG bit, STBY bit, and DISP bit. Register No. bits select one of the data registers according to the register number written. The BUSY FLAG bit indicates the internal operation state if read. The STBY bit activates the standby function. The DISP bit turns the display on or off. This register is selected when RS pin is 0.

Bits D4 and D3 are invalid.

D7	D6	D5	D4	D3	D2	D1	D0
BUSY FLAG	STBY	DISP	—		Register No.		

(1) STBY
1: Standby function on
0: Normal (standby function off)

Note: When standby function is on, all registers are reset to 0's.

(2) DISP
1: LCD on
0: LCD off

(3) Register No.

No.	Bit 2	Bit 1	Bit 0	Register
0	0	0	0	Display memory
1	0	0	1	X address register
2	0	1	0	Y address register
3	0	1	1	Control register
4	1	0	0	Mode register
5	1	0	1	C select register

(4) BUSY FLAG (can be read only)
1: Busy state
0: Ready state

Figure 27 Address Register

2. Display Memory (DRAM) (Accessed with RS = 1, Register Number = (B'000)

Although display memory (Figure 28) is not a register, it can be handled as one. 8- or 6-bit data can be selected by the control register WLS bit according to the character font in use. If 6-bit data is selected, D7 and D6 bits are invalid.

3. X Address Register (XAR) (Accessed with RS = 1, Register Number = (B'001)

This register (Figure 29) contains 3 invalid bits (D7 to D5) and 5 valid bits (D4 to D0). It sets X addresses and confirms X addresses after writing or reading to or from the display memory.

4. Y Address Register (YAR) (Accessed with RS = 1, Register Number = (B'010)

This register (Figure 30) contains 1 invalid bit (D7) and 7 valid bits (D6 to D0). It sets Y addresses and confirms Y addresses after writing or reading to or from the display memory.

D7	D6	D5	D4	D3	D2	D1	D0
8-bit data							
*	*	6-bit data					

Reading bits marked with * return 0s and writing them is invalid.

Figure 28 Display Memory

D7	D6	D5	D4	D3	D2	D1	D0
—			XAD				

XAD: 0 to 20 (H'00 to H'14) when display data is 8 bits long and 0 to 27 (H'00 to H'1B) when display data is 6 bits long. A maximum of H'1F is programmable.

Figure 29 X Address Register

D7	D6	D5	D4	D3	D2	D1	D0
—	YAD						

YAD: 0 to 64 (H'00 to H'40)

Figure 30 Y Address Register

5. Control Register (FCR) (Accessed with RS = 1, Register Number = (B'011)

This register (Figure 31), containing eight bits, has a variety of functions such as specifying the method for accessing RAM, determining RAM valid area, and selecting the function of the LCD driving signal output pins. It must be initialized as soon as possible after power-on since it determines the overall operation of the HD66108T. The PON bit may have to be reset afterwards. If the DUTY bits are rewritten after initialization at power-on (if values other than the initial values are desired), the display memory will not preserve data; the display memory must be set again after a time period of t_{CL1} or longer. For determining t_{CL1}, refer to equation 1 (Section 3.1).

D7	D6	D5	D4	D3	D2	D1	D0
INC	WLS	PON	ROS		DUTY		

(1) INC (address increment direction select)
1: X address is incremented
0: Y address is incremented

(2) WLS (word length (of display data) select)
1: 6-bit word
0: 8-bit word

(3) PON (row data protect on)
1: Protect function on
0: Protect function off

(4) ROS (row output (function of LCD driving output pins) select)

No.	Bit 4	Bit 3	Contents
0	0	0	165 column outputs
1	0	1	65 row outputs from the right side
2	1	0	65 row outputs from the left and right sides
3	1	1	33 row outputs from the right side

(5) DUTY (multiplexing duty ratio)

No.	Bit 2	Bit 1	Bit 0	Multiplexing Duty Ratio
0	0	0	0	1/32
1	0	0	1	1/34
2	0	1	0	1/36
3	0	1	1	1/48
4	1	0	0	1/50
5	1	0	1	1/64
6	1	1	0	1/66
7	1	1	1	Invalid (testing mode)

Figure 31 Control Register

6. Mode Register (MDR) (Accessed with RS = 1, Register Number = (B'100)

This register (Figure 32), containing 3 invalid bits (D7 to D5) and 5 valid bits (D4 to D0), selects a system clock and type of LCD driving waveform. It must also be initialized after power-on since it determines overall HD66108T operation like the FCR register. If the FFS bits are rewritten after initialization at power-on (if values other than the initial values are desired), the display memory will not preserve data; the display memory must be set again after a time period of t_{CL1} or longer. For determining t_{CL1}, refer to equation 1 in section 3.1).

D7	D6	D5	D4	D3	D2	D1	D0
—			FFS			DWS	

(1) FFS (frame frequency select)

No.	Bit 4	Bit 3	Bit 2	Frequency-Division Ratio
0	0	0	0	1
1	0	0	1	1/2
2	0	1	0	1/3
3	0	1	1	1/4
4	1	0	0	1/6
5	1	0	1	1/8
6	1	1	0	2
7	1	1	1	—

(2) DWS (LCD driving waveform select)

No.	Bit 1	Bit 0	Driving Waveform
0	0	0	A-type waveform
1	0	1	B-type waveform
2	1	0	C-type waveform
3	1	1	—

Figure 32 Mode Register

7. C Select Register (CSR) (Accessed with RS = 1, Register Number = (B’101)

This register (Figure 33) contains 2 invalid bits (D7 and D6) and 5 valid bits (D5 to D0). It controls C-type waveforms and is activated only when MDR register’s DWS bits are set for this type of waveform.

D7	D6	D5	D4	D3	D2	D1	D0
—		EOR	CLN				

(1) EOR (B-type waveform M signal $\oplus$ no. of counting lines on/off)
1: EOR function on
0: EOR function off

(2) CLN (No. of counting lines in C-type waveform)
1 to 31 should be set in these bits; 0 must not be set.

Figure 33 C Select Register

Reset Function

The $\overline{\text{RESET}}$ pin starts the HD66108T after power-on. A $\overline{\text{RESET}}$ signal must be input via this pin for at least 20 µs to prevent system failure due to excessive current created after power-on. Figure 34 shows the reset definition.

(1) The Status of Pins during Reset

Table 7 shows the reset status of output pins. The pins return to normal operation after reset.

Table 7 The Status of Pins during Reset

Pin	Status
OSC2	Outputs clock pulses or oscillates
CO	Outputs clock pulses
CL1	Low (master chip) or high-impedance (slave chip)
FLM	Low (master chip) or high-impedance (slave chip)
M	Low (master chip) or high-impedance (slave chip)
Xn	V4 (column output pins)
Xn’	V5 (row output pins)

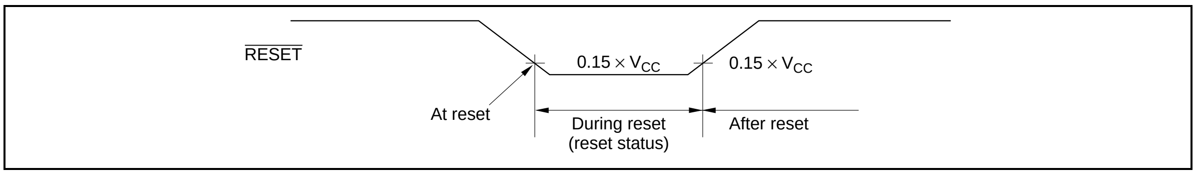


Figure 34 Reset Definition

(2) The Status of Registers during Reset

The $\overline{RESET}$ signal has no effect on registers or register bits except for the address register's STBY bit and the X and Y address registers, which are reset to 0's by the signal. Table 8 shows the reset status of registers.

(3) Status after Reset

The display memory does not preserve data which has been written to it before reset; it must be set again after reset.

A $\overline{RESET}$ signal terminates the standby mode.

Table 8 The Status of Registers during Reset

Register	Status
Address register	Pre-reset status with the STBY bit reset to 0
X address register	Reset to 0's
Y address register	Reset to 0's
Control register	Pre-reset status
Mode register	Pre-reset status
C select register	Pre-reset status
Display memory	Preserves no pre-reset data

Precautionary Notes When Using the HD66108T

(1) Install a 0.1-µF bypass capacitor as close to the LSI as possible to reduce power supply impedance (V_{CC}–GND and V_{CC}–V_{EE}).

(2) Do not leave input pins open since the HD66108T is a CMOS LSI; refer to “Pin Functions” on how to deal with each pin.

(3) When using the internal oscillation clock, attach an oscillation resistor as close to the LSI as possible to reduce coupling capacitance.

(4) Make sure to input the reset signal at power-on so that internal units operate as specified.

(5) Maintain the LCD driving power at V_{CC} during standby state so that DC is not applied to an LCD, in which Xn pins are fixed at V4 or V5 level.

Programming Restrictions

(1) After busy time is terminated, an X or Y address is not incremented until 0.5-clock time has passed. If an X or Y address is read during this time period, non-updated data will be read. (The addresses are incremented even in this case.) In addition, the address increment direction should not be changed during this time since it will cause malfunctions.

(2) Although the maximum output rows is 33 when 33-row-output mode from the right side is specified, any multiplexing duty ratio can be specified. Therefore, row output data sufficient to fill the specified duty must be input in the Y direction. Figure 35 shows how to set row data in the case of 1/34 multiplexing duty ratio. In this case, 0s must be set in Y33 since data for the 34th row (Y33) are not output.

(3) Do not set the C select register’s CLN bits to 0 for the M signal of C-type waveform.

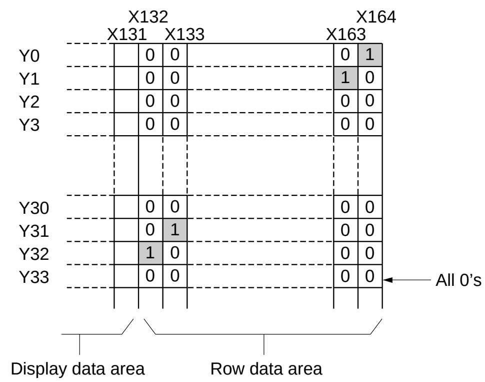


Figure 35 How to Set Row Data for 33-Row Output from the Right Side

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage (1)	V_{CC1} to V_{CC3}	–0.3 to +7.0	V
Power supply voltage (2)	V_{CC}–V_{EE}	–0.3 to +16.5	V
Input voltage	Vin	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{op}	–20 to +75	°C
Storage temperature	T_{stg}	–40 to +125	°C

Notes: 1. Permanent LSI damage may occur if the maximum ratings are exceeded.
Normal operation should be under recommended operating conditions (V_{CC} = 2.7 to 6.0V, GND = 0V, Ta = –20 to +75°C). If these conditions are exceeded, LSI malfunctions could occur.
2. Power supply voltages are referenced to GND = 0V. Power supply voltage (2) indicates the difference between V_{CC} and V_{EE}.

Electrical Characteristics

DC Characteristics (1) (V_{CC} = 5V ±20%, GND = 0V, V_{CC} – V_{EE} = 6.0 to 15V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input high voltage	OSC1	V_{IH1}	0.8 × V_{CC}	—	V_{CC} + 0.3	V		
	$\overline{M}$/S, CL1, FLM, M, TEST1, TEST2	V_{IH2}	0.7 × V_{CC}	—	V_{CC} + 0.3	V		
	$\overline{RESET}$	V_{IH3}	0.85 × V_{CC}	—	V_{CC} +0.3	V		
	The other inputs	V_{IH4}	2.0	—	V_{CC} + 0.3	V	V_{CC} = 5V ±10%	5
Input low voltage	OSC1	V_{IL1}	–0.3	—	0.2 × V_{CC}	V		
	$\overline{M}$/S, CL1, FLM, M, TEST1, TEST2	V_{IL2}	–0.3	—	0.3 × V_{CC}	V		
	$\overline{RESET}$	V_{IL3}	–0.3	—	0.15 × V_{CC}	V		
	The other inputs	V_{IL4}	–0.3	—	0.8	V	V_{CC} = 5V ±10%	6
Output high voltage	CO, CL1, FLM, M	V_{OH1}	0.9 × V_{CC}	—	—	V	$–I_{OH}$ = 0.1 mA	
	DB7–DB0	V_{OH2}	2.4	—	—	V	$–I_{OH}$ = 0.2 mA V_{CC} = 5V ±10%	7
Output low voltage	CO, CL1, FLM, M	V_{OL1}	—	—	0.1 × V_{CC}	V	I_{OL} = 0.1 mA	
	DB7–DB0	V_{OL2}	—	—	0.4	V	I_{OL} = 1.6 mA V_{CC} = 5V ±10%	8
Input leakage current	All except DB7–DB0, CL1, FLM, M	I_{IIL}	–2.5	—	2.5	µA	Vin = 0 to V_{CC}	
Tri-state leakage current	DB7–DB0, CL1, FLM, M	I_{TSL}	–10	—	10	µA	Vin = 0 to V_{CC}	
V pins leakage current	V1L, V1R, V3, V4, V6L, V6R, VMHn, VMLn	I_{VL}	–10	—	10	µA	Vin = V_{EE} to V_{CC}	
Current consumption	During display	I_{CC1}	—	—	400	µA	External clock f_{OSC} = 500 kHz	1
		I_{CC2}	—	—	1.0	mA	Internal oscillation R_f = 91 kΩ	1
	During standby	I_{SB}	—	—	10	µA		1, 2

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
ON resistance between Vi and Xj	X0–X164	R_{ON}	—	—	10	kΩ	$\pm I_{LD}$ = 50 µA V_{CC}–V_{EE} = 10V	3
V pins voltage range		ÆV	—	—	35	%		4
Oscillating frequency		f_{OSC}	315	450	585	kHz	R_f = 91 kΩ	

Notes: 1. When voltage applied to input pins is fixed to V_{CC} or to GND and output pins have no load capacity.

2. When the LSI is not exposed to light and Ta = 0 to 40°C with the STBY bit = 1. If using external clock pulses, input pins must be fixed high or low. Exposing the LSI to light increases current consumption.
3. I_{LD} indicates the current supplied to one measured pin.
4. ÆV = 0.35 × (V_{CC}–V_{EE}). For levels V1, V2, and V3, the voltage supplied should be between the V_{CC} and the ÆV and for levels V4, V5, and V6, the voltage supplied should be between the V_{EE} and the ÆV (Figure 36).
5. V_{IH4} (min) = 0.7 × V_{CC} when used under conditions other than V_{CC} = 5V ±10%.
6. V_{IL4} (max) = 0.15 × V_{CC} when used under conditions other than V_{CC} = 5V ±10%.
7. V_{OH2} (min) = 0.9 × V_{CC} (–I_{OH} = 0.1 mA) when used under conditions other than V_{CC} = 5V ±10%.
8. V_{OL2} (max) = 0.1 × V_{CC} (I_{OL} = 0.1 mA) when used under conditions other than V_{CC} = 5V ±10%.

DC Characteristics (2) (V_{CC} = 2.7 to 4.0V, GND = 0V, V_{CC}–V_{EE} = 6.0 to 15V, Ta = –20 to +75°C, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Input high voltage	$\overline{RESET}$	V_{IH1}	0.85 × V_{CC}	—	V_{CC} + 0.3	V		
	The other inputs	V_{IH2}	0.7 × V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	$\overline{M}$/S, OSC1, CL1, FLM, TEST1, TEST2, M	V_{IL1}	–0.3	—	0.3 × V_{CC}	V		
	The other inputs	V_{IL2}	–0.3	—	0.15 × V_{CC}	V		
Output high voltage		V_{OH1}	0.9 × V_{CC}	—	—	V	$-I_{OH}$ = 50 µA	
Output low voltage		V_{OL1}	—	—	0.1 × V_{CC}	V	I_{OL} = 50 µA	
Input leakage current	All except DB7–DB0, CL1, FLM, M	I_{IIL}	–2.5	—	2.5	µA	Vin = 0 to V_{CC}	
Tri-state leakage current	DB7–DB0, CL1, FLM, M	I_{TSL}	–10	—	10	µA	Vin = 0 to V_{CC}	
V pins leakage current	V1L, V1R, V3, V4, V6L, V6R, VMHn, VMLn	I_{VL}	–10	—	10	µA	Vin = V_{EE} to V_{CC}	
Current consumption	During display	I_{CC1}	—	—	260	µA	External clock f_{OSC} = 500 kHz	1
		I_{CC2}	—	—	700	µA	Internal oscillation R_f = 75 kΩ	1
	During standby state	I_{SB}	—	—	10	µA		1, 2
ON resistance between Vi and Xj	X0–X164	R_{ON}	—	—	10	kΩ	$\pm I_{LD}$ = 50 µA V_{CC}–V_{EE} = 10V	3
V pins voltage range		ÆV	—	—	35	%		4
Oscillating frequency		f_{OSC}	315	450	585	kHz	R_f = 75 kΩ	

Notes: 1. When voltage applied to input pins is fixed to V_{CC} or to GND and output pins have no load capacity. Exposing the LSI to light increases current consumption.

2. When the LSI is not exposed to light and Ta = 0 to 40°C with the STBY bit = 1. If using external clock pulses, input pins must be fixed high or low.

3. I_{LD} indicates the current supplied to one measured pin.

4. ÆV = 0.35 × (V_{CC}–V_{EE}). For levels V1, V2, and V3, the voltage supplied should be between the V_{CC} and the ÆV and for levels V4, V5, and V6, the voltage supplied should be between the V_{EE} and the ÆV (Figure 36).

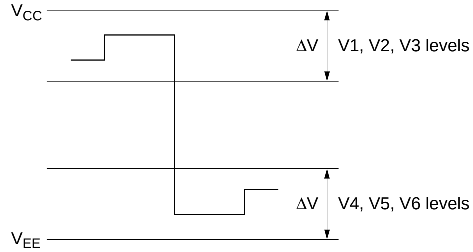


Figure 36 Driver Output Waveform and Voltage Levels

AC Characteristics (1) (V_{CC} = 4.5 to 6.0V, GND = 0V, Ta = –20 to +75°C, unless otherwise noted)

1. CPU Bus Timing (Figure 37)

Item	Symbol	Min	Max	Unit	
$\overline{RD}$ high-level pulse width	t_{WRH}	190	—	ns	
$\overline{RD}$ low-level pulse width	t_{WRL}	190	—	ns	
$\overline{WR}$ high-level pulse width	t_{WWH}	190	—	ns	
$\overline{WR}$ low-level pulse width	t_{WWL}	190	—	ns	
$\overline{WR}$–$\overline{RD}$ high-level pulse width	t_{WWRH}	190	—	ns	
$\overline{CS}$, RS setup time	t_{AS}	0	—	ns	
$\overline{CS}$, RS hold time	t_{AH}	0	—	ns	
Write data setup time	t_{DSW}	100	—	ns	
Write data hold time	t_{DHW}	0	—	ns	
Read data output delay time	t_{DDR}	—	150	ns	Note
Read data hold time	t_{DHR}	20	—	ns	Note
External clock cycle time	t_{CYC}	0.25	5.0	µs	
External clock high-level pulse width	t_{WCH}	0.1	—	µs	
External clock low-level pulse width	t_{WCL}	0.1	—	µs	
External clock rise and fall time	t_r, t_f	—	20	ns	

Note: Measured by test circuit 1 (Figure 39).

2. LCD Interface Timing (Figure 38)

Item		Symbol	Min	Max	Unit	Notes
$\overline{M}$/S = 0	CL1 High-level pulse width	t_{WCH1}	35	—	µs	1, 4
	CL1 Low-level pulse width	t_{WCL1}	35	—	µs	1, 4
	FLM Delay time	t_{DFL1}	–2.0	+2.0	µs	4
	FLM Hold time	t_{HFL1}	–2.0	+2.0	µs	4
	M output delay time	t_{DMO1}	–2.0	+2.0	µs	4
$\overline{M}$/S = 1	CL1 High-level pulse width	t_{WCH2}	35	—	µs	4
	CL1 Low-level pulse width	t_{WCL2}	$11 \times t_{CYC}$	—	µs	2, 4
	FLM Delay time	t_{DFL2}	–2.0	$1.5 \times t_{CYC}$	µs	3, 4
	FLM Hold time	t_{HFL2}	–2.0	+2.0	µs	4
	M delay time	t_{DMI}	–2.0	+2.0	µs	4

Notes: 1. When R_{OSC} is 91 kΩ (V_{CC} = 4.0 to 6V) or 75 kΩ (V_{CC} = 2.0 to 4.0V) and bits FFS are set for 1.
2. When bits FFS are set for 1 or 2. The value is $19 \times t_{CYC}$ in other cases.
3. When bits FFS are set for 1 or 2. The value is $8.5 \times t_{CYC}$ in other cases.
4. Measured by test circuit 2 (Figure 39).

AC Characteristics (2) (V_{CC} = 2.7 to 4.5V, GND = 0V, Ta = –20 to +75°C, unless otherwise noted)

1. CPU Bus Timing (Figure 37)

Item	Symbol	Min	Max	Unit	
$\overline{RD}$ high-level pulse width	t_{WRH}	1.0	—	µs	
$\overline{RD}$ low-level pulse width	t_{WRL}	1.0	—	µs	
$\overline{WR}$ high-level pulse width	t_{WWH}	1.0	—	µs	
$\overline{WR}$ low-level pulse width	t_{WWL}	1.0	—	µs	
$\overline{WR}$–$\overline{RD}$ high-level pulse width	t_{WWRH}	1.0	—	µs	
$\overline{CS}$, RS setup time	t_{AS}	0.5	—	µs	
$\overline{CS}$, RS hold time	t_{AH}	0.1	—	µs	
Write data setup time	t_{DSW}	1.0	—	µs	
Write data hold time	t_{DHW}	0	—	µs	
Read data output delay time	t_{DDR}	—	0.5	µs	Note
Read data hold time	t_{DHR}	20	—	ns	Note
External clock cycle time	t_{CYC}	1.6	5.0	µs	
External clock high-level pulse width	t_{WCH}	0.7	—	µs	
External clock low-level pulse width	t_{WCL}	0.7	—	µs	
External clock rise and fall time	t_r, t_f	—	0.1	µs	

Note: Measured by test circuit 2 (Figure 39).

2. LCD Interface Timing (Figure 38)

Item		Symbol	Min	Max	Unit	Notes
$\overline{M}$/S = 0	CL1 High-level pulse width	t_{WCH1}	35	—	µs	1, 4
	CL1 Low-level pulse width	t_{WCL1}	35	—	µs	1, 4
	FLM Delay time	t_{DFL1}	–2.0	+2.0	µs	4
	FLM Hold time	t_{HFL1}	–2.0	+2.0	µs	4
	M output delay time	t_{DMO1}	–2.0	+2.0	µs	4
$\overline{M}$/S = 1	CL1 High-level pulse width	t_{WCH2}	35	—	µs	4
	CL1 Low-level pulse width	t_{WCL2}	$11 \times t_{CYC}$	—	µs	2, 4
	FLM Delay time	t_{DFL2}	–2.0	$1.5 \times t_{CYC}$	µs	3, 4
	FLM Hold time	t_{HFL2}	–2.0	+2.0	µs	4
	M delay time	t_{DMI}	–2.0	+2.0	µs	4

Notes: 1. When R_{OSC} is 91 kΩ (V_{CC} = 4.0 to 6V) or 75 kΩ (V_{CC} = 2.7 to 4.0V) and bits FFS are set for 1.
2. When bits FFS are set for 1 or 2. The value is $19 \times t_{CYC}$ in other cases.
3. When bits FFS are set for 1 or 2. The value is $8.5 \times t_{CYC}$ in other cases.
4. Measured by test circuit 2 (Figure 39).

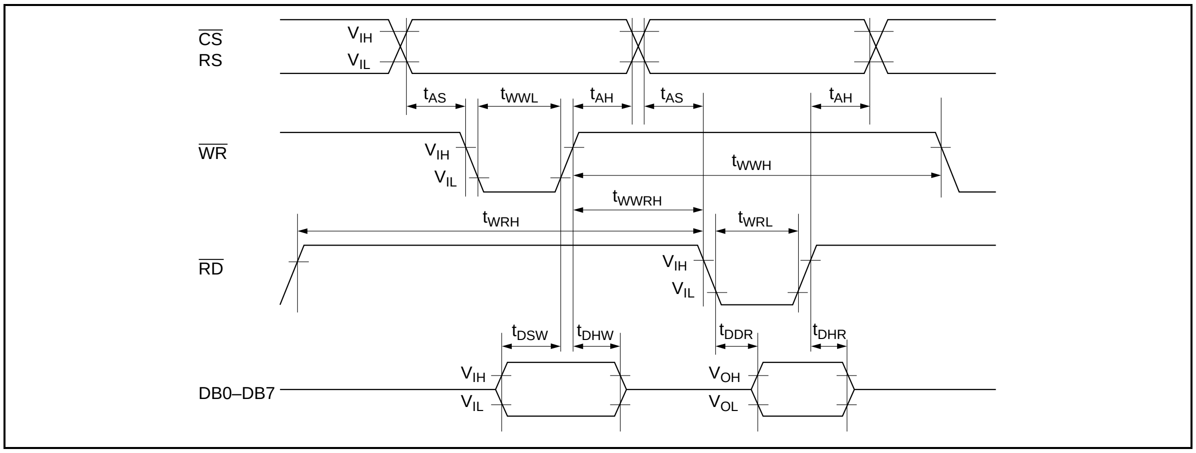


Figure 37 CPU Bus Timing

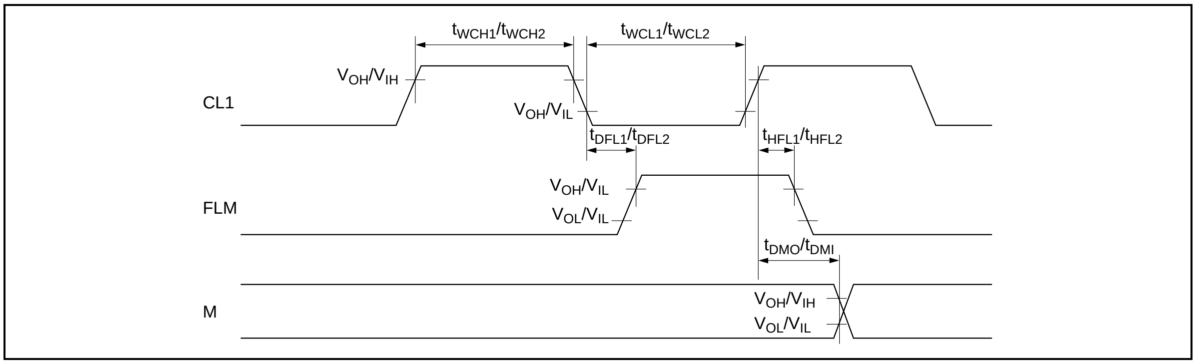


Figure 38 LCD Interface Timing

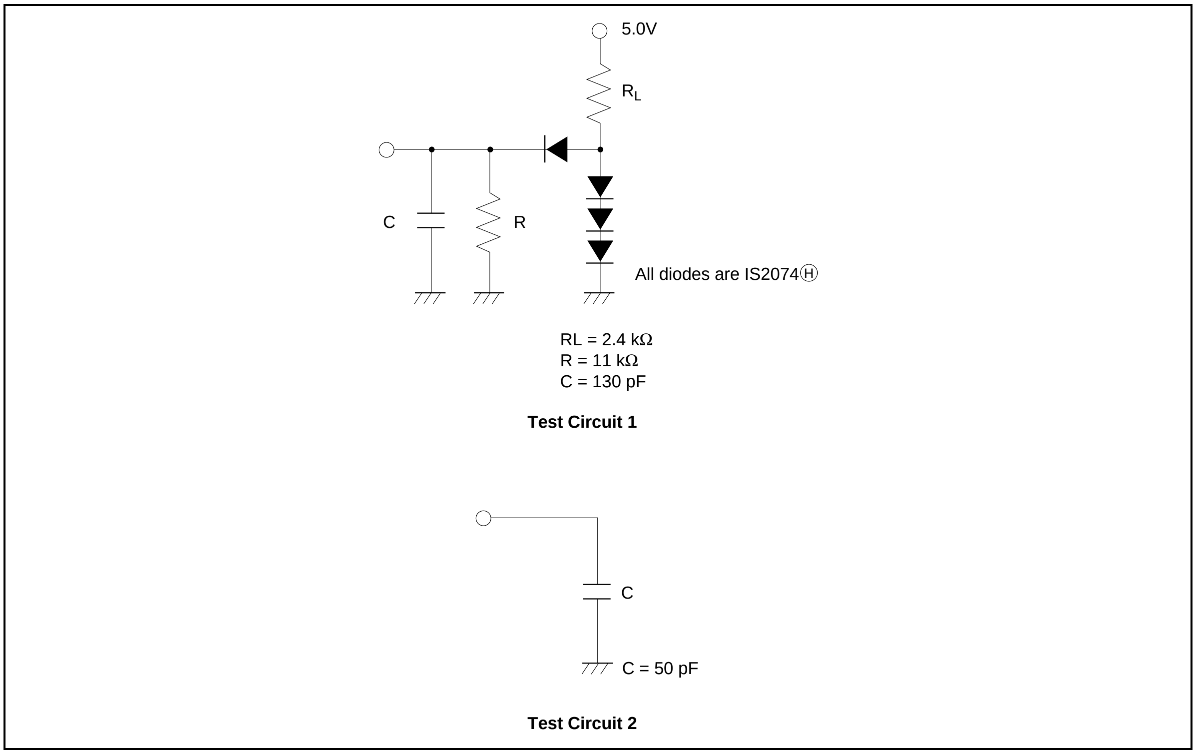


Figure 39 Load Circuits