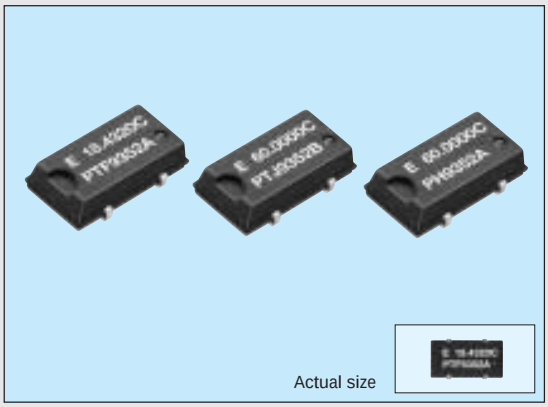
HIGH-FREQUENCY CRYSTAL OSCILLATOR

SG-636 series

Product number (please refer to page 1)

Q33636xxxxxxx00

- A small SMD that enables high-density mounting.
- A general-purpose device with builtin heat-resisting cylindrical AT-cut crystal and allowing almost the same temperature condition for soldering as SMD IC.
- Low current consumption by output enable function(OE) or standby function(ST).



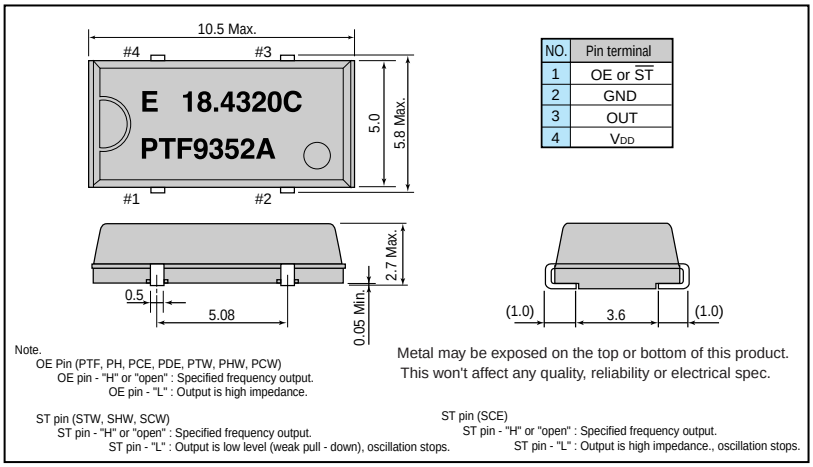
Specifications (characteristics)

Item		Symbol	Specifications				Remarks
			SG-636PTF	SG-636PH	SG-636SCE/PCE	SG-636PDE	
Output frequency range		f_0	2.21675 MHz to 41.0000 MHz	41.0001 MHz to 70.0000 MHz	2.21675 MHz to 40.0000 MHz	2.21675MHz to 40.0000MHz	Refer to page 31. "Frequency range"
Power source voltage	Max. supply voltage	V_{DD}-GND	-0.5 V to +7.0 V				
	Operating voltage	V_{DD}	5.0 V ±0.5 V		3.3 V ±0.3 V	2.5 V ±0.25 V	
Temperature range	Storage temperature	T_{STG}	-55 °C to +100 °C				Stored as bare product after unpacking
	Operating temperature	T_{OPR}	-20 °C to +70 °C				Refer to page 31. "Frequency range"
Frequency stability		$\Delta f/f_0$	C: ±100 x 10^{-6}				
Current consumption		Iop	17 mA Max.	35 mA Max.	9 mA Max.	5 mA Max.	No load condition
Output disable current		I_{OE}	10 mA Max.	20 mA Max.	5 mA Max.	3 mA Max.	OE=GND, $\overline{ST}$=GND 2 µA Max.(SCE)
Duty	CMOS level	t_w/t	40 % to 60 %		45 % to 55 %		CMOS load: 1/2 V_{DD} level
	TTL level		45 % to 55 %	—			TTL load: 1.4 V level
Output voltage		V_{OH}	V_{DD} -0.4 V Min.				I_{OH} =-8 mA (PTF) /-4 mA (PH / SCE / PCE / PDE)
		V_{OL}	0.4 V Max.				I_{OL} =16 mA (PTF) /4 mA (PH / SCE / PCE / PDE)
Output load condition (fan out)	CMOS level	C_L	50 pF Max.	20 pF Max.(≤ 55 MHz) 15 pF Max.(> 55 MHz)	30 pF Max.	15 pF Max.	
	TTL level	N	10 TTL Max.	5 LSTTL Max.	—		C_L≤15 pF
Output enable/disable input voltage		V_{IH}	2.0 V Min.		0.8 V_{DD} Min.		OE,$\overline{ST}$ (SCE)
		V_{IL}	0.8 V Max.		0.2 V_{DD} Max.		
Output rise time	CMOS level	t_{TLH}	7 ns Max.		5 ns Max.		CMOS load: 20 %→80 % V_{DD}
	TTL level		5 ns Max.		—		TTL load: 0.4 V→2.4 V
Output fall time	CMOS level	t_{THL}	7 ns Max.		5 ns Max.		CMOS load: 80 %→20 % V_{DD}
	TTL level		5 ns Max.		—		TTL load: 2.4 V→0.4 V
Oscillation start up time		tosc	4 ms Max.	10 ms Max.	4 ms Max.		Time at minimum operating voltage to be 0 s
Aging		fa	±5 x 10^{-6} /year Max.				Ta=+25 °C,V_{DD}=5.0 V / 3.3 V / 2.5 V,first year
Shock resistance		S.R.	±20 x 10^{-6} Max.				Three drops on a hard board from 750 mm or excitation test with 29400 m/s² x 0.3 ms x 1/2 sine wave in 3 directions

Note: • Unless otherwise stated,characteristics (specifications) shown in the above table are based on the rated operating temperature and voltage condition.
• External by-pass capacitor is required.

External dimensions

(Unit: mm)



NO.	Pin terminal
1	OE or $\overline{ST}$
2	GND
3	OUT
4	V_{DD}

Note.
OE Pin (PTF, PH, PCE, PDE, PTW, PHW, PCW)
OE pin - "H" or "open" : Specified frequency output.
OE pin - "L" : Output is high impedance.

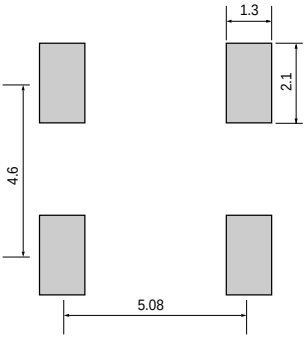
ST pin (STW, SHW, SCW)
ST pin - "H" or "open" : Specified frequency output.
ST pin - "L" : Output is low level (weak pull - down), oscillation stops.

Metal may be exposed on the top or bottom of this product.
This won't affect any quality, reliability or electrical spec.

ST pin (SCE)
ST pin - "H" or "open" : Specified frequency output.
ST pin - "L" : Output is high impedance., oscillation stops.

Recommended soldering pattern

(Unit: mm)



Specifications (characteristics)

Item		Symbol	Specifications			Remarks
			SG-636PTG	SG-636PHG	SG-636PCG/SCG	
Output frequency range		f_O	2.21675 MHz to 33.0000 MHz			Refer to page 31. "Frequency range"
Power source voltage	Max. supply voltage	V_{DD}-GND	-0.5 V to +7.0 V			
	Operating voltage	V_{DD}	4.5 V to 5.5 V		2.7 V to 3.6 V	
Temperature range	Storage temperature	T_{STG}	-55 °C to +100 °C			Stored as bare product after unpacking
	Operating temperature	T_{OPR}	-20 °C to +70 °C			Refer to page 31. "Frequency range"
Frequency stability		$\Delta f/f_0$	B : ±50 x 10^{-6} C : ±100 x 10^{-6}			-20 °C to +70 °C
Current consumption		I_{OP}	25 mA Max.		12 mA Max.	No load condition
Output disable current		I_{OE}	20 mA Max.		10 mA Max.	OE=GND (P∗G)
Standby current		I_{ST}	—		50 µA Max.	$\overline{ST}$=GND (SCG)
Duty	CMOS level	tw/t	—	45 % to 55 %		50 % V_{DD}, CL = 25 pF
	TTL level		40 % to 60 %	—		1.4 V Level, CL = 25 pF
Output voltage		V_{OH}	2.4 V Min.	—	V_{DD} -0.4 V Min.	I_{OH} = -8 mA
			—	V_{DD} -0.4 V Max.	—	I_{OH} = -16 mA
		V_{OL}	—	0.4 V Max.		I_{OL} = 8 mA
			0.4 V Max.	—		I_{OL} = 16 mA
Output load condition (fan out)		CL	25 pF			
Output enable disable input voltage	CMOS level	V_{IH}	2.0 V Min.		70 % V_{DD} Min.	OE, $\overline{ST}$
	TTL level	V_{IL}	0.8 V Max.		20 % V_{DD} Max.	OE, $\overline{ST}$
Output rise time	CMOS level	t_{TLH}	—	3.4 ns Max.	4.0 ns Max.	20 % to 80 % V_{DD}, CL ≤ 25 pF
	TTL level		1.2 ns Max.	—	—	0.8 V to 2.0 V CL ≤ 25 pF
			2.4 ns Max.	—	—	0.4 V to 2.4 V CL ≤ 25 pF
Output fall time	CMOS level	t_{THL}	—	3.4 ns Max.	4.0 ns Max.	80 % to 20 % V_{DD} CL ≤ 25 pF
	TTL level		1.2 ns Max.	—	—	2.0 V to 0.8 V CL ≤ 25 pF
			2.4 ns Max.	—	—	2.4 V to 0.4 V CL ≤ 25 pF
Oscillation start up time		t_{OSC}	12 ms Max.			Time at minimum operating voltage to be 0 s
Aging		fa	±5 x 10^{-6} /year Max.			Ta=+25 °C, V_{DD} =5.0 V / 3.3 V, First year
Shock resistance		S.R.	±20 x 10^{-6} Max.			Three drops on a hard board from 750 mm or excitation test with 29400 m/s2 x 0.3 ms x 1/2 sine wave in 3 directions

Specifications (characteristics)

Item		Symbol	Specifications			Remarks
			SG-636PTW/STW	SG-636PHW/SHW	SG-636PCW/SCW	
Output frequency range		f_O	32.0001 MHz to 135.0000 MHz			Refer to page 31. "Frequency range"
Power source voltage	Max. supply voltage	V_{DD}-GND	-0.5 V to +7.0 V			
	Operating voltage	V_{DD}	5.0 V ± 0.5 V		3.3 V ± 0.3 V	
Temperature range	Storage temperature	T_{STG}	-55 °C to +100 °C			Stored as bare product after unpacking
	Operating temperature	T_{OPR}	-20 °C to +70 °C			Refer to page 31. "Frequency range"
Frequency stability		$\Delta f/f0$	B : ±50 x 10^{-6} C : ±100 x 10^{-6}			
Current consumption		I_{OP}	45 mA Max.		28 mA Max.	No load condition
Output disable current		I_{OE}	30 mA Max.		16 mA Max.	OE=GND(P∗W)
Standby current		I_{ST}	50 µA Max.			$\overline{ST}$=GND(S∗W)
Duty		tw/t	40 % to 60 %	—	—	TTL load : 1.4 V, CL = Max.
			45 % to 55 %	—	—	TTL load : 1.4 V, 5TTL + 15 pF, fo ≤ 66.6667 MHz
			—	40 % to 60 %	40 % to 60 %	CMOS load : 50% V_{DD}, CL = Max.
			—	45 % to 55%	—	CMOS load : 50% V_{DD}, CL = 25 pF, fo ≤ 66.6667 MHz
Output voltage		V_{OH}	V_{DD} -0.4 V Min.			I_{OH}= -16 mA (∗TW/HW)/-8 mA(∗CW)
		V_{OL}	0.4 V Max.			I_{OL}= 16 mA (∗TW/HW)/8 mA(∗CW)
Output load condition (fan out)		CL	15 pF	—	—	fo ≤ 135 MHz
			5 TTL + 15 pF	—	—	fo ≤ 90 MHz
			25 pF	—	—	fo ≤ 66.6667 MHz
			—	15 pF	15 pF	fo ≤ 135 MHz
			—	25 pF	—	fo ≤ 90 MHz
			—	50 pF	—	fo ≤ 66.6667MHz
Output enable disable input voltage		V_{IH}	2.0 V Min.		70 % V_{DD} Min.	OE,$\overline{ST}$
		V_{IL}	0.8 V Max.		20 % V_{DD} Max.	OE,$\overline{ST}$
Output rise time		t_{TLH}	2.0 ns Max.	—	—	TTL load: 0.8 V→2.0 V, CL = Max.
			4.0 ns Max.	—	—	TTL load: 0.4 V→2.4 V, CL = Max.
			—	3.0 ns Max.	—	CMOS load: 20 %→80 % V_{DD}, CL= 25 pF
			—	4.0 ns Max.	—	CMOS load: 20 %→80 % V_{DD}, CL= 50 pF
			—	—	3.0 ns Max.	CMOS load: 20 %→80 % V_{DD}, CL= 15 pF
Output fall time		t_{THL}	2.0 ns Max.	—	—	TTL load: 2.0 V→0.8 V, CL = Max.
			4.0 ns Max.	—	—	TTL load: 2.4 V→0.4V, CL = Max.
			—	3.0 ns Max.	—	CMOS load: 80 %→20 % V_{DD}, CL= 25 pF
			—	4.0 ns Max.	—	CMOS load: 80 %→20 % V_{DD}, CL= 50 pF
			—	—	3.0 ns Max.	CMOS load: 80 %→20 % V_{DD}, CL= 15 pF
Oscillation start up time		t_{OSC}	10 ms Max.			Time at minimum operating voltage to be 0 s
Aging		fa	±5 x 10^{-6} /year Max.			Ta=+25 °C, VDD =5.0 V / 3.3 V, first year
Shock resistance		S.R.	±20 x 10^{-6} Max.			Three drops on a hard board from 750 mm or excitation test with 29400 m/s2 x 0.3 ms x 1/2 sine wave in 3 directions