

# AZ100LVEL16VR

## ECL/PECL Oscillator Gain Stage & Buffer with Selectable Enable

### FEATURES

- High Bandwidth for  $\geq 1\text{GHz}$
- Similar Operation as AZ100EL16VO
- Operating Range of 3.0V to 5.5V
- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- Available in a 3x3mm MLP Package

### PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
MLP 16	AZ100LVEL16VRL	AZM16R
MLP 16 T&R	AZ100LVEL16VRLR1	AZM16R
MLP 16 T&R	AZ100LVEL16VRLR2	AZM16R
DIE	AZ100LVEL16VRX	N/A

### DESCRIPTION

The AZ100LVEL16VR is a specialized oscillator gain stage with high gain output buffer including an enable. The  $Q_{HG}/\bar{Q}_{HG}$  outputs have a voltage gain several times greater than the  $Q/\bar{Q}$  outputs.

The AZ100LVEL16VR provides a selectable enable that allows continuous oscillator operation. See truth table below for enable function. If Enable pull-up is desired in the CMOS mode, an external  $\leq 20\text{k}\Omega$  resistor connecting EN to  $V_{CC}$  will override the on-chip pull-down resistor. The AZ100LVEL16VR also provides a  $V_{BB}$  and  $470\Omega$  internal bias resistors from D to  $V_{BB}$  and  $\bar{D}$  to  $V_{BB}$ . The  $V_{BB}$  pin can support 1.5mA sink/source current. Bypassing  $V_{BB}$  to ground with a  $0.01\ \mu\text{F}$  capacitor is recommended.

Outputs  $Q/\bar{Q}$  each have a selectable on-chip pull-down current source. See truth table below for current source functions. External resistors may also be used to increase pull-down current to a maximum total of 25mA.

Outputs  $Q_{HG}/\bar{Q}_{HG}$  each have an optional on-chip pull-down current source of 10mA. When pad/pin  $V_{EEP}$  is left open (NC), the output current sources are disabled and the  $Q_{HG}/\bar{Q}_{HG}$  operate as standard PECL/ECL. When  $V_{EEP}$  is connected to  $V_{EE}$ , the current sources are activated. The  $Q_{HG}/\bar{Q}_{HG}$  pull-down current can be decreased, by using a resistor to connect from  $V_{EEP}$  to  $V_{EE}$ .

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

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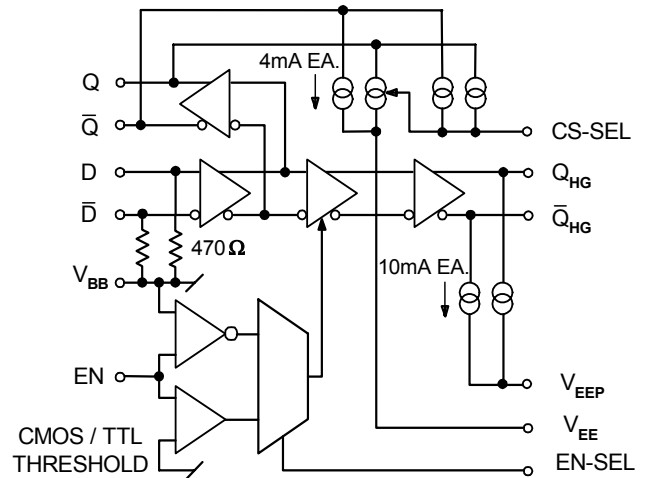
## ENABLE TRUTH TABLE

EN-SEL	EN	Q/Q̄	Q <sub>HG</sub>	Q̄ <sub>HG</sub>
NC	PECL Low, V <sub>EE</sub> or NC	Data	Data	Data
NC	PECL High or V <sub>CC</sub>	Data	Low	High
V <sub>EE</sub> *	CMOS Low or V <sub>EE</sub>	Data	Low	High
V <sub>EE</sub> *	CMOS High or V <sub>CC</sub>	Data	Data	Data
V <sub>EE</sub>	NC, no external pull-up	Data	Low	High
V <sub>EE</sub>	NC, with ≤20kΩ to V <sub>CC</sub>	Data	Data	Data

\*Connections to V<sub>CC</sub> or V<sub>EE</sub> must be less than 1Ω.

## PIN DESCRIPTION

PIN	FUNCTION
D/D̄	Data Inputs
Q/Q̄	Data Outputs
Q <sub>HG</sub> /Q̄ <sub>HG</sub>	Data Outputs w/High Gain
V <sub>BB</sub>	Reference Voltage Output
EN-SEL	Selects Enable Logic
EN	Enable Input
CS-SEL	Selects Q and Q̄ Current Source Magnitude
V <sub>EEP</sub>	Optional Q <sub>HG</sub> and Q̄ <sub>HG</sub> Current Sources
V <sub>EE</sub>	Negative Supply
V <sub>CC</sub>	Positive Supply



## CURRENT SOURCE TRUTH TABLE

CS-SEL	Q	Q̄
NC	4mA typ.	4mA typ.
V <sub>EE</sub> *	8mA typ.	8mA typ.
V <sub>CC</sub> *	0	4mA typ.

**Absolute Maximum Ratings are those values beyond which device life may be impaired.**

Symbol	Characteristic	Rating	Unit
V <sub>CC</sub>	PECL Power Supply (V <sub>EE</sub> = 0V)	0 to +8.0	Vdc
V <sub>I</sub>	PECL Input Voltage (V <sub>EE</sub> = 0V)	0 to +6.0	Vdc
V <sub>EE</sub>	ECL Power Supply (V <sub>CC</sub> = 0V)	-8.0 to 0	Vdc
V <sub>I</sub>	ECL Input Voltage (V <sub>CC</sub> = 0V)	-6.0 to 0	Vdc
I <sub>OUT</sub>	Output Current --- Continuous --- Surge	50 100	mA
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C

## 100K ECL DC Characteristics (V<sub>EE</sub> = -3.0V to -5.5V, V<sub>CC</sub> = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage <sup>2</sup>	-1045	-835	-995	-835	-995	-835	-995	-835	mV
V <sub>OL</sub>	Output LOW Voltage <sup>2</sup>	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V <sub>IH</sub>	Input HIGH Voltage									
	D/D̄, EN (PECL) EN (CMOS/TTL)	-1165 V <sub>EE</sub> +2000	-880 V <sub>CC</sub>	-1165 V <sub>EE</sub> +2000	-880 V <sub>CC</sub>	-1165 V <sub>EE</sub> +2000	-880 V <sub>CC</sub>	-1165 V <sub>EE</sub> +2000	-880 V <sub>CC</sub>	mV
V <sub>IL</sub>	Input LOW Voltage									
	D/D̄, EN (PECL) EN (CMOS/TTL)	-1810 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	-1810 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	-1810 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	-1810 V <sub>EE</sub>	-1475 V <sub>EE</sub> + 800	mV
V <sub>BB</sub>	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I <sub>IL</sub>	Input LOW Current EN <sup>3</sup>	0.5		0.5		0.5		0.5		μA
I <sub>IH</sub>	Input HIGH Current EN <sup>3</sup>		150		150		150		150	μA
I <sub>EE</sub>	Power Supply Current <sup>1</sup>		48		48		48		54	mA

1. Specified with V<sub>EEP</sub> and CS-SEL open.
2. Specified with V<sub>EEP</sub> and CS-SEL connected to V<sub>EE</sub>.
3. Specified with EN-SEL open.

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## 100K LVPECL DC Characteristics ( $V_{EE} = \text{GND}$ , $V_{CC} = +3.3\text{V}$ )

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,3</sup>	2255	2465	2305	2465	2305	2465	2305	2465	mV
$V_{OL}$	Output LOW Voltage <sup>1,3</sup>	1375	1745	1400	1655	1480	1680	1400	1680	mV
$V_{IH}$	Input HIGH Voltage									
	D/D, EN (PECL) <sup>1</sup> EN (CMOS/TTL)	2135 2000	2420 $V_{CC}$	2135 2000	2420 $V_{CC}$	2135 2000	2420 $V_{CC}$	2135 2000	2420 $V_{CC}$	mV
$V_{IL}$	Input LOW Voltage									
	D/D, EN (PECL) <sup>1</sup> EN (CMOS/TTL)	1490 GND	1825 800	1490 GND	1825 800	1490 GND	1825 800	1490 GND	1825 800	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	1910	2050	1910	2050	1910	2050	1910	2050	mV
$I_{IL}$	Input LOW Current EN <sup>4</sup>	0.5		0.5		0.5		0.5		$\mu\text{A}$
$I_{IH}$	Input HIGH Current EN <sup>4</sup>		150		150		150		150	$\mu\text{A}$
$I_{EE}$	Power Supply Current <sup>2</sup>		48		48		48		54	mA

- For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
- Specified with  $V_{EEP}$  and CS-SEL open.
- Specified with  $V_{EEP}$  and CS-SEL connected to  $V_{EE}$ .
- Specified with EN-SEL open.

## 100K PECL DC Characteristics ( $V_{EE} = \text{GND}$ , $V_{CC} = +5.0\text{V}$ )

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,3</sup>	3955	4165	4005	4165	4005	4165	4005	4165	mV
$V_{OL}$	Output LOW Voltage <sup>1,3</sup>	3075	3445	3100	3338	3100	3338	3100	3338	mV
$V_{IH}$	Input HIGH Voltage									
	D/D, EN (PECL) <sup>1</sup> EN (CMOS/TTL)	3835 2000	4120 $V_{CC}$	3835 2000	4120 $V_{CC}$	3835 2000	4120 $V_{CC}$	3835 2000	4120 $V_{CC}$	mV
$V_{IL}$	Input LOW Voltage									
	D/D, EN (PECL) <sup>1</sup> EN (CMOS/TTL)	3190 GND	3525 800	3190 GND	3525 800	3190 GND	3525 800	3190 GND	3525 800	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	3610	3750	3610	3750	3610	3750	3610	3750	mV
$I_{IL}$	Input LOW Current EN <sup>4</sup>	0.5		0.5		0.5		0.5		$\mu\text{A}$
$I_{IH}$	Input HIGH Current EN <sup>4</sup>		150		150		150		150	$\mu\text{A}$
$I_{EE}$	Power Supply Current <sup>2</sup>		48		48		48		54	mA

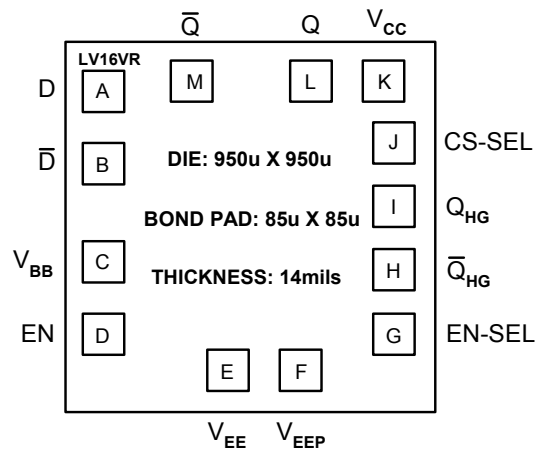
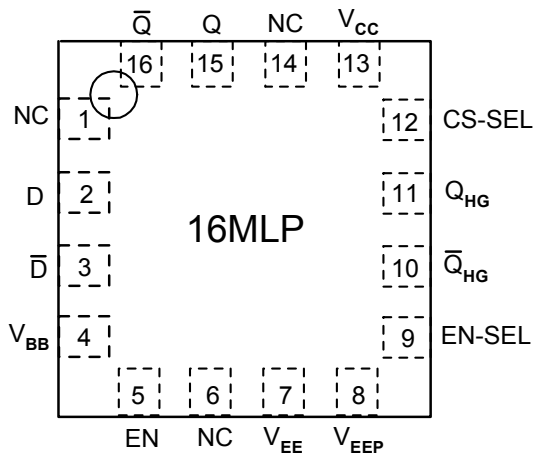
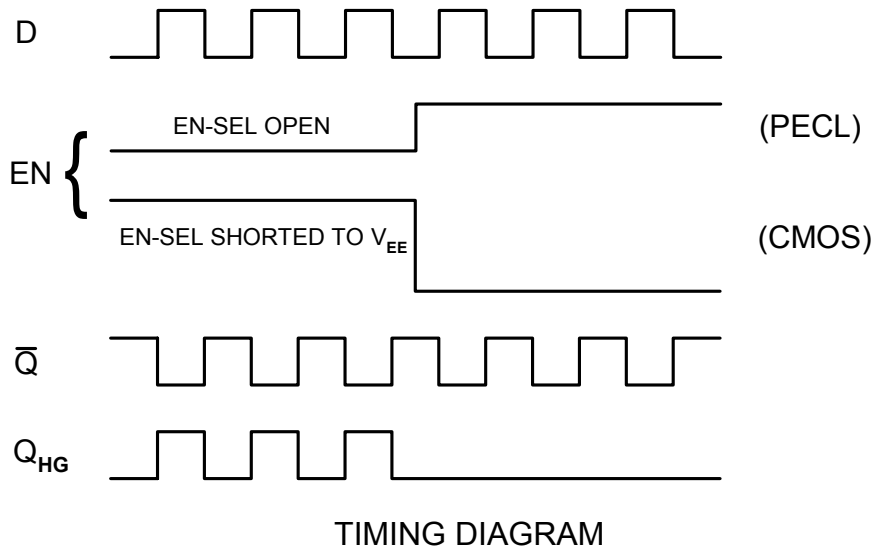
- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- Specified with  $V_{EEP}$  and CS-SEL open.
- Specified with  $V_{EEP}$  and CS-SEL connected to  $V_{EE}$ .
- Specified with EN-SEL open.

## AC Characteristics ( $V_{EE} = -3.0\text{V}$ to $-5.5\text{V}$ ; $V_{CC} = \text{GND}$ or $V_{EE} = \text{GND}$ ; $V_{CC} = +3.0\text{V}$ to $+5.5\text{V}$ )

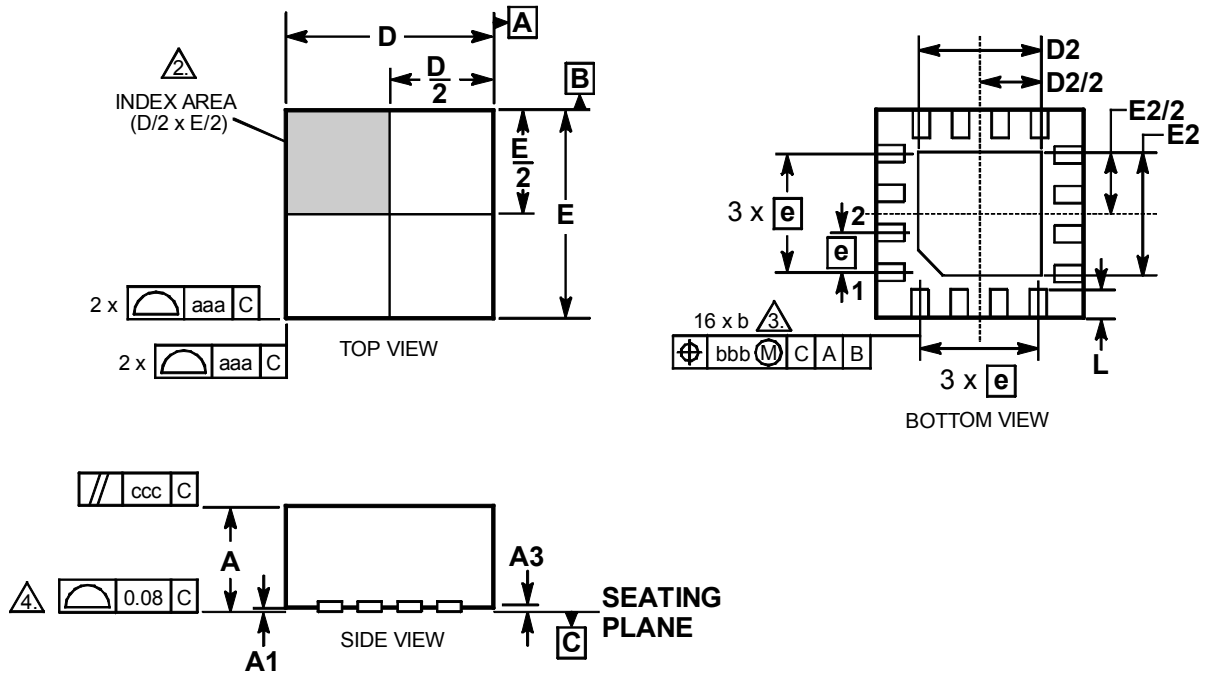
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{PLH} / t_{PHL}$	Propagation Delay													
	D to Q/Q Outputs <sup>1</sup> (SE) D to Q <sub>HG</sub> /Q <sub>HG</sub> Outputs <sup>1</sup> (SE)			400 550			400 550			400 550			430 630	ps
$t_{SKEW}$	Duty Cycle Skew <sup>2</sup> (SE)		5	20		5	20		5	20		5	20	ps
$V_{PP}(\text{AC})$	Minimum Input Swing <sup>3</sup>	80			80			80			80			mV
$t_r / t_f$	Output Rise/Fall Times <sup>1</sup> (20% - 80%)	100		260	100		260	100		260	100		260	ps

- Output specified with  $V_{EEP}$  and CS-SEL connected to  $V_{EE}$  with an AC coupled 50 $\Omega$  load.
- Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.
- $V_{PP}$  is the minimum peak-to-peak differential input swing for which AC parameters guaranteed. The device has a voltage gain of  $\approx 20$  to Q/Q outputs and a voltage gain of  $\approx 100$  to Q<sub>HG</sub>/Q<sub>HG</sub> outputs.

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**PACKAGE DIAGRAM  
MLP 16**



- NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
  2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
  3. DIMENSION  $b$  APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM THE PAD TIP.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	

## AZ100LEVEL16VR

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