LH1594/LH1595

80-Segment and 17-Common Outputs LCD Driver IC with A Built-in CGROM

DESCRIPTION

The LH1594/LH1595 are LCD drivers with a built-in character ROM suitable for driving small scale dot-matrix LCD panels, and which are capable of being directly connected to the bus line of a microcomputer. The 8-bit parallel or serial data transferred from a microcomputer is used to generate LCD drive signals for displaying characters. Incorporating a character ROM which has font characters configured in the format of 5 x 8 dots and a character RAM which allows the user to define characters, the LH1594/LH1595 provide a higher freedom of display. Since the LH1594/LH1595 have 80 output pins for a segment drive circuit and 17 output pins for a common drive circuit in a single chip, a display system for 16 characters x 2 lines can be implemented easily. The LH1594/LH1595 enable an LCD system for battery-operated, hand-carrying information equipment by securing lower power consumption and wider operating voltage range.

FEATURES

- Built-in CGROM : 240 characters
  (5 x 8 x 240 = 9 600 bits)
- Built-in CGRAM : 8 characters
  (5 x 8 x 8 = 320 bits)
- Built-in SEGRAM : 80 segments
  (16 x 7 = 112 bits)
- Built-in display data RAM : 32 characters
  (32 x 8 = 256 bits)
- Format of font character : 5 x 8 dots including 1 dot which also serves to display a cursor
- General 8-bit MPU interface : Possible to directly connect 80-family or 68-family MPU to bus line
- Possible to make serial interface
  (I^2C BUS* format is for LH1594)
- Ratio of display duty cycle :
  1/8, 1/9, 1/16 or 1/17 (selectable by command)
- Abundant command functions
  – Display of 2 lines by 16 characters
  – Display ON/OFF
  – Normal/reverse display control
  – Busy flag readout
  – Cursor display
  – Blinking : per character
  – Display double fonts lengthwise
  – Power saving mode
- LCD drive power circuit
  – Built-in booster circuit : Two or three times voltage boost is possible
  – Built-in voltage converter : Generates LCD drive voltages (V_0, V_1, V_2, V_3 and V_4) based on the boosted voltage
  – Built-in power bias ratio :
    1/4 or 1/5 bias (selectable by command)
  – Built-in electronic volume : Controllable in 16 steps
  – Supply voltages
    Logic system : +2.2 to +5.5 V
    LCD drive system : +4.0 to +11.0 V
- Operating temperature : –30 to +85 ˚C
- Package : 151-pin TCP (Tape Carrier Package)

* Purchase of I^2C components of Sharp Corporation, or one of its sublicensed Associated Companies conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

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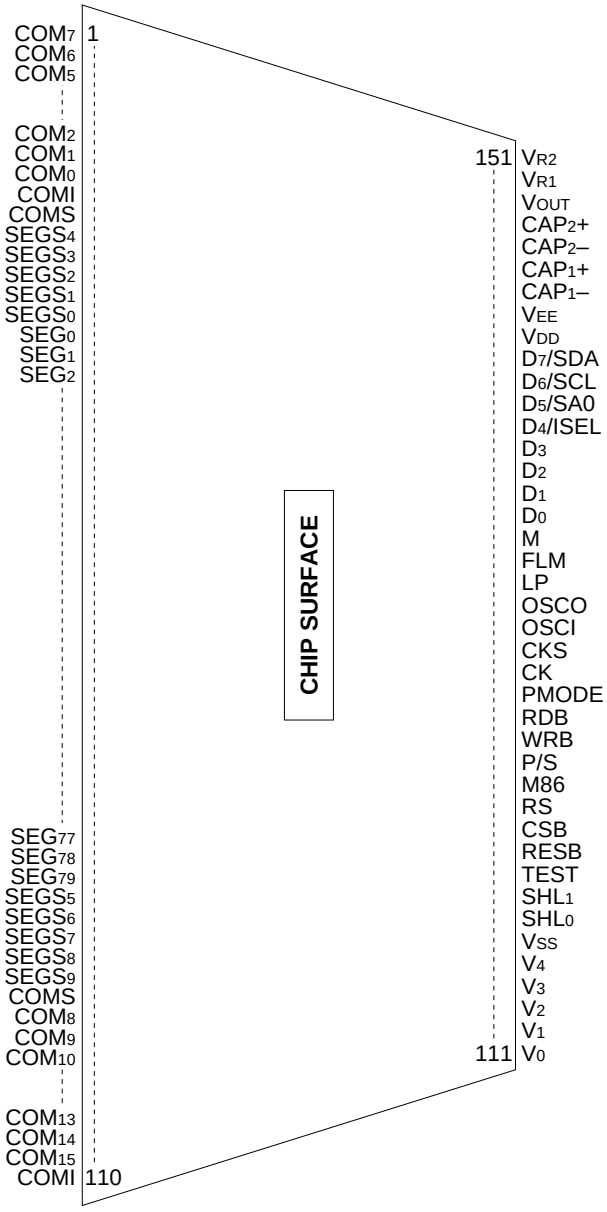
PIN CONNECTIONS

151-PIN TCP TOP VIEW



NOTE :

Doesn't prescribe TCP outline.

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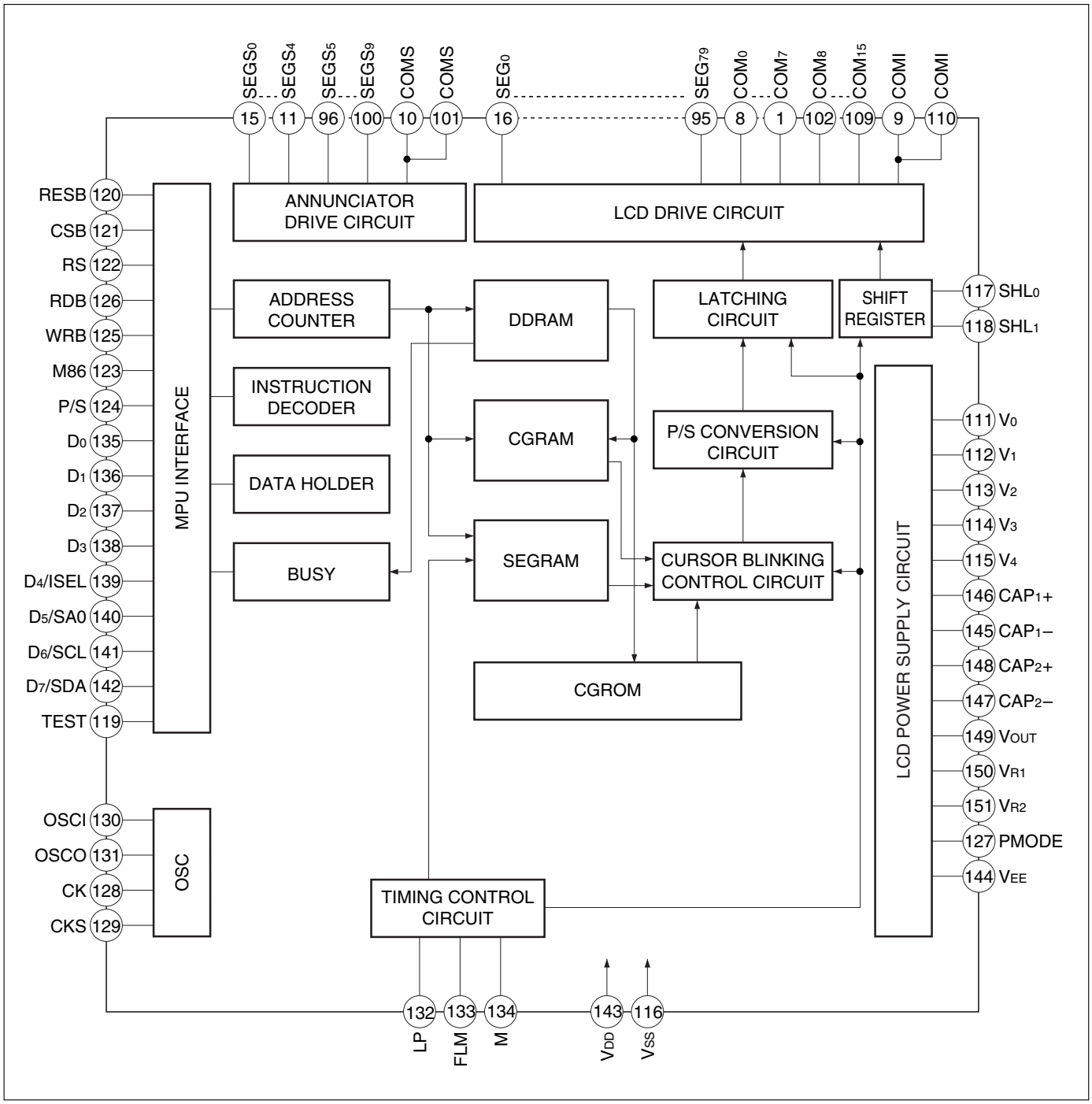
BLOCK DIAGRAM



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1. PIN DESCRIPTION

1.1. Power Supply Pins

SYMBOL	I/O	DESCRIPTION
V_{DD}	Power supply	Power supply pin for logic, connected to +2.2 to +5.5 V.
V_{SS}	Power supply	Ground pin, connected to 0 V.
V_0 V_1 V_2 V_3 V_4	Power supply	Bias power supply pins for LCD drive voltage. • When using an external power supply, convert impedance by using resistance-division of LCD drive power supply or operational amplifier before adding voltage to the pins. • When using the external power supply, maintain the following power supply conditions. $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_0$ • When the power supply circuit is ON, LCD drive voltage of V_0 to V_4 are generated by the internal booster circuit and voltage converter. • When using the internal power supply, be sure to connect each capacitor between V_0 to V_4 and V_{SS}.

1.2. LCD Power Supply Circuit Pins

SYMBOL	I/O	DESCRIPTION
CAP_{1+}	O	Connecting pin for the internal booster's capacitor + side. The capacitor is connected between CAP_{1-} and CAP_{1+}.
CAP_{1-}	O	Connecting pin for the internal booster's capacitor − side. The capacitor is connected between CAP_{1+} and CAP_{1-}.
CAP_{2+}	O	Connecting pin for the internal booster's capacitor + side. The capacitor is connected between CAP_{2-} and CAP_{2+}.
CAP_{2-}	O	Connecting pin for the internal booster's capacitor − side. The capacitor is connected between CAP_{2+} and CAP_{2-}.
V_{EE}	Power Supply	Voltage supply pin for generating boosted voltage in the internal booster circuit. Usually the same voltage level as V_{DD}.
V_{OUT}	Power Supply/ O	Output pin of boosted voltage in the internal booster circuit. The capacitor must be connected between V_{SS} and V_{OUT}.
V_{R1} V_{R2}	I	Used as input pins for voltage converter. Voltage must be input between the V_{EE} and V_{OUT} pins by voltage divided by resistors.
PMODE	I	Pin for controlling LCD power supply. A combination of PMODE pin and ON/OFF command of power supply (PON) enables selection of a specific drive operation.

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1.3. System Bus Pins

SYMBOL	I/O	DESCRIPTION
D_0 D_1 D_2 D_3 D_4/ISEL D_5/SA0 D_6/SCL D_7/SDA	I/O	• When set to parallel interface mode (P/S = "H"). Used as an 8-bit bi-directional data bus (D_7 to D_0), which is connected to 8-bit MPU data bus. • When set to serial interface mode (P/S="L"). Used as serial interface signals (SDA, SCL, SA0, ISEL). [SDA] **LH1594** : I/O pin for the I^2C BUS data line when serial interface is selected. Must be connected to a positive power supply via pull-up resistor. **LH1595** : Serial-data input pin at time of serial interface selection. [SCL] **LH1594** : Input pin for the I^2C BUS clock signal when serial interface is selected. Must be connected to a positive power supply via pull-up resistor. **LH1595** : Serial clock pin at time of serial interface selection. [SA0] **LH1594** : Used for LSB bit of slave address for I^2C BUS (7 bits width). Must be fixed to "H" or "L". **LH1595** : Must be set to "L". If set to "H", LH1595 operation is not warranty. [ISEL] **LH1594** : Used to identify I^2C BUS. When using I^2C BUS, fix to "H". If ISEL is set to "L", LH1594 operation is not warranty. **LH1595** : Must be set to "L". If set to "H", LH1595 operation is not warranty.
CSB	I	Chip selection input pin that decoded address bus signal is input.
RS	I	Distinguishes display RAM data/commands of D_7 to D_0 data transferred from MPU. 1 : The data of D_7 to D_0 show the display RAM data. 0 : The data of D_7 to D_0 show the command data.
RESB	I	Initialized by setting to "L". The reset signals of the system are normally input. Reset operation is performed in accordance with RESB signal level.
RDB (E)	I	• In connecting to 80-family MPU : This RDB is a pin for connecting the RDB signal of 80-family MPU. When the signal enters in the "L" state, the data bus of this IC turns to the "output" state. • In connecting to 68-family MPU : This RDB becomes a pin for connecting the enable clock signal of 68-family MPU. When the signal enters in the "H" state, the data bus of this IC turns to the "active" state.

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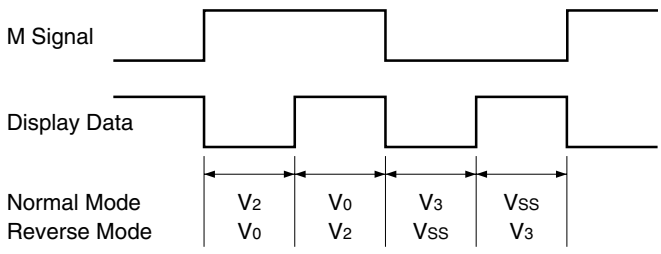
SYMBOL	I/O	DESCRIPTION
WRB (R/W)	I	• In connecting to 80-family MPU : This WRB is a pin for connecting the WRB signal of 80-family MPU, and when WRB signal is "L", this pin is "active". The data bus signal is input at the rising edge of WRB signal. • In connecting to 68-family MPU : This WRB becomes a pin for connecting the R/W signal of controlling read/write of 68-family MPU. R/W = "H" : Read R/W = "L" : Write
M86	I	MPU interface-type shift pin. M86 = "H" : 68-family interface M86 = "L" : 80-family interface Fixed to either "H" or "L".
P/S	I	Used to shift between parallel interface and serial interface. P/S = "H" for parallel interface. Fix SDA and SCL pins to either "H" or "L". P/S = "L" for serial interface. Fix D_3 to D_0 pins to High-Z, RDB and WRB pins to either "H" or "L".
TEST	I	For testing. Fix to "L".

1.4. LCD Drive Circuit Signals

SYMBOL	I/O	DESCRIPTION
LP	O	The latching signal of display data to count up the display line counter at the rising, and to output the LCD drive signals at the falling.
FLM	O	Output pin for LCD display synchronous signals (first line marker). When FLM pin is set to "H", the display starting line address is preset in the display line counter.
M	O	Output pin for alternating signals of LCD drive output.
SEG_0-SEG_{79}	O	Segment output pins for LCD drive. According to the data of the display data, non-lighted at "0", lighted at "1" (Normal mode) non-lighted at "1", lighted at "0" (Reverse mode) and, by a combination of M signal and display data, one signal level among V_0, V_2, V_3, and V_{SS} is selected. 

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<table>
<tr><th>SYMBOL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>COM0-COM15</td><td>O</td><td>Common output pins for LCD drive.
By a combination of the scanning data and M signal, one signal level among V0, V1, V4 and VSS is selected.
<table>
<tr><th>Data</th><th>M</th><th>Output level</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>COMI</td><td>O</td><td>Common output pin for marker display.
When executing duty + 1 (PLUS) command, it functions as a common output pin.
Having two output pins for COMI, they output same level. It is able to select output pin for COMI when wiring pattern.
<table>
<tr><th></th><th>Duty + 1 ON</th><th>Duty + 1 OFF</th></tr>
<tr><td>COMI state</td><td>COM16 (when displaying 2 lines),
COM8 (when displaying 1 line)</td><td>V0 or V4</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>Common drive output pin for static LCD drive (for annunciator display).
Having two output pins for COMS, they output same level. It is able to select output pin for COMS when wiring pattern.
When DA = "0", outputs VSS level.</td></tr>
<tr><td>SEGS0-SEGS9</td><td>O</td><td>Segment drive output pin for static LCD drive (for annunciator display).
One level is selected from VDD and VSS levels depending on the combination of COMS signal and display data.
When DA = "0", outputs VSS level.</td></tr>
<tr><td>SHL0
SHL1</td><td>I</td><td>Input pin to control the transfer direction of the segment and common signal output data.
SHL0 = "0" : Segment data display direction is SEG0 to SEG79.
SHL0 = "1" : Segment data display direction is SEG79 to SEG0.
SHL1 = "0" : Common data display direction is COM0 to COM15.
SHL1 = "1" : Common data display direction is COM15 to COM0.</td></tr>
</table>

1.5. Pins for Oscillation Circuit

<table>
<tr><th>SYMBOL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>OSCI
OSCO</td><td>I
O</td><td>Feedback-resistance connecting pin for the internal oscillation circuit.</td></tr>
<tr><td>CK</td><td>I</td><td>Input pin of display master clock.
When using CK pin as an input of the master clock, fix OSCI pin to VSS.
When using the internal oscillation circuit as the display master clock, fix CK pin to VSS.</td></tr>
<tr><td>CKS</td><td>I</td><td>Selection input pin of display master clock.
CKS = "H" : Input the external clock to CK pin.
CKS = "L" : The internal oscillation circuit by using OSCI and OSCO pins is used.</td></tr>
</table>

* Master clock : Clock for oscillation circuit or external clock.

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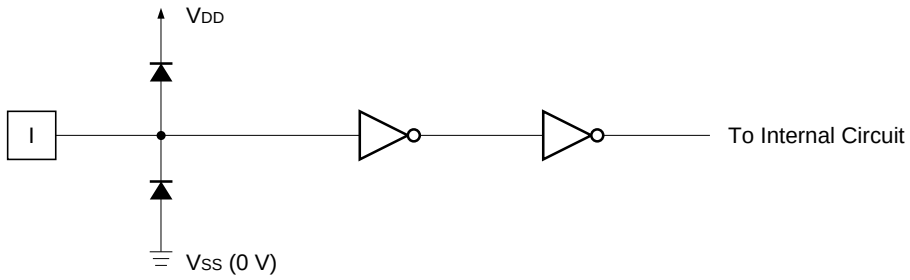
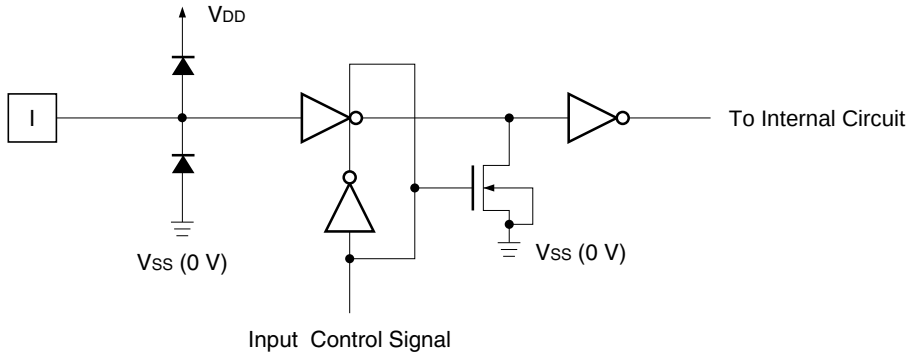
1.6. Input/Output Circuits



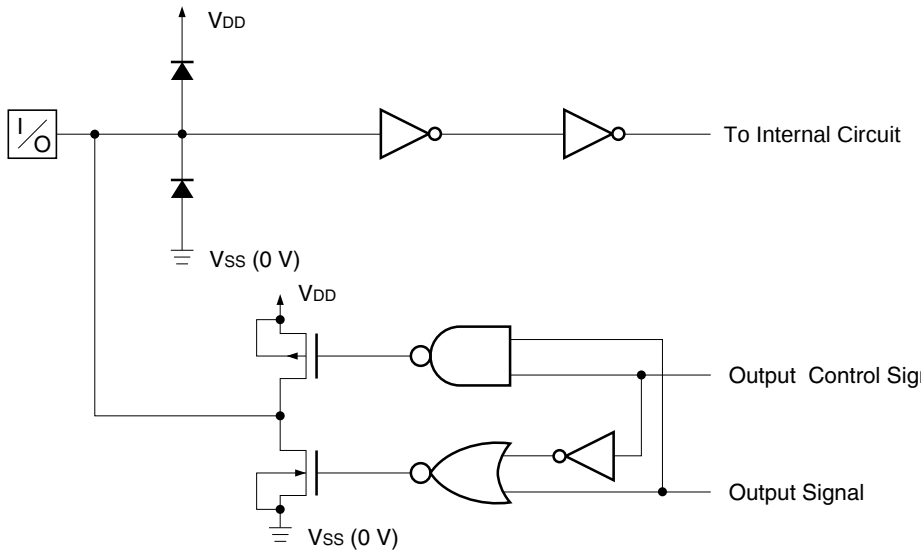
【Applicable pins】
M86, P/S, SHL0, SHL1,
OSCI, CK, CKS,
PMODE, RESB, TEST

Fig. 1 Input Circuit (1)



【Applicable pins】
CSB, RS, WRB,
RDB

Fig. 2 Input Circuit (2)



【Applicable pin】
OSCO

Fig. 3 Input/Output Circuit (1)

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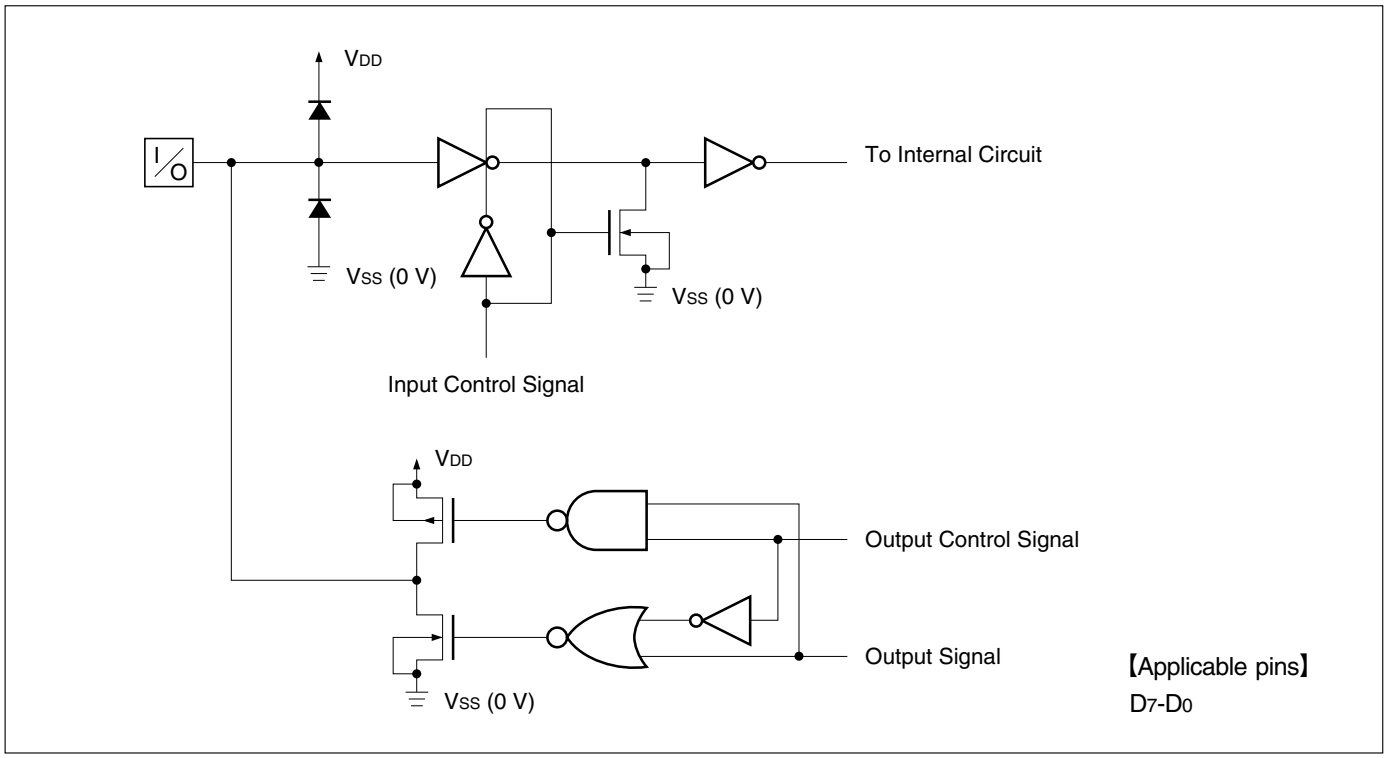

Fig. 4 Input/Output Circuit (2)

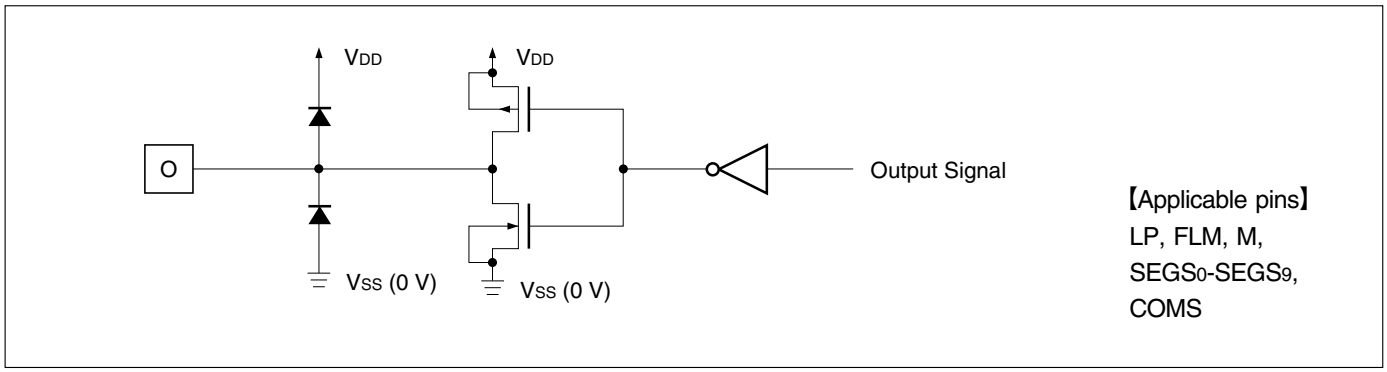

Fig. 5 Output Circuit

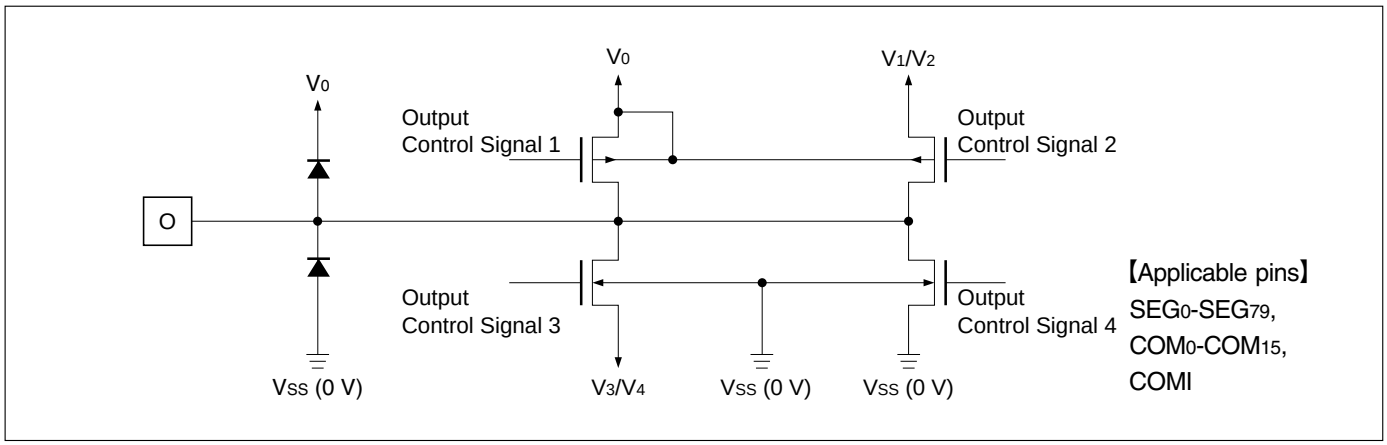

Fig. 6 LCD Drive Output Circuit

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2. FUNCTIONAL DESCRIPTION

2.1. MPU Interface

2.1.1. INTERFACE TYPE SELECTION

The LH1594/LH1595 transfer data through 8-bit parallel I/O (D_7 to D_0) or serial data input (SDA, SCL).

The selection between parallel interface and serial interface is made by setting the state of P/S pin to "H" or "L".

P/S	I/F TYPE	CSB	RS	RDB	WRB	M86	SDA	SCL	DATA BUS
H	Parallel	CSB	RS	RDB	WRB	M86	–	–	D_7 to D_0
L	Serial	– (LH1594) CSB (LH1595)	– (LH1594) RS (LH1595)	–	–	–	SDA	SCL	–

2.1.2. PARALLEL INPUT

The LH1594/LH1595 can transfer data in parallel by directly connecting 8-bit MPU to the data bus when parallel interface is selected with P/S pin.

As an 8-bit MPU, either 80-family MPU interface or 68-family MPU interface is selected with M86 pin.

M86	MPU TYPE	CSB	RS	RDB	WRB	DATA
H	68-family MPU	CSB	RS	E	R/W	D_7 to D_0
L	80-family MPU	CSB	RS	RDB	WRB	D_7 to D_0

2.1.3. DATA IDENTIFICATION

The LH1594/LH1595 can identify the data of 8-bit data bus by combinations of RS, RDB and WRB signals.

RS	68-FAMILY	80-FAMILY		FUNCTION
	R/W	RDB	WRB	
0	1	0	1	Reads out busy flags
0	0	1	0	Writes to commands
1	1	0	1	Reads from data RAM
1	0	1	0	Writes to data RAM

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2.1.4. SERIAL INTERFACE

[FOR LH1594]

The serial interface for the LH1594 is I^2C BUS format. I^2C BUS is for bi-directional two-line communication between different ICs or other modules.

LH1594 always operates as a slave device, so sending data of start and stop is controlled by start/stop bits which are sent by master device.

[FOR LH1595]

The serial interface of LH1595 can accept inputs of SDA and SCL in the chip selection state (CSB = "L"). When not in the chip selection state, the internal shift register and counter are reset to their initial condition.

Serial data SDA are input sequentially in order of D_7 to D_0 at the rising edge of serial clock (SCL) and are converted into 8-bit parallel data (by serial to parallel conversion) at the rising edge of the 8th serial clock, being processed in accordance with the data.

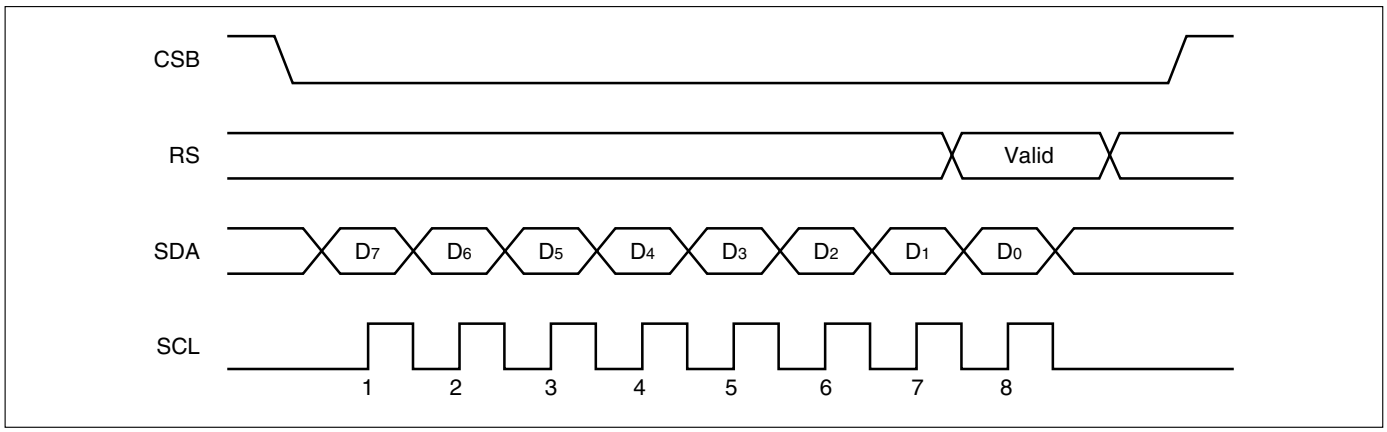
The identification whether the serial data inputs (SDA) are display data or commands is judged by input to RS pin.

RS = "H" : Display data

RS = "L" : Commands

After completing 8-bit data transferring, or when making no access, be sure to set serial clock input (SCL) to "L".

Protection of SDA and SCL signals against external noise should be taken in actual wiring. To prevent the successive recognition errors of transferring data from external noise, release the chip selection state (CSB = "H") at every completion of 8-bit data transferring.



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2.2. Busy Flag

When the busy flag is "1", this indicates that the LH1594/LH1595 are internally operating. In this state, the LH1594/LH1595 do not accept the next instruction. As shown in the command function table, the busy flag is output to the data bus D_7 when RS is "0" or R/W is "1" (for the 68-family interface), and when RS is "0" or RDB is "0" (for the 80-family interface). The busy flag is generated only when the display clear command or the ACL command is executed. It must be confirmed that the busy flag is "0" before the next instruction can be executed.

2.3. Address Counter (AC)

The address counter (AC) is used to address the DDRAM, CGRAM, or SEGRAM. When the addressing instruction is written into the AC, the address information is transferred to the AC. Simultaneously, the instruction also determines which RAM is to be selected among the DDRAM, CGRAM, and SEGRAM. After data is written into (read out from) the DDRAM, CGRAM, or SEGRAM, the AC is automatically counted up or down by one. As shown in the command function table, the AC outputs data to the data buses D_6 to D_0 when RS is "0" and R/W is "1" (for the 68-family interface).

2.4. Display Data RAM (DDRAM)

The DDRAM stores display data presented with 8-bit character codes. Its capacity is 32 characters in a format of 8 bits.

2.5. Character Generator ROM (CGROM)

The CGROM generates 240 different character patterns in a format of 5 x 8 dots from 8-bit character codes.

2.6. Character Generator RAM (CGRAM)

The CGRAM allows user-written programs to freely overwrite characters. Eight different types of characters can be written in a format of 5 x 8 dots.

2.7. Segment RAM (SEGRAM)

The SEGRAM allows user-written programs to freely control icons and marks. When the COMI outputs the selection signal, the data stored in the SEGRAM is read out to display 80 segments.

2.8. Timing Generation Circuit

The timing generation circuit generates the timing signals to operate the internal circuits, including the DDRAM, CGROM, CGRAM, and SEGRAM, as well as those for segment and common drive outputs. Readout of the display data to the LCD drive circuit is completely independent of MPU. Therefore, a MPU that has no relationship the read-out operation of the display data can access it.

2.9. Cursor Blinking Control Circuit

This circuit generates the cursor, the blinking cursor, or the reverse-display cursor. The cursor or the blinking cursor appears in the digit that corresponds to the address in the DDRAM which is specified in the address counter.

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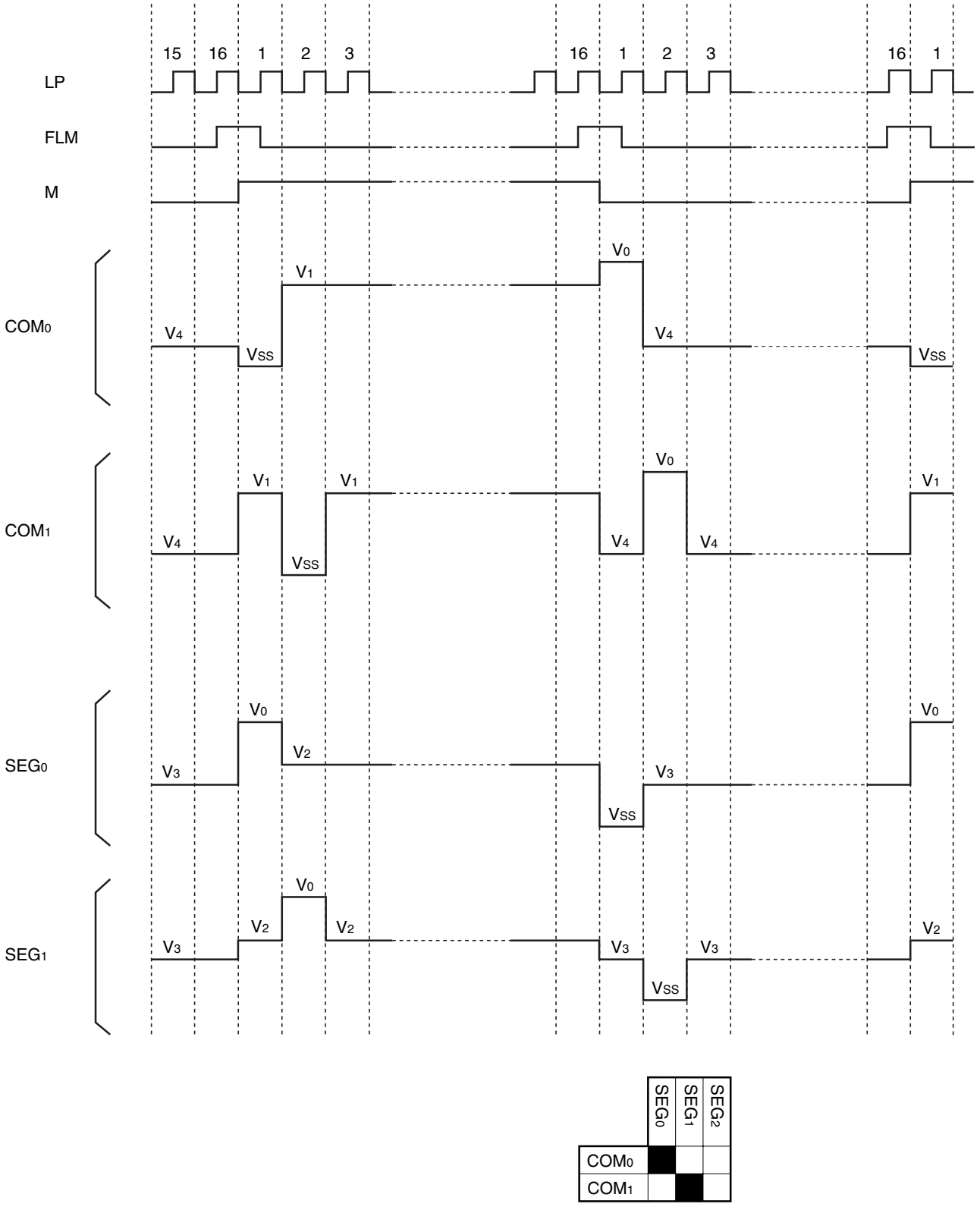
2.10. Output Timing of LCD Driver

Display timing at normal mode, 1/16 duty



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2.11. LCD Drive Circuit

This drive circuit generates 4 levels of LCD drive voltage. The circuit has 80 segment outputs and 17 common outputs and outputs combined display data and M signal. Character data is transferred by 80 bits from the CGROM or the CGRAM to the segment drive circuit.

One of the common outputs, COMI is for marker display only. A common drive circuit that has a shift register sequentially outputs common scan signals.

2.12. Oscillation Circuit

The frequency of this CR oscillator is controlled by the feedback resistor R_F.

The output from this oscillator is used as the timing signal source of the display and the boosting clock to the booster circuit.

If external clock is used, maintain OSCI pin at V_{SS} and OSCO pin open (NC), and feed the clock to CK pin.

The duty cycle of the external clock must be 50%.

The CKS pin is used to select either internal oscillation circuit or external clock.

CKS	OSCILLATION CIRCUIT	EXTERNAL CLOCK
L	Enabled	Disabled
H	Disabled	Enabled

2.13. Annunciator Circuit

This is the drive circuit which generates 2-value levels for static LCD drive. This circuit provides displaying annunciators for icons or marks. It consists of common drivers (COMS x 2) and 10 segment drivers ($SEGS_0$ to $SEGS_9$). One level is selected from V_{DD} and V_{SS} levels for static LCD drive. When this circuit is not displaying annunciator, it outputs V_{SS} level.

2.14. Power Supply Circuit

This circuit supplies voltages necessary to drive an LCD. The circuit consists of booster circuit and voltage converter.

Boosted voltage from the booster circuit is fed to the voltage converter which converts this high input voltage into V_0, V_1, V_2, V_3 and V_4 which are used to drive the LCD.

This internal power supply should not be used to drive a large LCD panel containing many pixels or a large LCD panel that has large capacity consisting of more than one chip. Otherwise, display quality will degrade considerably. Instead, use an external power supply.

This internal power supply is controlled by the power supply circuit ON/OFF command (PON).

When the internal power supply is turned off, the booster circuit and voltage converter are also turned off.

When using the external power supply, turn off the internal power supply, disconnect pins CAP_1+, CAP_1-, CAP_2+, CAP_2-, V_{OUT}, V_{EE}, V_{R1} and V_{R2}, and keep PMODE pin at V_{SS}. Then, feed external LCD drive voltages to pins V_0, V_1, V_2, V_3 and V_4.

This circuit can be changed by the state of PMODE pin.

PON	PMODE	BOOSTER CIRCUIT	VOLTAGE CONVERTER	EXTERNAL VOLTAGE INPUT	NOTE
0	0	Disabled	Disabled	V_0, V_1, V_2, V_3, V_4	1
0	1	Disabled	Disabled	V_0, V_1, V_2, V_3, V_4	1
1	0	Enabled	Enabled	–	
1	1	Disabled	Enabled	V_{OUT}, V_{R1}, V_{R2}	2

NOTES :

1. Because the booster circuit and voltage converter are not functioning, disconnect pins CAP_1+, CAP_1-, CAP_2+, CAP_2-, V_{OUT}, V_{EE}, V_{R1}, and V_{R2}.
   Apply external LCD drive voltages to corresponding pin.
2. Because the booster circuit is not functioning, disconnect pins CAP_1+, CAP_1-, CAP_2+, CAP_2- and V_{EE}.
   Derive the voltage source to be supplied to the voltage converter from V_{OUT} pin and then output LCD drive voltage to V_{R1}, and V_{R2} pins. The voltage level at V_{R1} and V_{R2} pins must be $V_{R2} \leq V_{R1} \leq V_{OUT}$.

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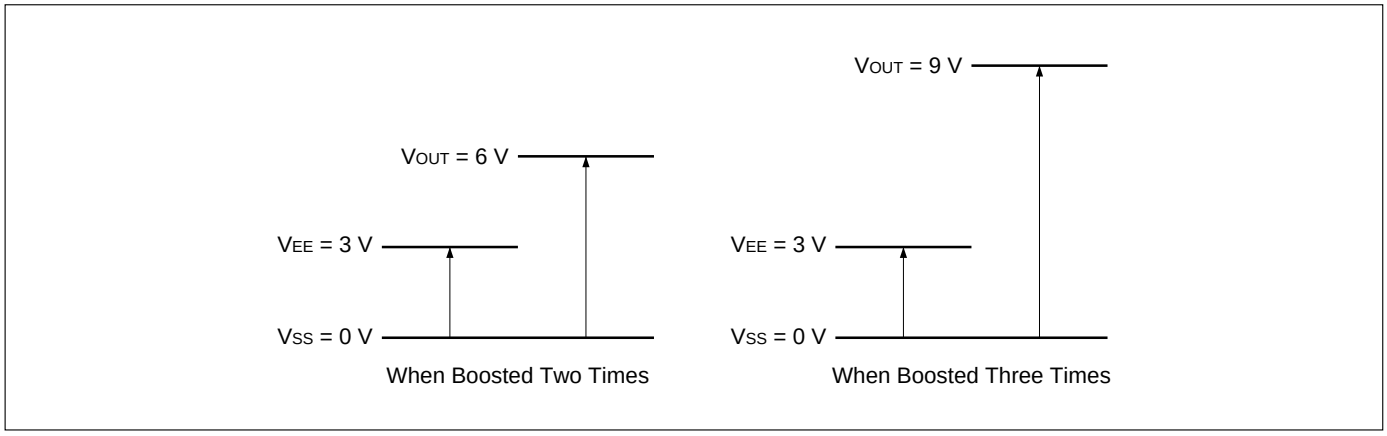
2.15. Booster Circuit

Placing capacitor C_1 across CAP_{1+} and CAP_{1-} and across CAP_{2+} and CAP_{2-} and across V_{OUT} and V_{SS} boosts the voltage coming from V_{EE} and V_{SS} three times and outputs the boosted voltage to V_{OUT} pin.

Placing C_1 across CAP_{1+} and CAP_{1-} and shorting together pins CAP_{1+} and CAP_{2+} limits the output on V_{OUT} pin to two times the input voltage.

Since the booster circuit uses the clock derived from the internal oscillation circuit or external clock as the boosting clock, the internal oscillation circuit must be enabled, or if external clock is selected, it must be fed to CK pin.

The output level at the V_{OUT} pin does not exceed the recommended maximum operating voltage (11.0 V) when the voltage is boosted. If this value is exceeded, the operation of the LH1594/LH1595 are not covered by warranty.



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2.16. Voltage Control Circuit

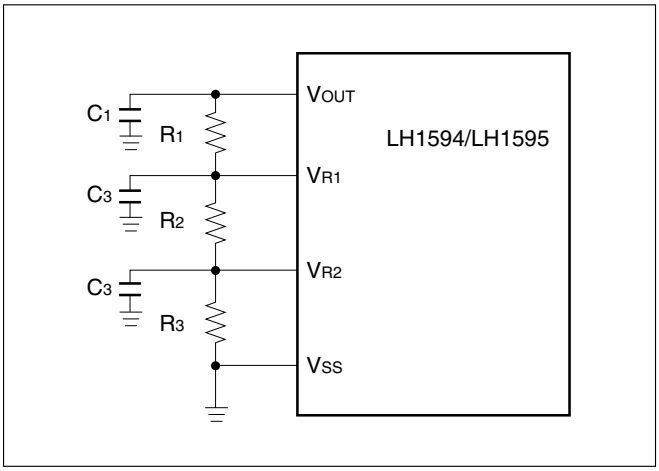
The boosted voltage at the V_{OUT} pin is connected to the V_{R1} and V_{R2} pins and then the LCD drive voltages (V_0, V_1, V_2, V_3, and V_4) are generated via the voltage converter circuit. The input level at the V_{R1} and V_{R2} must meet the electric potential condition of $V_{R1} \geq V_{R2}$. The internal electronic volume divides the electric potential between the V_{R1} and V_{R2} into 16 segments.

Since the V_{R1} and V_{R2} pins have high input impedance, the input voltage levels at the V_{R1} and V_{R2} are determined by the resistance ratio of R_1, R_2, and R_3. The current flowing between the V_{OUT} and V_{SS} pins is determined by the combined resistance of R_1, R_2, and R_3.

Therefore, R_1, R_2, and R_3 must be selected in accordance with the above current as well as the input voltage levels at the V_{R1} and V_{R2}.

The boosted voltage at the V_{OUT} pin originates from the voltage supplied at the V_{EE} pin.

Thus, the DC path current generated with R_1, R_2, and R_3 connected between the V_{OUT} and V_{SS} pins is supplied as current at the V_{EE} pin. The electric current value, three times larger than the DC path current generated between the V_{OUT} and V_{SS} pins when the voltage is tripled, is added as supply current at the V_{EE} pin (two times larger current is added for doubled voltage). Take sufficient care that the input levels at the V_{R1} and V_{R2} pins do not fluctuate with external noise (connect capacitor C_3).



Example of Voltage Control Circuit

2.17. Electronic Volume

The voltage converter incorporates an electronic volume, which allows the LCD drive voltage level V_0 to be controlled with a command and also allows the tone of LCD to be controlled.

If 4-bit data is stored in the register of the electronic volume, one level can be selected among 16 voltage values for the LCD drive voltage V_0.

The voltage control range of the electronic volume is determined by the input voltage levels at the V_{R1} and V_{R2}. This means that the voltage range of (V_{R1} to V_{R2}) is the controllable voltage range of the electronic volume. The electric potential relation between the V_{R1} and V_{R2} pins must be $V_{R1} \geq V_{R2}$. The input voltage levels at the V_{R1} and V_{R2} pins must be selected in accordance with the voltage levels to be obtained with the electronic volume.

2.18. LCD Drive Voltage Generation Circuit

The voltage converter contains the voltage generation circuit. The LCD drive voltages other than V_0, that is, V_1, V_2, V_3 and V_4, are obtained by dividing V_0 through a resistor network. The LCD drive voltages from LH1594/LH1595 are biased at 1/4 or 1/5.

When using the internal power supply, connect a stabilizing capacitor C_2 to each of pins V_0 to V_4.

The capacitance of C_2 should be determined while observing the LCD panel to be used. In this case, connect a capacitor C_3 to stabilize input voltage to V_{R1} and V_{R2}. A value of C_3 can be defined selectively.

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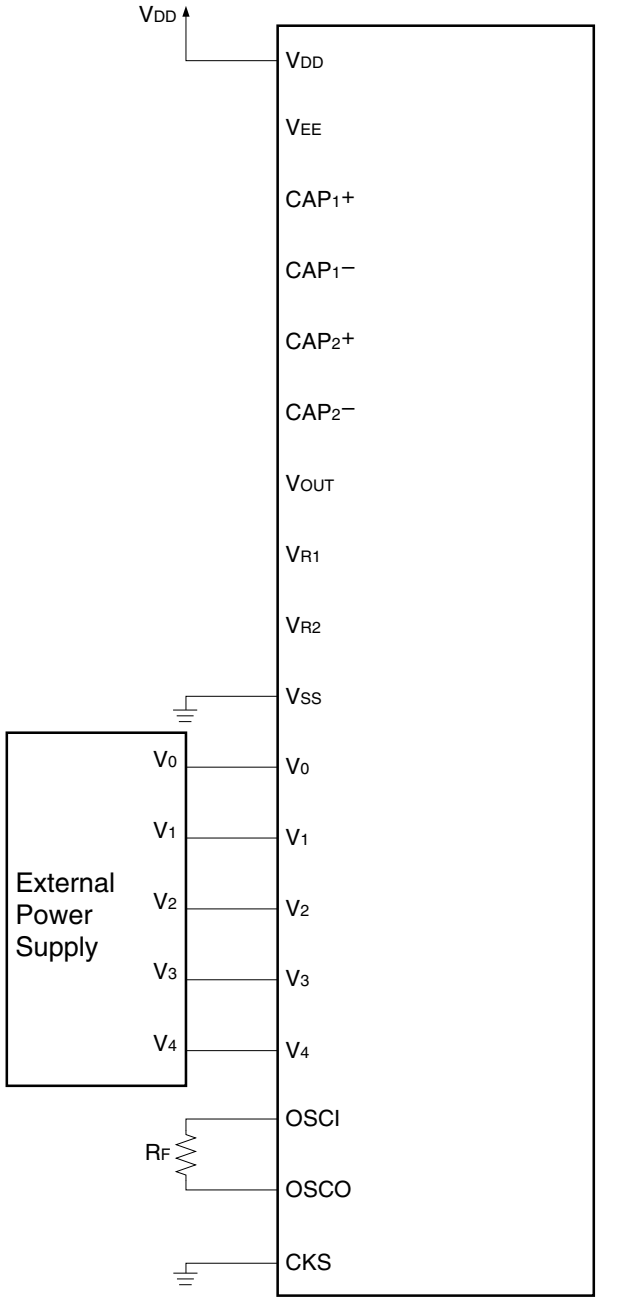
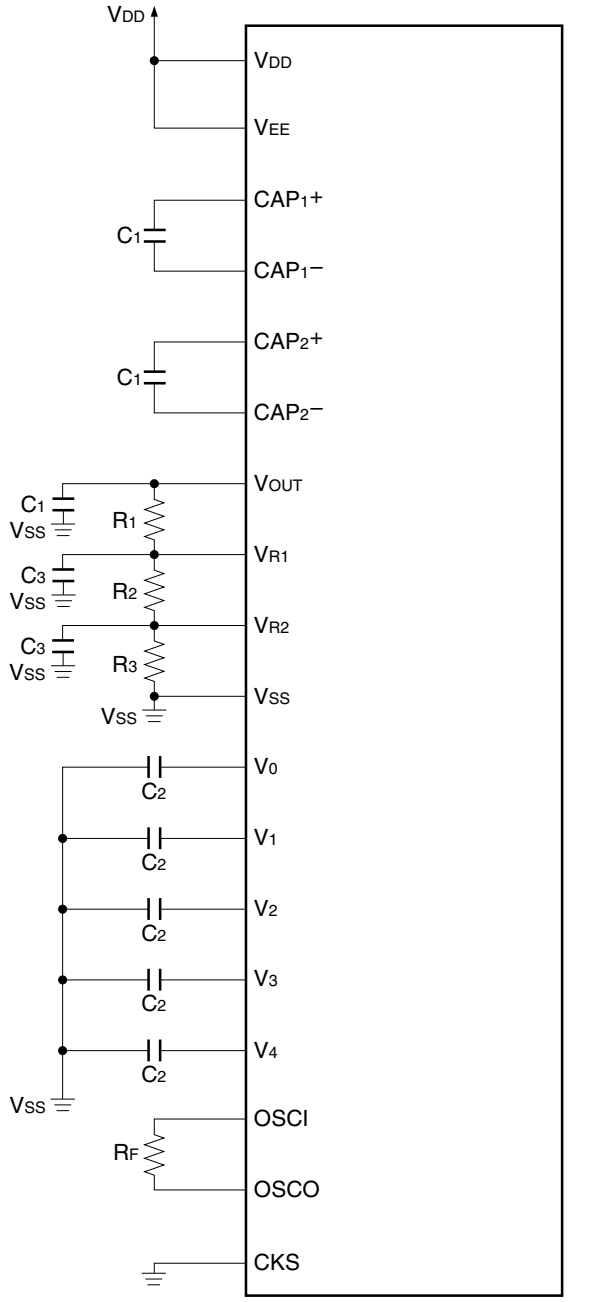
2.19. Example of Power Supply Circuit



When Using The External Power Supply



When Using The Internal Power Supply

Recommended values

C_1	1.0 to 5.0 µF (B)*
C_2	0.1 to 5.0 µF (B)*
C_3	0.01 to 0.1 µF
R_F	1.2 MΩ
$R_1 + R_2 + R_3$	2.0 to 4.0 MΩ

* B characteristics must be used with C_1 and C_2.

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2.20. Initialization

The LH1594/LH1595 are initialized by setting RESB pin to "L". Normally, RESB pin is initialized together with MPU by connecting to the reset pin of MPU. When power is ON, be sure to reset operation.

PARAMETER	PIN DESCRIPTION
Function	RE = 0 : Writes to expanded register disabled. BE = 0 : SEGRAM blink OFF DUB = 0 : Normal display mode (Displaying double fonts lengthwise OFF) BT = 0 : Blinking type is normal/ reverse display.
Entry mode	I/D = 1 : Increments by one. S = 0 : No shift occurs.
Display mode	NL = 0 : Displays 2 lines.
Display control (1)	D = 0 : Display OFF C = 0 : Cursor OFF B = 0 : Blink OFF
Display control (2)	PLUS = 0 : 1/16 duty REV = 0 : Normal display ALON = 0 : Normal display
Power control	HALT = 0 : Power saving OFF PON = 0 : Power supply circuit OFF ACL = 0 : ACL operation OFF BIAS : 1/5 bias
Register in electronic volume	(1, 1, 1, 1)
Annunciator control	DA = 0 : Annunciator display OFF I0 to I9 = (0, 0, 0, 0, 0, 0, 0, 0, 0, 0)
RAM data	DDRAM : Not determined. CGRAM : Not determined. SEGRAM : Not determined.

3. PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

① When using an external power supply

- When connecting the power supply
  After connecting the logic system power supply, make reset operation and then apply external LCD drive voltages to corresponding pins. (V_0, V_1, V_2, V_3, V_4 or V_{OUT}, V_{R1} and V_{R2})
- When disconnecting the power supply
  After executing HALT command, disconnect external LCD drive voltages and then disconnect the logic system power supply.

② When using the internal power supply

- When connecting the power supply
  After connecting the logic system power supply, make reset operation and then execute PON command.
- When disconnecting the power supply
  After executing HALT command, disconnect the logic system power supply.

It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_{OUT} or V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

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4. COMMAND FUNCTION

Since the instructions for the LH1594/LH1595 are executed within execution cycle time, the MPU can be operated at a high speed without a waiting time. The busy state check is only necessary when the display clear command or the ACL command is executed.

4.1. Command Function Table

INSTRUCTION	INSTRUCTION CODE										DESCRIPTION
	RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
RAM data write	0/1	1	WRITE DATA								Writes to data RAM.
RAM data read	0/1	1	READ DATA								Reads from data RAM.
Display clear set	0/1	0	0	0	0	0	0	0	0	1	Specifies address 0 from DDRAM in AC after clearing all display.
Cursor home set	0/1	0	0	0	0	0	0	0	1	*	Allocates address 0 for DDRAM in AC and resets shifted display.
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Specifies cursor moving direction and whether or not to shift display.
Display mode set	1								*	NL	Sets display 2 lines or 1line (NL).
Display control (1) set	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF all display (D). Turns ON/OFF cursor (C). Specifies blinking character indicated by cursor (B).
Display control (2) set	1							PLUS	REV	ALON	Specifies duty + 1 (PLUS). Displays data in reverse display (REV). Turns ON all display (ALON).
Cursor/display shift set	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing data in DDRAM.
Power control set	1						BIAS	HALT	PON	ACL	Specifies HALT ON (HALT). Turns ON power supply circuit (PON). Specifies resetting (ACL). Sets bias ratio (BIAS).
Function set	0/1	0	0	0	1	BE	DUB	RE	BT	*	Enables writes to expanded register (RE). Enables blinking for SEGRAM (BE). Enables display double font lengthwise (DUB). Sets blinking character type (BT).
CGRAM address set	0	0	0	1	ACG						Sets CGRAM address.
SEGRAM address set	1				*	*	ASEG				Sets SEGRAM address.
DDRAM address set	0	0	1	0	*	ADD					Sets DDRAM address.
Electronic volume set	1				*	*	DVOL				Sets electronic volume.
Annunciator control set	0	0	1	1	I5	I4	I3	I2	I1	I0	Sets data for annunciator (I0 to I9).
	1				DA	*	I9	I8	I7	I6	Enables display annunciator (DA).
Busy flag/address read	0/1	0	BF	*	AC						Reads out busy flag and data from AC.

* mark means "Don't care".

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4.2. Write Data to RAM

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0/1	1	D	D	D	D	D	D	D	D

Writes binary 8-bit data D_7 to D_0 to the CGRAM or DDRAM or SEGRAM.
The RAM is to be written into is determined by the previous specification of CGRAM or DDRAM or SEGRAM address setting. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode.

4.3. Read Data to RAM

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0/1	1	D	D	D	D	D	D	D	D

Reads binary 8-bit data D_7 to D_0 from the CGRAM or DDRAM or SEGRAM.
The most recent set address command determines the RAM is to be read. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode.

4.4. Display Clear Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0/1	0	0	0	0	0	0	0	0	1

Space code "20_H" (for 32 characters) is written to all addresses in the DDRAM. The address counter specifies DDRAM address 0.
If the display is shifted, it is reset in place. This means that the display is cleared and the cursor or blinking cursor, if displayed, returns to the left end in the first line.
Set the I/D of the increment mode to "Increment". "S" will not change.
When the clearing of the display starts, the busy flag is generated. Therefore, to execute an instruction after clearing the display, monitor the busy flag and then execute the next instruction after checking that the flag has been released; or allow a waiting period of 34 times the master clock frequency.

4.5. Cursor Home Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0/1	0	0	0	0	0	0	0	1	*

* mark means "Don't care".

Specify DDRAM address 0 in the address counter. If the display is shifted, it is reset in place. The data in the DDRAM remains unchanged. The cursor or the blinking cursor, if displayed, returns to the left end in the first line.

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4.6. Entry Mode Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	1	I/D	S

When the extended register enable bit (RE) is "0", the following I/D, and S bits are accessed :

I/D : When any character code is written into or read out from the DDRAM, the DDRAM address is shifted by +1 (I/D = 1) or −1 (I/D = 0). In case of +1, the cursor or the blinking cursor moves to the right. This is also applicable when any data is written into or read out from the CGRAM or SEGRAM.

S : If S = 1, the entire display is shifted to either the left or right when any character code is written into the DDRAM. If I/D = 1, the entire display is shifted to the left; or if I/D = 0, the entire display is shifted to the right. Therefore, if I/D = 1, the cursor looks stationary with only the display shifted. When any character code is read out from the DDRAM, the display is not shifted. If S = 0, the display remains unshifted. When any data is written into or read out from the CGRAM or SEGRAM, the display also remains unshifted.
When duty + 1 command is ON (PLUS = 1), if S = 1 and any code is written into DDRAM, the line that COMI scans is also shifted, so that this command is allowed only when duty + 1 command is OFF (PLUS = 0) state.

4.7. Display Mode Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	1	*	NL

* mark means "Don't care".

When the extended register enable bit (RE) is "1", the following NL bit is accessed :

NL : This command selects the displaying lines.
NL = "0" : Displays 2 lines. Display duty ratio is 1/16.
NL = "1" : Displays 1 line. Display duty ratio is 1/8.

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4.8. Display Control (1) Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	1	D	C	B

When the extended register enable bit (RE) is "0", the following D, C, and B bits are accessed :

D : Turns ON the display if D = 1; or turns OFF the display if D = 0. Since the data in the DDRAM is retained, the display can be resumed by specifying D = 1.

C : Displays the cursor if C = 1; or hides the cursor if C = 0. Even if the cursor is hidden, I/D and other features remain unchanged when the display data is written. The cursor is shown with 5 dots in the 8th line.

B : Blinks the character in the cursor position if B = 1. This blinking turns ON/OFF all dots displayed in reverse. The blinking frequency is 300 ms when f_{OSC} = 55 kHz and displays 2 lines. This value varies in proportion to the inverse number of f_{OSC}.

4.9. Display Control (2) Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	PLUS	REV	ALON

When the extended register enable bit (RE) is "1", the PLUS, REV, and ALON bits are accessed. Once the specified values are stored in this register, they are retained even if the RE bit is set to "0".

PLUS : Specifies "duty + 1". Toggles the display duty. The COMI pin functions as the COM_8 (when displaying 1 line) or COM_{16} (when displaying 2 lines) for marker. When the COMI is scanned, the data in the SEGRAM is output as display data from the segment driver.
PLUS = "0" : Sets the display duty to 1/8 (when displaying 1 line) or 1/16 (when displaying 2 lines).
PLUS = "1" : Sets the display duty to 1/9 (when displaying 1 line) or 1/17 (when displaying 2 lines).

REV : Toggles between normal and reverse videos for display.
REV = "0" : Normal video
REV = "1" : Reverse video

ALON : Toggles between normal and fully lit-up displays regardless the data type in the DDRAM. The setting of this bit takes priority over that of REV.
ALON = "0" : Normal display
ALON = "1" : Fully lit-up display

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4.10. Cursor/Display Shift Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	1	S/C	R/L	*	*

* mark means "Don't care".

When the extended register enable bit (RE) is "0", the following S/C and R/L bits may be set.
The cursor position or the display is shifted to the left or right without writing the display data or reading it out. This may be used to modify or search the display. The cursor movement from the 1st to 2nd line occurs after the 16th digit in the 1st line. Note that all the lines are shifted simultaneously.
When duty + 1 command is ON (PLUS = 1), if S = 1 and any code is written into DDRAM, the line that COMI scans is also shifted, so that this command is allowed only when duty + 1 command is OFF (PLUS = 0) state.

S/C	R/L	ACTION
0	0	Shifts cursor to left (counts down the AC by one).
0	1	Shifts cursor to right (counts up the AC by one).
1	0	Shifts entire display to left. Cursor moves as display is shifted.
1	1	Shifts entire display to right. Cursor moves as display is shifted.

If only the display shift is made, the address counter (AC) remains unchanged.

4.11. Power Control Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	1	BIAS	HALT	PON	ACL

BIAS : This command selects the displaying bias ratio.
BIAS = "0" : 1/5 bias
BIAS = "1" : 1/4 bias

HALT : Turns ON/OFF the power saving mode. When the LH1594/LH1595 enter the power saving mode, the supply current can be reduced to nearly the standby current value.
HALT = "0" : Normal mode
HALT = "1" : Power saving mode
The internal state in the power saving mode is described below.
- The oscillation and power circuits are stopped.
- The LCD drive is disabled. The output from the segment and common drivers are made at the V_{SS} level.
- The clock input at the CK pin is inhibited.

PON : Turns ON/OFF the internal power supply circuit.
PON = "0" : Turns OFF the power supply circuit.
PON = "1" : Turns ON the power supply circuit.
The booster circuit and the voltage converter become active when the power supply circuit is turned on. The operating section in the circuits varies depending on the setting of the PMODE pin. See **Table in Section 2.14.** for details.

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ACL : The internal circuit can be initialized.
ACL = "0" : Normal mode.
ACL = "1" : ACL operation is ON.
When the ACL command is turned on, the busy flag is generated. Therefore, to execute an instruction after ACL operation, monitor the busy flag and then execute the next instruction after checking that the flag has been released; or allow a waiting period of 2 times the master clock frequency.

4.12. Function Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0/1	0	0	0	1	BE	DUB	RE	BT	*

* mark means "Don't care".

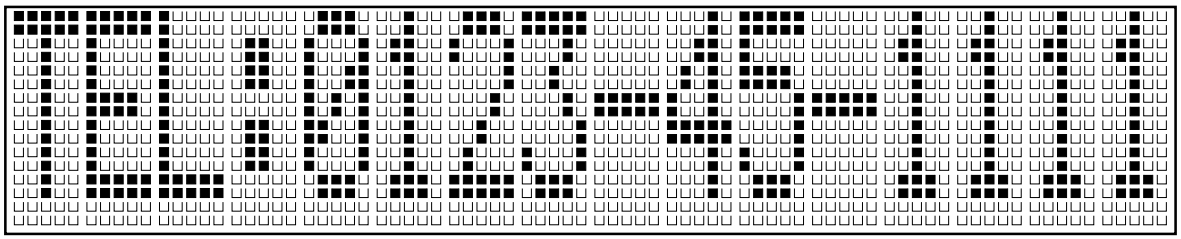
RE : This bit is the enable bit for extended register. If RE = "1", the extended function setting can be accessed. When setting instruction, it is necessary to follow the state of RE bit. (refer to **"INSTRUCTION CODE"** in section 4.1..) RE bit consists of register, once the specified value is stored in this register, it is retained the value.

BE : When BE = "1", the information which is stored in the SEGRAM using its upper 2 bits is used to allow for blinking the display data from the SEGRAM.

DUB : This bit is toggled the display double fonts lengthwise.
DUB = "0" : Displays normal mode.
DUB = "1" : Displays double fonts lengthwise.

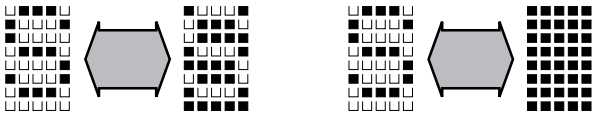
NOTES :

- Double fonts lengthwise can display only first line.
- Not using these setting, when displaying 1 line mode. (NL = 1)



Example of Display (DUB = "1")

BT : This command selects the character blinking type.
BT = "0" : Displaying normal/reverse per 32 frames.
BT = "1" : Displaying normal/black per 32 frames.



Example of Display (BT = "0") Example of Display (BT = "1")

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4.13. CGRAM Address Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	A	A	A	A	A	A

If the extended register enable bit (RE) is "0", CGRAM addresses may be specified.
In the above example, the address shown in binary number for "AAAAAA" is allocated in the address counter. Subsequently data is written into or read from the MPU in reference to the CGRAM.

4.14. SEGRAM Address Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	A	A	A	A

* mark means "Don't care".

If the extended register enable bit (RE) is "1", SEGRAM addresses may be specified.
The SEGRAM address shown in binary number for "AAAA" is allocated in the address counter. Subsequently data is written into or read from the MPU in reference to the SEGRAM.

4.15. DDRAM Address Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	*	A	A	A	A	A

* mark means "Don't care".

If the extended register enable bit (RE) is "0", DDRAM addresses may be specified.
The DDRAM address shown in binary number for "AAAAA" is allocated in the address counter. Subsequently data is written into or read from the MPU in reference to the DDRAM.

4.16. Electronic Volume Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	*	*	MSB	·····		LSB

* mark means "Don't care".

The LCD drive voltage V_0 output from the internal power supply circuit can be controlled and the display tone on the LCD can be also controlled.
The LCD drive voltage V_0 takes one out of 16 voltage values by setting 4-bit data register.
If the electronic volume is not used, specify (1, 1, 1, 1) in the 4-bit data register. After the LH1594/LH1595 are reset, the 4-bit data register is automatically set to (1, 1, 1, 1).

MSB	·····		LSB	V_0
0	0	0	0	Smaller
1	1	1	1	Larger

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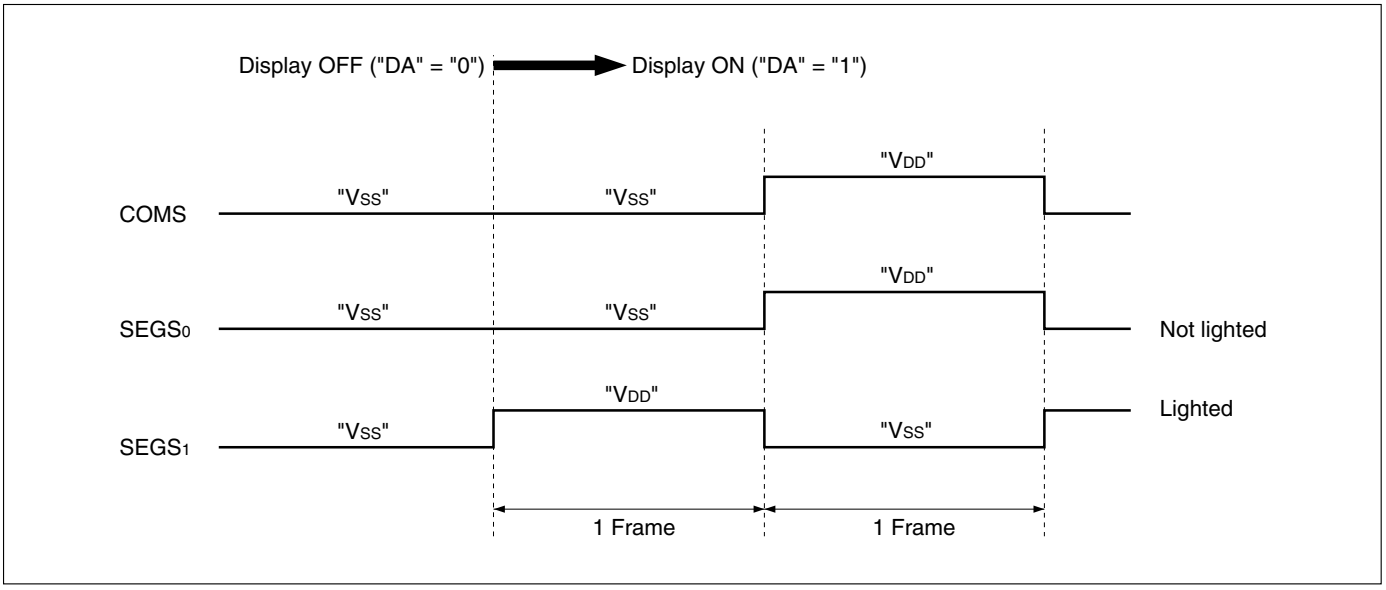
4.17. Annunciator Control Register Set

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	I5	I4	I3	I2	I1	I0
1				DA	*	I9	I8	I7	I6

* mark means "Don't care".

I0 to I9 : These bits are setting data for annunciator. Io to I9 correspond to $SEGS_0$ to $SEGS_9$ for static LCD drive outputs.

DA : When DA = "1", output pin for static LCD drive (for annunciator display). One level is selected from V_{DD} and V_{SS} levels depending on the combination of COMS signal and display data (I0 to I9). When DA = "0", outputs V_{SS} level.



Example of Outputs for Annunciator (DA = "1", I0 = "0", I1 = "1")

4.18. Busy Flag/Address Read

RE	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0/1	0	BF	*	A	A	A	A	A	A

* mark means "Don't care".

"BF = 1" indicates that the LH1594/LH1595 are internally operating and the next instruction is not accepted until "BF = 0".

The busy flag is only generated when the display is cleared or the ACL command is executed. Therefore, any other instruction can be executed without monitoring the busy flag.

Simultaneously, the address counter value presented in binary number for "AAAAAA" is read out. The address counter is used by the DDRAM, CGRAM, and SEGRAM. The data read out from the RAMs is determined by specifying a command before reading out.

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4.19. Example of Instructions vs. Display

NO.	INSTRUCTION									DISPLAY	ACTION
	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	Power ON										No display appears.
2	Function set										"0" is written to RE bit.
	0	0	0	1	*	*	0	0	*		
3	Display clear										Display is cleared.
	0	0	0	0	0	0	0	0	1		
4	Display ON/OFF control									_	Turns ON display and cursor. If display is cleared, display is filled with blank spaces.
	0	0	0	0	0	1	1	1	0		
5	Entry mode set									_	Counts up address by one and moves cursor to right when data is written to RAM.
	0	0	0	0	0	0	1	1	0		
6	DDRAM data write									S_	Writes "S".
	1	0	1	0	1	0	0	1	1		
7	:										
	:										
8	DDRAM data write									SHARP_	Writes "P".
	1	0	1	0	1	0	0	0	0		
9	DDRAM address set									SHARP	Sets DDRAM address so that cursor is positioned at the top of 2nd line.
	0	1	0	*	1	0	0	0	0	_	
10	DDRAM data write									SHARP	Writes "L".
	1	0	1	0	0	1	1	0	0	L_	
11	:										
	:										
12	DDRAM data write									SHARP	Writes "R".
	1	0	1	0	1	0	0	1	0	LCDDRIVER_	
13	:										
	:										
14	Cursor home									SHARP	Resets both display and cursor in place (address 0).
	0	0	0	0	0	0	0	1	*	LCDDRIVER	

* mark means "Don't care".

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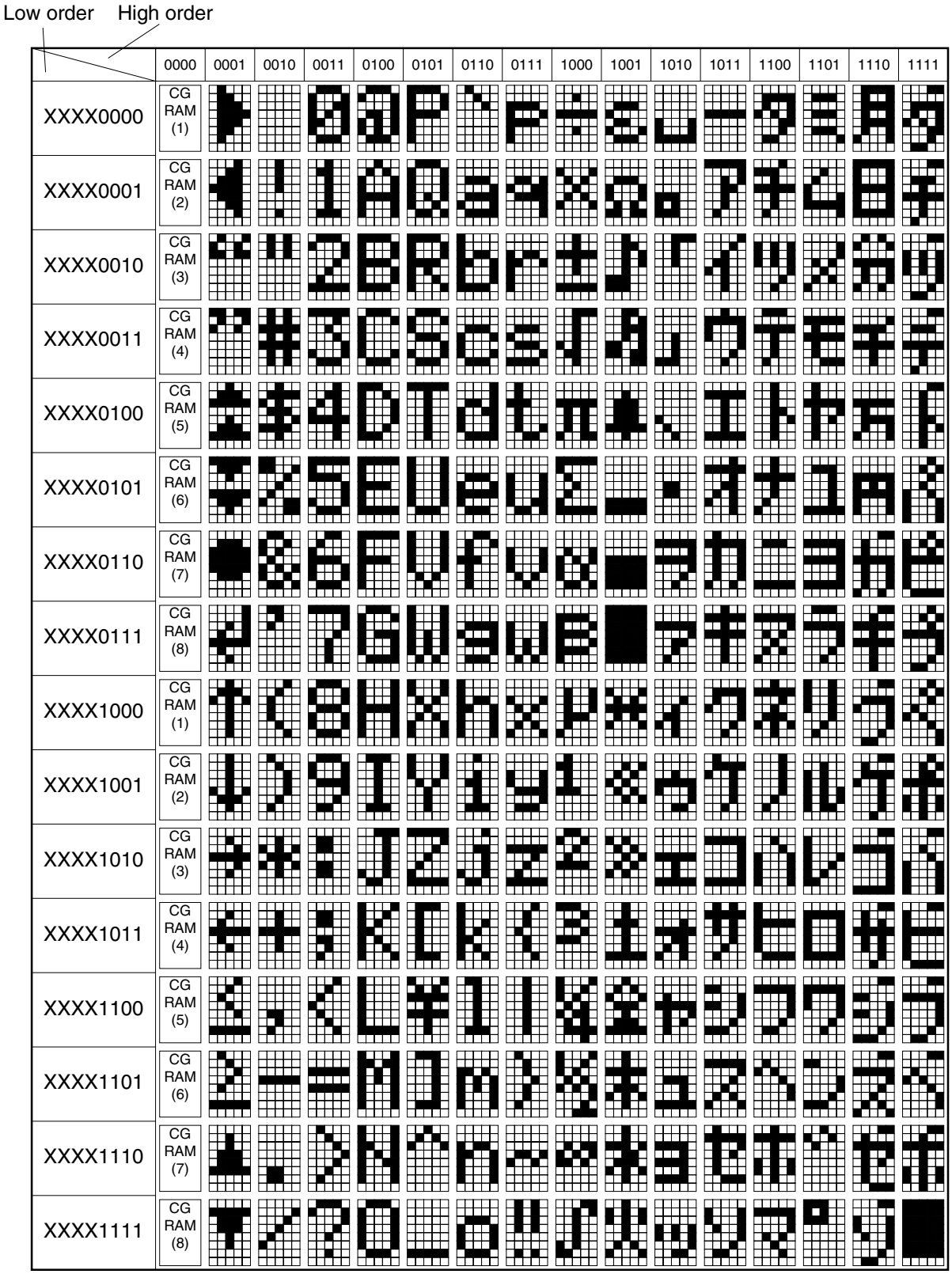
5. CONFIGURATION OF CGROM

Character codes vs. character patterns



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6. CONFIGURATION OF CGRAM

CGRAM addresses vs. character codes (DDRAM) and character patterns (CGRAM).

CHARACTER CODE								CGRAM ADDRESS						CGRAM DATA								
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_5	A_4	A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	*	0	0	0	0	0	0	0	0	0	*	*	*	1	0	0	0	1	
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				0	1	0	1	0	
											1	0	0				0	0	1	0	0	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	**(Y)**
											1	1	1				0	0	0	0	0	
				:					:						:							
0	0	0	0	*	1	1	1	1	1	1	0	0	0	*	*	*	1	0	0	0	1	
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	**(H)**
											1	1	1				0	0	0	0	0	

* mark means "Don't care".

Upper section : Character pattern 1 (Y display)
Lower section : Character pattern 2 (H display)

NOTES:

1. Character code bits D_2 to D_0 correspond to CGRAM addresses A_5 to A_3 (3 bits : 8 types).
2. CGRAM addresses A_2 to A_0 correspond to line positions of the character pattern (3 bits : 8 lines).
3. The columns of the character pattern are laid out with bit 0 allocated to the right end. Therefore, the pattern of bits 4 to 0 is displayed.
4. If the upper 4 bits (D_7 to D_4) of the character code are zeros, the CGRAM is selected. Since bit D_3 is "Don't care", "00_H" and "08_H" are the same CGRAM address.
5. If the CGRAM data is "1", data is displayed; if "0", data isn't displayed.

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7. CONFIGURATION OF SEGRAM

SEGRAM addresses vs. display patterns

SEGRAM ADDRESS				SEGRAM DATA							
A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	B_1	B_0	*	S_0	S_1	S_2	S_3	S_4
0	0	0	1	B_1	B_0	*	S_5	S_6	S_7	S_8	S_9
0	0	1	0	B_1	B_0	*	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}
0	0	1	1	B_1	B_0	*	S_{15}	S_{16}	S_{17}	S_{18}	S_{19}
0	1	0	0	B_1	B_0	*	S_{20}	S_{21}	S_{22}	S_{23}	S_{24}
0	1	0	1	B_1	B_0	*	S_{25}	S_{26}	S_{27}	S_{28}	S_{29}
0	1	1	0	B_1	B_0	*	S_{30}	S_{31}	S_{32}	S_{33}	S_{34}
0	1	1	1	B_1	B_0	*	S_{35}	S_{36}	S_{37}	S_{38}	S_{39}
1	0	0	0	B_1	B_0	*	S_{40}	S_{41}	S_{42}	S_{43}	S_{44}
1	0	0	1	B_1	B_0	*	S_{45}	S_{46}	S_{47}	S_{48}	S_{49}
1	0	1	0	B_1	B_0	*	S_{50}	S_{51}	S_{52}	S_{53}	S_{54}
1	0	1	1	B_1	B_0	*	S_{55}	S_{56}	S_{57}	S_{58}	S_{59}
1	1	0	0	B_1	B_0	*	S_{60}	S_{61}	S_{62}	S_{63}	S_{64}
1	1	0	1	B_1	B_0	*	S_{65}	S_{66}	S_{67}	S_{68}	S_{69}
1	1	1	0	B_1	B_0	*	S_{70}	S_{71}	S_{72}	S_{73}	S_{74}
1	1	1	1	B_1	B_0	*	S_{75}	S_{76}	S_{77}	S_{78}	S_{79}

* mark means "Don't care".

D_7 and D_6 : Blink control

D_4 to D_0 : Pattern displayed

NOTES :

1. Data stored in the SEGRAM is output for one-line display when COMI is selected.
2. Pins S_0 to S_{79} are segment drive pins. Pin S_0 is shown at the left end on the screen.
3. After output at pin S_{79}, output at pin S_0 is repeated.
4. For SEGRAM data, the lower 5 bits are used for display data.
5. If BE bit in the function set register is set to "1", the upper 1 bit (D_7) in SEGRAM is used to control the blinking of the lower 5-bit pattern. When D_7 is set to "1", the lower 5-bit display blinks. If bit D_6 is "1", only the pattern of bit D_4 can be blinked.
6. If SEGRAM data is "1", data is displayed; if "0", data isn't displayed.

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8. CONFIGURATION OF DDRAM

Display positions vs. display data RAM (DDRAM) addresses

	DIGIT															
	1st	**2nd**	**3rd**	**4th**	**5th**	**6th**	**7th**	**8th**	**9th**	**10th**	**11th**	**12th**	**13th**	**14th**	**15th**	**16th**
COM_0 to COM_7	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
COM_8 to COM_{15}	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

The above addressing is used because 16 digits are displayed. The DDRAM stores data for 32 characters.

If the display data is shifted, the DDRAM addresses are changed as follows :

Shift to right

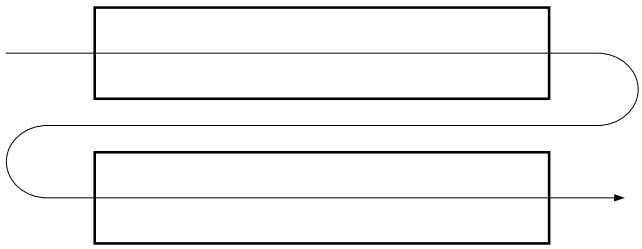
	DIGIT															
	1st	**2nd**	**3rd**	**4th**	**5th**	**6th**	**7th**	**8th**	**9th**	**10th**	**11th**	**12th**	**13th**	**14th**	**15th**	**16th**
COM_0 to COM_7	1F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
COM_8 to COM_{15}	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

Shift to left

	DIGIT															
	1st	**2nd**	**3rd**	**4th**	**5th**	**6th**	**7th**	**8th**	**9th**	**10th**	**11th**	**12th**	**13th**	**14th**	**15th**	**16th**
COM_0 to COM_7	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
COM_8 to COM_{15}	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	00

NOTE :

- The memory in the DDRAM is configured as follows :



Display area (16 characters x 2 lines)

As shown above, the 2nd data appears following the end of the data in the 1st line. Notice that the addresses are consecutive.

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9. DESCRIPTION OF SERIAL INTERFACE [FOR LH1594]

LH1594 is built in I²C BUS format interface.
The I²C BUS is for bi-directional two-line communication between different ICs or modules.

9.1. I²C BUS Protocol

I²C BUS protocol consists of a data receiver and data transmitter.
The device which controls protocol is the master, the device which is controlled is the slave.
The master controls data transfer and provides clock signal.
The LH1594 is used as a slave receiver or slave transmitter.

9.1.1. DATA TRANSFER

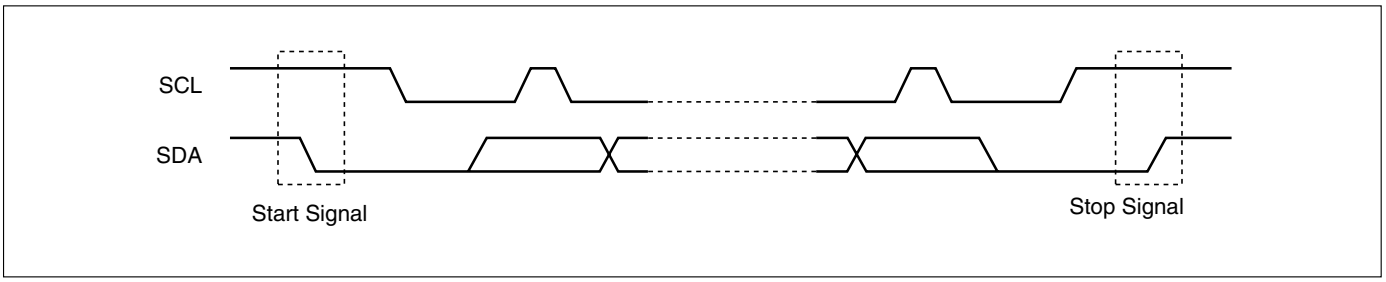
A change of SDA-state is allowed while SCL is low level. If SDA changes while SCL is high, this action is recognized as start bit or stop bit.

9.1.2. START SIGNAL

When the bus is not busy, SDA transfers high to low while SCL is high. This state is defined as the start condition.

9.1.3. STOP SIGNAL

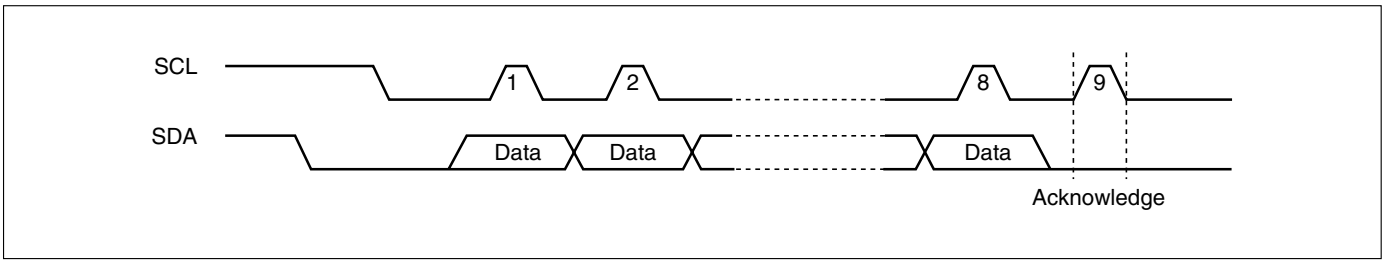
When the bus is not busy, SDA transfers low to high while SCL is high. This state is defined as the stop condition.



Start/Stop Timing

9.1.4. ACKNOWLEDGE

Acknowledge bit is used to confirm data transfer.
A transmitter (master or slave) releases the bus line after receiving 8-bit data. During next clock (9th clock) receive, put low level on the bus to indicate data receive completely.



Acknowledge Timing

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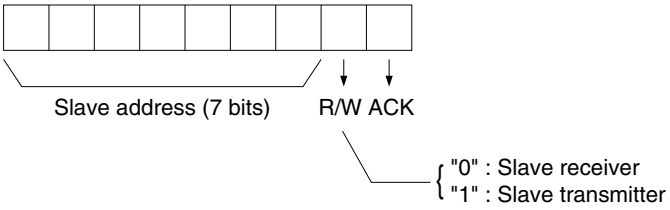
9.1.5. DEVICE ADDRESS CODE

After sending start bit, master device must transfer 8-bit device address code at first. Address code consists of 7 bits slave address and 1 bit R/W.
During read operation, R/W bit is "1". During write operation, R/W bit is "0".



Send Data at First Cycle

9.1.6. DEVICE ADDRESSING

Bus master must generate start-condition to start data transfer between 2 devices.
After generating start condition, master puts 8-bit word on SDA bus line.
LH1594 is fixed higher order bits (corresponding to DB7 to DB2). To identify device, it is fixed to "011101".
Next 1 bit is used to select LCD driver among some devices connecting to same bus.
LH1594 can connect to same bus, up to 2 chips. SA0 is used for LSB bit for identifying device.
8th bit (R/W bit) defines operation mode.

R/W = "0" : Write operation
R/W = "1" : Read operation

0	1	1	1	0	1	SA0	R/W

LH1594 Slave Address

9.1.7. SECOND TRANSFERRED DATA

During slave receive mode, LH1594 is specified as a control-byte waiting mode after receiving start condition and first cycle of 1 byte. Control-byte consists of 3 bits.
These bits are used to specify function mode for operating instruction.

Co : This bit defines transfer mode.
"0" : From next transfer byte, only data byte can be transferred.
"1" : Next transfer byte is data byte and after next transfer byte, control-byte must be input again.

RS : RS corresponds to "RS" signal in command function table. This bit identifies transfer data.

R/W : This bit defines read/write mode.
"0" : Readable mode
"1" : Write enable mode.

C_0	RS	R/W	*	*	*	*	*

* mark means "Don't care".

Transfer Data at Second Cycle

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9.2. Description of Pins Connected with The I²C BUS

SCL

Serial clock input pin.
SCL is used for clock of all data I/O.

SDA

SDA is bi-directional pin, which is used for data I/O.
SDA is open drain pin, connect to V_{DD} via pull-up resistor.

SA0

SA0 is used for LSB bit of slave address (7 bits width). Must be fixed to "H" or "L" externally.

ISEL

ISEL selects whether to use I²C BUS or not.
When ISEL is "H", I²C BUS is enable.
If ISEL is low, I²C BUS operation of LH1594 is not warrantied.

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9.3. Example of I²C BUS Operation

STEP	I²C BUS TRANSFER BYTE	DISPLAY	OPERATION
1	START I²C BUS		Initialized. Nothing display.
2	Send slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1		During the acknowledge cycle SDA will be pulled down by LH1594.
3	Send control byte C0 RS R/W ACK 0 0 0 0 0 0 0 0 1		Control bits RS, C0 and R/W are specified.
4	Set function D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 0 1 0 0 0 0 0 1		Sets RE bit to "0".
5	Clear display D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 0 0 0 0 0 0 1 1		Display clear.
6	Control display ON/OFF D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 0 0 0 1 1 1 0 1	_	Display and cursor are ON. All displays are cleared by operating display clear.
7	Set entry mode D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 0 0 0 0 1 1 0 1	_	Entry mode set. When writing into RAM, address is increased by 1 and cursor is shifted to right.
8	Set CGRAM address D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 1 0 0 0 0 0 0 1	_	Sets address to write into CGRAM.
9	Start condition	_	Sets RS bit to "1" and generated start condition again for writing.
10	Send slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	_	
11	Send control byte C0 RS R/W ACK 0 1 0 0 0 0 0 0 1	_	
12	Write CGRAM data D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 0 0 CG4 CG3 CG2 CG1 CG0 1	_	Writes data into CGRAM.
13	: : :		
14	Start condition	_	Generates start condition again for setting RS "0".

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STEP	I²C BUS TRANSFER BYTE	DISPLAY	OPERATION
15	Send slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	_	
16	Send control byte C0 RS R/W ACK 0 0 0 0 0 0 0 0 1	_	
17	Set DDRAM address D7 D6 D5 D4 D3 D2 D1 D0 ACK 1 0 0 0 0 0 0 0 1	_	Sets address for writing into DDRAM.
18	Start condition	_	Sets RS "1" and generates start condition again for writing into DDRAM.
19	Send slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	_	
20	Send control byte C0 RS R/W ACK 0 1 0 0 0 0 0 0 1	_	
21	Write DDRAM data D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 1 0 1 0 0 1 1 1	S_	Writes "S".
22	: : :		
23	Write DDRAM data D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 1 0 1 0 0 0 0 1	SHARP_	Writes "P".
24	Start condition	SHARP_	Generates start condition again for setting RS "0".
25	Send slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	SHARP_	
26	Send control byte C0 RS R/W ACK 0 0 0 0 0 0 0 0 1	SHARP_	
27	Set DDRAM address D7 D6 D5 D4 D3 D2 D1 D0 ACK 1 0 0 1 0 0 0 0 1	SHARP _	Sets DDRAM address so that cursor is positioned at the top of 2nd line.

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STEP	I²C BUS TRANSFER BYTE	DISPLAY	OPERATION
28	Start condition	SHARP _	Sets RS "1" and generates start condition again for writing into DDRAM.
29	Send slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	SHARP _	
30	Send control byte C0 RS R/W ACK 0 1 0 0 0 0 0 0 1	SHARP _	
31	Write DDRAM data D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 1 0 0 1 1 0 0 1	SHARP L_	Writes "L".
32	: : :		
33	Write DDRAM data D7 D6 D5 D4 D3 D2 D1 D0 ACK 0 1 0 1 0 0 1 0 1	SHARP LCDDRIVER_	Writes "R".
34	Start condition	SHARP LCDDRIVER_	Generates start condition again for setting RS "0".
35	Send slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 0 1	SHARP LCDDRIVER_	
36	Send control byte C0 RS R/W ACK 1 0 0 0 0 0 0 0 1	SHARP LCDDRIVER_	Sets control bit C0 "1".
37	Set DDRAM address D7 D6 D5 D4 D3 D2 D1 D0 ACK 1 0 0 0 0 0 0 0 1	SHARP LCDDRIVER_	Sets address for reading out DDRAM data.
38	Send control byte C0 RS R/W ACK 0 1 1 0 0 0 0 0 1	SHARP LCDDRIVER_	Sets control bit RS "1" and R/W "1".
39	Start condition	SHARP LCDDRIVER_	Generates start condition again for reading out DDRAM.
40	Send slave address SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK 0 1 1 1 0 1 0 1 1	SHARP LCDDRIVER_	Sets R/W "1" for reading out DDRAM data.

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STEP	I²C BUS TRANSFER BYTE	DISPLAY	OPERATION
41	Read out data D7 D6 D5 D4 D3 D2 D1 D0 ACK MSB ··· ··· ··· ··· ··· ··· LSB 0	SHARP LCDDRIVER_	Reads out DDRAM data from MSB to LSB. Master outputs acknowledge.
42	: : :		
43	Read out data D7 D6 D5 D4 D3 D2 D1 D0 ACK MSB ··· ··· ··· ··· ··· ··· LSB 1	SHARP LCDDRIVER_	As master does not output acknowledge, data will not be output in the next cycle.
44	Stop condition	SHARP LCDDRIVER_	Generates stop condition and finishes.

10. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	−0.3 to +6.0	V	1, 2
Supply voltage (2)	V_{EE}	V_{EE}	−0.3 to +6.0	V	
Supply voltage (3)	V_{OUT}	V_{OUT}	−0.3 to +13.0	V	
Supply voltage (4)	V_{R1}, V_{R2}	V_{R1}, V_{R2}	−0.3 to +13.0	V	
Supply voltage (5)	V_0	V_0	−0.3 to +13.0	V	
Supply voltage (6)	V_1, V_2, V_3, V_4	V_1, V_2, V_3, V_4	−0.3 to V_0 + 0.3	V	
Input voltage	V_I	D_7-D_0, CSB, RS, M86, RDB, WRB, CK, CKS, OSCI, P/S, RESB, PMODE, SHL_0, SHL_1, TEST	−0.3 to V_{DD} + 0.3	V	
Storage temperature	T_{STG}		−45 to +125	˚C	

NOTES :

1. T_A = +25 ˚C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

11. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{DD}	V_{DD}	+2.2		+5.5	V	1
	V_{EE}	V_{EE}	+2.4		+5.5	V	2
Operating voltage	V_0	V_0	+4.0		+11.0	V	3
	V_{OUT}	V_{OUT}	+4.0		+11.0	V	
	V_{R1}, V_{R2}	V_{R1}, V_{R2}	+4.0		+11.0	V	4
Operating temperature	T_{OPR}		−30		+85	˚C	

NOTES :

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. When using the booster circuit, power supply, V_{EE} at the primary circuit must be used within the above-described range. If the drive voltage of LCD panel can be boosted by utilizing the voltage level of V_{DD}, usually connect this pin to V_{DD} power supply.
3. Ensure that voltages are set such that $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_0$.
4. The operating range is adjusted by the external circuit constructed between V_{OUT} and V_{R1}, V_{R2}. The electric potential relation between the V_{R1}, V_{R2} and V_{OUT} pins must be $V_{R2} \leq V_{R1} \leq V_{OUT}$.

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12. ELECTRICAL CHARACTERISTICS

12.1. DC Characteristics

(Unless otherwise specified, V_{SS} = 0 V, V_{DD} = +2.2 to +5.5 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS		APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}			D_7-D_0, CSB, RS, M86, RDB, WRB, CK, CKS, OSCI, P/S, RESB, PMODE, SHL_0, SHL_1	0		0.2V_{DD}	V	
Input "High" voltage	V_{IH}				0.8V_{DD}		V_{DD}	V	
Output "Low" voltage	V_{OL}	I_{OL} = 0.4 mA		D_7-D_0, LP, FLM, M			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = −0.4 mA			V_{DD} − 0.4			V	
Input leakage current	I_{LI}	V_I = V_{SS} or V_{DD}		CSB, RS, M86, RDB, WRB, CK, CKS, OSCI, P/S, RESB, PMODE, SHL_0, SHL_1	−10		10	µA	
Output leakage current	I_{LO}	V_I = V_{SS} or V_{DD}		D_7-D_0, LP, FLM, M	−10		10	µA	1
LCD drive output ON resistance	R_{ON1}	$\lvert\Delta V_{ON}\rvert$ = 0.5 V	V_0 = 8 V	SEG0-SEG79, COM0-COM15, COMI		4	8	kΩ	2
Static LCD drive output ON resistance	R_{ON2}	$\lvert\Delta V_{ON}\rvert$ = 0.5 V		SEGS0-SEGS9, COMS			8	kΩ	
Standby current	I_{STB}	CK = 0 V, CSB = V_{DD}	V_{DD} = 3 V	V_{DD}			5	µA	3
			V_{DD} = 5 V				10		
Supply current (1)	I_{DD1}	Boosting 3 times	V_{DD} = 3 V, V_0 = 6 V	V_{DD}, V_{EE}		50	90	µA	4
Supply current (2)	I_{DD2}	Boosting 2 times	V_{DD} = 3 V, V_0 = 5 V	V_{DD}, V_{EE}		35	60	µA	4
Oscillation frequency	f_{OSC}	R_F = 1.2 MΩ±2%	V_{DD} = 3 V	OSCO	30	55	80	kHz	5
Boosted output voltage	V_{OUT}	Boosting 3 times	V_{EE} = 3 V	V_{OUT}	8.6			V	6
		Boosting 2 times	V_{EE} = 3 V		5.7				
Reset ("L") pulse width	t_{RW}			RESB	10			µs	

NOTES :

1. Applied when D_7 to D_0, LP, FLM, and M are in the high impedance state.
2. Resistance when 0.5 V is applied between each output pin and each power supply (V_0, V_1, V_2, V_3, V_4 or V_{SS}). Applied when power is supplied at power bias ratio of 1/7 in the external power supply mode.
3. Current at the V_{DD} pin when the master clock stops, the chip is not selected (CSB = V_{DD}), and no load is used. All circuits stop.
4. Applied when no access is made by the MPU when the internal oscillation circuit (R_F = 1.2 MΩ) and power supply circuit (PMODE = "L") are used. The electronic volume is pre-set (the code is "1 1 1 1"). The display is fully lit-up (ALON = "1") and the LCD drive pin is not loaded.
   Measuring conditions : V_{DD} = V_{EE}, V_{R1} = V_{R2}, C_1 = C_2 = 1 µF, R_1 + R_2 + R_3 = 4 MΩ, the current flowing through voltage control resistors (R_1, R_2, and R_3) is included.
5. Oscillation frequency when connecting a feedback resistor (R_F) of 1.2 MΩ between OSCI and OSCO.
6. Applied when the internal oscillation circuit (R_F = 1.2 MΩ) and power supply circuit (PMODE = "L") are used. Measuring conditions : C_1 = C_2 = 1 µF, V_{OUT} pin is connected only to C_1 and the LCD drive pin is not loaded.

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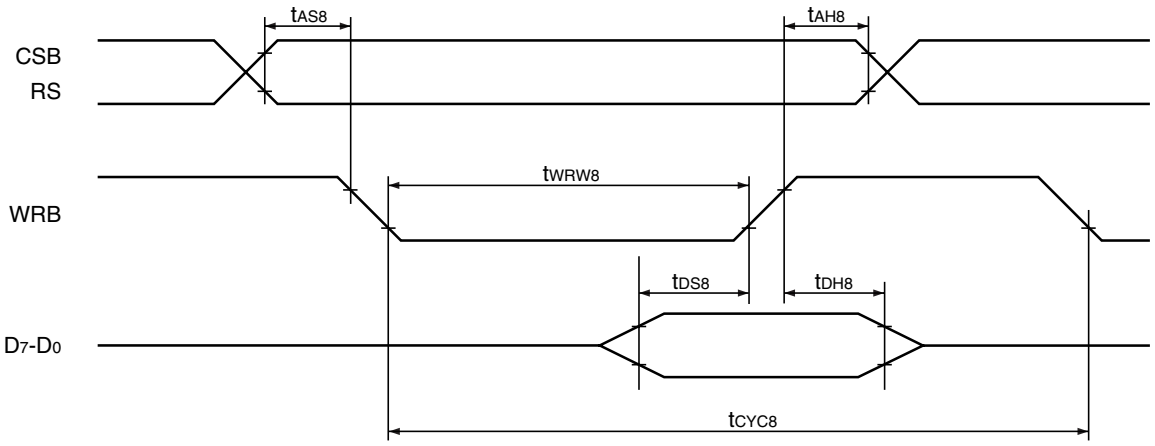
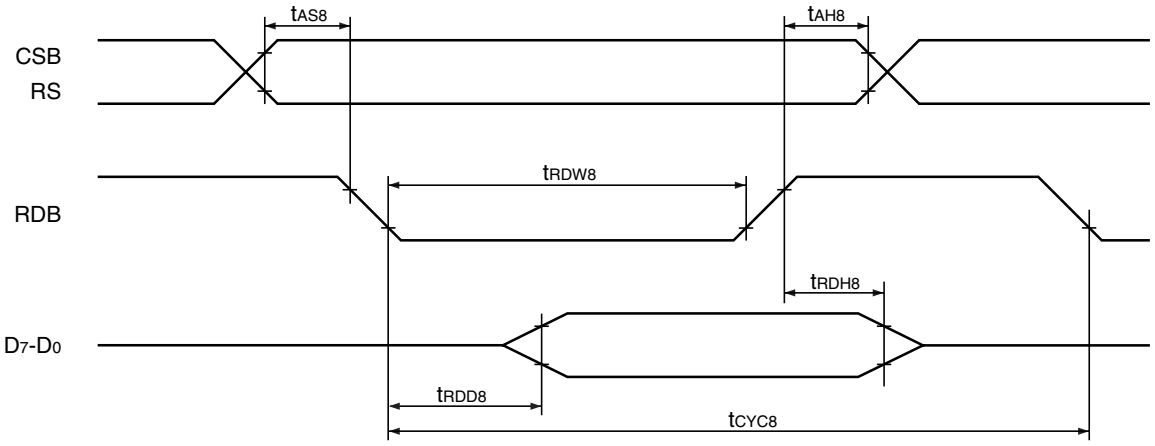
12.2. AC Characteristics

12.2.1. SYSTEM BUS READ/WRITE TIMING (80-FAMILY MPU)

(Write Timing)



(Read Timing)



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(80-family MPU Timing Characteristics) (V_{DD} = 4.5 to 5.5 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH8}		CSB	60		ns
Address setup time	t_{AS8}		RS	20		ns
System cycle time	t_{CYC8}		WRB RDB	400		ns
Read pulse width	t_{RDW8}			200		ns
Write pulse width	t_{WRW8}			50		ns
Data setup time	t_{DS8}		D_7-D_0	50		ns
Data hold time	t_{DH8}			20		ns
Read data output delay time	t_{RDD8}	C_L = 15 pF	D_7-D_0		150	ns
Read data hold time	t_{RDH8}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 2.7 to 4.5 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH8}		CSB	100		ns
Address setup time	t_{AS8}		RS	40		ns
System cycle time	t_{CYC8}		WRB RDB	600		ns
Read pulse width	t_{RDW8}			400		ns
Write pulse width	t_{WRW8}			100		ns
Data setup time	t_{DS8}		D_7-D_0	100		ns
Data hold time	t_{DH8}			40		ns
Read data output delay time	t_{RDD8}	C_L = 15 pF	D_7-D_0		300	ns
Read data hold time	t_{RDH8}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 2.2 to 2.7 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH8}		CSB	200		ns
Address setup time	t_{AS8}		RS	80		ns
System cycle time	t_{CYC8}		WRB RDB	1 200		ns
Read pulse width	t_{RDW8}			600		ns
Write pulse width	t_{WRW8}			150		ns
Data setup time	t_{DS8}		D_7-D_0	150		ns
Data hold time	t_{DH8}			80		ns
Read data output delay time	t_{RDD8}	C_L = 15 pF	D_7-D_0		500	ns
Read data hold time	t_{RDH8}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

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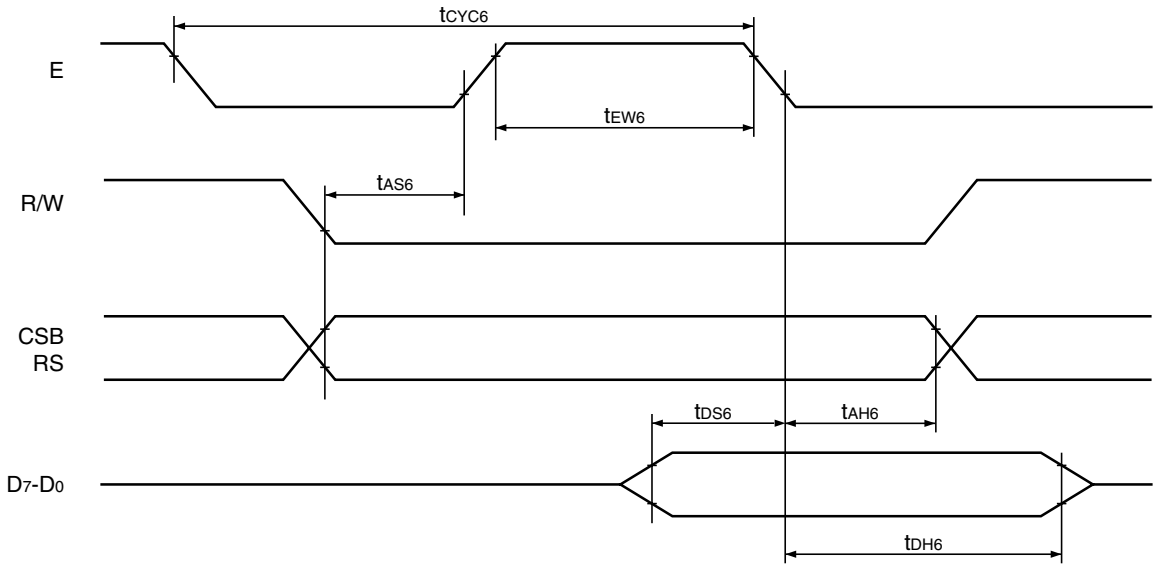
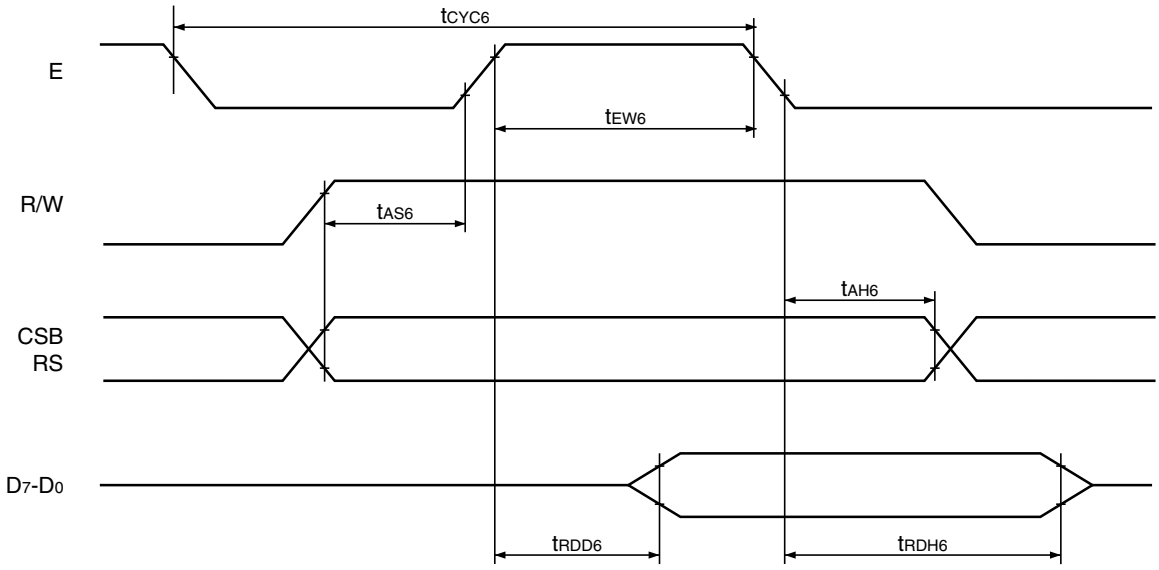
12.2.2. SYSTEM BUS READ/WRITE TIMING (68-FAMILY MPU)

(Write Timing)



(Read Timing)



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(68-family MPU Timing Characteristics) (V_{DD} = 4.5 to 5.5 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	60		ns
Address setup time	t_{AS6}		RS	20		ns
System cycle time	t_{CYC6}		E	400		ns
Enable pulse width (READ)	t_{EW6}			200		ns
Enable pulse width (WRITE)				50		ns
Data setup time	t_{DS6}		D_7-D_0	50		ns
Data hold time	t_{DH6}			20		ns
Read data output delay time	t_{RDD6}	C_L = 15 pF	D_7-D_0		150	ns
Read data hold time	t_{RDH6}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 2.7 to 4.5 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	100		ns
Address setup time	t_{AS6}		RS	40		ns
System cycle time	t_{CYC6}		E	600		ns
Enable pulse width (READ)	t_{EW6}			400		ns
Enable pulse width (WRITE)				100		ns
Data setup time	t_{DS6}		D_7-D_0	100		ns
Data hold time	t_{DH6}			40		ns
Read data output delay time	t_{RDD6}	C_L = 15 pF	D_7-D_0		300	ns
Read data hold time	t_{RDH6}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 2.2 to 2.7 V, T_{OPR} = −30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Address hold time	t_{AH6}		CSB	200		ns
Address setup time	t_{AS6}		RS	80		ns
System cycle time	t_{CYC6}		E	1 200		ns
Enable pulse width (READ)	t_{EW6}			600		ns
Enable pulse width (WRITE)				150		ns
Data setup time	t_{DS6}		D_7-D_0	150		ns
Data hold time	t_{DH6}			80		ns
Read data output delay time	t_{RDD6}	C_L = 15 pF	D_7-D_0		500	ns
Read data hold time	t_{RDH6}			10		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

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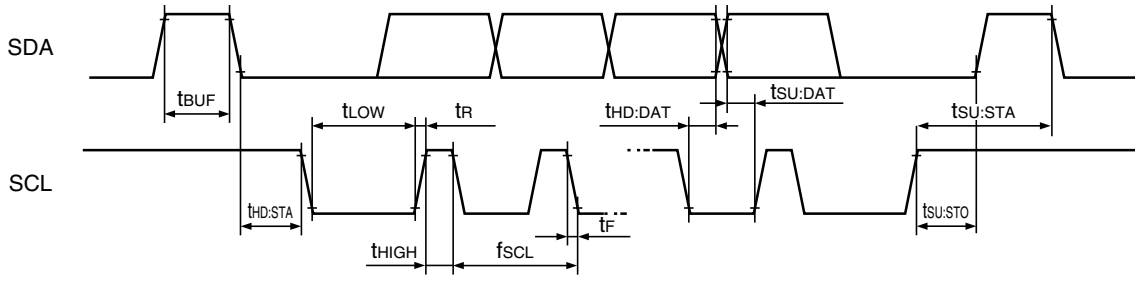
12.2.3. SERIAL INTERFACE TIMING (I^2C BUS) [FOR LH1594]



(V_{DD} = 2.2 to 5.5 V, T_{OPR} = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
SCL clock frequency	f_{SCL}		SCL		100	kHz
Start condition hold time	$t_{HD:STA}$			4.7		µs
SCL LOW time	t_{LOW}			4.7		µs
SCL HIGH time	t_{HIGH}			4		µs
Bus free time	t_{BUF}		SDA	4.7		µs
Data setup time	$t_{SU:DAT}$			250		ns
Data hold time	$t_{HD:DAT}$			0		ns
Setup time for START condition	$t_{SU:STA}$		SCL SDA	4.7		µs
Setup time for STOP condition	$t_{SU:STO}$			4		µs
SCL and SDA rise time	t_R				1	µs
SCL and SDA fall time	t_F				0.3	µs

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

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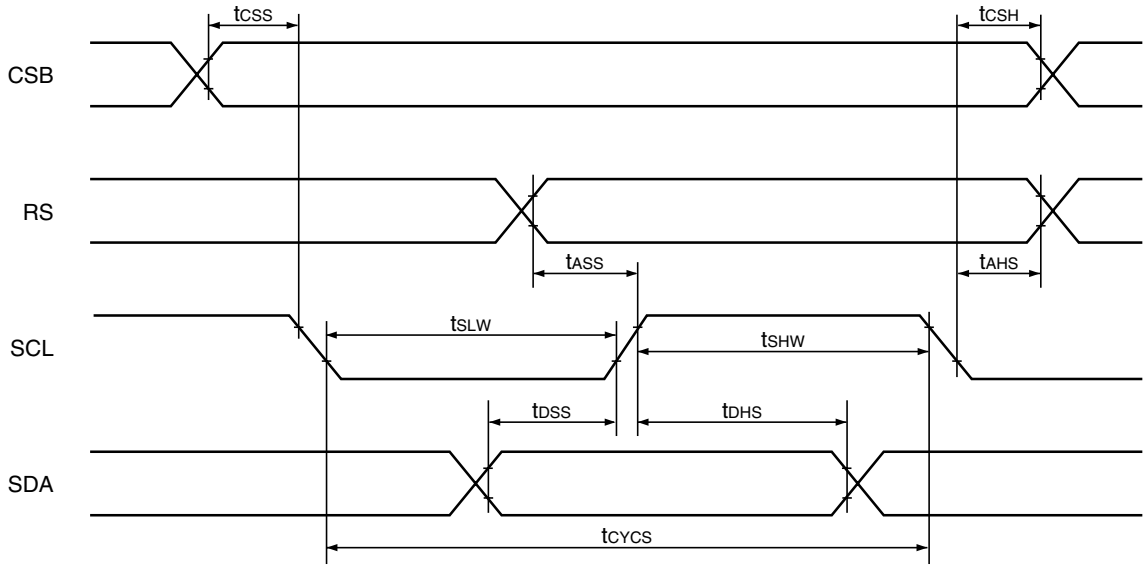
12.2.4. SERIAL INTERFACE TIMING [FOR LH1595]



(V_{DD} = 4.5 to 5.5 V, T_{OPR} = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Serial clock period	t_{CYCS}		SCL	500		ns
SCL "H" pulse width	t_{SHW}			200		ns
SCL "L" pulse width	t_{SLW}			200		ns
Address setup time	t_{ASS}		RS	40		ns
Address hold time	t_{AHS}			40		ns
Data setup time	t_{DSS}		SDA	200		ns
Data hold time	t_{DHS}			200		ns
CSB to SCL time	t_{CSS}		CSB	40		ns
CSB hold time	t_{CSH}			40		ns
Input signal rise and fall time	t_R, t_F		All of above pins		15	ns

(V_{DD} = 2.2 to 4.5 V, T_{OPR} = −30 to +85 ˚C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	MAX.	UNIT
Serial clock period	t_{CYCS}		SCL	1 000		ns
SCL "H" pulse width	t_{SHW}			400		ns
SCL "L" pulse width	t_{SLW}			400		ns
Address setup time	t_{ASS}		RS	80		ns
Address hold time	t_{AHS}			80		ns
Data setup time	t_{DSS}		SDA	400		ns
Data hold time	t_{DHS}			400		ns
CSB to SCL time	t_{CSS}		CSB	80		ns
CSB hold time	t_{CSH}			80		ns
Input signal rise and fall time	t_R, t_F		All of above pins		30	ns

NOTE : All the timings must be specified relative to 20% and 80% of V_{DD} voltage.

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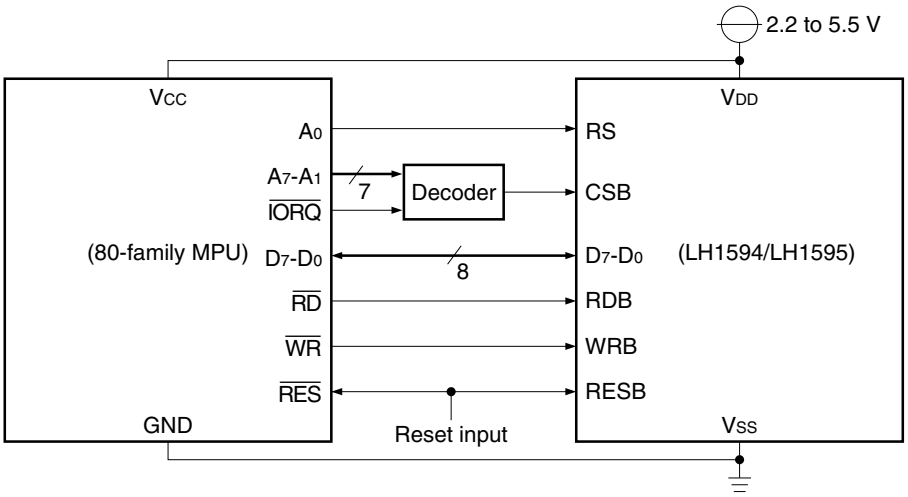
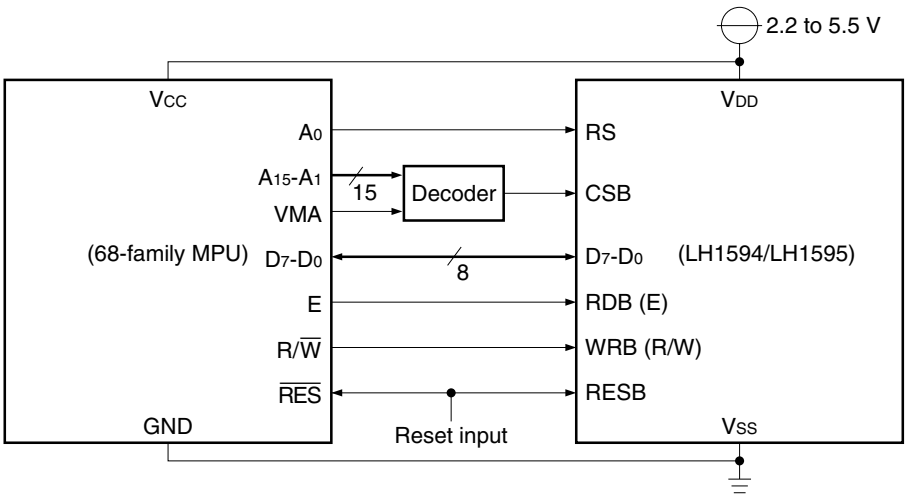
13. CONNECTION EXAMPLES OF REPRESENTATIVE APPLICATIONS

(a) Connection to The 80-family MPU



(b) Connection to The 68-family MPU



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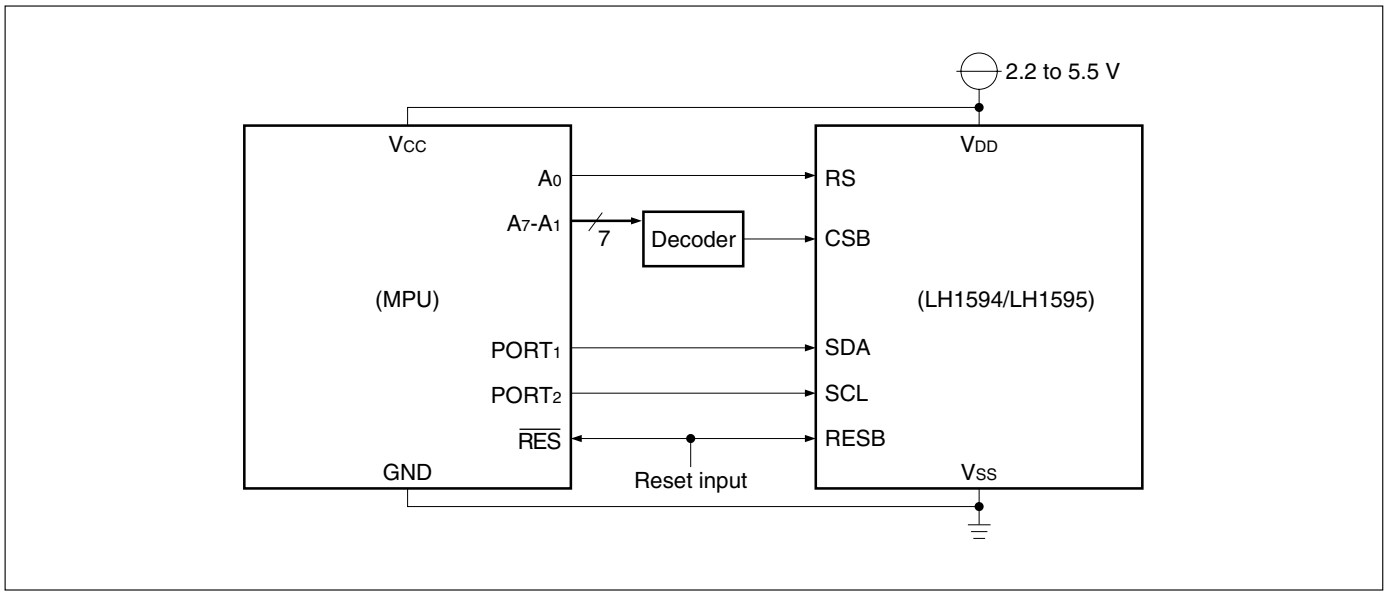
(c) Connection to The MPU with Serial Interface



* When connecting multiple LH1594/LH1595s, input to each CSB pin by varying the decoder conditions of address signals.

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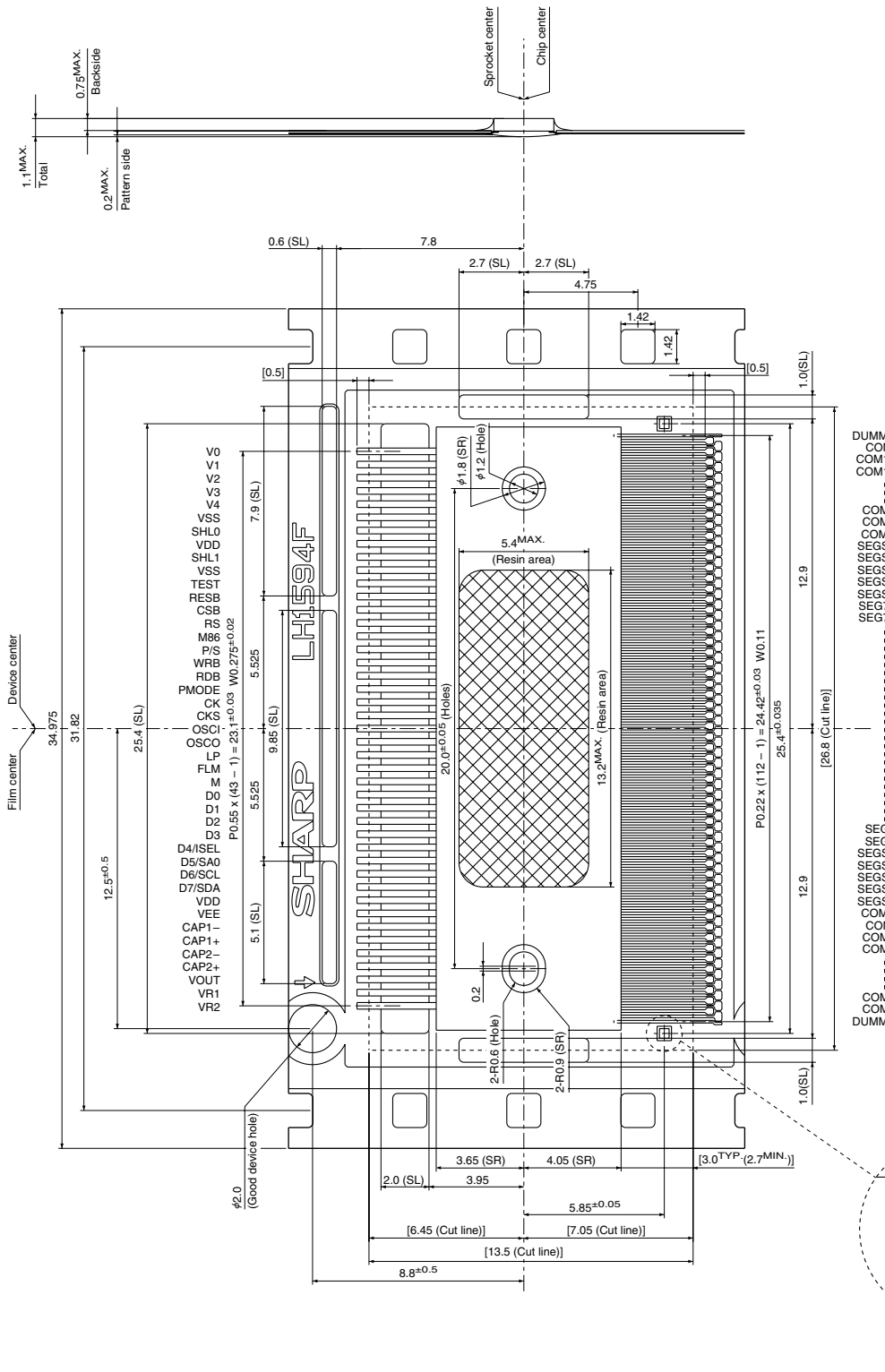
14. PACKAGE

(Unit : mm)



● Tape Material

Substrate	UPILEX S75
Adhesive	#7100
Cu foil [thickness]	VLP 25 µm
Solder resist	Epoxy resin

● Tape Specification

Tape width	35 mm
Tape type	Super wide
Perforation pitch	4 pitches

LH1594F

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