MX29F040C

4M-BIT [512K x 8] CMOS SINGLE VOLTAGE 5V ONLY EQUAL SECTOR FLASH MEMORY

FEATURES

- 524,288 x 8 only
- Single power supply operation
  - 5.0V only operation for read, erase and program operation
- Fast access time: 55/70/90ns
- **Compatible with MX29F040 device**
- Low power consumption
  - 30mA maximum active current(5MHz)
  - 1uA typical standby current
- Command register architecture
  - Byte Programming (9us typical)
  - Sector Erase
  8 equal sectors of 64K-Byte each
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability
  - Automatically program and verify data at specified address
- Erase suspend/Erase Resume
  - Suspends an erase operation to read data from, or program data to, another sector that is not being erased, then resumes the erase
- Status Reply
  - Data# Polling & Toggle bit for detection of program and erase cycle completion
- Sector protect/chip unprotect for 5V only system
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Temporary sector unprotect allows code changes in previously locked sectors
- 100,000 minimum erase/program cycles
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
  - 32-pin PLCC, TSOP or PDIP
  - **All Pb-free devices are RoHS Compliant**
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash
- 20 years data retention

GENERAL DESCRIPTION

The MX29F040C is a 4-mega bit Flash memory organized as 512K bytes of 8 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F040C is packaged in 32-pin PLCC, TSOP, PDIP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29F040C offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F040C has separate chip enable (CE#) and output enable (OE#) controls.

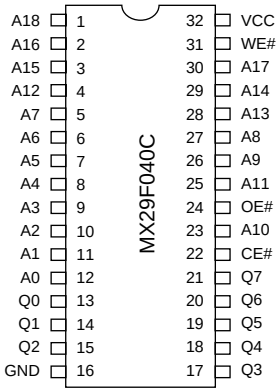
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F040C uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F040C uses a 5.0V±10% VCC supply to perform the High Reliability Erase and auto Program/ Erase algorithms.

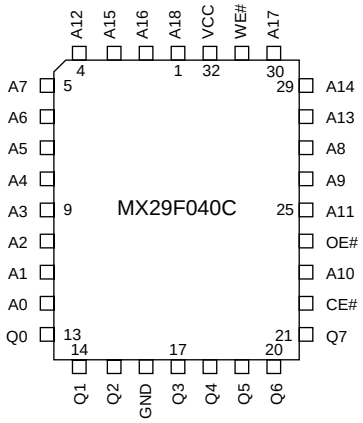
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

32 PDIP



32 PLCC



32 TSOP (Standard Type) (8mm x 20mm)

PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
GND	Ground Pin
VCC	+5.0V single power supply

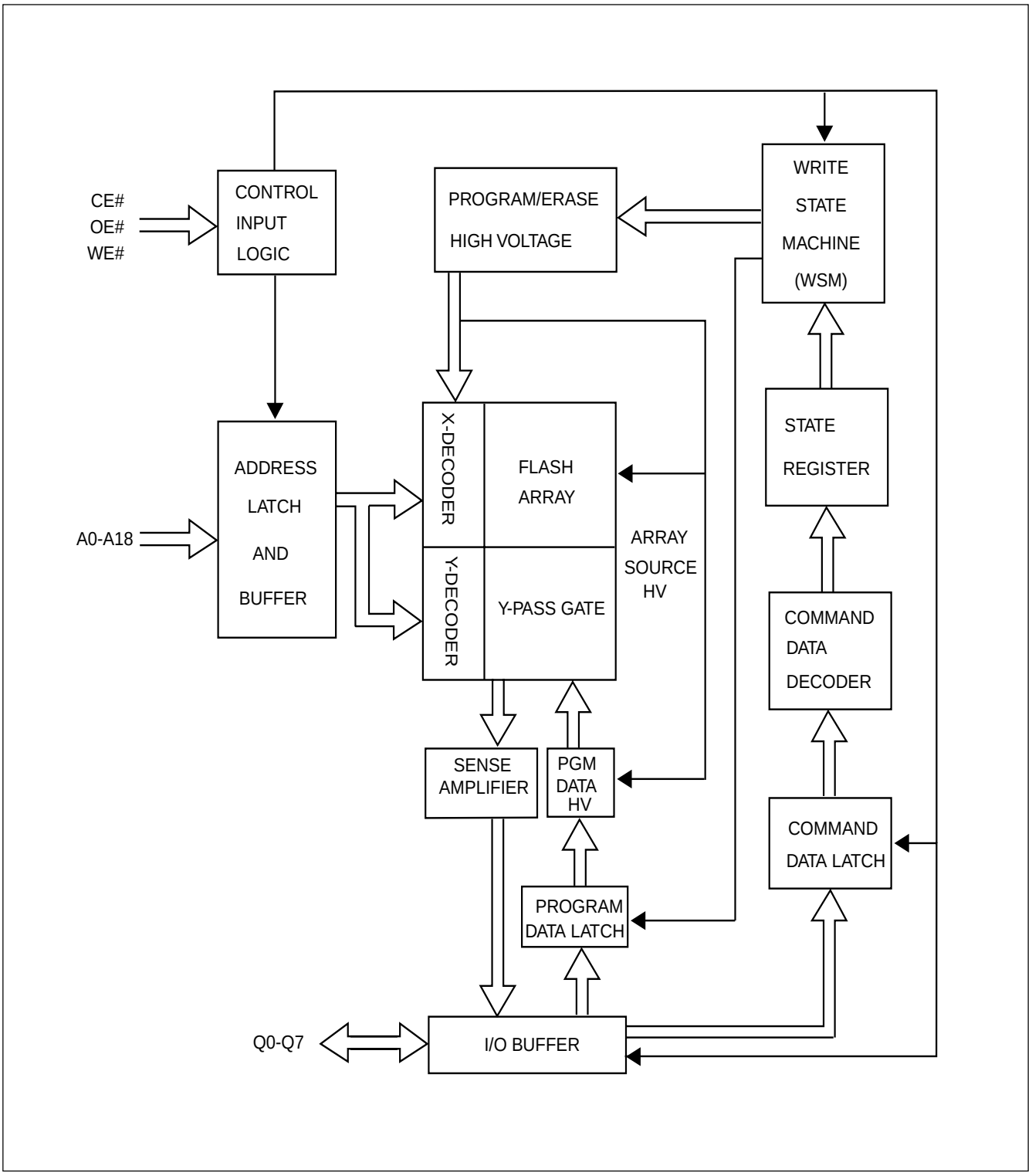
SECTOR STRUCTURE

MX29F040C SECTOR ADDRESS TABLE

Sector	A18	A17	A16	Address Range
SA0	0	0	0	00000h-0FFFFh
SA1	0	0	1	10000h-1FFFFh
SA2	0	1	0	20000h-2FFFFh
SA3	0	1	1	30000h-3FFFFh
SA4	1	0	0	40000h-4FFFFh
SA5	1	0	1	50000h-5FFFFh
SA6	1	1	0	60000h-6FFFFh
SA7	1	1	1	70000h-7FFFFh

Note: All sectors are 64 Kbytes in size.

BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX29F040C is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX29F040C is less than 4.5 seconds.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 4 second. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX29F040C is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm require the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to Data# Polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge of WE# or CE#, whichever happens later, and data are latched on the rising edge of WE# or CE#, whichever happens first.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29F040C electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

TABLE 1. SOFTWARE COMMAND DEFINITIONS

Command	Bus Cycle	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXXH	F0H										
Read	1	RA	RD										
Read Silicon ID	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
Sector Protect Verify	4	555H	AAH	2AAH	55H	555H	90H	(SA)X 02	00H 01H				
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend	1	XXXH	B0H										
Sector Erase Resume	1	XXXH	30H										
Unlock for sector protect/unprotect	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	20H

Note:
1. ADI = Address of Device identifier; A1=0, A0 = 0 for manufacture code,A1=0, A0 = 1 for device code A2-A18=Do not care.
   (Refer to table 3)
   DDI = Data of Device identifier : C2H for manufacture code, A4H for device code.
   X = X can be VIL or VIH
   RA=Address of memory location to be read.
   RD=Data to be read at location RA.
2. PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   SA = Address to the sector to be erased.
3. The system should generate the following address patterns: 555H or 2AAH to Address A10~A0 .
   Address bit A11~A18=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA). Write Sequence may be initiated with A11~A18 in either state.
4. For Sector Protect Verify Operation : If read out data is 01H, it means the sector has been protected. If read out data is 00H, it means the sector is still not being protected.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 1 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device (when applicable).

TABLE 2. MX29F040C BUS OPERATION

Mode \ Pins	CE#	OE#	WE#	A0	A1	A6	A9	Q0 ~ Q7
Read Silicon ID Manufacturer Code(1)	L	L	H	L	L	X	V_{ID}(2)	C2H
Read Silicon ID Device Code(1)	L	L	H	H	L	X	V_{ID}(2)	A4H
Read	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	D_{IN}(3)
Sector Protect without 12V system (6)	L	H	L	X	X	L	H	X
Chip Unprotect without 12V system (6)	L	H	L	X	X	H	H	X
Verify Sector Protect/Unprotect without 12V system (7)	L	L	H	X	H	X	H	Code(5)
Reset	X	X	X	X	X	X	X	HIGH Z

Notes :

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 1 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H means unprotected.
   Code=01H means protected.
   A18~A16=Sector address for sector protect.
6. Refer to sector protect/unprotect algorithm and waveform.
   Must issue "unlock for sector protect/unprotect" command before "sector protect/unprotect without 12V system" command.
7. The "verify sector protect/unprotect without 12V system" is only following "Sector protect/unprotect without 12V system" command.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29F040C contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL,A0=VIL retrieves the manufacturer code of C2H. A read cycle with A1=VIL, A0=VIH returns the device code of A4H for MX29F040C.

SET-UP AUTOMATIC CHIP/SECTOR ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last WE# or CE#, whichever happens first pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

TABLE 3. EXPANDED SILICON ID CODE

Pins	A0	A1	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code (Hex)
Manufacture code	VIL	VIL	1	1	0	0	0	0	1	0	C2H
Device code for MX29F040C	VIH	VIL	1	0	1	0	0	1	0	0	A4H
Sector Protection Verification	X	VIH	0	0	0	0	0	0	0	1	01H (Protected)
	X	VIH	0	0	0	0	0	0	0	0	00H(Unprotected)

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of WE# or CE#, whichever happens later, while the command (data) is latched on the rising edge of WE# or CE#, whichever happens first. Sector addresses selected are loaded into internal register on the sixth falling edge of WE# or CE#, whichever happens later. Each successive sector load cycle started by the falling edge of WE# or CE#, whichever happens later must begin within 30us from the rising edge of the preceding WE# or CE#, whichever happens first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase (30H) or Erase Suspend (B0H) during the time-out period resets the device to read mode.

TABLE 4. Write Operation Status

	Status		Q7 Note1	Q6	Q5 Note2	Q3	Q2
In Progress	Byte Program in Auto Program Algorithm		Q7#	Toggle	0	N/A	No Toggle
	Auto Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program	Q7#	Toggle	0	N/A	N/A
Exceeded Time Limits	Byte Program in Auto Program Algorithm		Q7#	Toggle	1	N/A	No Toggle
	Auto Erase Algorithm		0	Toggle	1	1	Toggle
	Erase Suspend Program		Q7#	Toggle	1	N/A	N/A

Note:
1. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. Q5 switches to '1' when an Auto Program or Auto Erase operation has exceeded the maximum timing limits. See "Q5:Exceeded Timing Limits " for more information.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20us to suspend the erase operations. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and program commands.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended sectors.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing. However, a 400us time delay must be required after the erase resume command, if the system implements an endless erase suspend/resume loop, or the number of erase suspend/resume is exceeded 1024 times. The erase times will be expended if the erase behavior always be suspended.

SET-UP AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, A three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next WE# or CE# pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the WE# or CE#, whichever happens first pulse. The rising edge of WE# or CE#, whichever happens first also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program operation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode (no program verify command is required).

DATA# POLLING-Q7

The MX29F040C also features Data# Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The Data# Polling feature is valid after the rising edge of the fourth WE# or CE#, whichever happens first pulse of the four write pulse sequences for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is competed. Upon completion of the erase operation, the data on Q7 will read "1". The Data# Polling feature is valid after the rising edge of the sixth WE# or CE#, whichever happens first pulse of six write pulse sequences for automatic chip/sector erase.

The Data# Polling feature is active during Automatic Program/Erase algorithm or sector erase time-out. (see section Q3 Sector Erase Timer)

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# or CE#, whichever happens first pulse in the command sequence (prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 4 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit I is valid after the rising edge of the final WE# or CE#, whichever happens first pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 4 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5
Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data# Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

DATA PROTECTION

The MX29F040C is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

Q3
Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data# Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data# Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data# Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns (typical) on CE# or WE# will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of OE# = VIL, CE# = VIH or WE# = VIH. To initiate a write cycle CE# and WE# must be a logical zero while OE# is a logical one.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

POWER-UP SEQUENCE

The MX29F040C powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

SECTOR PROTECTION WITHOUT 12V SYSTEM

The MX29F040C also feature a sector protection method in a system without 12V power supply. The programming equipment do not need to supply 12 volts to protect sectors. The details are shown in sector protect algorithm and waveform.

CHIP UNPROTECT WITHOUT 12V SYSTEM

The MX29F040C also feature a chip unprotection method in a system without 12V power supply. The programming equipment do not need to supply 12 volts to unprotect all sectors. The details are shown in chip unprotect algorithm and waveform.

CAPACITANCE (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN1	Input Capacitance			8	pF	VIN = 0V
CIN2	Control Pin Capacitance			12	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

READ OPERATION

DC CHARACTERISTICS (TA = -40°C to 85°C, VCC = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN = GND to VCC
ILO	Output Leakage Current			10	uA	VOUT = GND to VCC
ISB1	Standby VCC current			1	mA	CE# = VIH
ISB2			1	5	uA	CE# = VCC + 0.3V
ICC1	Operating VCC current			30	mA	IOUT = 0mA, f=5MHz
ICC2				50	mA	IOUT = 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(NOTE 1)		0.8	V	
VIH	Input High Voltage	0.7xVCC		VCC + 0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA, VCC=VCC MIN
VOH1	Output High Voltage(TTL)	2.4			V	IOH = -2mA, VCC=VCC MIN
VOH2	Output High Voltage(CMOS)	VCC-0.4			V	IOH = -100uA,VCC=VCC MIN

Notes :

1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns.
   If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS (TA =-40°C to 85°C, VCC = 5V±10%)

		29F040C-55		29F040C-70		29F040C-90			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	Conditions
tACC	Address to Output Delay		55		70		90	ns	CE#=OE#=VIL
tCE	CE# to Output Delay		55		70		90	ns	OE#=VIL
tOE	OE# to Output Delay		30		30		35	ns	CE#=VIL
tDF	OE# High to Output Float (Note 1)	0	20	0	20	0	20	ns	CE#=VIL
tOH	Address to Output hold	0		0		0		ns	CE#=OE#=VIL

TEST CONDITIONS:

- Input pulse levels: 0.45V/0.7xVCC for 70ns & 90ns, 0V/0.7xVCC for 55ns
- Input rise and fall times: is equal to or less than 10ns for 70ns & 90ns, 5ns for 55ns
- Output load: 1 TTL gate + 100pF (Including scope and jig) for 70ns & 90ns, 1TTLgate+30pF for 55ns max.
- Reference levels for measuring timing: 0.8V, 2.0V for 70ns & 90ns,1.5V for 55ns

Note :

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

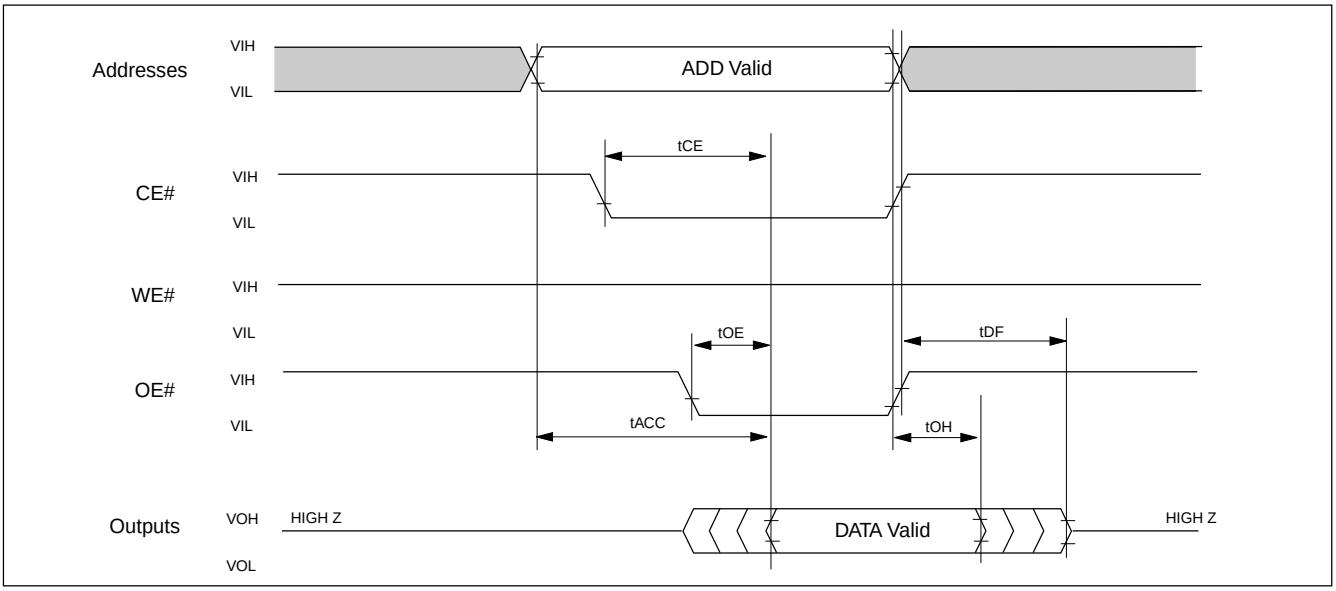
ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 125°C
Ambient Temperature with Power Applied	-55°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

READ TIMING WAVEFORMS



COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

DC CHARACTERISTICS (TA = -40°C to 85°C, VCC = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ICC1 (Read)	Operating VCC Current			30	mA	IOUT=0mA, f=5MHz
ICC2				50	mA	IOUT=0mA, f=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		2		mA	CE#=VIH, Erase Suspended

NOTES:

1. VIL min. = -0.6V for pulse width is equal to or less than 20ns.
2. If VIH is over the specified maximum value, programming operation cannot be guaranteed.
3. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
4. All current are in RMS unless otherwise noted.

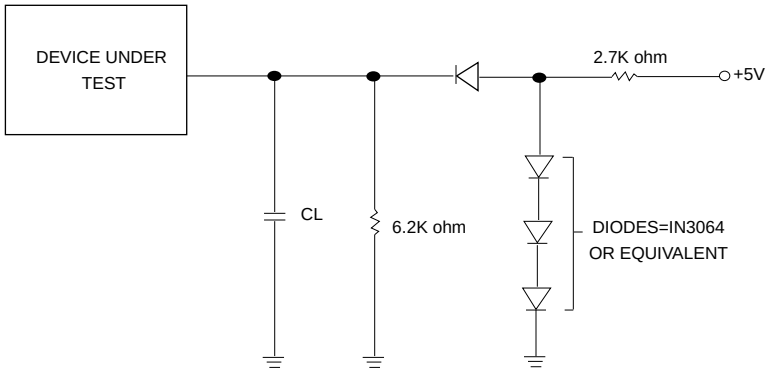
AC CHARACTERISTICS TA = -40°C to 85°C, VCC = 5V ±10%

SYMBOL	PARAMETER		Speed Option			UNIT
			55(Note 2)	70	90	
tOES	OE# setup time	MIN.	0	0	0	ns
tCWC	Command programming cycle	MIN.	55	70	90	ns
tCEP	WE# programming pulse width	MIN.	35	35	45	ns
tCEPH	WE# programming pulse width High	MIN.	20	20	20	ns
tAS	Address setup time	MIN.	0	0	0	ns
tAH	Address hold time	MIN.	45	45	45	ns
tDS	Data setup time	MIN.	30	30	45	ns
tDH	Data hold time	MIN.	0	0	0	ns
tCESC	CE# setup time before command write	MIN.	0	0	0	ns
tDF	Output disable time (Note 1)	MAX.	20	20	20	ns
tAETC	Erase time in auto chip erase	TYP.	4	4	4	s
		MAX.	32	32	32	s
tAETB	Erase time in auto sector erase	TYP.	0.7	0.7	0.7	s
		MAX.	15	15	15	s
tAVT	Programming time in auto verify	TYP.	9	9	9	us
		MAX.	300	300	300	us
tBAL	Sector address load time	MIN.	50	50	50	us
tCH	CE# Hold Time	MIN.	0	0	0	ns
tCS	CE# setup to WE# going low	MIN.	0	0	0	ns

Notes:

1. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Under condition of VCC=5V±10%,CL=30pF,VIH/VIL=0.7xVCC/0V,VOH/VOL=1.5V/1.5V,IOL=2mA,IOH=2mA.

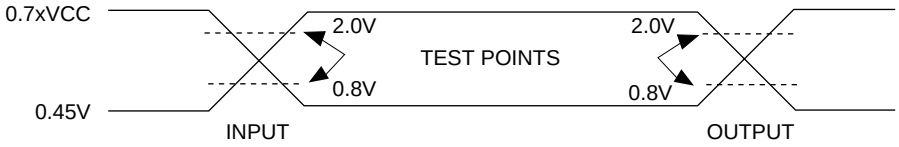
SWITCHING TEST CIRCUITS



CL=100pF Including jig capacitance for 70ns and 90ns

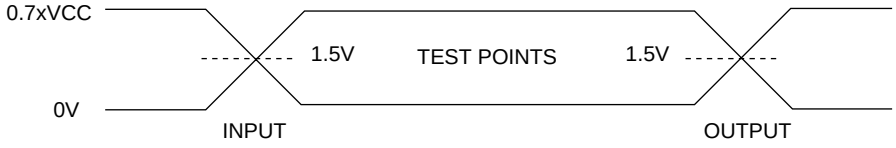
CL=30pF Including jig capacitance for 55ns

SWITCHING TEST WAVEFORMS for 29F040C-70 and 29F040C-90



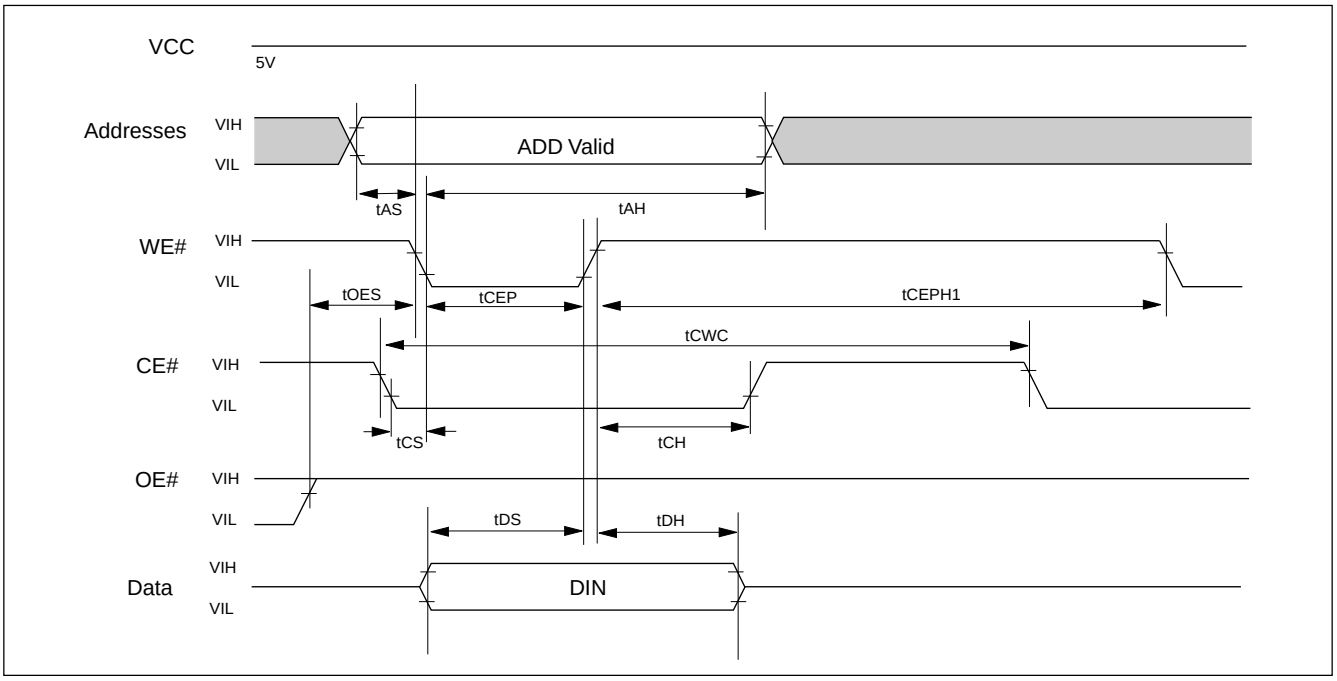
AC TESTING: Inputs are driven at 0.7xVCC for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are < 10ns.

SWITCHING TEST WAVEFORMS for 29F040C-55



AC TESTING: Inputs are driven at 0.7xVCC for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are < 5ns.

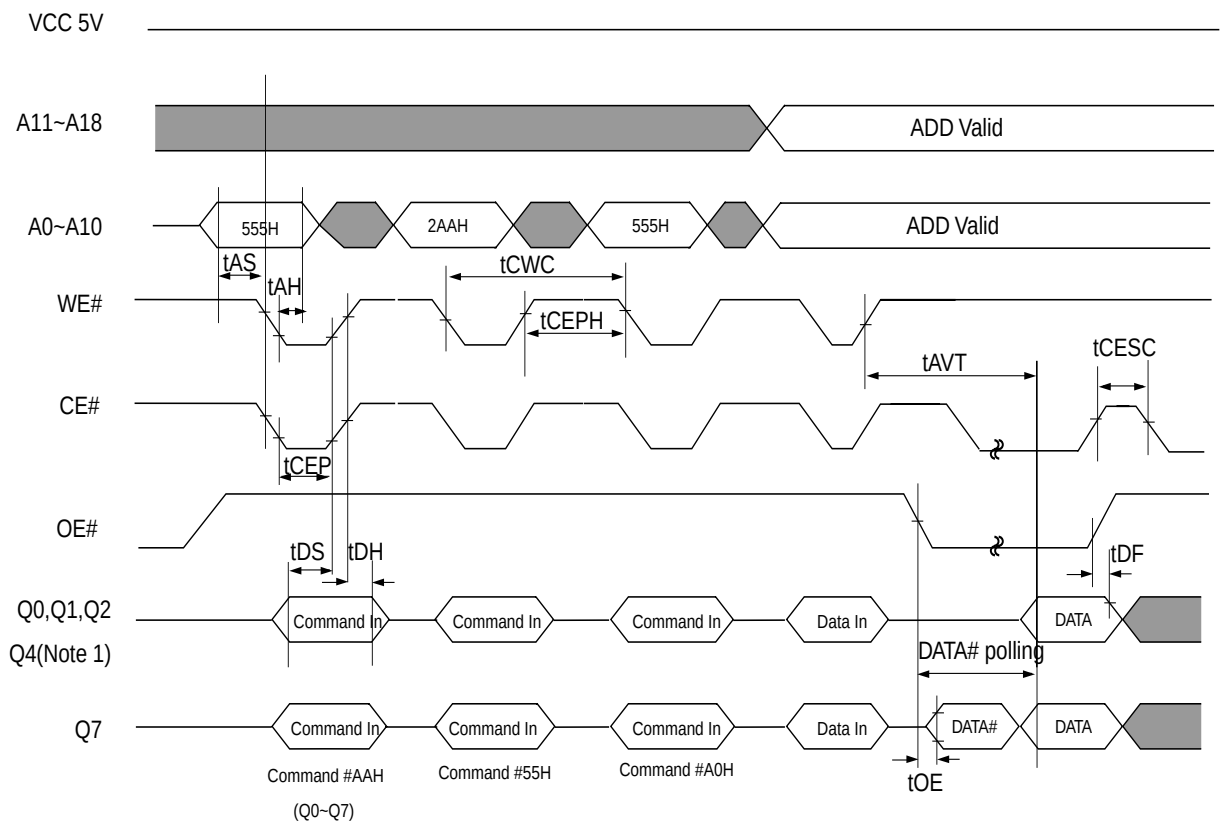
COMMAND WRITE TIMING WAVEFORM



AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by Data# Polling and toggle bit checking after automatic verification starts. Device outputs DATA# during programming and DATA# after programming on Q7.(Q6 is for toggle bit; see toggle bit, Data# Polling, timing waveform)

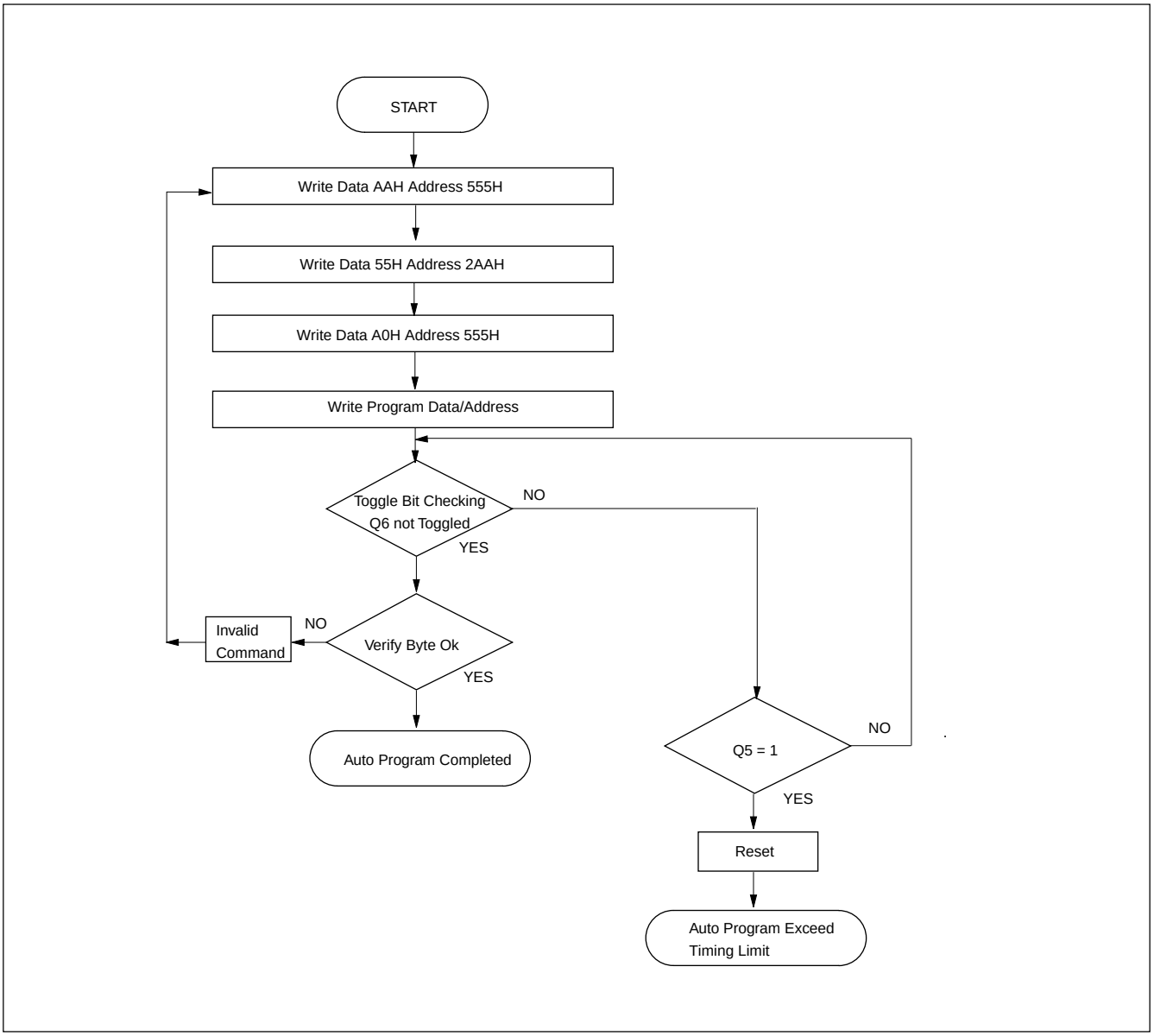
AUTOMATIC PROGRAMMING TIMING WAVEFORM



Note :

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit

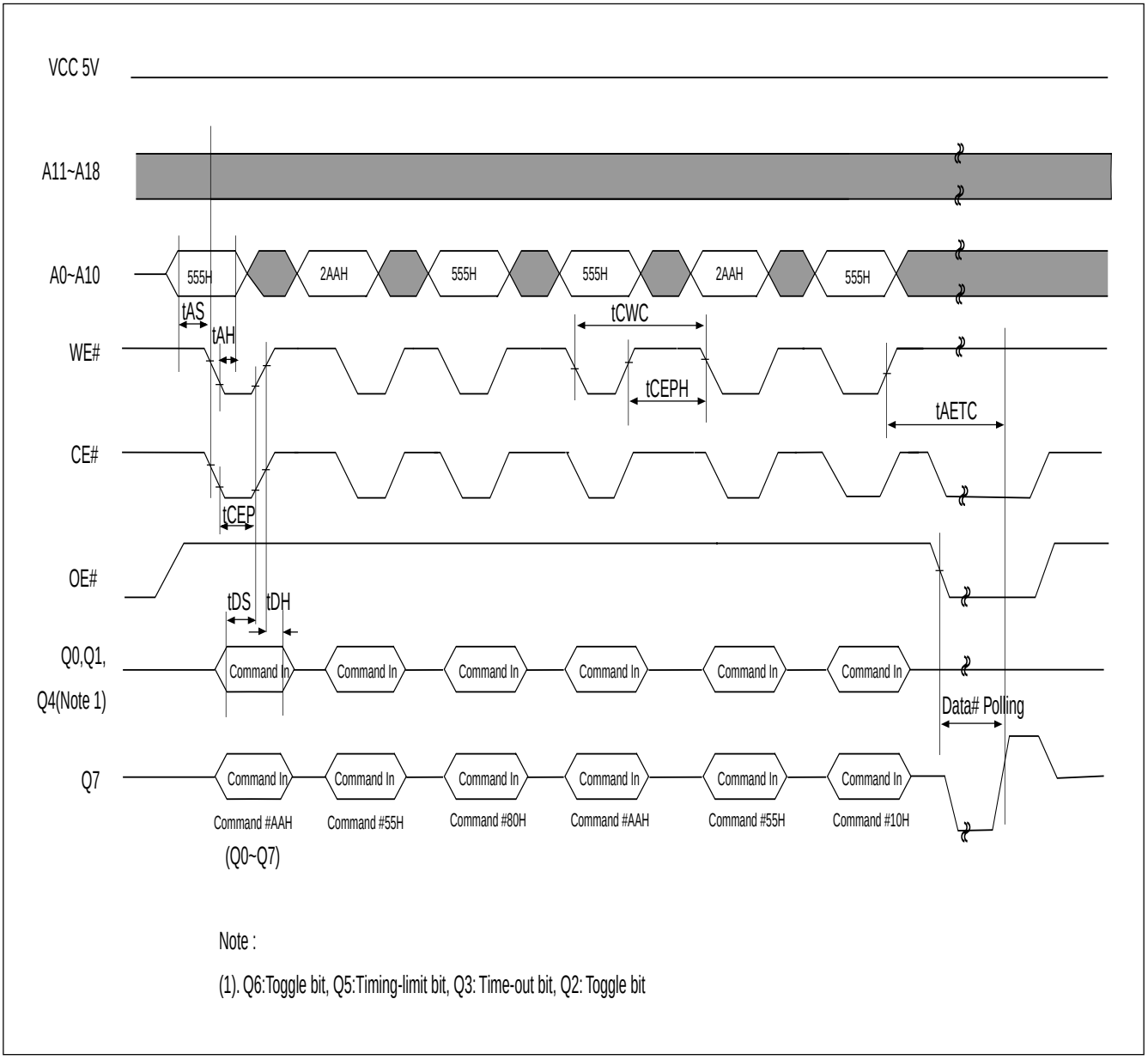
AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verification is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by Data# Polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, Data# Polling, timing waveform)

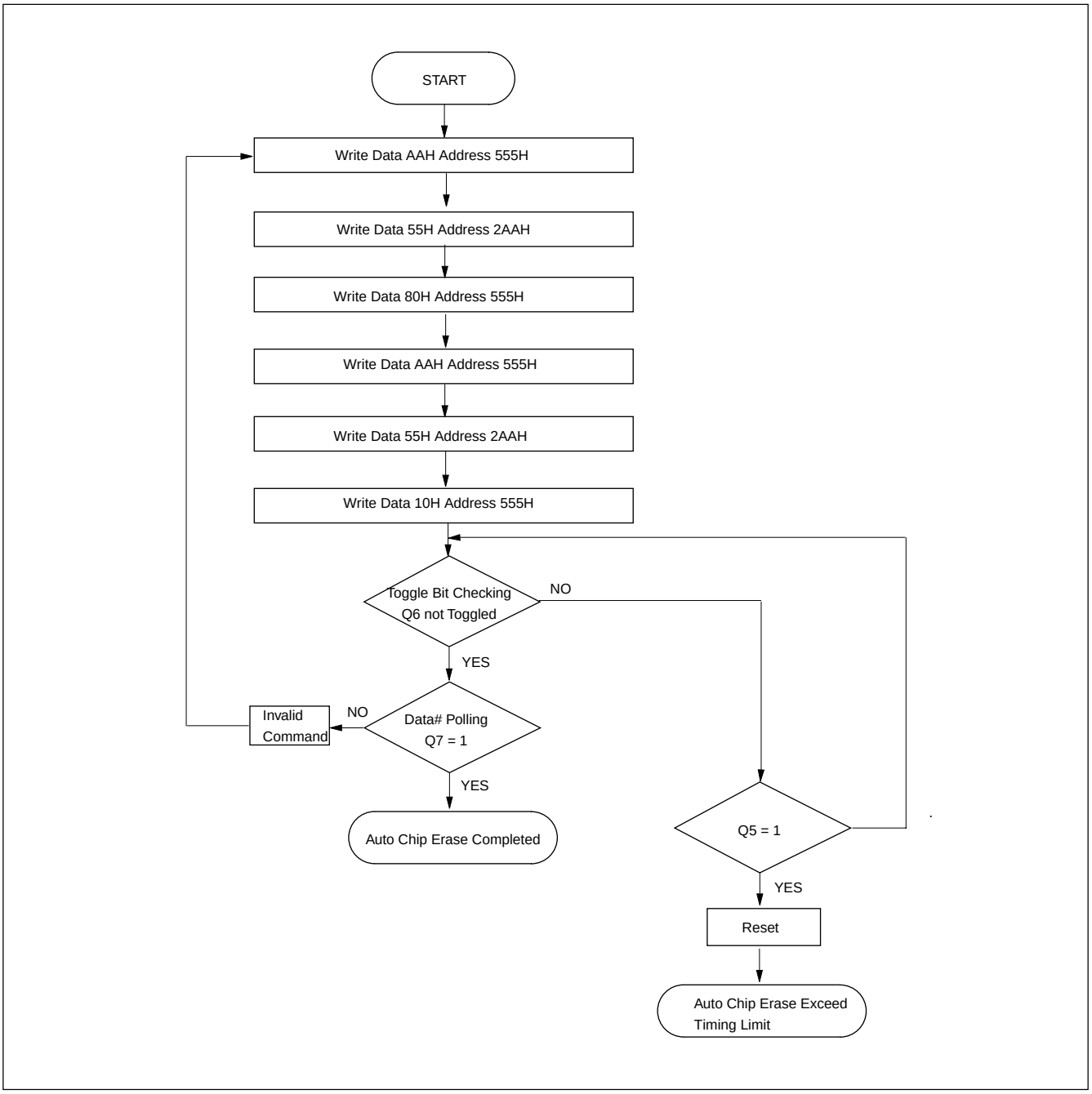
AUTOMATIC CHIP ERASE TIMING WAVEFORM



Note :

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

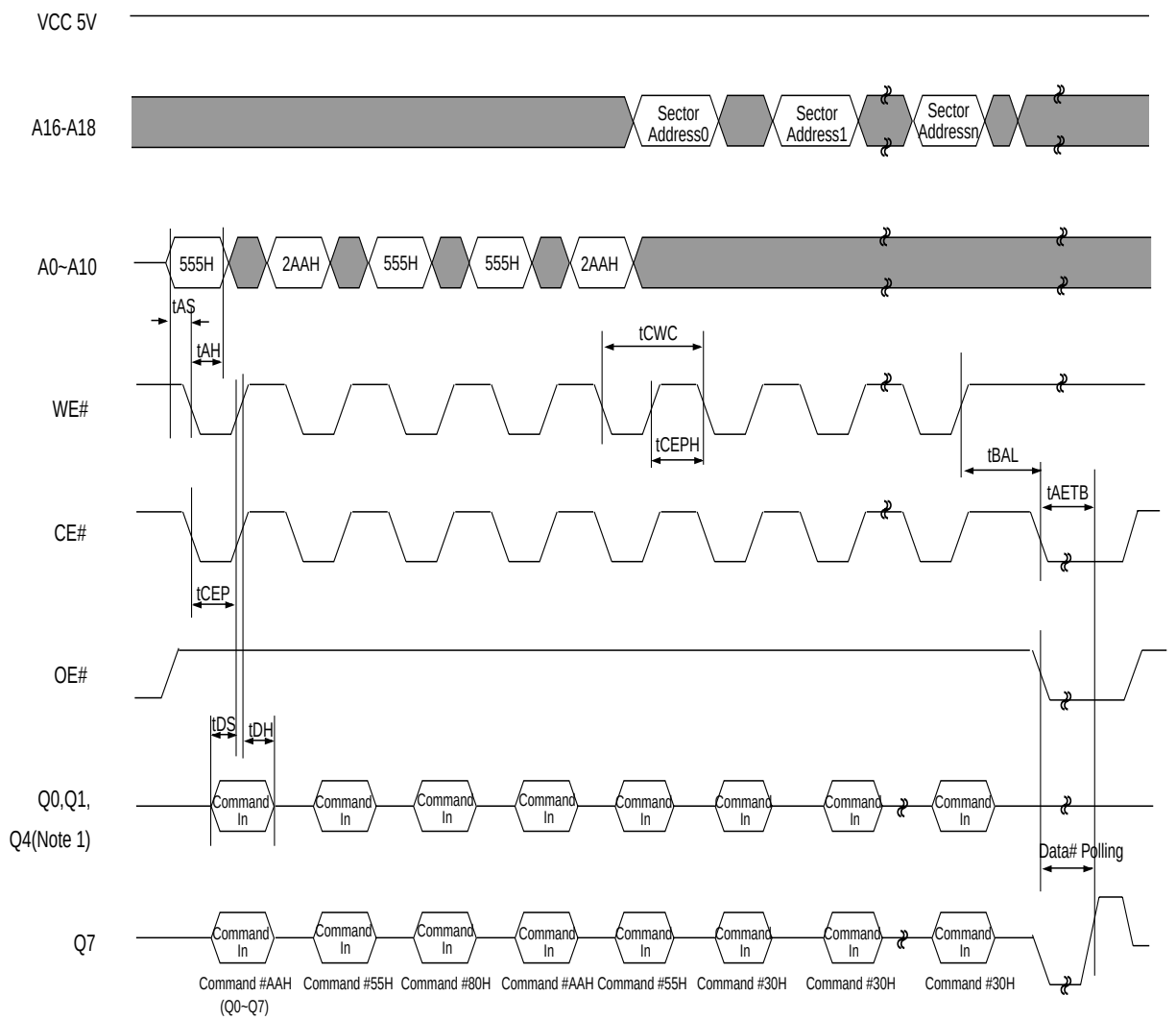
AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART



AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Sector data indicated by A16 to A18 are erased. External erase verify is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by Data# Polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, Data# Polling, timing waveform)

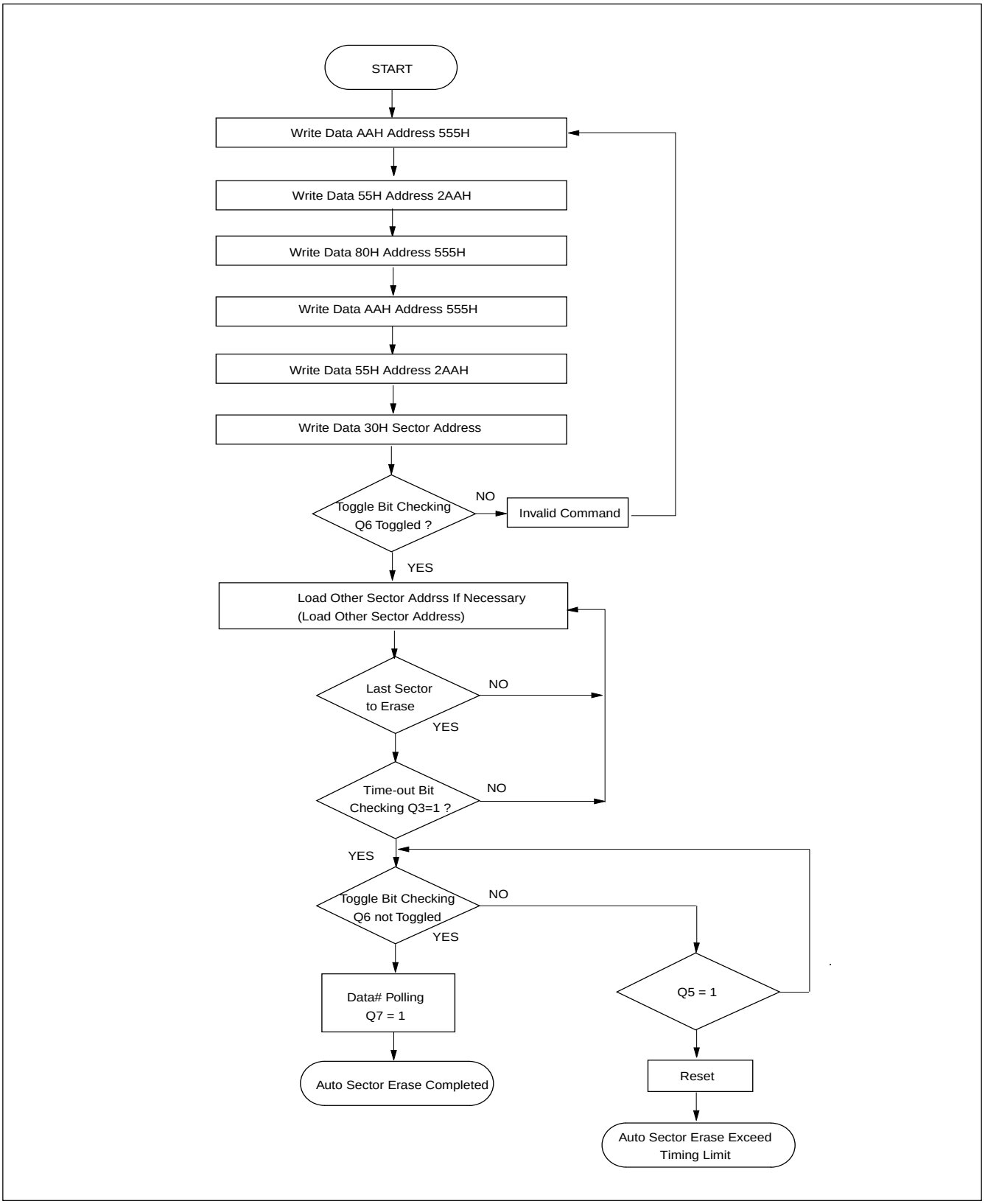
AUTOMATIC SECTOR ERASE TIMING WAVEFORM



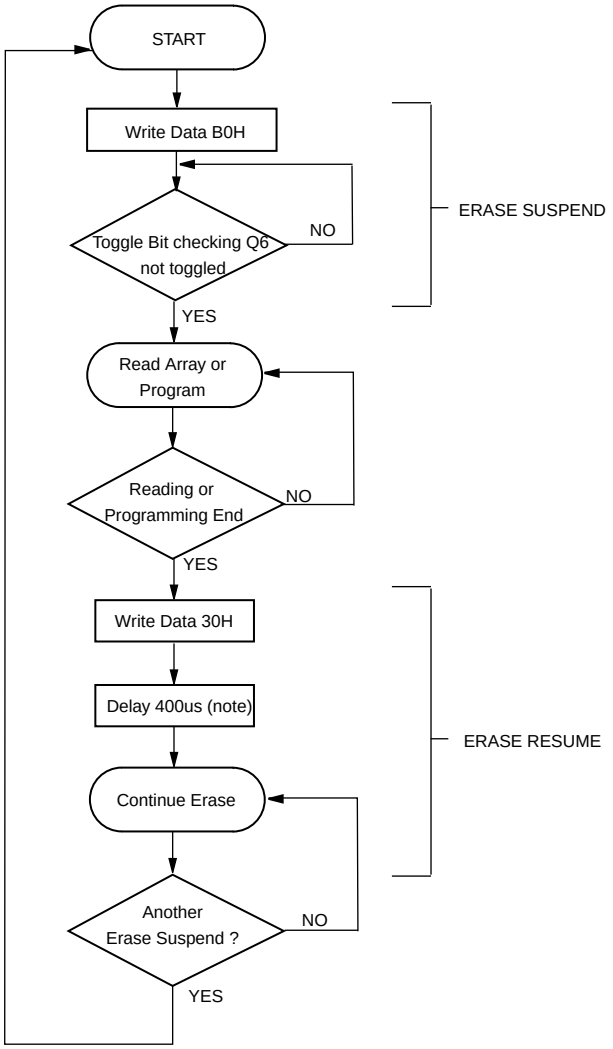
Note :

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

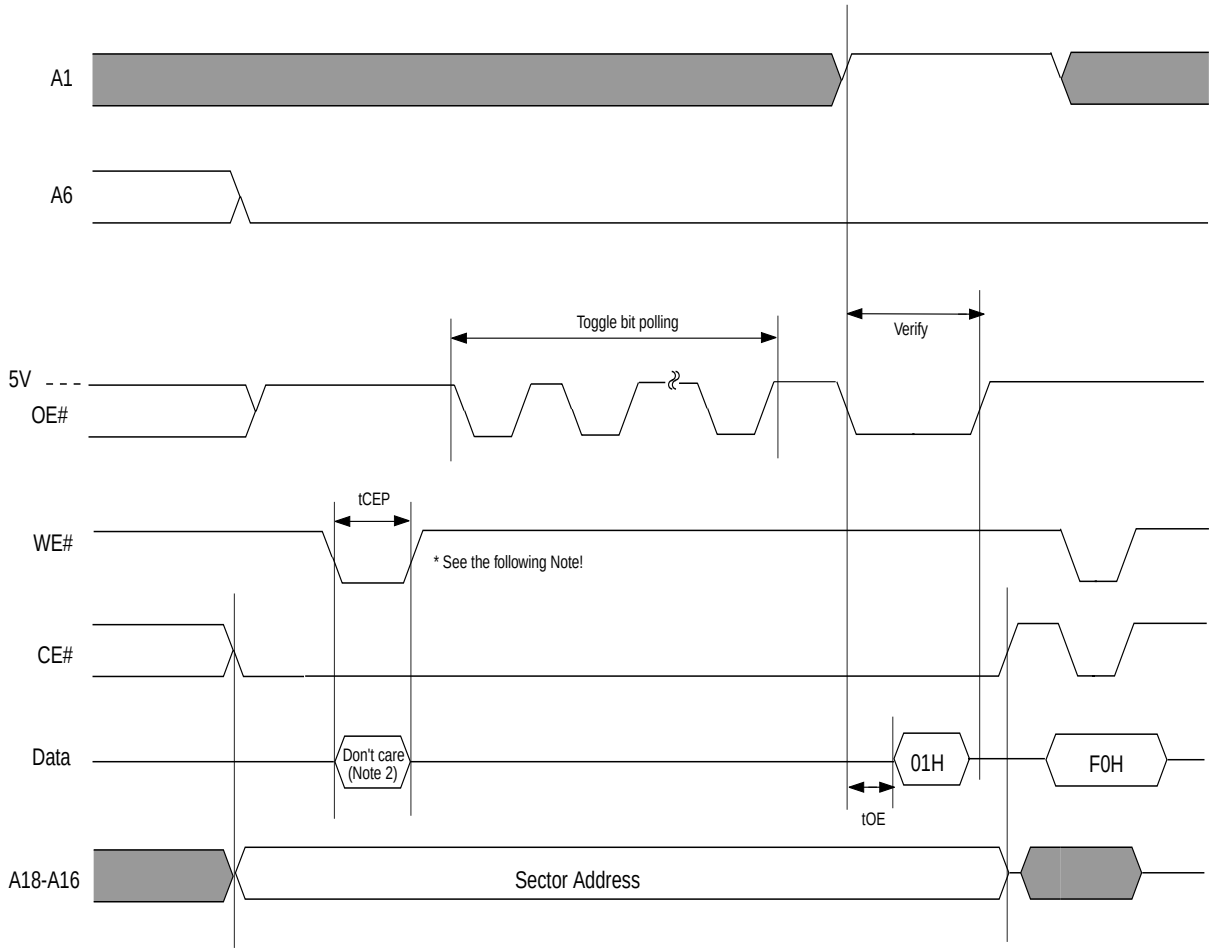


ERASE SUSPEND/ERASE RESUME FLOWCHART



Note: If the system implements an endless erase suspend/resume loop, or the number of erase suspend/resume is exceeded 1024 times, then the 400us time delay must be put into consideration.

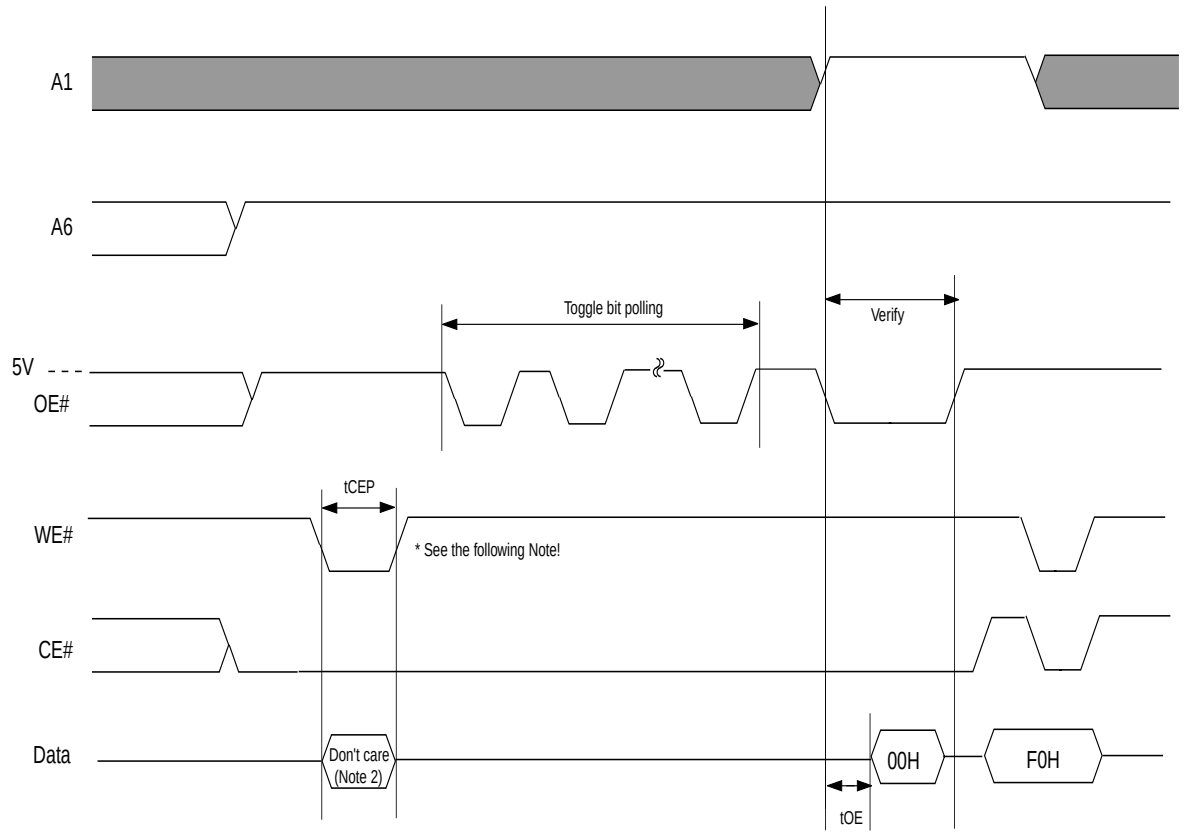
TIMING WAVEFORM FOR SECTOR PROTECTION FOR SYSTEM WITHOUT 12V



Note1: Must issue "unlock for sector protect/unprotect" command before sector protection for a system without 12V provided.

Note2: Except F0H

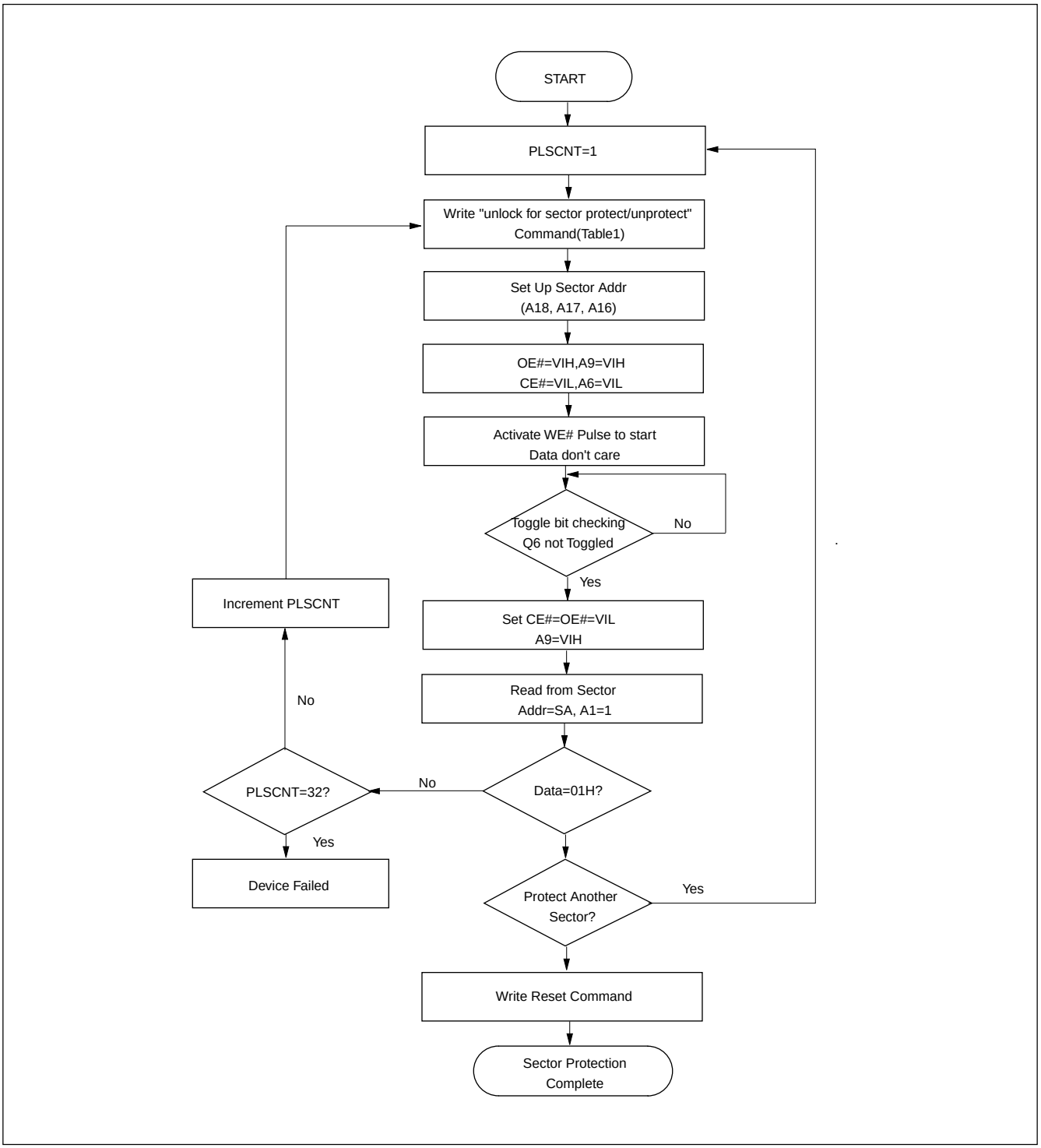
TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITHOUT 12V



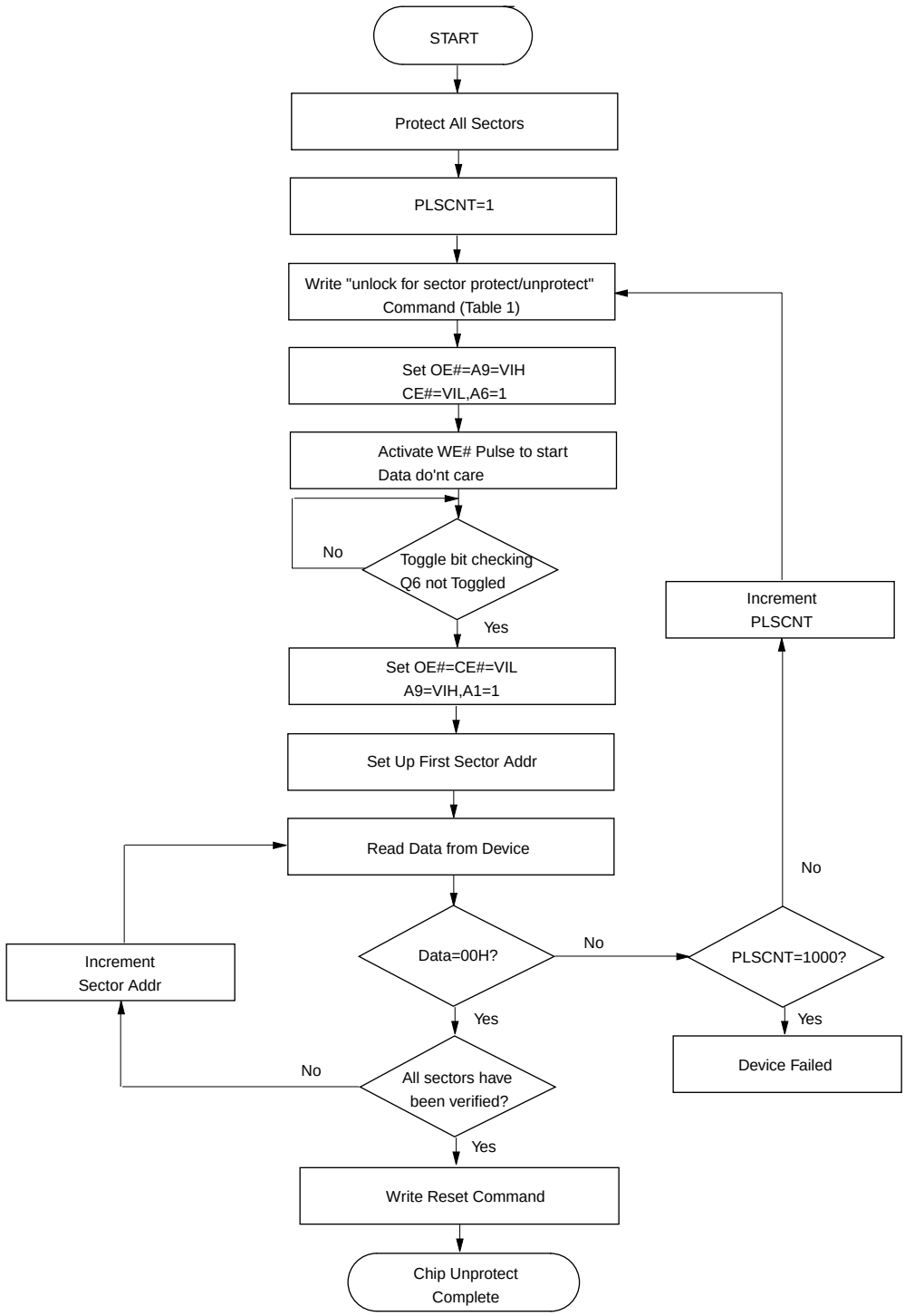
Note1: Must issue "unlock for sector protect/unprotect" command before sector unprotection for a system without 12V provided.

Note2: Except F0H

SECTOR PROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V

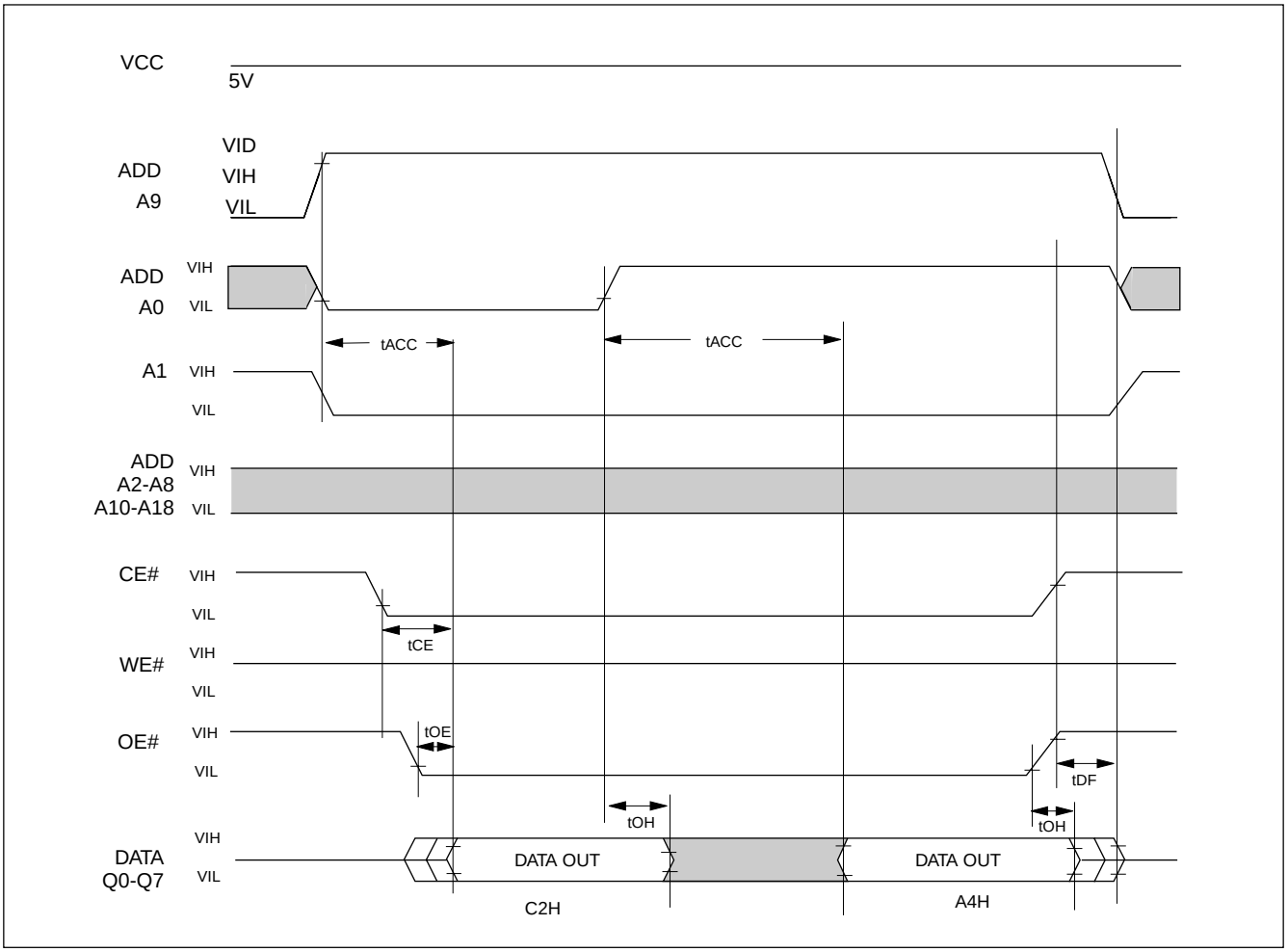


CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V



* It is recommended before unprotect whole chip, all sectors should be protected in advance.

ID CODE READ TIMING WAVEFORM



ERASE AND PROGRAMMING PERFORMANCE (1)

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX.(3)	
Sector Erase Time		0.7	15	sec
Chip Erase Time		4	32	sec
Byte Programming Time		9	300	us
Chip Programming Time		4.5	13.5	sec
Erase/Program Cycles	100,000			Cycles

Note: 1.Not 100% Tested, Excludes external system level over head.
2.Typical values measured at 25° C,5V.
3.Maximunm values measured at 25° C,4.5V.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.		

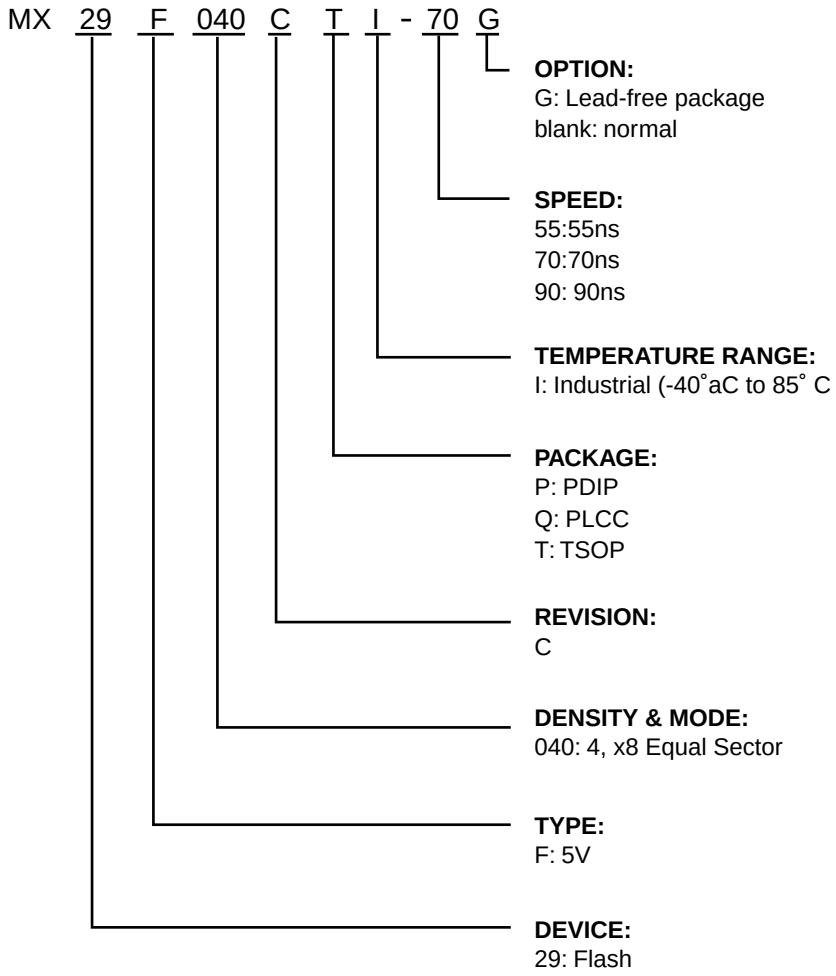
DATA RETENTION

PARAMETER	MIN.	UNIT
Data Retention Time	20	Years

ORDERING INFORMATION

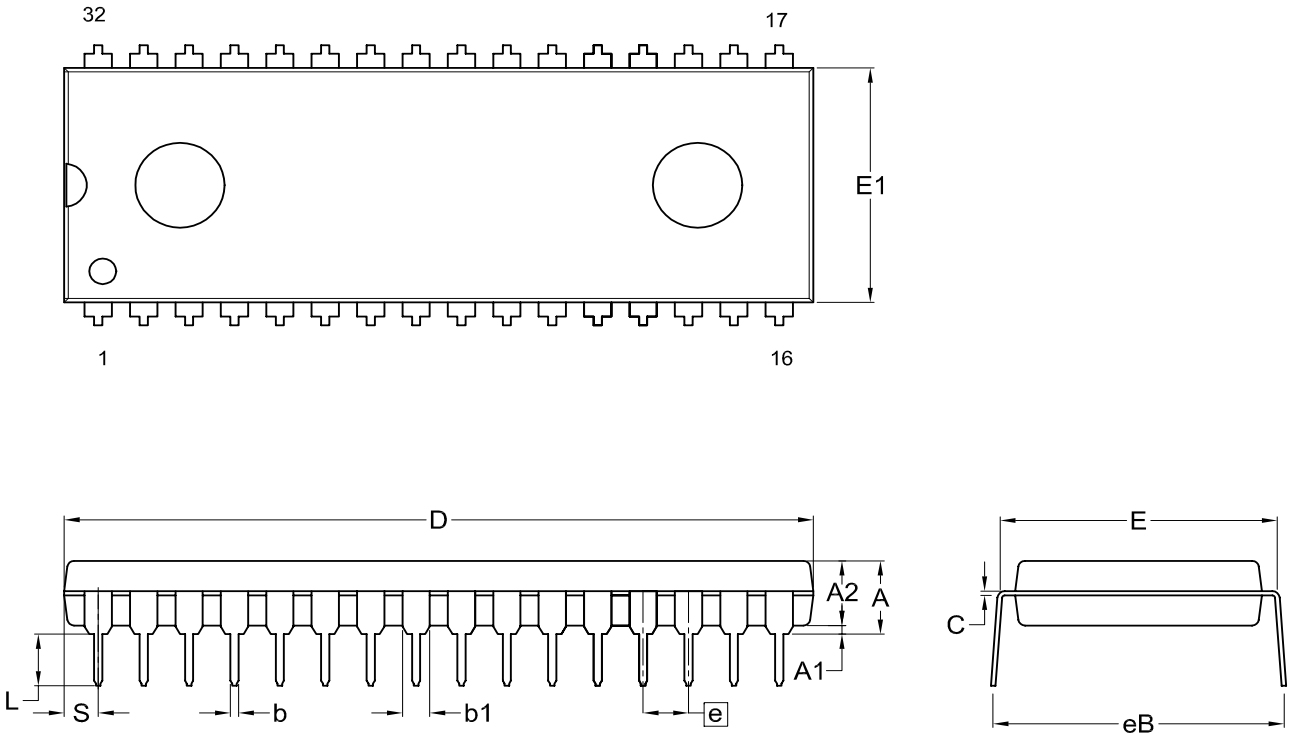
PART NO.	Access Time (ns)	Operating Current MAX.(mA)	Standby Current MAX.(uA)	Temperature Range	PACKAGE	Remark
MX29F040CQI-55	55	30	5	-40°C~85°C	32 Pin PLCC	
MX29F040CQI-70	70	30	5	-40°C~85°C	32 Pin PLCC	
MX29F040CQI-90	90	30	5	-40°C~85°C	32 Pin PLCC	
MX29F040CTI-55	55	30	5	-40°C~85°C	32 Pin TSOP (Normal Type)	
MX29F040CTI-70	70	30	5	-40°C~85°C	32 Pin TSOP (Normal Type)	
MX29F040CTI-90	90	30	5	-40°C~85°C	32 Pin TSOP (Normal Type)	
MX29F040CPI-55	55	30	5	-40°C~85°C	32 Pin PDIP	
MX29F040CPI-70	70	30	5	-40°C~85°C	32 Pin PDIP	
MX29F040CPI-90	90	30	5	-40°C~85°C	32 Pin PDIP	
MX29F040CQI-55G	55	30	5	-40°C~85°C	32 Pin PLCC	PB free
MX29F040CQI-70G	70	30	5	-40°C~85°C	32 Pin PLCC	PB free
MX29F040CQI-90G	90	30	5	-40°C~85°C	32 Pin PLCC	PB free
MX29F040CTI-55G	55	30	5	-40°C~85°C	32 Pin TSOP (Normal Type)	PB free
MX29F040CTI-70G	70	30	5	-40°C~85°C	32 Pin TSOP (Normal Type)	PB free
MX29F040CTI-90G	90	30	5	-40°C~85°C	32 Pin TSOP (Normal Type)	PB free
MX29F040CPI-55G	55	30	5	-40°C~85°C	32 Pin PDIP	PB free
MX29F040CPI-70G	70	30	5	-40°C~85°C	32 Pin PDIP	PB free
MX29F040CPI-90G	90	30	5	-40°C~85°C	32 Pin PDIP	PB free

PART NAME DESCRIPTION



PACKAGE INFORMATION

Title: Package Outline for PDIP 32L(600MIL)

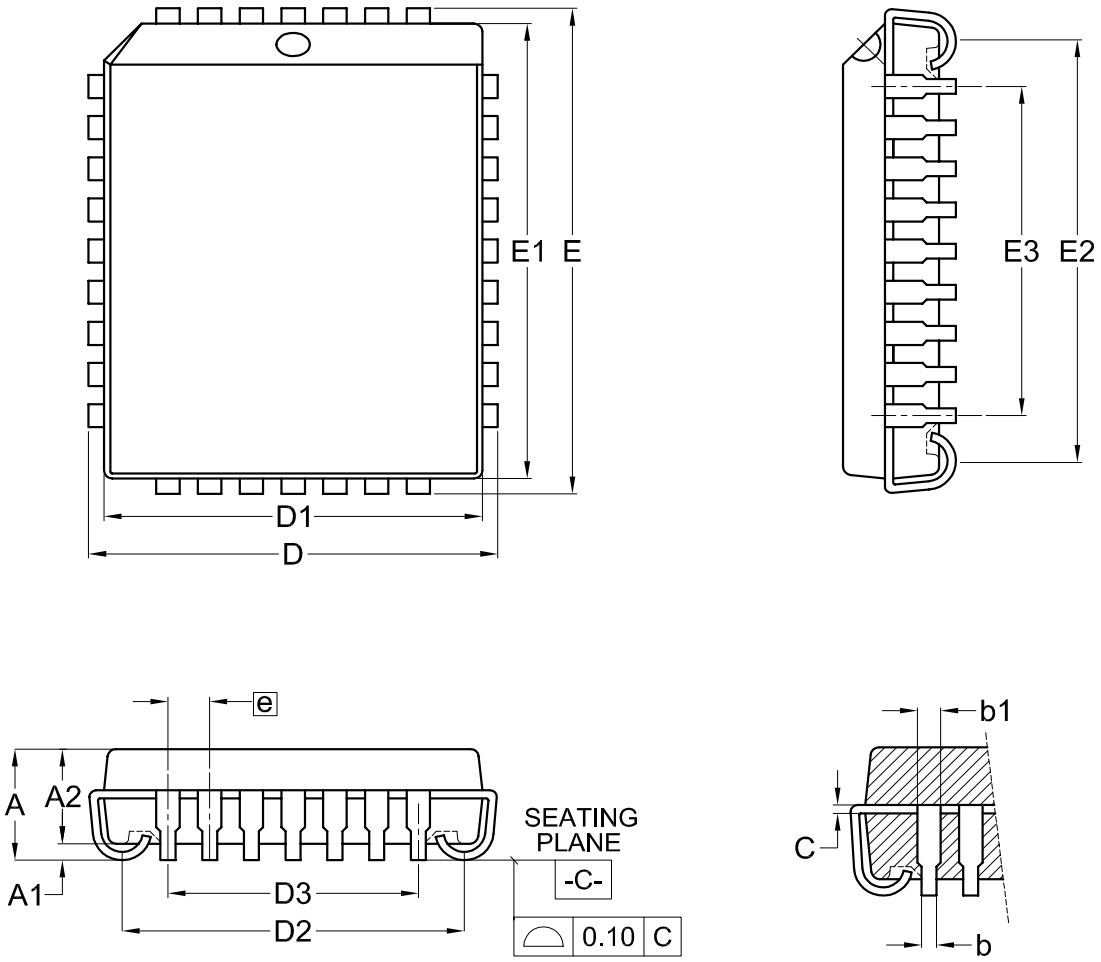


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	—	0.38	3.73	0.38	1.14	0.20	41.78	15.11	13.84		15.75	2.92	1.65
	Nom.	—	---	3.94	0.46	1.27	0.25	41.91	15.24	13.97	2.54	16.51	3.30	1.90
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	42.04	15.37	14.10		17.27	3.68	2.16
Inch	Min.	---	0.015	0.147	0.015	0.045	0.008	1.645	0.595	0.545		0.620	0.115	0.065
	Nom.	---	---	0.155	0.018	0.050	0.010	1.650	0.600	0.550	0.100	0.650	0.130	0.075
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	1.655	0.605	0.555		0.680	0.145	0.085

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.2	7				11-24-'03

Title: **Package Outline for 32L PLCC**

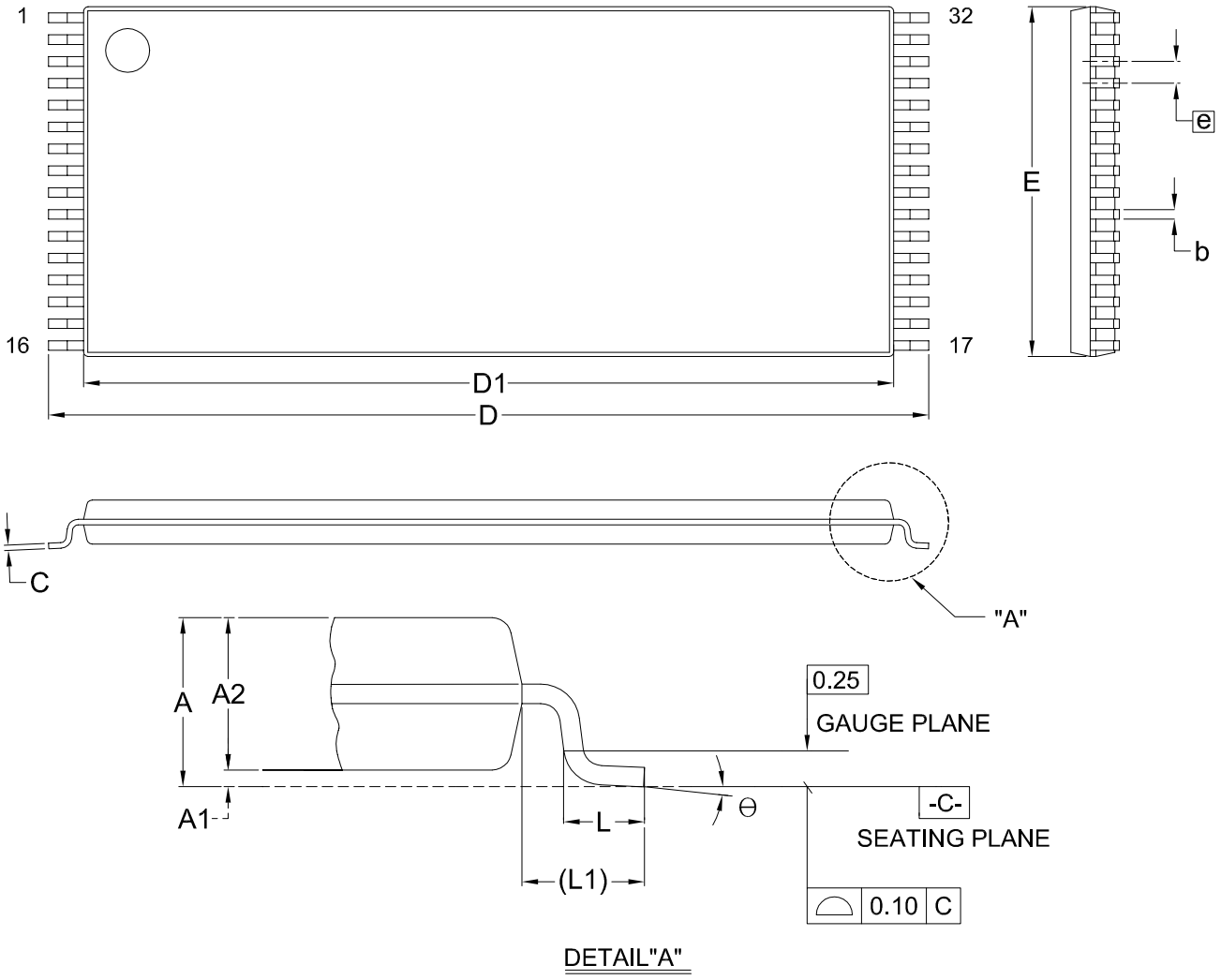


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
mm	Min.	---	0.38	2.69	0.38	0.61	0.20	12.32	11.36	10.11		14.86	13.98	12.65		
	Nom.	---	0.58	2.79	0.46	0.71	0.25	12.45	11.43	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.81	2.89	0.54	0.81	0.30	12.58	11.50	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.447	0.398		0.585	0.550	0.498		
	Nom.	---	0.023	0.110	0.018	0.028	0.010	0.490	0.450	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.032	0.114	0.021	0.032	0.012	0.495	0.453	0.422		0.595	0.556	0.522		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-2002	7	MS-016			12-10-'03

Title: **Package Outline for TSOP(I) 32L (8X20mm)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	9	MO-142			11-26-'03

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Preliminary" title	P1	DEC/20/2005
	2. Removed commercial grade	All	
	3. Added access time: 55ns; Removed access time: 120ns	All	

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