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## Revision History

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1 System Overview

1.1 System Block Diagram

Figure 1-1 SPHE8202R System Block Diagram
1.2 System Feature

- SOC (RF integrated)
- Support MPEG4
- Support USB 2.0 (Full Speed)
- Support 3 in 1 Card Reader (SD, MS, MS-pro, MMC)
- SDRAM: Support 16M bits to 256M bits, with 16 bits mode
- ROM/FLASH: Support SPI flash
- Support boot-trap mode
- TV: 4 TV DAC output (full current output)
- Audio: internal DAC 5.1ch output, support AC3, DTS and SPDIF OUT
- MIC: Support internal ADC (1ch) function
- Support IR / VFD interface
- Support 8bits game pad
- Support full color Native32 game
- Support CD-Ripping
2 Component Layout

Figure 2-1 SPHE8202R Layout (Top View)
3.1 Video

(1) SPHE8202R

- Video
- filter
- COMP
- 1uF
- Rset
- 1K ohm

![Figure 3-1 SD DAC - buffer + filter + protector](image)

(2) SPHE8202R

- Video power
- 3.3V
- SPHE8202R
- Video power pin
- bypass

![Figure 3-2 HD DAC - HPA00191DR](image)
3.2 SDRAM

(1) SPHE8202R support 16-bit mode

Figure 3-3  SDRAM 16-bit mode

(2) SDRAM data bus damping 33 ohm SDRAM clock RC (R 33 ohm C 10 pF) SPHE8202R

Figure 3-4  SDRAM data bus and clock
3.3 SPI Flash (Serial Peripheral Interface Flash)

- SPI flash
- 3-5
- R1: 10K ohm
- R2: 0 ohm

![SPI Flash Circuit](image)

Figure 3-5  SPI Flash Circuit

3.4 Audio

(1) SPHE8202R
- Audio
- DAC
- ADC
- power
- 3.3V
- ground
- 3-6

![Audio power](image)

Figure 3-6  Audio power
(2) SPHE8202R Audio DAC output Audio ADC mapping release Audio DAC output mapping

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<thead>
<tr>
<th>8202R Pin Number</th>
<th>Function</th>
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<tr>
<td>56</td>
<td>CENTER</td>
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<tr>
<td>57</td>
<td>SW</td>
</tr>
<tr>
<td>59</td>
<td>RS</td>
</tr>
<tr>
<td>60</td>
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<td>65</td>
<td>FL</td>
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<td>66</td>
<td>FR</td>
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3.5 RESET Circuit

![Diagram of Reset Circuit]

Figure 3-7 Reset Circuit
3.6 UART

debug SPHE8202R code UART

Figure 3-8 UART port

3.7 Card Reader

8202R card reader interface card sense pin card reader

3.8 Servo (OPU & Motor Driver)

Servo power ground

(1) A+5V Power

OPU power connector pad

Bypass

Figure 3-9 A+5V power
(2) M+5V Power

![Diagram of M+5V power](image)

Figure 3-10  M+5V power

(3) RF3.3V power

![Diagram of RF3.3V power](image)

Figure 3-11  RF3.3V power
(4) RF

RF traces are routed away from sensitive areas to prevent interference. PUHRF is connected to ground through an AC-coupled trace. SPHE8202R is used as a motor driver. AC coupling is used to filter out noise.

Figure 3-12 PHURF layout

(5)

SPHE8202R is used as a motor driver. LPF is used to filter the signal. Close to SPHE8202R, certain components are used for filtering.

Figure 3-13 Motor Driver
3.9 Servo DVDVR/CDVR Application

Figure 3-14  DVDVR/CDVR circuit

Figure 3-15  DVDVR/CDVR circuit
4 EMI Considerations

4.1 Crystal

Figure 4-1 Crystal layout

4.2 Loader Control Signals

Figure 4-2 Load control signals
4.3 PCB Layout

(1) Power trace

![Figure 4-3  Power trace layout](image)

(2) I/O connector

![Figure 4-4  Power trace with I/O connector](image)
(3) Ground plane (power and ground plane)

Figure 4-5: Ground plane

(4) Ground plane

Figure 4-6: Ground plane
(5) IC power trace IC IC IC

EMI Bad design

Figure 4-7 IC

4.4 USB EMI

USB

120 2A 90

Figure 4-8 USB
Figure 4-9 SDCW2012-2-900

- Common Mode
- Differential Mode

SDCW2012-2-900 100MHz
4.6 4-9

Only for ZIHUAN