SONY

CXA3355ER

GPS Down Converter IC

Description

The CXA3355ER is an IC developed as a GPS RF down converter. This IC realizes a reduction in the number of external parts by integrating an LNA, image rejection mixer, IF filter, PLL and VCO (L, C) into a small package with low current consumption.

Features

- Includes all functions required for the GPS down converter
- Low voltage operation: V_{CC} = 1.6 to 2.0V
- Low current consumption (active mode):
  11mA (Typ. at V_{CC} = 1.8V, IF ≈ 1MHz)
- Low current consumption (power save mode) < 1µA
- Total gain ≈ 100dB
- Total NF ≈ 4dB
- On-chip VCO and PLL
- Supports typical TCXO frequencies (13MHz, 16.368MHz, 18.414MHz, etc.)
- On-chip LNA (LNA NF: 2.0dB)
- Image rejection mixer
- On-chip IF filter, and an external filter can be connected as an option for further band narrowing.
- 1-bit IF output
- Antenna sense function

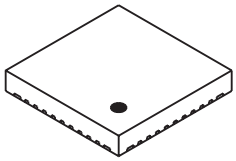
Applications

GPS down converter IC

Structure

SiGe BiCMOS monolithic IC

44 pin VQFN (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

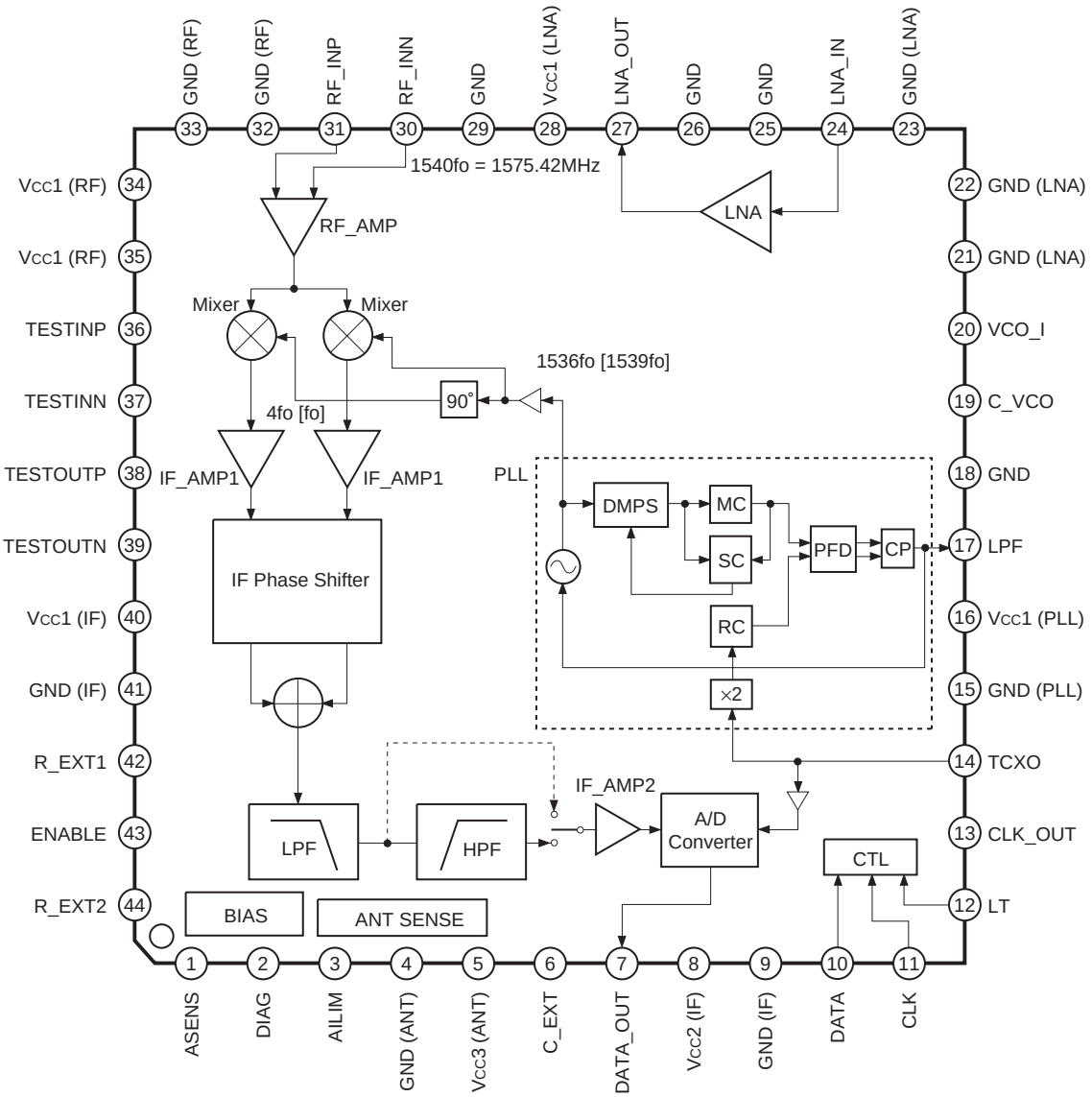
• Supply voltage	$V_{CC}1$	–0.2 to +2.5	V
	$V_{CC}2$	–0.2 to +3.6	V
	$V_{CC}3$	–0.2 to +3.6	V
• Operating temperature	Topr	–40 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

Supply voltage	$V_{CC}1$	1.6 to 2.0	V
	$V_{CC}2$	1.6 to 3.3	V
	$V_{CC}3$	2.7 to 3.3	V

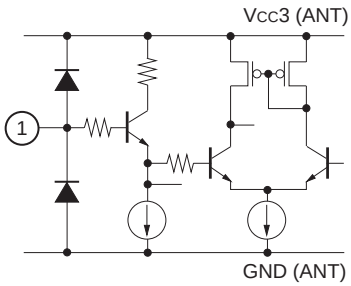
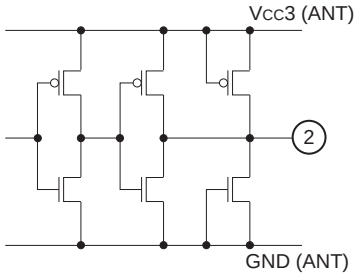
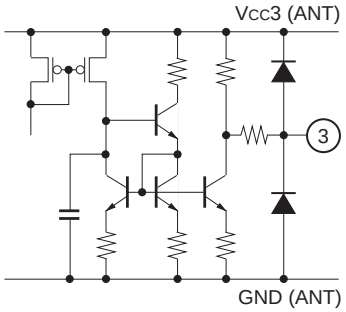
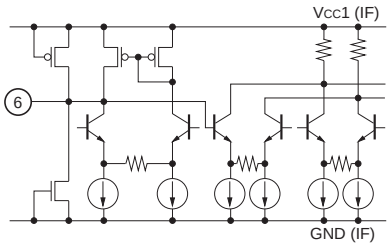
E04156-PS

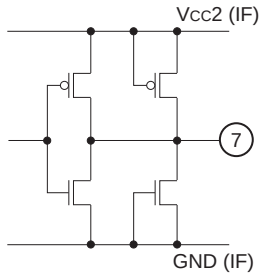
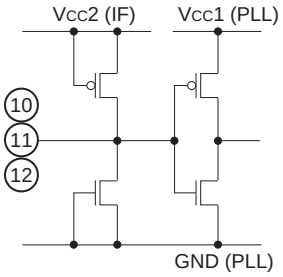
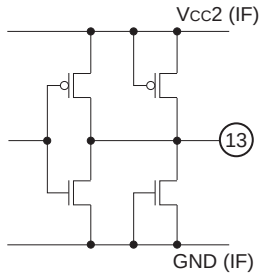
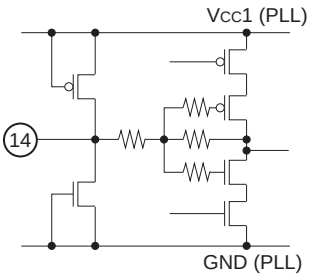
Block Diagram and Pin Configuration

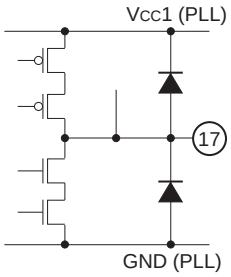
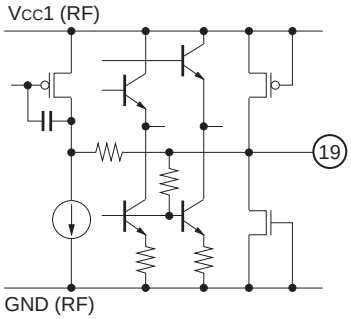
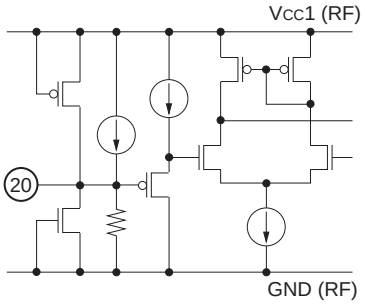
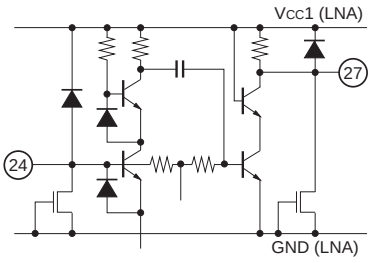


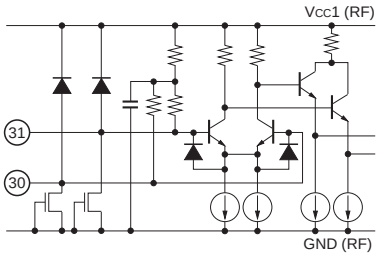
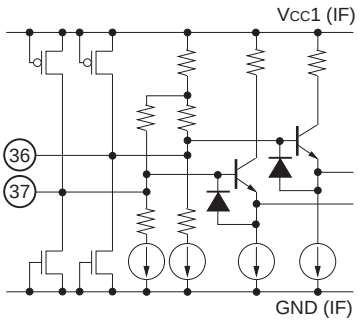
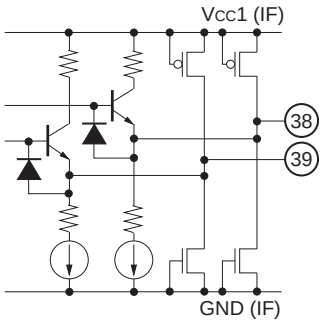
fo mode: IF = 1.023MHz
4fo mode: IF = 4.092MHz

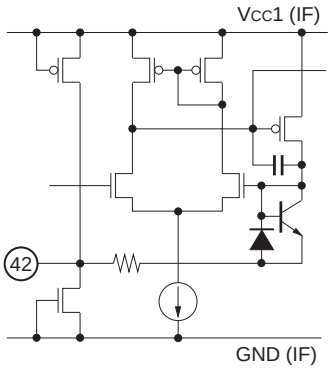
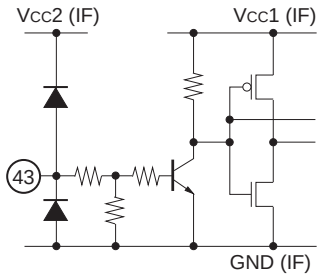
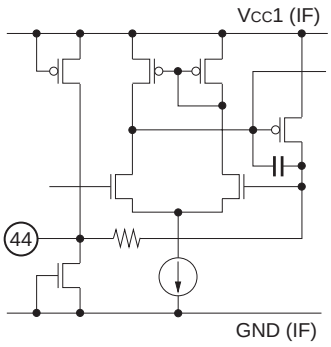
Pin Description

Pin No.	Symbol	Standard pin voltage [V]		Equivalent circuit	Description
		DC	AC		
1	ASENS	—	—		Antenna sense input.
2	DIAG	—	—		Antenna sense output.
3	AILIM	—	—		Antenna sense current limitation. Connect to the external PNP transistor base pin.
4	GND (ANT)	0	—		Antenna sense GND.
5	Vcc3 (ANT)	3.0	—		Antenna sense Vcc. Leave open when not using the antenna sense function.
6	C_EXT	1.2	—		Capacitor connection for canceling the offset.

Pin No.	Symbol	Standard pin voltage [V]		Equivalent circuit	Description
		DC	AC		
7	DATA_OUT	—	1.8Vp-p		Data (IF) output.
8	Vcc2 (IF)	1.8	—		IF block Vcc.
9	GND (IF)	0	—		IF block GND.
10	DATA	—	—		Serial data input.
11	CLK	—	—		Serial data clock input.
12	LT	—	—		Latch signal input.
13	CLK_OUT	—	1.8Vp-p		TCXO clock output. Leave open when not using the TCXO clock.
14	TCXO	—	—		Reference frequency input.
15	GND (PLL)	0	—		PLL block GND.
16	Vcc1 (PLL)	1.8	—		PLL block Vcc.

Pin No.	Symbol	Standard pin voltage [V]		Equivalent circuit	Description
		DC	AC		
17	LPF	1.2	—		PLL loop filter connection.
18	GND	0	—		GND.
19	C_VCO	1.1	—		Capacitor connection for decoupling the VCO bias circuit.
20	VCO_I	0.1	—		Capacitor connection for decoupling the VCO bias circuit.
21	GND (LNA)	0	—		LNA block GND.
22	GND (LNA)	0	—		LNA block GND.
23	GND (LNA)	0	—		LNA block GND.
24	LNA_IN	0.8	—		LNA input.
27	LNA_OUT	1.8	—		LNA output.

Pin No.	Symbol	Standard pin voltage [V]		Equivalent circuit	Description
		DC	AC		
25	GND	0	—		GND.
26	GND	0	—		GND.
28	Vcc1 (LNA)	1.8	—		LNA block Vcc.
29	GND	0	—		GND.
30	RF_INN	1.7	—		RF amplifier input.
31	RF_INP	1.7	—		
32	GND (RF)	0	—		RF block GND.
33	GND (RF)	0	—		RF block GND.
34	Vcc1 (RF)	1.8	—		RF block Vcc.
35	Vcc1 (RF)	1.8	—		RF block Vcc.
36	TESTINP	1.3	—		IF signal input when using an external filter.
37	TESTINN	1.3	—		IF signal input when using an external filter.
38	TESTOUTP	0.5	—		IF signal output when using an external filter.
39	TESTOUTN	0.5	—		IF signal output when using an external filter.
40	Vcc1 (IF)	1.8	—		IF block Vcc.
41	GND (IF)	0	—		IF block GND.

Pin No.	Symbol	Standard pin voltage [V]		Equivalent circuit	Description
		DC	AC		
42	R_EXT1	0.5	—		External resistor connection. (bias)
43	ENABLE	—	—		ENABLE signal input. High (V_IH: 1.2V min.): Active mode Low (V_IL: 0.2V max.): Power save mode
44	R_EXT2	1.2	—		External resistor connection. (bias)

Electrical Characteristics

DC Characteristics

($V_{CC}1$ = $V_{CC}2$ = 1.8V, $V_{CC}3$ = OPEN, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current 1	$I_{CC}1$	fo mode, excluding the antenna sense circuit	7	11	15	mA
Supply current 2	$I_{CC}2$	4fo mode, excluding the antenna sense circuit	9	13	17	mA
Supply current 3	$I_{CC}3$	Power save mode	—	0.1	1	µA
Input impedance	Zin	Pin 36 (TESTINP), Pin 37 (TESTINN)	50	100	200	Ω
Output impedance	Zout	Pin 38 (TESTOUTP), Pin 39 (TESTOUTN)	50	100	200	Ω

Note: fo mode and 4fo mode use the following power-on reset conditions.

fo mode: TCXO = 18.414MHz, f_{LO} = 1574.397MHz, IF = 1.023MHz

4fo mode: TCXO = 16.368MHz, f_{LO} = 1571.328MHz, IF = 4.092MHz

AC Characteristics

($V_{CC}1$ = $V_{CC}2$ = 1.8V, $V_{CC}3$ = OPEN, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total voltage gain	G	Excluding the A/D converter	85	100	—	dB
LNA NF1	NF1	50Ω matching, fo mode	—	3.0	6	dB
LNA NF2	NF2	50Ω matching, 4fo mode	—	2.0	5	dB
Total NF1	TNF1	50Ω matching, fo mode	—	5.0	8.5	dB
Total NF2	TNF2	50Ω matching, 4fo mode	—	4.0	7.5	dB
P-1dB input	P1dB	Up to before the A/D converter	—	–100	—	dBm
Image rejection ratio	IMRR	Detuning frequency = 1.023MHz, 4.092MHz	—	–40	–20	dBc
LPF1 (fo mode)	LPF1	@150kHz Normalized at the 1.023MHz level	–5	—	4	dB
LPF2 (fo mode)	LPF2	@2.046MHz Normalized at the 1.023MHz level	–13	—	2	dB
LPF3 (fo mode)	LPF3	@6MHz Normalized at the 1.023MHz level	—	—	–13	dB
BPF1 (4fo mode)	BPF1	@1MHz Normalized at the 4.092MHz level	—	—	–6	dB
BPF2 (4fo mode)	BPF2	@3.069MHz Normalized at the 4.092MHz level	–9	—	6.5	dB
BPF3 (4fo mode)	BPF3	@5.115MHz Normalized at the 4.092MHz level	–9	—	6.5	dB
BPF4 (4fo mode)	BPF4	@12MHz Normalized at the 4.092MHz level	—	—	–6	dB
C/N 100K	C/N	4fo mode, TCXO = 16.368MHz	—	–70	–55	dBc/Hz
Spurious component	Sp	4fo mode, ratio of the carrier level and the reference leak level	—	–40	—	dBc

Note: fo mode and 4fo mode use the following power-on reset conditions.

fo mode: TCXO = 18.414MHz, f_{LO} = 1574.397MHz, IF = 1.023MHz

4fo mode: TCXO = 16.368MHz, f_{LO} = 1571.328MHz, IF = 4.092MHz

IF Output Signal (DATA_OUT) (Vcc1 = Vcc2 = 1.8V, Vcc3 = OPEN, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
DATA_OUT rise time	DTr	Pin 7 (DATA_OUT) 10 to 90% Load = 1MΩ//13pF	—	6	—	ns
DATA_OUT fall time	DTf	Pin 7 (DATA_OUT) 10 to 90% Load = 1MΩ//13pF	—	4	—	ns

ENABLE Signal (Vcc1 = 1.8 ± 0.2V, Vcc1 ≤ Vcc2 ≤ 3.3V, 2.7V ≤ Vcc3 ≤ 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage high level	EVIH	Pin 43 (ENABLE) input voltage high level threshold voltage	1.2	—	Vcc2 + 0.2	V
Input voltage low level	EVIL	Pin 43 (ENABLE) input voltage low level threshold voltage	–0.1	—	0.2	V

Power-on Reset Function (Vcc1 = 1.8 ± 0.2V, Vcc1 ≤ Vcc2 ≤ 3.3V, 2.7V ≤ Vcc3 ≤ 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Allowable rise time	MTr	ENABLE and power supply (Vcc1, Vcc2) rise time for the power-on reset function to operate. **Note:** Use an ENABLE and power supply (Vcc1, Vcc2) rise time of 100ms or less.	—	—	100	ms

TCXO (Vcc1 = Vcc2 = 1.8V, Vcc3 = OPEN, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input level	Vtcxo	Input level to Pin 14 (TCXO)	0.2	0.6	1.2	Vp-p
CLK_OUT rise time	CTr	Pin 13 (CLK_OUT) 10 to 90% Load = 1MΩ//13pF	—	6	—	ns
CLK_OUT fall time	CTf	Pin 13 (CLK_OUT) 10 to 90% Load = 1MΩ//13pF	—	4	—	ns

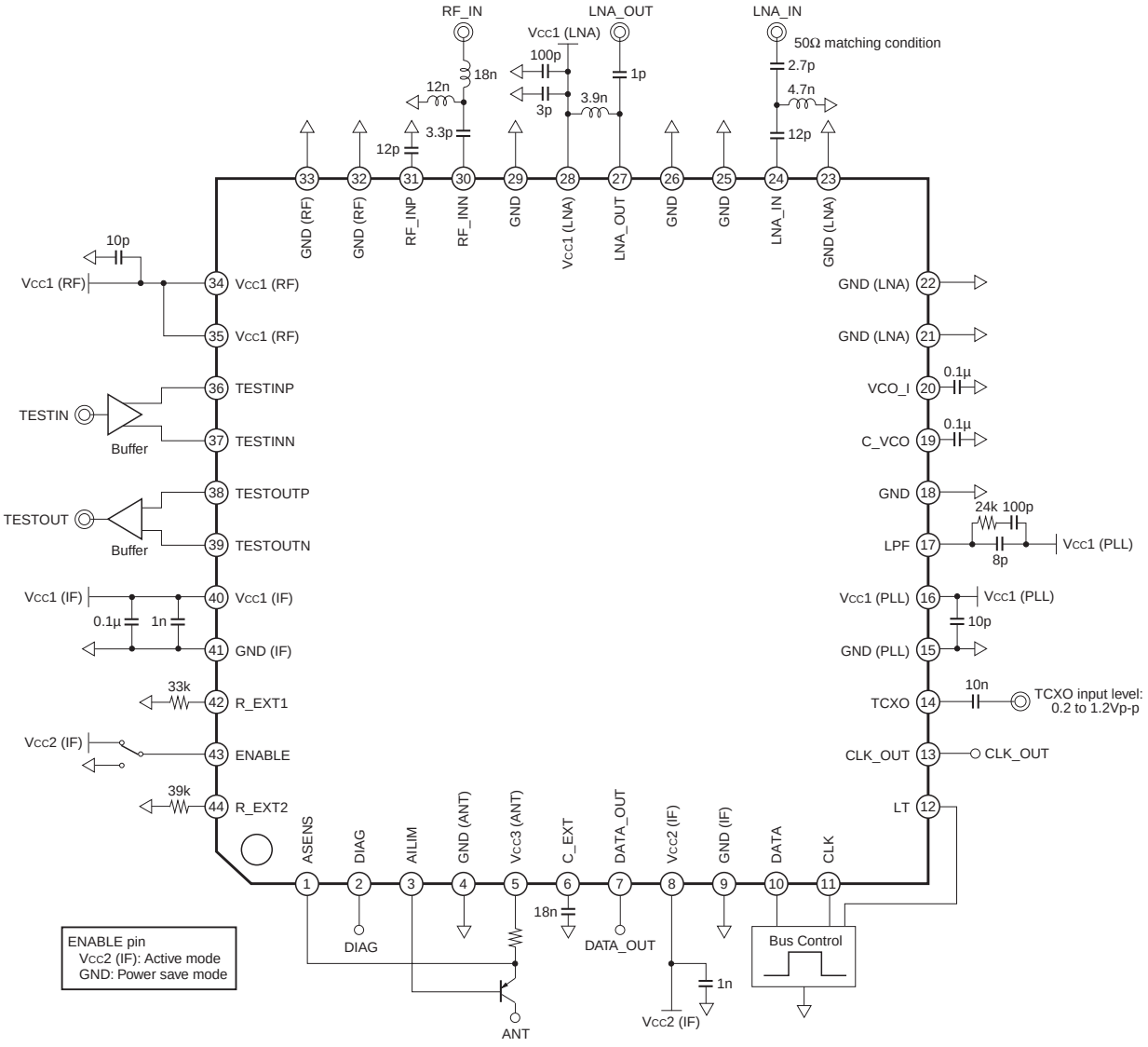
Threshold Voltage Value (Vcc1 = 1.8 ± 0.2V, Vcc1 ≤ Vcc2 ≤ 3.3V, 2.7V ≤ Vcc3 ≤ 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logic input voltage high level	VIH	Logic input pins = Pin 10 (DATA), Pin 11 (CLK), Pin 12 (LT)	Vcc2 – 0.2	—	Vcc2 + 0.2	V
Logic input voltage low level	VIL	Logic input pins = Pin 10 (DATA), Pin 11 (CLK), Pin 12 (LT)	–0.1	—	0.2	V
Logic output voltage high level	VOH	Logic output pin = Pin 2 (DIAG)	Vcc3 – 0.2	—	Vcc3	V
		Logic output pins = Pin 7 (DATA_OUT), Pin 13 (CLK_OUT)	Vcc2 – 0.2	—	Vcc2	V
Logic output voltage low level	VOL	Logic output pins = Pin 7 (DATA_OUT), Pin 13 (CLK_OUT)	0	—	0.2	V

Threshold Voltage Value (Antenna Sense) ($V_{CC}1 = V_{CC}2 = 1.8V$, $V_{CC}3 = 3V$, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Threshold voltage 1	Vs1	Threshold voltage at which connection of the prescribed load is detected from the open status	10	30	60	mV
Threshold voltage 2	Vs2	Threshold voltage for switching to the short status from the prescribed load connected status	140	170	200	mV

Electrical Characteristics Measurement Circuit



* The RF block bypass capacitors should have excellent high frequency characteristics.
* Use parts with a tolerance of ±1% for the following resistor elements. Other parts should have a tolerance of ±5%.
  - Pin 17 (LPF)
  - Pin 42 (R_EXT1)
  - Pin 44 (R_EXT2)

Measurement Methods

Note: The measurement methods in 4fo mode (TCXO = 16.368MHz, IF = 4.092MHz) are described below.

1) Total Gain

Input: LNA_IN

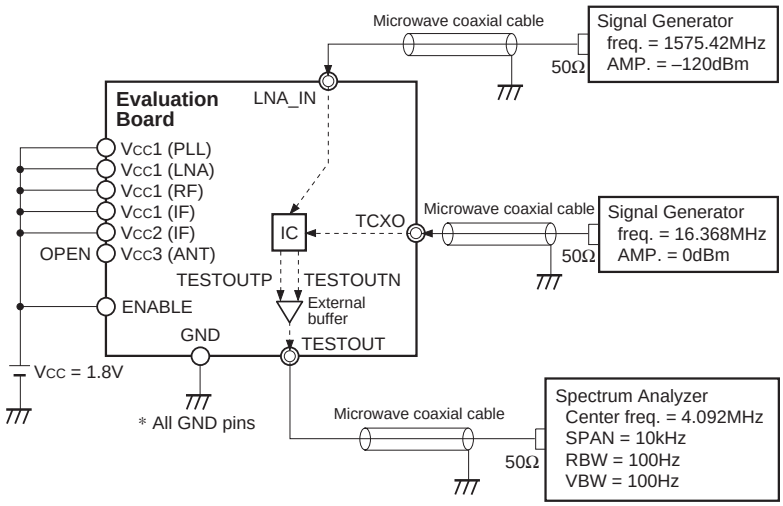
Output: TESTOUTP (Pin 38), TESTOUTN (Pin 39) ··· [Pins 38 and 39 are differential output.]

Serial data setting: Test output block "4" (IF AMP2 output block) ··· See page 19.

Monitor method: (1) Perform differential – single conversion using an external buffer circuit and measure the output level. ··· [Sony recommended method]

(2) Measure Pins 38 and 39 with a differential probe.

* Total Gain: Output level [dBm] – SG input level to LNA_IN [dBm]



2) LNA NF

Input: LNA_IN

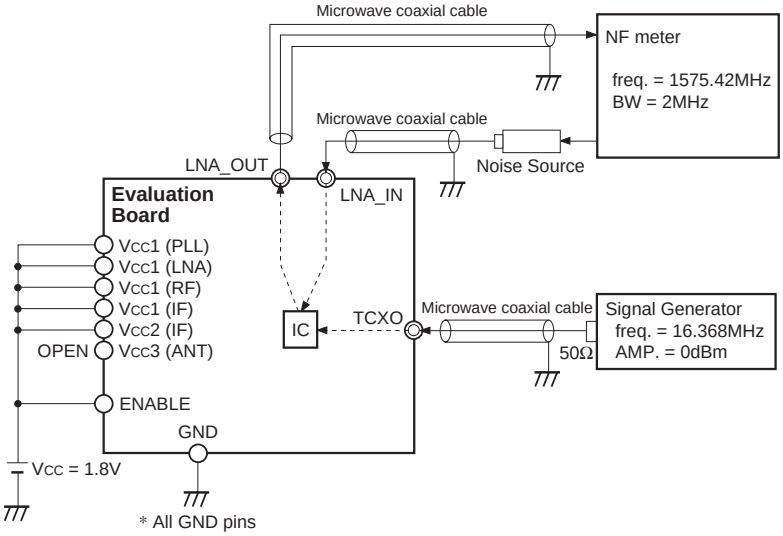
Output: LNA_OUT

* Compensate for the evaluation board and coaxial cable loss, and measure the NF value at the IC end.

[Sony recommended measuring instruments]

Noise source: Agilent 346A

NF meter: Agilent N8973A



3) Total NF

Input: LNA_IN

Output: TESTOUTP (Pin 38), TESTOUTN (Pin 39) ··· [Pins 38 and 39 are differential output.]

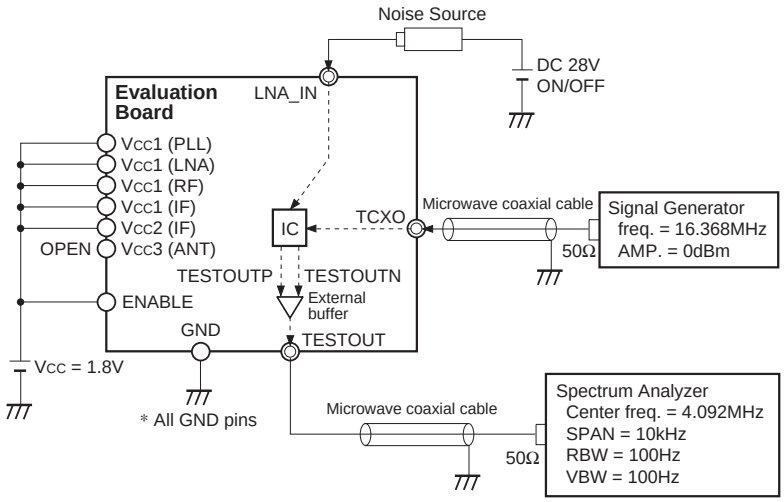
Serial data setting: Test output block "3" (IF filter output block) ··· See page 19.

Monitor method: (1) Perform differential – single conversion using an external buffer circuit and measure the output level. ··· [Sony recommended method]

(2) Measure Pins 38 and 39 with a differential probe.

* Total NF: Calculate NF from the noise power ratio when the DC 28V applied to the noise source is switched on and off.

Use the 346A made by Agilent as the noise source for measurement.



NF calculation formula

$$Y = \frac{N_{ON}}{N_{OFF}}$$

$$NF = 10 \log \left(\frac{ENR}{Y - 1} \right)$$

N_{ON}: Noise power when the DC 28V is on.

N_{OFF}: Noise power when the DC 28V is off.

ENR: Excess Noise Ratio

4) P-1dB Input

Input: LNA_IN

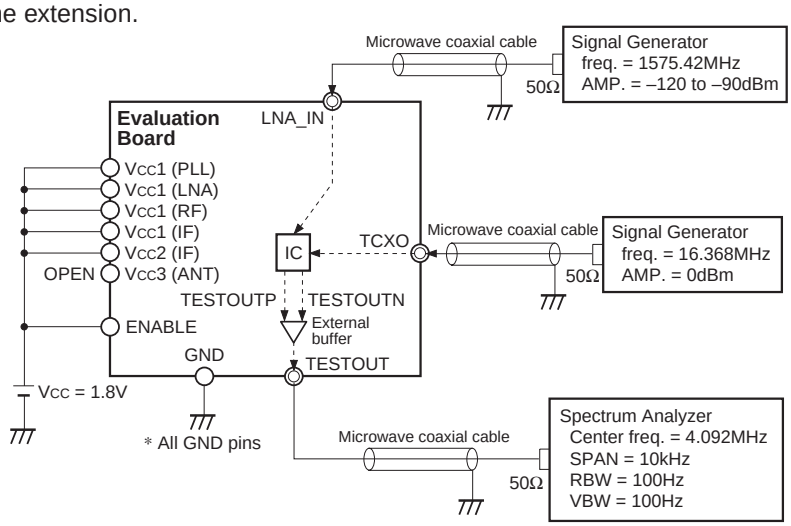
Output: TESTOUTP (Pin 38), TESTOUTN (Pin 39) ··· [Pins 38 and 39 are differential output.]

Serial data setting: Test output block "4" (IF AMP2 output block) ··· See page 19.

Monitor method: (1) Perform differential – single conversion using an external buffer circuit and measure the output level. ··· [Sony recommended method]

(2) Measure Pins 38 and 39 with a differential probe.

* P-1dB Input: Input level [dBm] at the point when the response drops by 1dB from the desired signal straight line extension.



5) Image Rejection Ratio

Input: LNA_IN

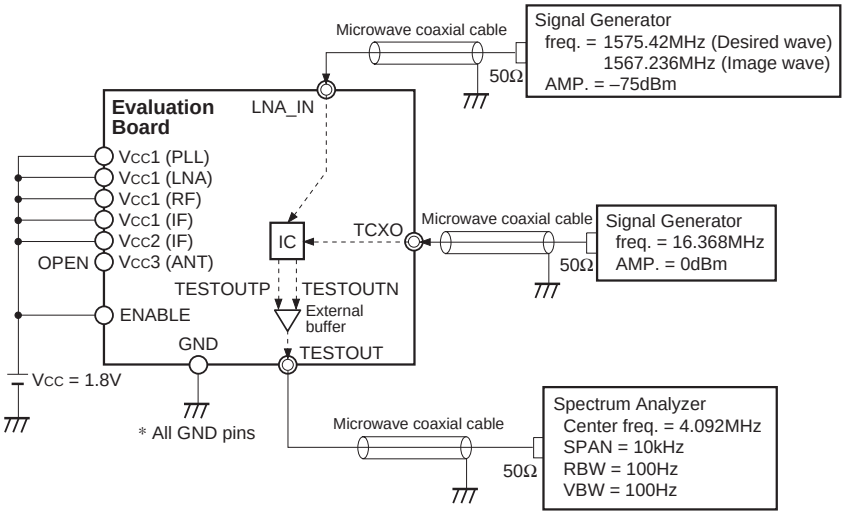
Output: TESTOUTP (Pin 38), TESTOUTN (Pin 39) ··· [Pins 38 and 39 are differential output.]

Serial data setting: Test output block "2" (Adder output block) ··· See page 19.

Monitor method: (1) Perform differential – single conversion using an external buffer circuit and measure the output level. ··· [Sony recommended method]

(2) Measure Pins 38 and 39 with a differential probe.

* IMRR (detuning frequency ≈ 4MHz): Image wave output level (at 1575.42MHz input) [dBm] – Desired wave output level (at 1567.236MHz input) [dBm]



6) Filter Response

Input: LNA_IN

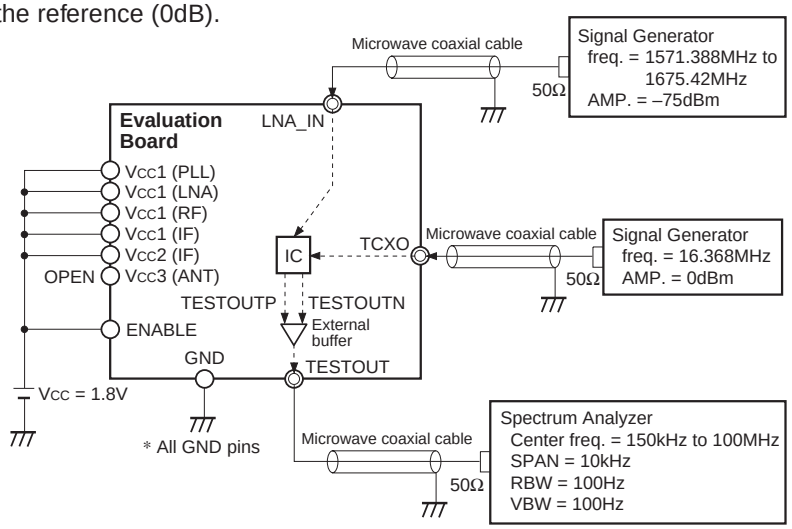
Output: TESTOUTP (Pin 38), TESTOUTN (Pin 39) ··· [Pins 38 and 39 are differential output.]

Serial data setting: Test output block "3" (IF filter output block) ··· See page 19.

Monitor method: (1) Perform differential – single conversion using an external buffer circuit and measure the output level. ··· [Sony recommended method]

(2) Measure Pins 38 and 39 with a differential probe.

* Filter Response: Vary the input frequency to LNA_IN and measure the output level. Normalize fo (4fo) to the reference (0dB).



7) C/N

Input: LNA_IN

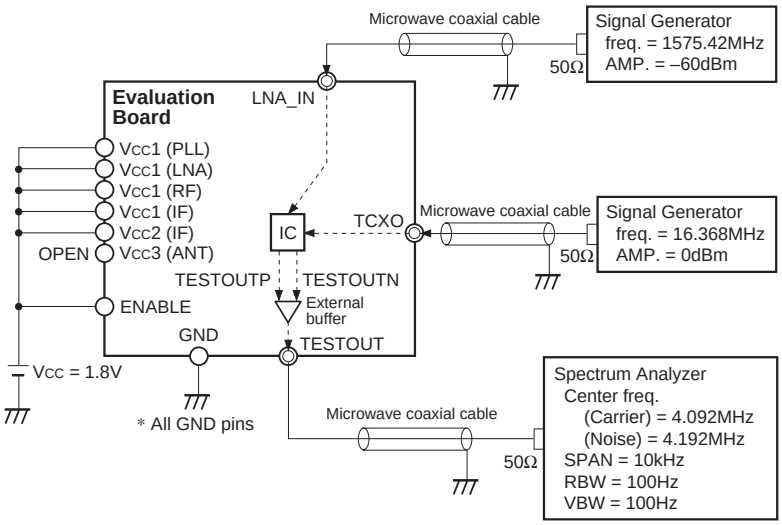
Output: TESTOUTP (Pin 38), TESTOUTN (Pin 39) ··· [Pins 38 and 39 are differential output.]

Serial data setting: Test output block "1I" (Ich mixer output block) ··· See page 19.

Monitor method: (1) Perform differential – single conversion using an external buffer circuit and measure the output level. ··· [Sony recommended method]

(2) Measure Pins 38 and 39 with a differential probe.

* C/N: Carrier + 100kHz noise level – Carrier level [dBc/Hz]



8) Spurious

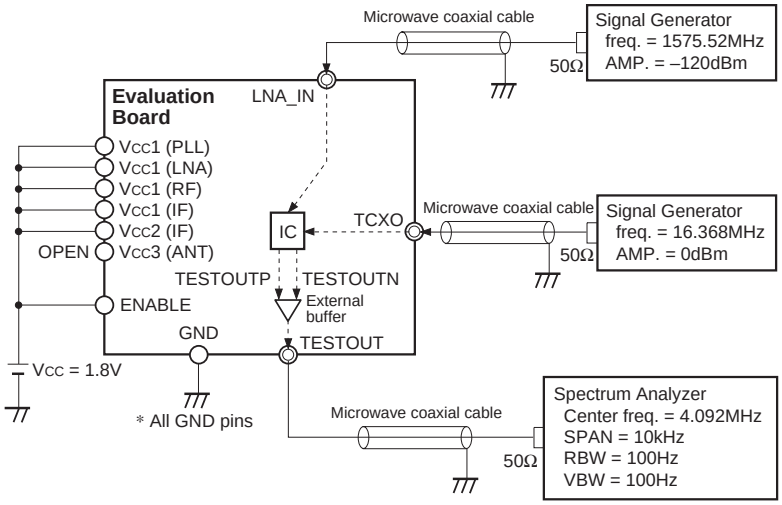
Input: LNA_IN

Output: TESTOUTP (Pin 38), TESTOUTN (Pin 39) ··· [Pins 38 and 39 are differential output.]

Serial data setting: Test output block "4" (IF AMP2 output block) ··· See page 19.

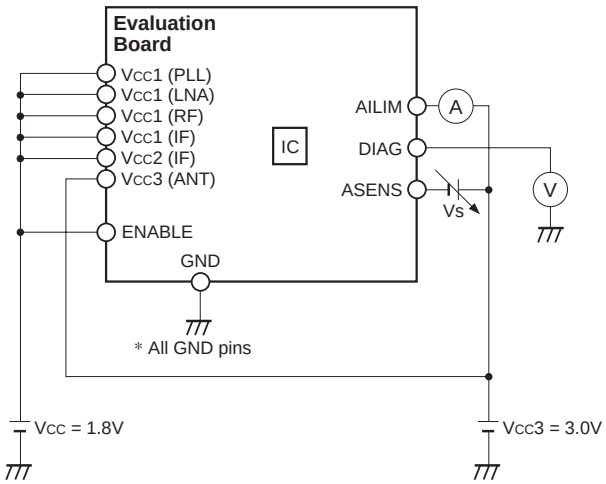
Measure the spurious components separated by a certain frequency from the carrier.

* Spurious: Each spurious output level – Carrier level [dBc]



9) Antenna Sense

- Vary Vs and measure the DIAG pin voltage.
- Vary Vs and measure the inflow current Ib to AILIM.

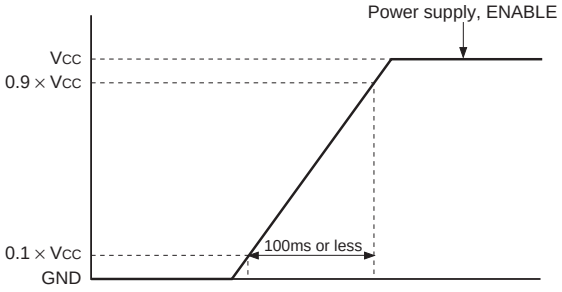


Initial Settings

The CXA3355ER is initialized by setting the ENABLE signal (Pin 43) from low level to high level.
The timing, etc. should satisfy the conditions below.
In addition, the TCXO frequency and IF frequency combinations in the table below can be obtained by setting Pin 10 (DATA), Pin 11 (CLK) and Pin 12 (LT) as shown in the table and then performing initialization. This eliminates the need for serial data setting.

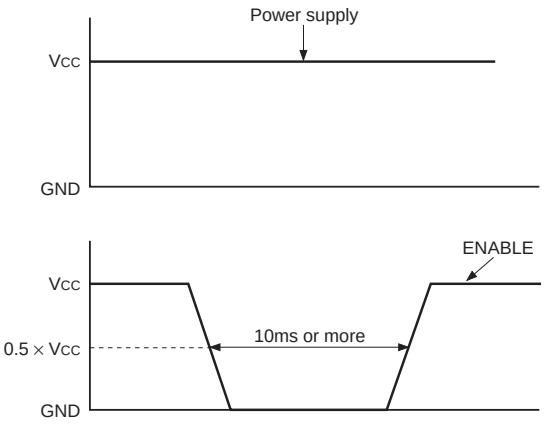
Pin 10 (DATA)	Pin 11 (CLK)	Pin 12 (LT)	TCXO frequency [MHz]	IF frequency [MHz]
GND	GND	GND	16.368	4.092
Vcc2	GND	GND	18.414	1.023
Vcc2	Vcc2	GND	13	0.976

1. During Power-on



The CXA3355ER is initialized by simultaneously raising the power supplies and the ENABLE signal (Pin 43) during power-on. The power supply and ENABLE signal (Pin 43) rise time should be 100ms or less.
In addition, the power supplies (Vcc1, Vcc2) should rise simultaneously. The antenna sense circuit power supply (Vcc3) should be left open except when using the antenna sense function.

2. Initialization After Power-on



After power-on, the CXA3355ER is initialized by setting the ENABLE signal (Pin 43) to low level for 10ms or more and then setting it to high level.

Serial Data Settings

The CXA3355ER can make the PLL counter settings, perform TCXO_CLK output, select the internal IF filter, and use the test I/O circuit according to the serial data settings (3-wire bus control). The transfer bit length is 18 bits, and there are four addresses. The address is set by the A1 and A0 bits. The timing, etc. should satisfy the conditions below.

Serial Data Format

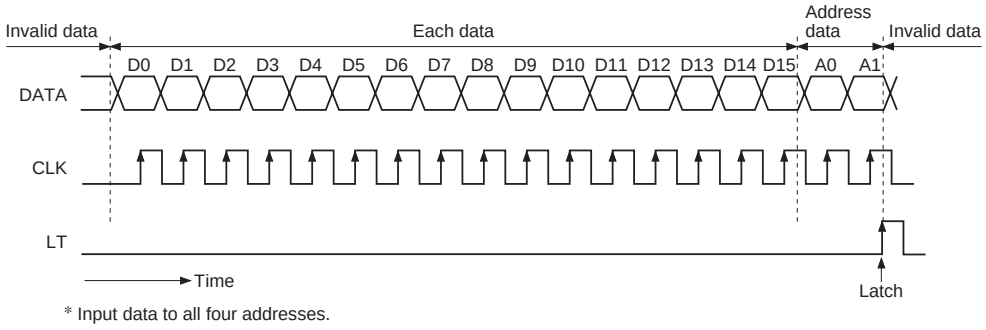
MSB LSB

A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0	0	0	0	CLK	0
0	1	SC4	SC3	SC2	SC1	SC0	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	0	TCL
1	0	TI2	TI1	TI0	TO2	TO1	TO0	0	0	0	0	0	0	0	0	FIL	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MC (0 to 10): Main counter frequency division value setting
SC (0 to 4): Swallow counter frequency division value setting
RC (0 to 8): Reference counter
CLK: TCXO CLK output (0: Not output, 1: Output)
FIL: Internal filter selection (0: fo mode LPF, 1: 4fo mode BPF)
TCL: IF block test I/O control (0: When not using the test I/O circuit, 1: When using the test I/O circuit)
TI (0 to 2): IF block test input location setting
TO (0 to 2): IF block test output location setting

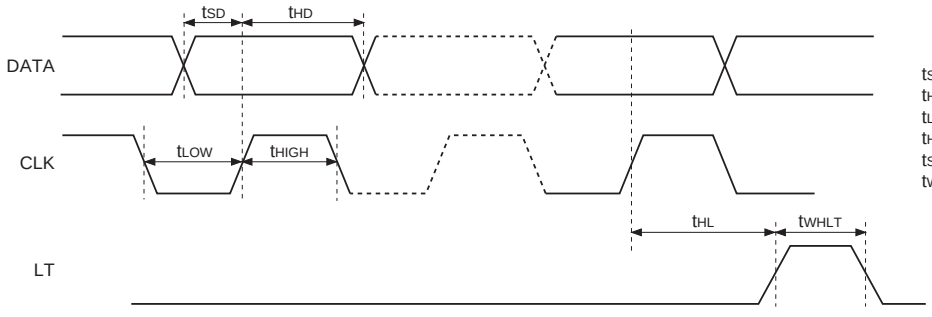
0: Logic input voltage low level
1: Logic input voltage high level

18-bit Data Format



* Input data to all four addresses.

Serial Data Interface Bus Timing (3-wire Bus Control)



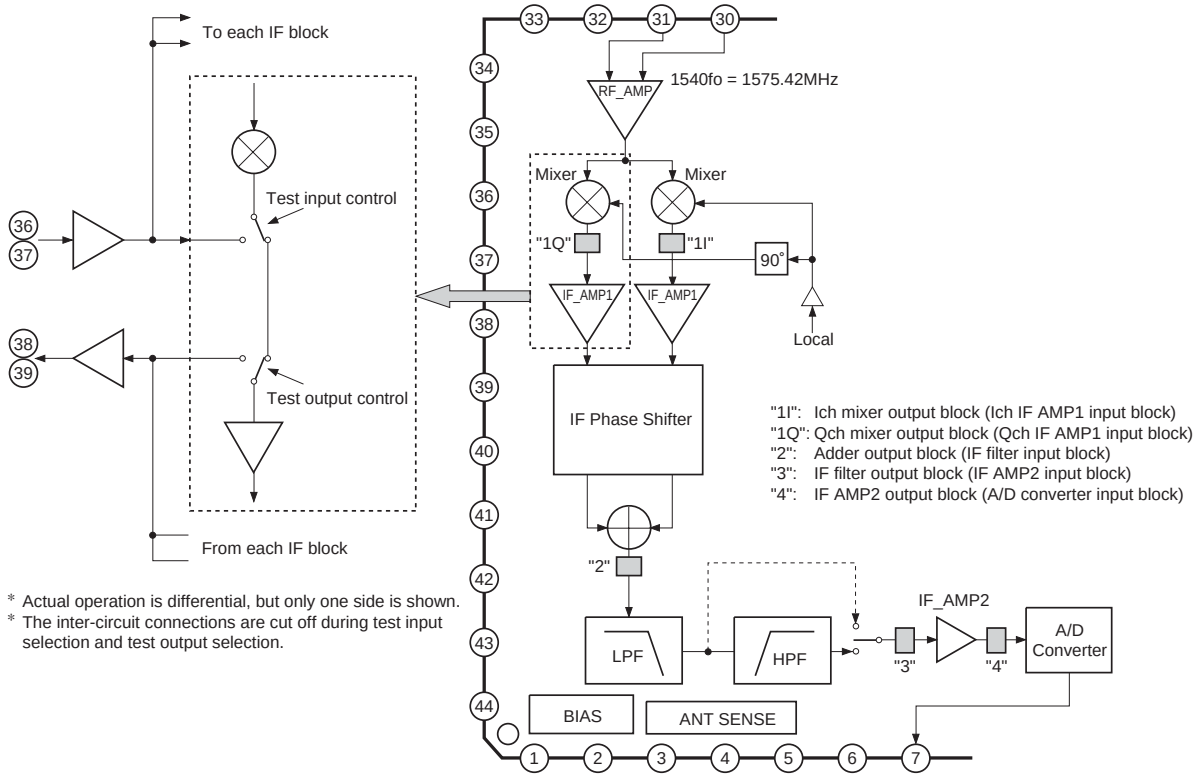
tSD = Data setup time
tHD = Data hold time
tLOW = Low period of CLK
tHIGH = High period of CLK
tSL = LT setup time
tWHLT = High pulse width (LT)

tWHLT ≥ 100ns
tSD, tHD, tLOW, tHIGH, tHL, tWHLT ≥ 50ns

Description of Functions

1. Test Circuit

The CXA3355ER has a test circuit for test signal I/O. The test circuit is connected between each IF block, and test I/O control can be performed by the serial data settings. The test circuit location, configuration and the serial data settings are as follows.



Test Circuit Location and Configuration

Serial Data Settings for Test Input Selection

TI2	TI1	TI0	Test input block
0	0	0	Normal operation
0	0	1	Ich IF AMP1 input block
0	1	0	Qch IF AMP1 input block
0	1	1	Not used.
1	0	0	Not used.
1	0	1	IF filter input block
1	1	0	IF AMP2 input block
1	1	1	A/D converter input block

Serial Data Settings for Test Output Selection

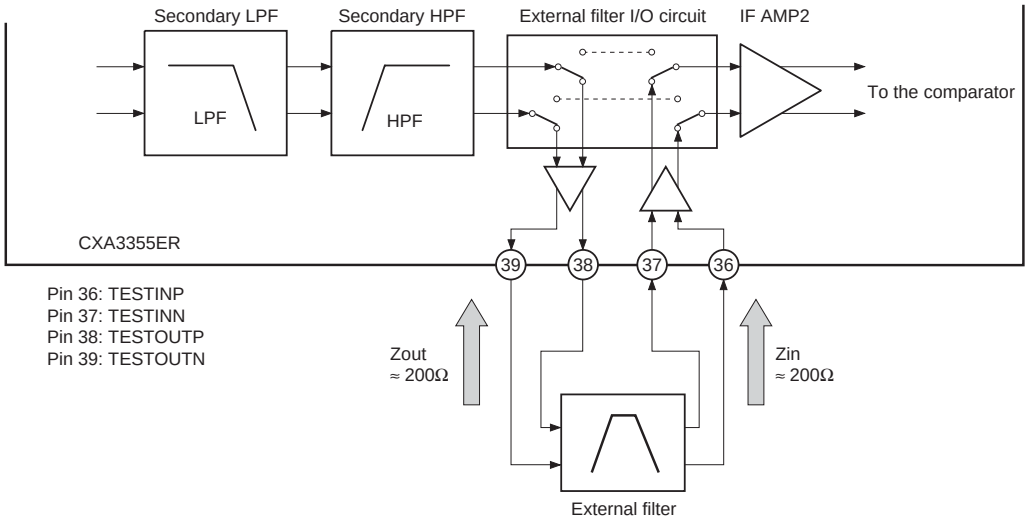
TO2	TO1	TO0	Test output block
0	0	0	Normal operation
0	0	1	Ich mixer output block
0	1	0	Qch mixer output block
0	1	1	Not used.
1	0	0	Not used.
1	0	1	Adder output block
1	1	0	IF filter output block
1	1	1	IF AMP2 output block

0: Logic input voltage low level
1: Logic input voltage high level

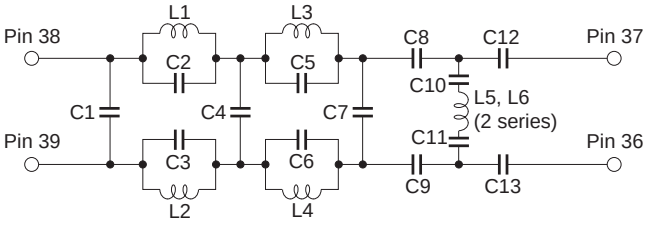
* Set the TCL register to "1" when using or to "0" when not using the test input circuit or the test output circuit. (See page 18.)

2. Using an External Filter

When using the CXA3355ER in 4fo mode with the initial settings (see page 17) which do not require serial data setting, input and output are performed via the test circuit located between the internal IF filter and the IF AMP2 in the following stage, so an external filter is necessary.
The external filter uses Pins 36 to 39. Differential I/O is performed with Pin 38 (TESTOUTP) and Pin 39 (TESTOUTN) as the internal IF filter output pins and Pin 36 (TESTINP) and Pin 37 (TESTINN) as the input pins to IF AMP2. Also, the impedance is 200Ω (differential) for both input and output.
Note that the bias voltage is determined inside the IC, so Pins 36 and 37 should not be connected directly with Pins 38 and 39. When not using an external filter, eliminate the DC components using an approximately 10nF capacitor.
The overall external filter block and the external filter configuration are shown below.



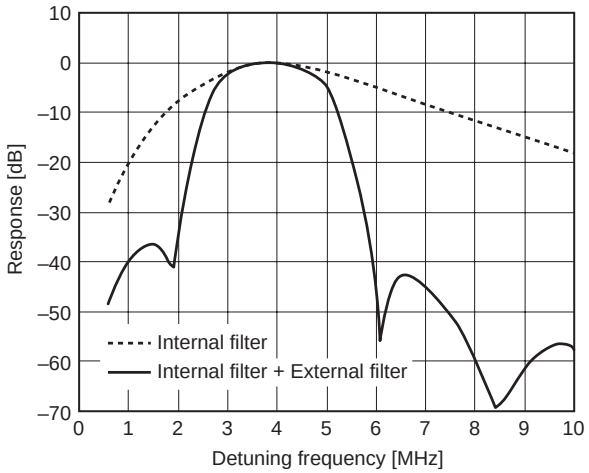
Overall External Filter Block



Chip C	[pF]
C1	91
C2, C3	300
C4	240
C5, C6	91
C7	130
C8, C9, C12, C13	680
C10, C11	1500

Chip L	[µH]
L1, L2	2.2
L3, L4	3.9
L5, L6	4.7

CXA3355ER IF Filter Response
(Example of representative characteristics)
Normalized at 4MHz



External Filter Configuration

Description of Operation

Overview of Operation

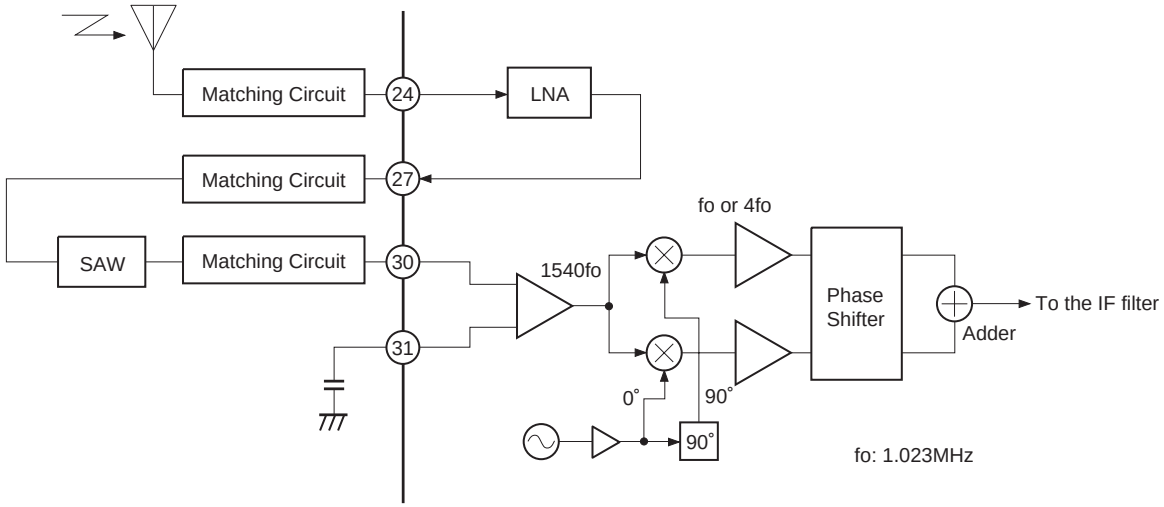
This IC down-converts the GPS (Global Positioning System) frequency of 1.57542GHz to fo (fo: 1.023MHz) or 4fo (4fo: 4.092MHz).
The internal configuration is divided into the analog block, consisting of the amplifier, mixer and filters, and the digital block (including the comparator block and the control block), which forms the PLL.
The analog block converts the frequency and amplifies the signal with the amplifier and the mixer, and eliminates undesired components with the filters.
The digital block can switch the PLL frequency division ratio in order to down convert the output signal to fo or 4fo.

1. LNA

The GPS signal that passes through the antenna is input to Pin 24 via a matching circuit as shown in the figure below.
The input signal is amplified by the LNA, and then output from Pin 27.
Always use matching circuits for the LNA input pin (Pin 24) and the LNA output pin (Pin 27), and match at 1.57542GHz.

2. RF Amplifier, RF Mixer, IF Phase Shifter and Adder

The signal amplified by the LNA passes through the SAW filter, and is then input to Pin 30 via a matching circuit.
The input signal is amplified by the RF amplifier, and then down-converted by the RF mixer to the fo (1.023MHz) or 4fo (4.092MHz) I and Q components. The IF signal down-converted to the I and Q components has the image component eliminated by the phase shifter and the adder, and is then input to the IF filter.
Always use a matching circuit for the RF amplifier input pin (Pin 30), and match at 1.57542GHz.



3. IF Filter

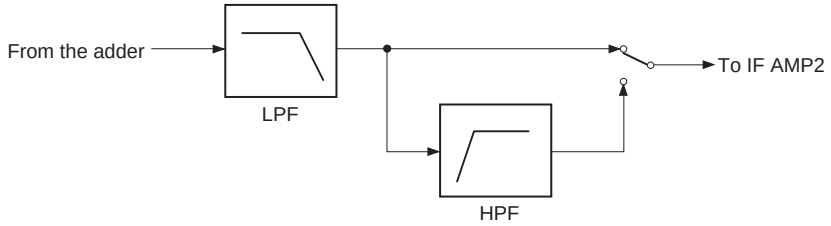
The IF signal that passed through the adder has the undesired components outside the band eliminated by the IF filter.

In fo mode the signal passes through only the LPF and is input to IF AMP2. In 4fo mode the signal passes through the LPF and then the HPF and is input to IF AMP2.

Note that fo mode and 4fo mode can be switched by the serial data setting.

Set the serial data setting register FIL to "0" for fo mode (LPF) or to "1" for 4fo mode (BPF).

In addition, an external filter can also be connected to this IC using Pins 36 to 39. (See page 20.)



4. IF AMP2 and A/D Converter

The signal that passed through the IF filter is amplified by IF AMP2, converted to a binary signal by the A/D converter, and then output from the DATA output pin (Pin 7). The A/D converter performs sampling at the TCXO CLK.

In addition, the A/D converter output voltage high level is $V_{CC}2$ (1.6 to 3.3V), so a wide range of interfaces can be supported.

5. TCXO (Pin 14)

Input the signal from the external oscillator to Pin 14 via a capacitor as the reference signal. Input frequencies from 10MHz to 26MHz are supported. The input signal level from the external oscillator should be 1.2Vp-p or less (0.6Vp-p typ., 0.2Vp-p min.). This is also the same in power save mode. However, using the typical level of 0.6Vp-p is recommended from the viewpoint of reducing harmful waves to the receive block, etc.

6. TCXO CLK Output (Pin 13)

This IC can output TCXO CLK from Pin 13 according to the serial data setting. The output voltage high level is $V_{CC}2$ (1.6 to 3.3V), so a wide range of interfaces can be supported.

Set the serial data setting register CLK to "0" when not using TCXO CLK, or to "1" when using TCXO CLK. (See page 18.)

7. PLL/VCO

The PLL is comprised by a VCO, frequency divider and phase/frequency comparator as shown in the figure below, and incorporates an inductor, varactor and all other necessary components. The loop filter is externally connected. Use components that satisfy the required characteristics.

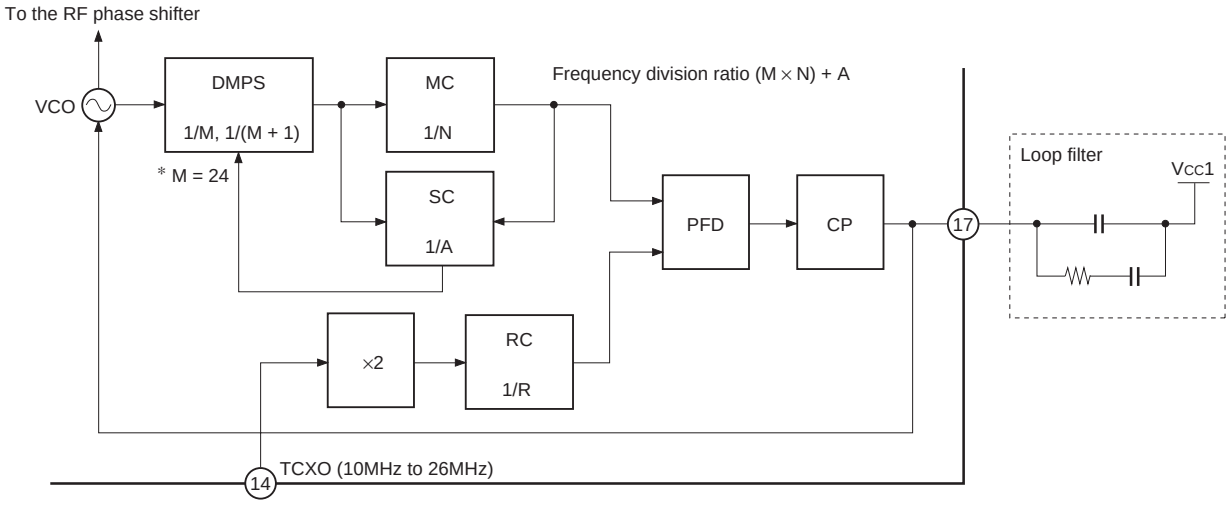
Serial data setting is unnecessary when this IC is used with the typical TCXO and IF combinations set by the initial settings shown in page 17.

When making serial data settings, set counter frequency division values that satisfy the following equations.

- $f_{VCO} = (M \times N + A) \times (f_{TCXO} \times 2) \div R$
- $(f_{TCXO} \times 2) \div R > 800kHz$
- $N \geq 3$, $R \geq 3$

f_{VCO}: VCO oscillation frequency, f_{TCXO}: TCXO frequency

MC data = N, SC data = A, RC data = R, DMPS data = M = 24 (fixed)



8. ENABLE (Pin 43)

Active mode and power save mode can be switched according to the level.

- High (V_IH: 1.2V min.): Active mode
- Low (V_IL: 0.2V max.): Power save mode

9. Antenna Sense

The power supply lines are separated internally, so antenna sense operation at the supply voltage ($V_{CC}3$) of 3.0 ± 0.3V is recommended. Note that the antenna sense function does not operate independently, so voltage should also be applied to the other power supply pins ($V_{CC}1$, $V_{CC}2$) for use in active mode. In addition, leave the power supply pin ($V_{CC}3$) open when not using the antenna sense function.

The antenna sense function checks whether an antenna is connected. Pin 2 (DIAG) outputs high voltage when an antenna is not connected, or low voltage when an antenna is connected. A current limiting circuit is provided as a countermeasure against short circuits.

The DIAG pin voltage switching point is as shown in the table below.

V1, V2, V3 and Ib in the table below are as follows.

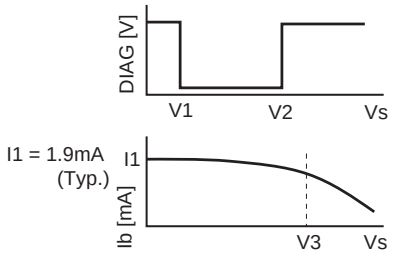
V1: 10 to 60mV → Threshold voltage at which connection of the prescribed load is detected from the open status

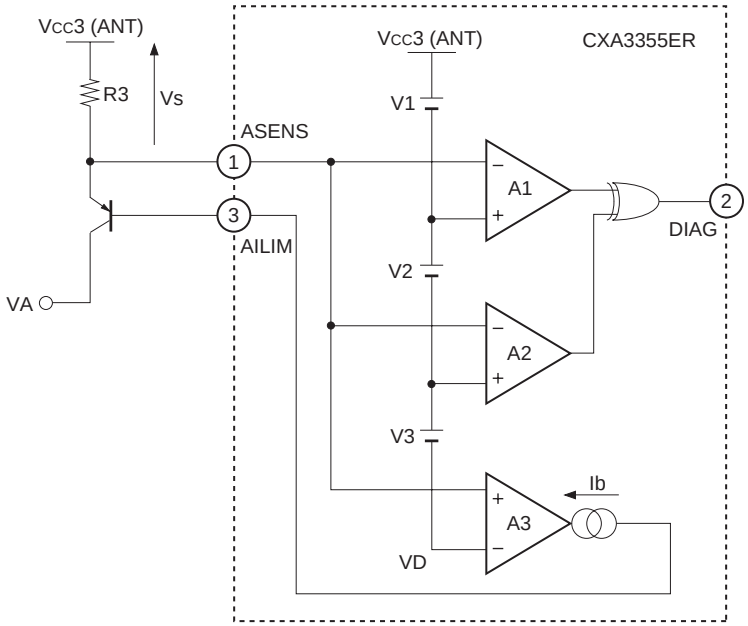
V2: 140 to 200mV → Threshold voltage for switching to the short status from the prescribed load connected status.

V3: 250mV → Current limiting threshold voltage.

Ib: 1.7 to 2.1mA → Base current in the normal connection status.

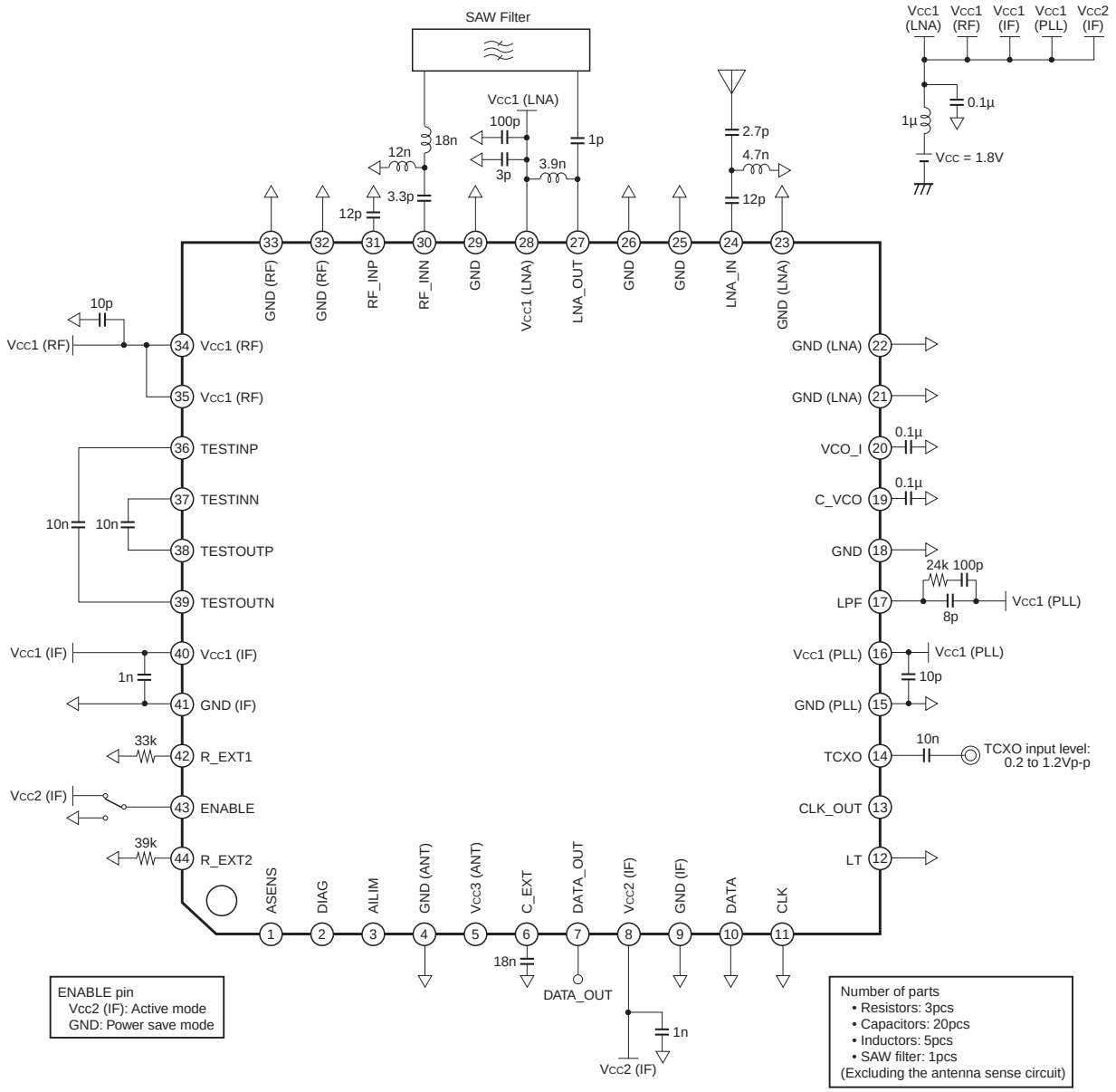
MODE	Connection status	DIAG voltage
Vs < V1	Open	High
V1 < Vs < V2	Normal connection	Low
V2 < Vs	Short	High





Antenna Sense Block Circuit

Application Circuit

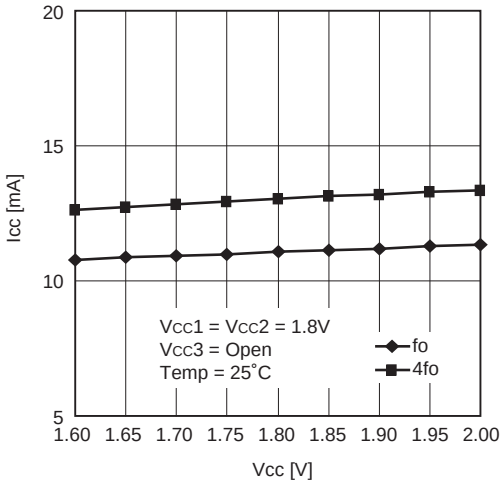


* This diagram shows the application circuit when the initial settings are made for 4fo mode. (See page 17.)
* The RF block bypass capacitors should have excellent high frequency characteristics.
* Use parts with a tolerance of ±1% for the following resistor elements. Other parts should have a tolerance of ±5%.
  - Pin 17 (LPF)
  - Pin 42 (R_EXT1)
  - Pin 44 (R_EXT2)

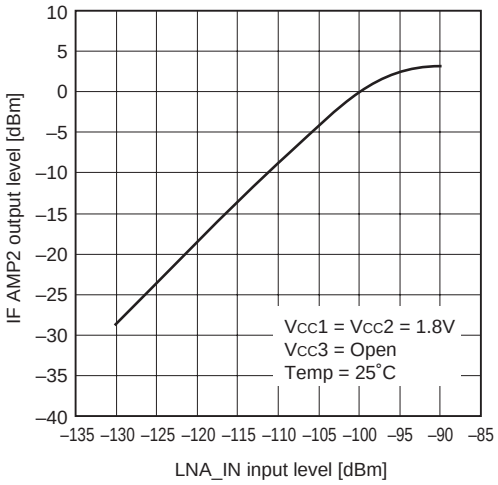
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Supplement Materials (Example of representative characteristics)

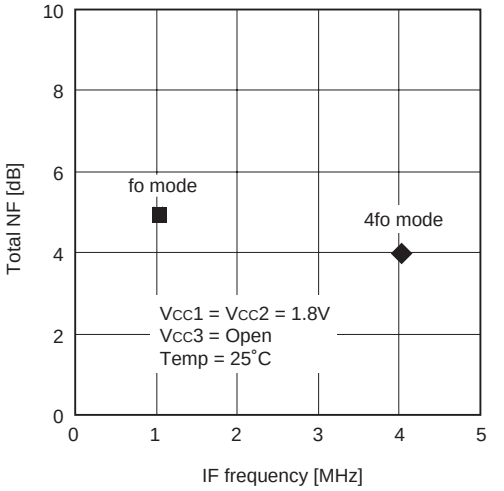
Graph 1. Icc



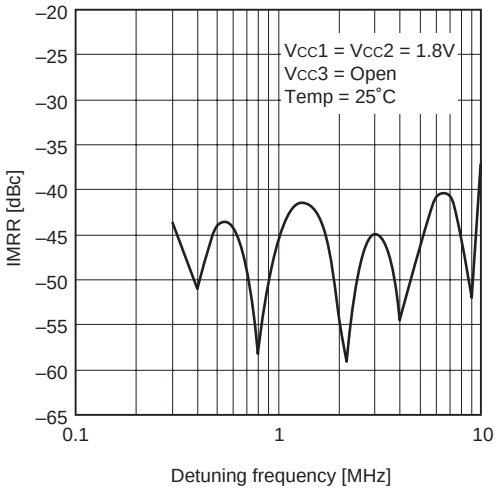
Graph 2. Total Gain



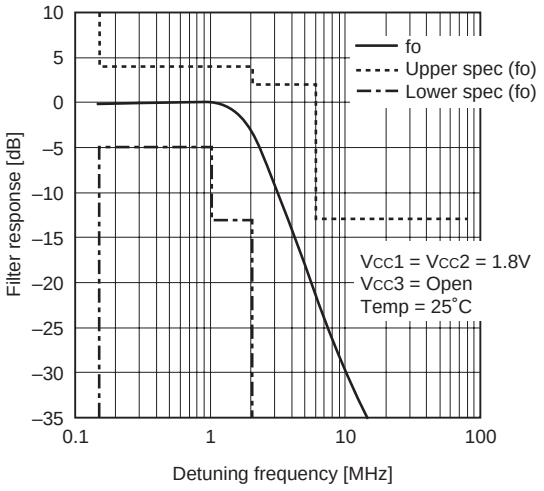
Graph 3. Total NF



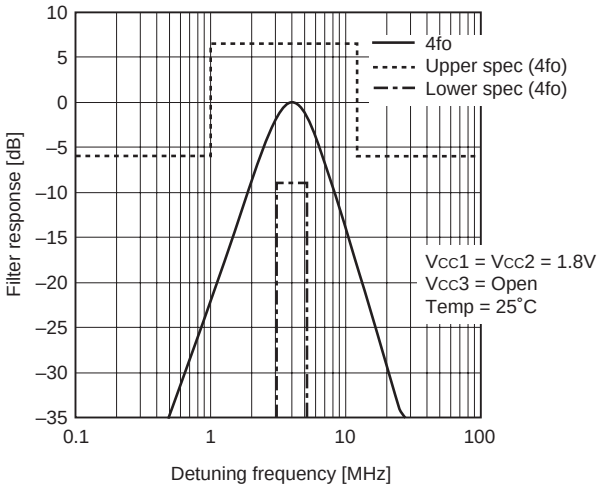
Graph 4. Image Rejection Ratio



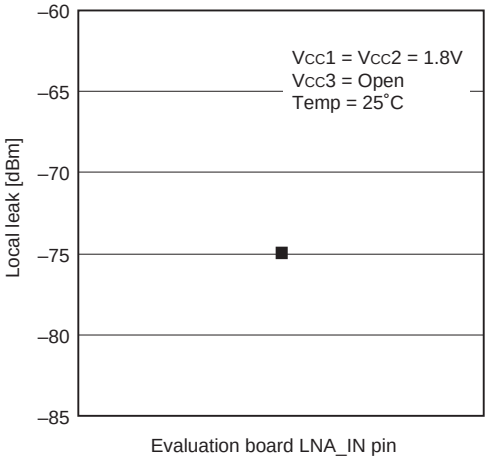
Graph 5. Filter Response (Normalized at 1.023MHz)



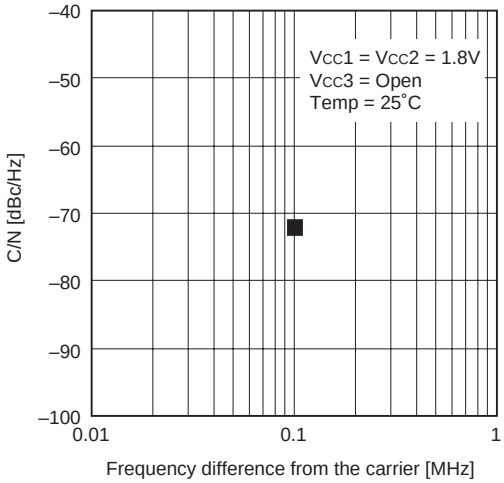
Graph 6. Filter Response (Normalized at 4.092MHz)



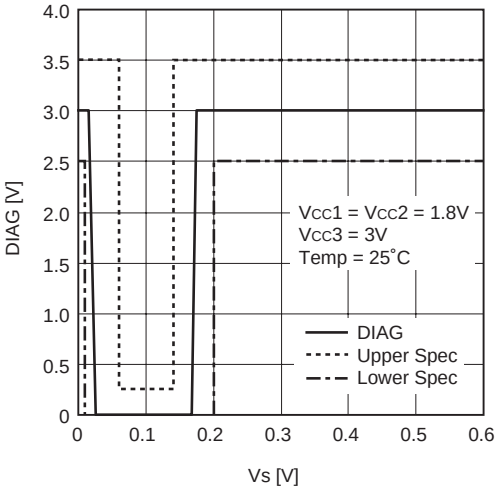
Graph 7. Local Leak



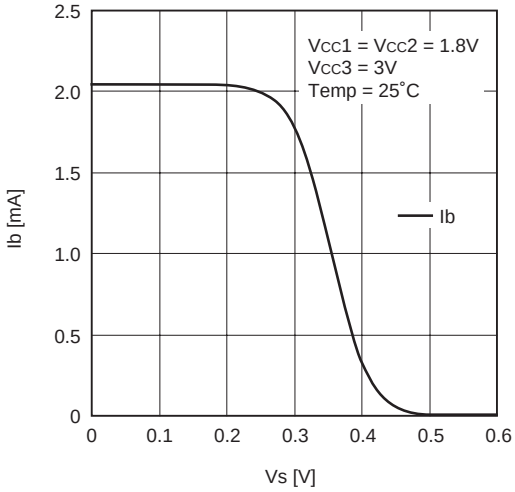
Graph 8. C/N



Graph 9a. Antenna Sense (Vs vs. DIAG)

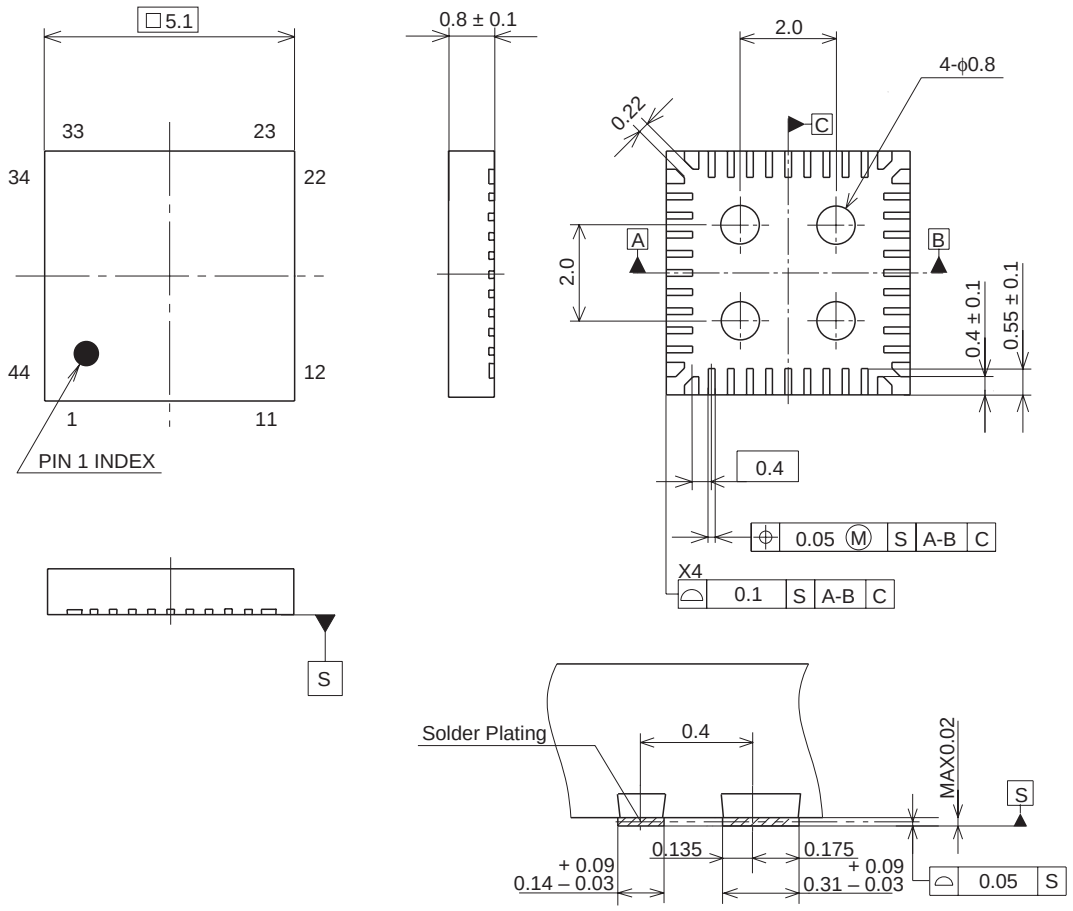


Graph 9b. Antenna Sense (Vs vs. Ib)



Package Outline Unit: mm

44PIN VQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.06g

SONY CODE	VQFN-44P-02
EIAJ CODE	————
JEDEC CODE	————

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm