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TC358743 Camera Serial Interface Converter Chipset (HDMI to MIPI®)

Highlights

- HDMI video and audio streams into MIPI® CSI-2 data to enable Application Processors with MIPI CSI-2 interface to process HDMI as input stream.
- Solutions are based on the latest versions of industry standards for HDMI 1.4 and MIPI CSI-2 1.01 interfaces.
- Support for common 3D formats and compatible protocols with the HDMI 1.4 standard
- Support for 1080P resolution at refresh rates of 60 fps.
- Applicable to products such as smart TVs, set-top boxes, and DVRs (digital video recorders)

Description

The Toshiba High Definition Multimedia Interface (HDMI) to Mobile Industry Processor Interface (MIPI®) Camera Serial Interface Type 2 (CSI-2) converter chipset, designated TC358743XBG, enables a Host processor with a MIPI CSI-2 interface to accept HDMI video and audio streams and process them as incoming data source. Application Processors can generate different types of video data for internal displays, external displays, as well as analog TV and HDMI TV; but some Application Processors have limitations in handling video data as an input source. A common input interface for video streams is MIPI CSI-2, which is a high-speed serial interface to an embedded camera. The Toshiba bridge, TC358743XBG, enables HDMI video stream to be processed by the Application Processor as a CSI-2 video stream. Audio is supported and can be transmitted over CSI-2 stream or over I2S.

The maximum resolution supported is 1080P at a refresh rate of 60 fps. The bridge supports common 3D video formats and protocols compatible with the HDMI 1.4 standard. The TC358743XBG supports a MIPI

CSI-2 interface to the Host with configurable 1, 2, 3, or 4 data lanes with lane speeds of up to 1 Gbps per lane.

The Toshiba TC358743XBG is a 64-pin device and is optimized for the portable market. It has a small package size of 6 mm x 6 mm, 0.65 mm ball pitch. It is designed with clock and power management circuitry to support lowpower states.

Features
HDMI-RX Interface
- HDMI 1.4
  - Video Formats Support (Up to 1080P)
    - RGB, YUV444: 24-bpp@60 fps
    - YUV422 24-bpp @60 fps
  - Audio Supports
    - Internal Audio PLL to track N/CTS value transmitted by the ACR packet
  - 3D support
  - Support for HDCP (High-bandwidth Digital Content Protection)
  - Support for DDC (Display Data Channel)

TC358743XBG Block Diagram: HDMI to CSI-2 Bridge Chip
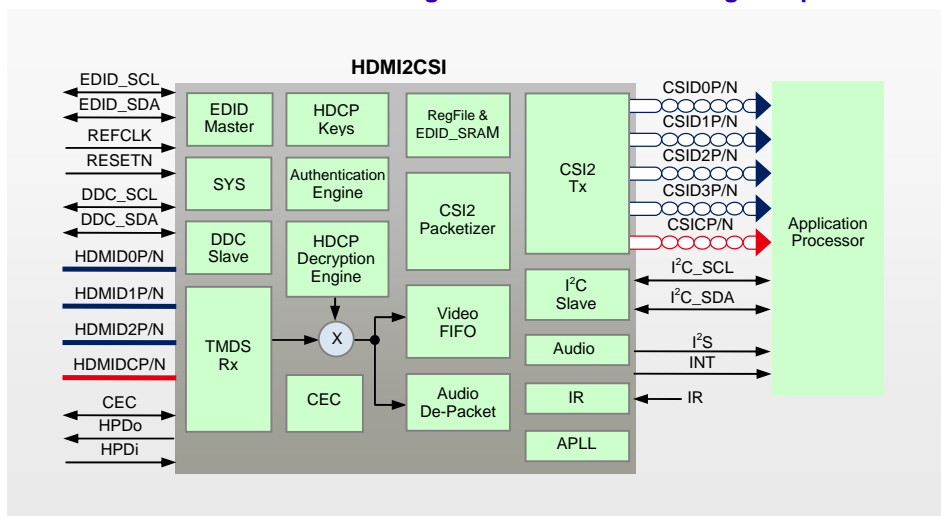
– Support for EDID (Extended Display Identification Data)
  • Release A, Revision 1 (Feb 9, 2000)
  • First 128 byte (EDID 1.3 structure)
  • First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
  • Embedded 1K-byte SRAM (EDID_SRAM)
– Maximum HDMI clock speed: 165 MHz
• Does not support Audio Return Path and HDMI Ethernet Channels

CSI-2 TX Interface
• MIPI CSI-2 compliant
  (Version 1.01 Revision 0.04 – 2 April 2009)
  – Supports up to 4 data lanes
• Supports up to 1 Gbps per data lane
  – Video, Audio and InfoFrame data can be transmitted

I²C Slave Interface
• Support for normal mode (100 KHz), fast mode (400 KHz), and ultra fast mode (2 MHz)
• Configure all H2C internal registers

Audio Output Interface
  Either I²S or TDM Audio interface available (pins are multiplexed)

I²S Audio Interface
• Single stereo channel
• Support Master Clock mode only
• Support 16, 18, 20 or 24-bit data (based on HDMI input stream)
• Support for left-justify or right-justify with MSB first

TDM (Time Division Multiplexed) Audio Interface
• Single data link
• Support Master Clock mode only
• Up to 2,4,6 or 8 channels (based on HDMI input stream)
• Support 16, 18, 20 or 24-bit PCM audio data word (based on HDMI input stream)

InfraRed (IR)
• Support NEC InfraRed protocol

Power Supply Inputs
• Core and MIPI D-PHY: 1.2V
• I/O: 1.8V – 3.3V
• HDMI: 3.3V
• APLL: 3.3V/2.5V

Package
• TC358743XBG: 64-pin, 6.0 x 6.0 mm,
  0.65 mm ball pitch, 1.2 mm height

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