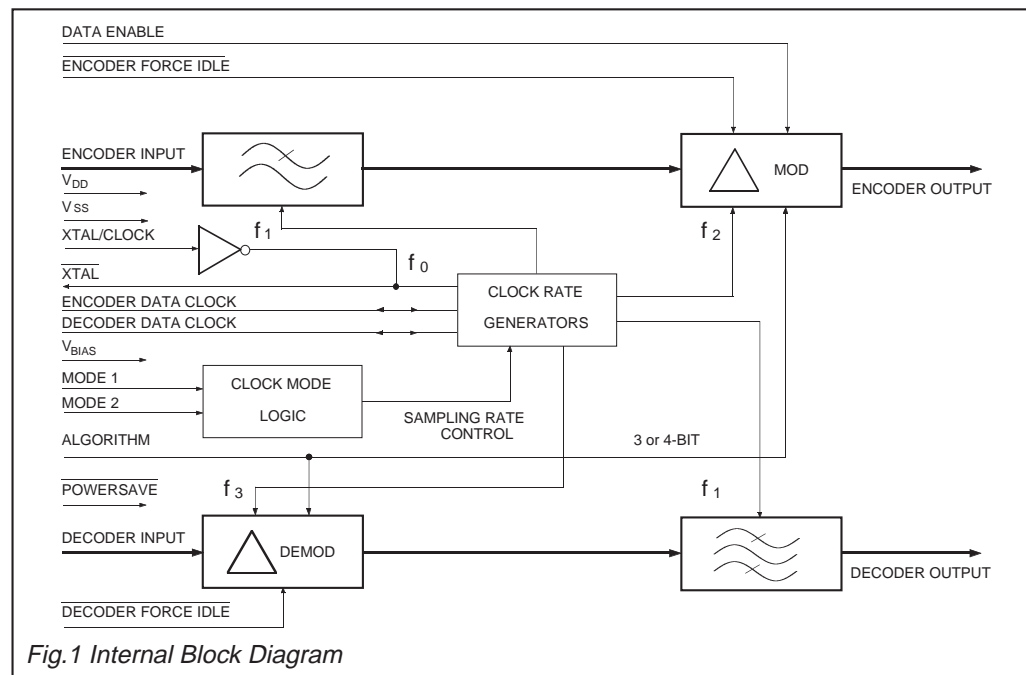




### Features/Applications

- Designed to Meet Mil-Std-188-113
- Military Communications
- Delta MUX, Switch and Phone Applications
- Single-Chip Full-Duplex Codec
- On-Chip Input and Output Filters
- Programmable Sampling Clocks
- 3 or 4-bit Compand Algorithm
- Forced Idle Facility
- Powersave Facility
- Single 5V CMOS Process
- Full-Duplex CVSD\* Codec



# FX629

### Brief Description

The FX629 is an LSI circuit designed as a \*Continuously Variable Slope Delta Codec and is intended for use in military communications systems.

Designed to meet Mil-Std-188-113 with external components, the device is suitable for applications in military Delta Multiplexers, switches and phones.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32 or 64 k bits/second from an internal clock generator or may be externally applied in the range 8 to 64 k bits/second. Sampling clock frequencies are output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications.

Encoder and Decoder forced idle facilities are provided, forcing a 10101010..... pattern in encode and a  $V_{DD}/2$  bias in decode.

The companding circuits may be operated with a pin-selected 3 or 4-bit algorithm.

The powersave facility puts the device into the standby mode thereby reducing current consumption when not operating.

A reference 1.024MHz oscillator uses an external clock pulse or Xtal input.

The FX629 is a low-power, 5 volt CMOS device and is available in 22-pin cerdip DIL package.

## Pin Number    Function

FX629J													
1	<b>Xtal/Clock</b> : Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 3.												
2	$\overline{\text{Xtal}}$ : Output of clock oscillator inverter. Xtal circuitry shown is in accordance with CML application note D/XT/1 April 1986.												
3	No connection												
4	<b>Encoder Data Clock</b> : A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependant upon clock mode 1, 2 inputs and Xtal frequency (see Clock Mode pins).												
5	<p><b>Encoder Output</b> : The encoder digital output, this is a three state output whose condition is set by Data Enable and Powersave inputs as shown :</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Data Enable</th> <th><math>\overline{\text{Powersave}}</math></th> <th>Encoder Output</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>Enabled</td> </tr> <tr> <td>0</td> <td>1</td> <td>High Z (o/c)</td> </tr> <tr> <td>1</td> <td>0</td> <td>V<sub>ss</sub></td> </tr> </tbody> </table>	Data Enable	$\overline{\text{Powersave}}$	Encoder Output	1	1	Enabled	0	1	High Z (o/c)	1	0	V <sub>ss</sub>
Data Enable	$\overline{\text{Powersave}}$	Encoder Output											
1	1	Enabled											
0	1	High Z (o/c)											
1	0	V <sub>ss</sub>											
6	<b>Encoder Force Idle</b> : When this pin is a logical '0' the encoder is forced to an idle state and the encoder digital output is 0101..., a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1M $\Omega$ Pullup.												
7	<b>Data Enable</b> : Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1M $\Omega$ Pullup.												
8	No connection												
9	<b>Bias</b> : Normally at V <sub>DD</sub> /2 bias, this pin requires to be externally decoupled by a capacitor, C <sub>4</sub> . Internally pulled to V <sub>SS</sub> when "Powersave" is a logical '0'.												
10	<b>Encoder Input</b> : The analogue signal input. Internally biased at V <sub>DD</sub> /2, external components are required on this input. The source impedance should be less than 100 $\Omega$ , output idle channel noise levels will improve with an even lower source impedance. See Fig. 3.												
11	V <sub>SS</sub> : Negative Supply.												

**Pin Number    Function**

FX629J																
12	No connection															
13	<b>Decoder Output</b> : The recovered analogue signal is output at this pin, it is the buffered output of a bandpass filter and requires external components. During "Powersave" this output is o/c.															
14	No connection															
15	<b>Powersave</b> : A logical '0' at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical '1' the codec operates normally. Internal 1MΩ Pullup.															
16	<b>Decoder Force Idle</b> : A logical '0' at this pin gates a 0101...pattern internally to the decoder so that the decoder output goes to $V_{DD}/2$ . When this pin is at a logical '1' the decoder operates as normal. Internal 1MΩ Pullup.															
17	<b>Decoder Input</b> : The received digital signal input. Internal 1MΩ Pullup.															
18	<b>Decoder Data Clock</b> : A Logic I/O port. External decode clock input or internal data clock output, dependant upon clock mode 1, 2 inputs, see Clock Mode pins.															
19	<b>Algorithm</b> : A logical '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1MΩ Pullup.															
20	<b>Clock Mode 2</b> :															
21	<table border="1"> <thead> <tr> <th>Clock Mode 1</th> <th>Clock Mode 2</th> <th>Facility</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>External clocks</td> </tr> <tr> <td>0</td> <td>1</td> <td>Internal, 64kb/s = <math>f \div 16</math></td> </tr> <tr> <td>1</td> <td>0</td> <td>Internal, 32kb/s = <math>f \div 32</math></td> </tr> <tr> <td>1</td> <td>1</td> <td>Internal, 16kb/s = <math>f \div 64</math></td> </tr> </tbody> </table>	Clock Mode 1	Clock Mode 2	Facility	0	0	External clocks	0	1	Internal, 64kb/s = $f \div 16$	1	0	Internal, 32kb/s = $f \div 32$	1	1	Internal, 16kb/s = $f \div 64$
Clock Mode 1	Clock Mode 2	Facility														
0	0	External clocks														
0	1	Internal, 64kb/s = $f \div 16$														
1	0	Internal, 32kb/s = $f \div 32$														
1	1	Internal, 16kb/s = $f \div 64$														
	<p>Clock rates refer to <math>f = 1.024</math> MHz Xtal/clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Optimum performance will be achieved when the applied external clocks are synchronous with the master Xtal/clock, and a sub-multiple of 128kHz.</p>															
22	<b>V<sub>DD</sub></b> : Positive Supply. A single + 5 volt power supply is required.															

# Codec Integration

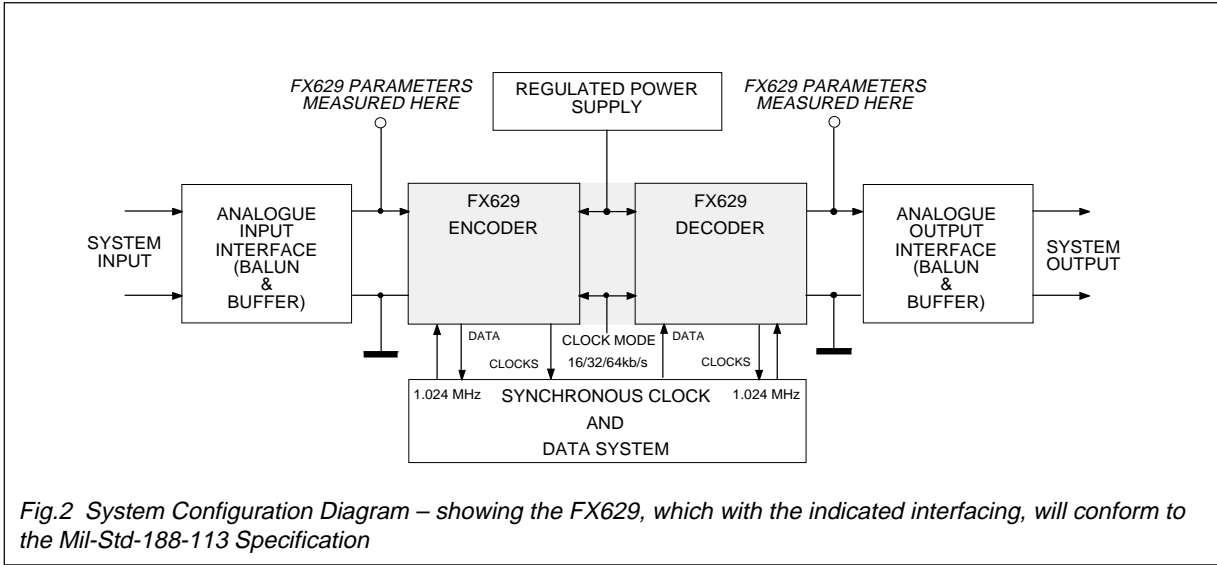


Fig.2 System Configuration Diagram – showing the FX629, which with the indicated interfacing, will conform to the Mil-Std-188-113 Specification

Component	Unit Value	Note – with reference to Figure 3 (below)
R <sub>1</sub>	1M	Oscillator Inverter bias resistor.
R <sub>2</sub>	Selectable	Xtal Drive limiting resistor.
C <sub>1</sub>	33p	Xtal Circuit drain capacitor.
C <sub>2</sub>	33p	Xtal Circuit gate capacitor.
C <sub>3</sub>	1.0μ	Encoder Input coupling capacitor – The drive source impedance to this input should be less than 100Ω. Output Idle channel noise levels will improve with an even lower source impedance.
C <sub>4</sub>	1.0μ	Bias decoupling capacitor.
C <sub>5</sub>	1.0μ	V <sub>DD</sub> decoupling capacitor.
X <sub>1</sub>	1.024 MHz	A 1.024 MHz Xtal/clock input will yield exactly 16/32/64 kb/s data clock rates. Xtal circuitry shown is in accordance with CML application note D/XT/1 April 1986.

Tolerance :- Resistors ± 10% Capacitors ± 20%

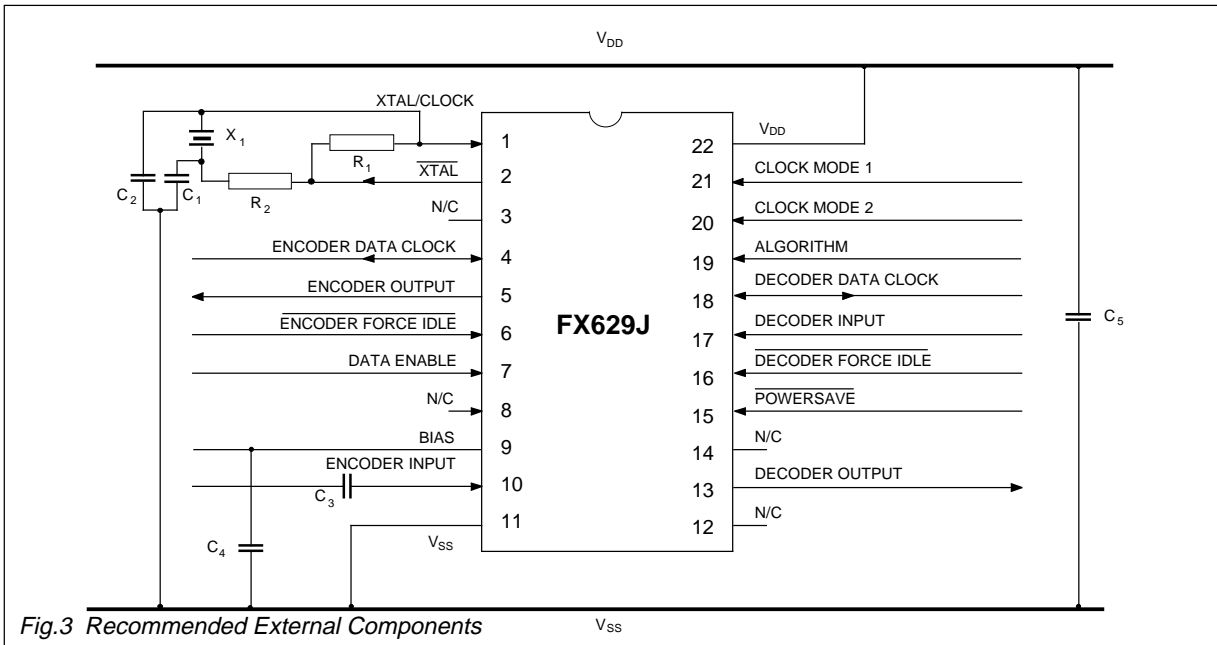
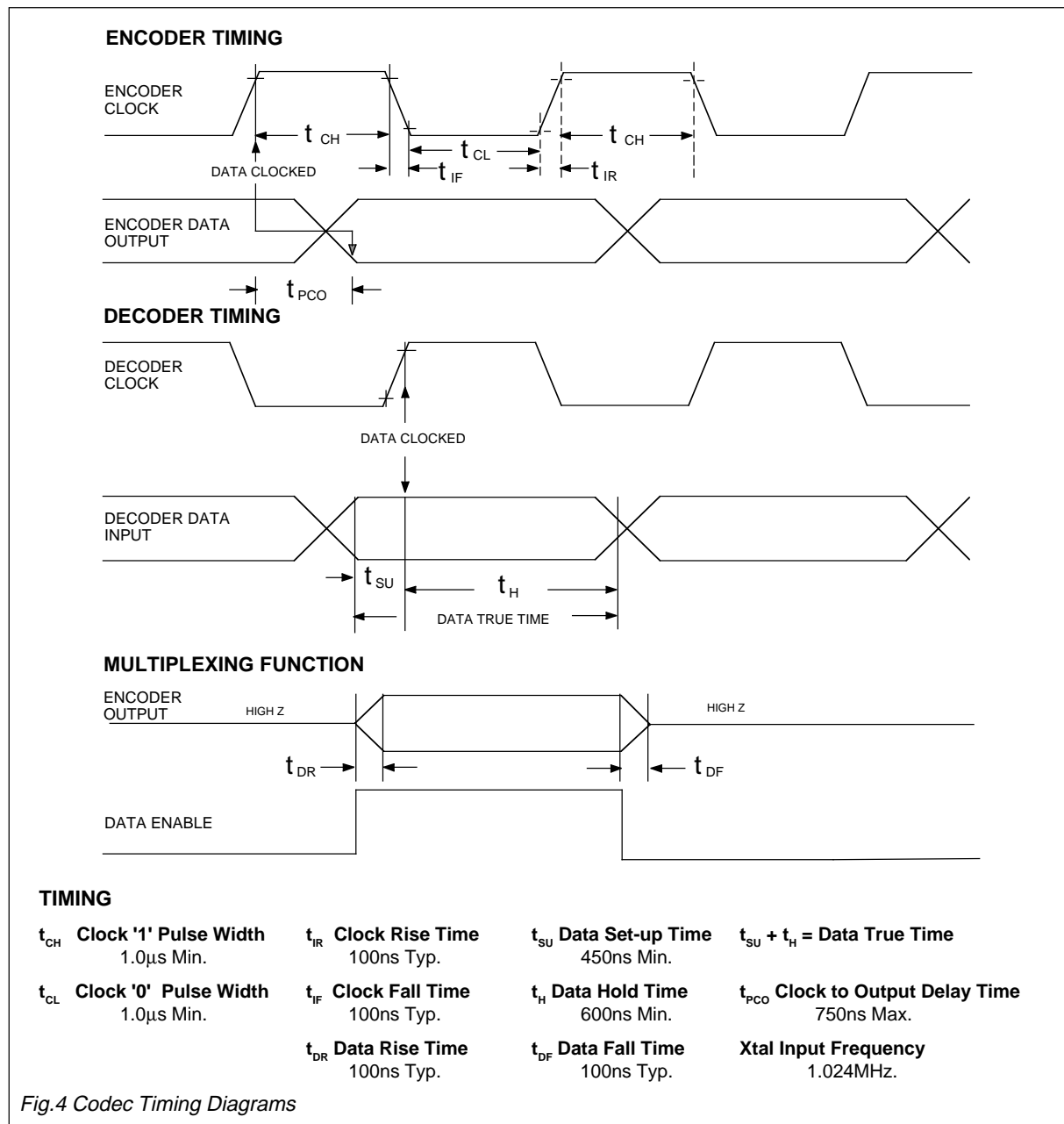


Fig.3 Recommended External Components

# Codec Timing Information



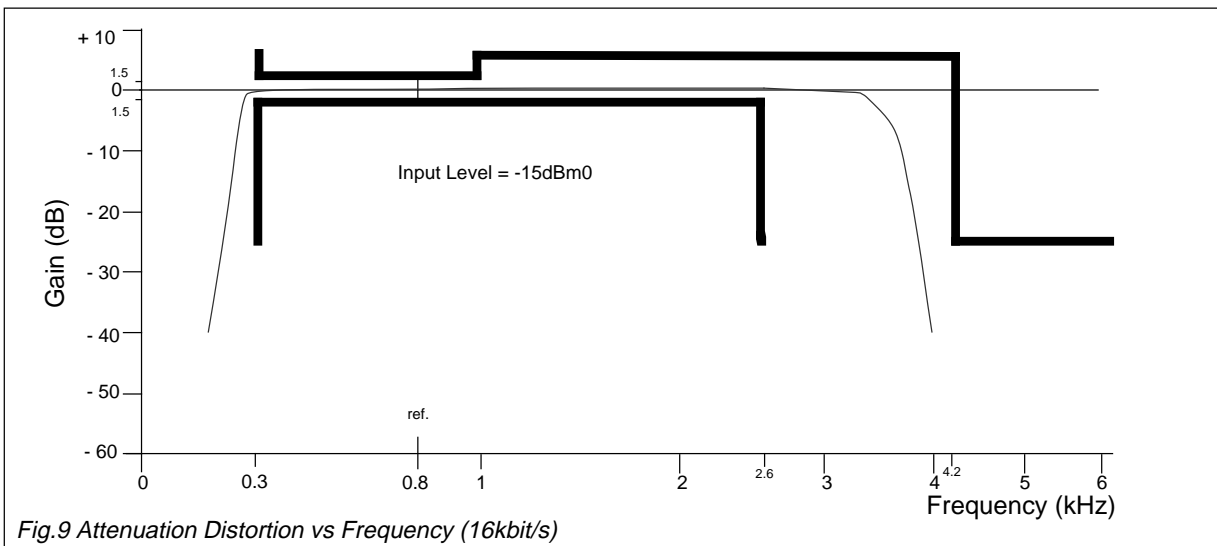
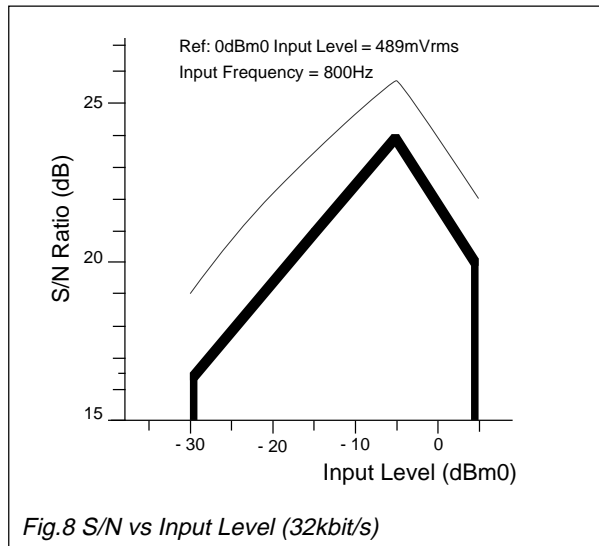
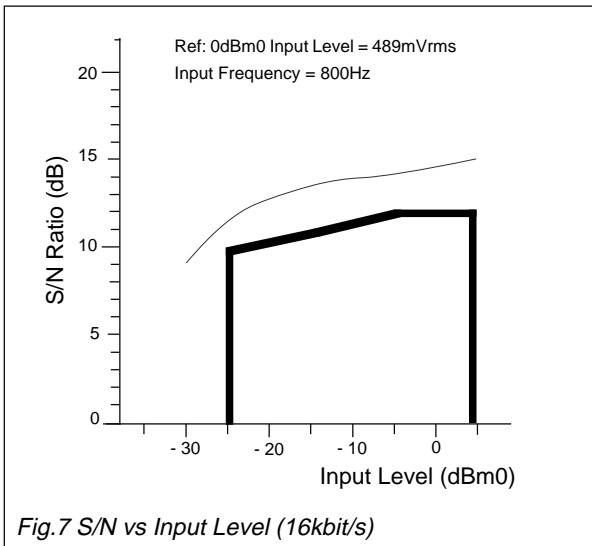
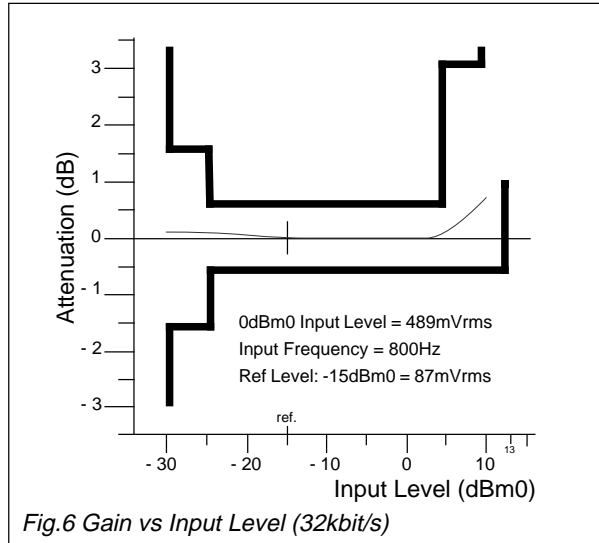
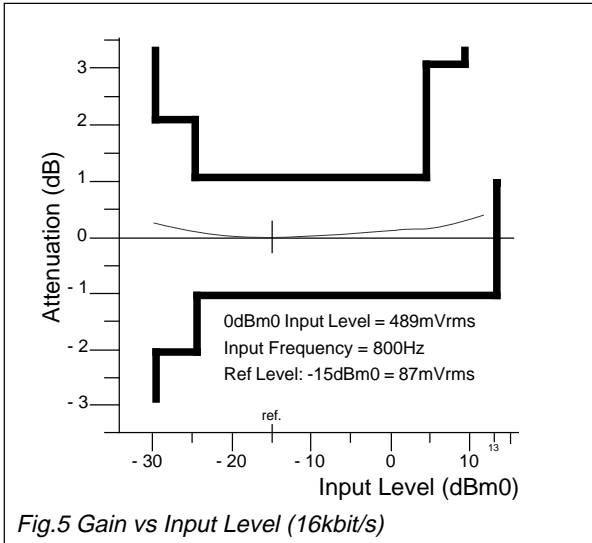
**Digital to Analogue Performance .....** Using the bit sequence tests shown in Table 1 (below) at the Decoder Input pin, the analogue signals measured at the Decoder Output pin are 800Hz  $\pm$  10Hz at the levels described.

Sample Rate	Bit Sequence at Decoder Input	"Run of Threes" (%)	Output Level (dBm0)
16kbit/s	11011011010010010010	0	-29.2 $\pm$ 2
32kbit/s	1101101101010100100100100100101010110110	0	-30.0 $\pm$ 2
16kbit/s	11111011010000010010	30	0 $\pm$ 1
32kbits	1111101101010101000010000010010101011110	30	0 $\pm$ 1

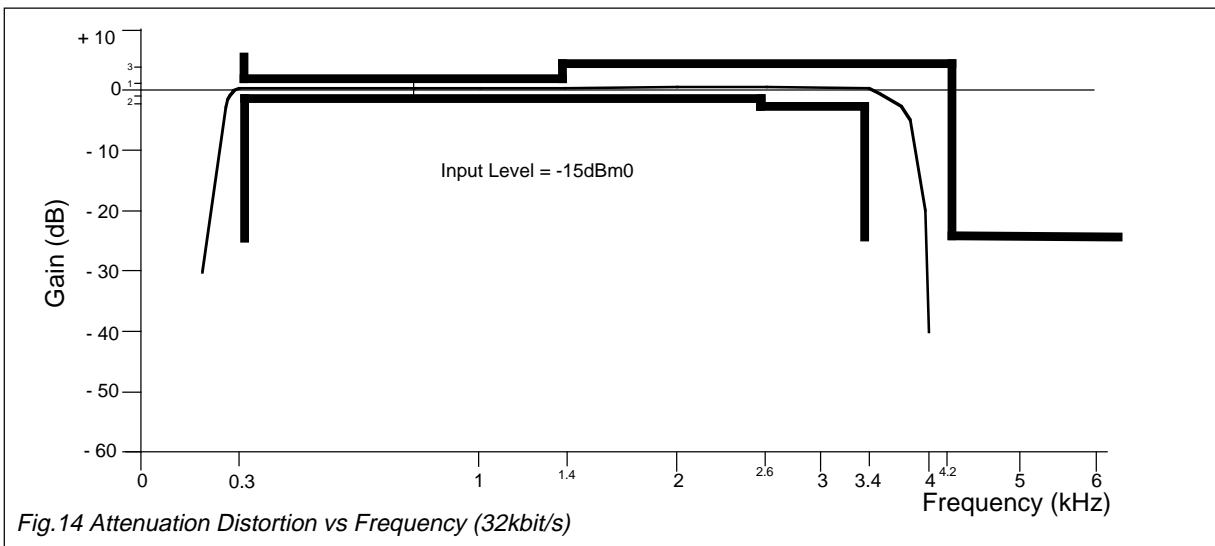
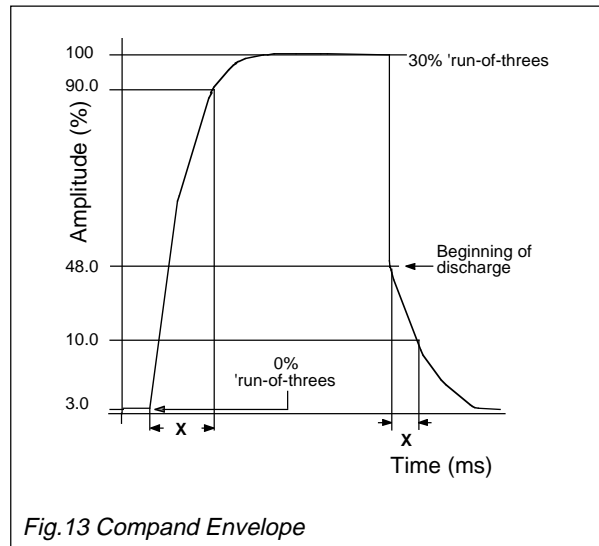
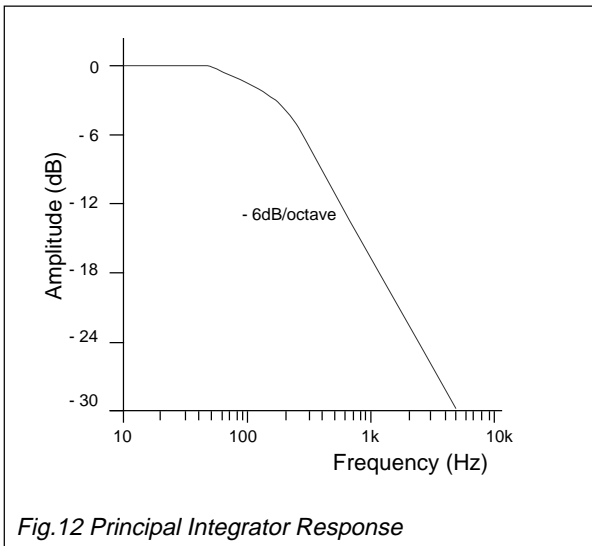
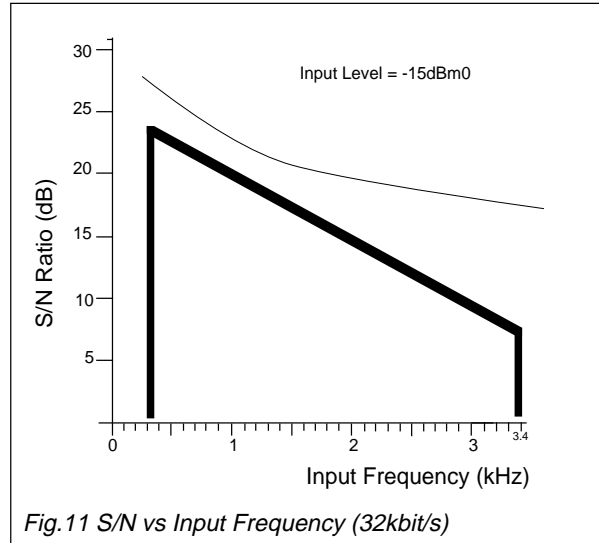
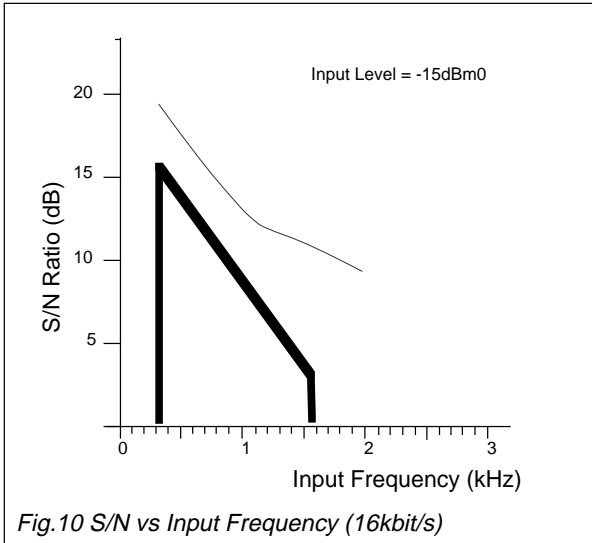
Table 1 Bit Sequence Tests and Results

at 800Hz

**Typical Codec Performance .....** relative to the Mil-Std-188-113 Specification



**Typical Codec Performance .....** relative to the Mil-Std-188-113 Specification



## Specifications

### Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref $V_{SS} = 0V$ )	-0.3 to ( $V_{DD} + 0.3V$ )
Source/sink current (supply pins)	$\pm 30mA$
(other pins)	$\pm 20mA$
Total device dissipation @ 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range: <b>FX629J</b>	-40°C to +85°C
Storage temperature range: <b>FX629J</b>	-55°C to +125°C

### Operating Limits

All characteristics are measured using the following parameters unless otherwise specified:

$V_{DD} = 5.0V$ ,  $T_{AMB} = 25^{\circ}C$ , Xtal/Clock  $f_0 = 1.024MHz$ , Audio Level 0dB ref (0dBm0) = 489 mV rms.

Audio Test Frequency = 800 Hz. Sample Clock Rate = 32kb/s. Compand Algorithm = 3-bit.

Characteristics	See Note	Min.	Typ.	Max.	Unit
<b>Static Values</b>					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)		–	5.5	–	mA
Supply Current (Powersave)		–	0.4	–	mA
Inputs Logic '1'	8	3.5	–	–	V
Inputs Logic '0'	8	–	–	1.5	V
Outputs Logic '1'	8	4.0	–	–	V
Outputs Logic '0'	8	–	–	1.0	V
Digital Input Impedance (Logic I/O pins)		1.0	10.0	–	MΩ
Digital Input Impedance (Logic input pins, pullup resistor)	2	300	–	–	kΩ
Digital Output Impedance		–	–	4	kΩ
Analogue Input Impedance	4	–	1.0	–	kΩ
Analogue Output Impedance	7	–	–	800	Ω
Three State Output Leakage Current (output disabled)		-4.0	–	+4.0	μA
Insertion Loss	3	-2.0	–	+2.0	dB
<b>Dynamic Values</b>					
<b>Encoder:</b>					
Analogue Signal Input Levels	5,9	-35.0	–	+12.0	dBm0
Principle Integrator Frequency		127	159	212	Hz
Encoder Passband		–	3400	–	Hz
Compand Time Constant		4.0	5.0	6.0	ms
<b>Decoder:</b>					
Analogue Signal Output Levels	5,9	-35.0	–	+12.0	dBm0
Decoder Passband		300	–	3400	Hz
<b>Encoder Decoder (Full codec):</b>					
Compression Ratio ( $C_d = 0.3$ to $C_d = 0.0$ )		–	16:1	–	
Passband		300	–	3400	Hz
Stopband		4.2	–	–	kHz
Stopband Attenuation (4200Hz to 6000Hz)		25.0	–	–	dB
(> 6kHz)		–	60.0	–	dB
Passband Gain		–	0	–	dB
Passband Ripple (300Hz – 1400Hz)		-1.0	–	+1.0	dB
(1400Hz – 2600Hz)		-1.0	–	+3.0	dB
(2600Hz – 3400Hz)		-2.0	–	+3.0	dB
Output Noise (Input short circuit)	9	–	-55.0	–	dBm0
Perfect Idle Channel Noise (Encoder forced)	9	–	-57.0	–	dBm0
Group Delay Distortion	6				
(1000Hz to 2600Hz)		–	–	450	μs
(600Hz to 2800Hz)		–	–	750	μs
(500Hz to 3000Hz)		–	–	1.5	ms
Xtal/Clock Frequency		–	1024	–	kHz



## Specifications .....

### Process Information

The following Table gives details of the process and test controls employed in the manufacture of the FX629 'Mil Std' Delta Codec.

Function	Reference	Remarks
Hermeticity		
Fine Leak Test –	Mil Std 883C	using Method 1014 – test condition A1.
Coarse Leak Test –	Mil Std 883C	using Method 1014 – test condition C.
Burnin	Mil Std 883C	using Method 1015 – test condition E. 168 Hours @ 85°C with 5v power, and clocks applied.
Temperature Cycling	Mil Std 883C	using Method 1010 – test condition B. 10 cycles -55°C to +125°C.

The following mechanical assembly tests are Qualified to BS9450

Vibration	BS9450	Section 1.2.6.8.1 55Hz to 500Hz at 98 m/sec acceleration.
Shock	BS9450	Section 1.2.6.6 981 m/sec for 6 msec.
Low Pressure	BS9450	Section 1.2.6.12 225mmHg (altitude 9000m). 600mmHg (altitude 2400m).
Transport and Storage – Operation – Humidity	BS9450	Section 1.2.6.4 96 Hours @ 45°C, 95% relative humidity plus condensed water.

- Notes:**
1. Dynamic characteristics are specified at 5V unless otherwise specified.
  2. All logic inputs except, Encoder and Decoder Data Clocks.
  3. For an Encoder/Decoder combination, insertion loss contributed by a single component is half this figure.
  4. Driven with a source impedance of <100Ω.
  5. Recommended values – See Figures 5, 6, 7 and 8.
  6. Group Delay Distortion for the full codec is relative to the delay with 820Hz, -20dB at the encoder input.
  7. An Emitter Follower output stage.
  8. 4.0V = 80%  $V_{DD}$ , 3.5V = 70%  $V_{DD}$ , 1.5V = 30%  $V_{DD}$ , 1.0V = 20%  $V_{DD}$ .
  9. Analogue Voltage Levels used in this Data Sheet: 0dBm0 = 489mVrms = - 4dBm = 0dB.  
-15dBm0 = 87mVrms. - 20dBm0 = 49mVrms = - 24dBm.

### Application Recommendations

Due to the very low levels of signal and idle channel noise required in Military applications – a noisy or badly regulated power supply could cause instability putting the overall system performance out of specification. Adherence to the points noted below will assist in minimizing this problem.

- |   |  |
|---|--|
| (a) Care should be taken on the design and layout of the printed circuit board.                         | (e) Inputs and outputs should be screened wherever possible.   |
| (b) All external components (as recommended in Figure 3) should be kept close to the package.           | (f) A "ground plane" connected to $V_{SS}$ will assist in eliminating external pick-up on the input and output pins.                                       |
| (c) Tracks should be kept short, particularly the Encoder Input capacitor and the $V_{BIAS}$ capacitor. | (g) It is recommended that the power supply rails have less than 1mVrms of noise allowed.  |
| (d) Xtal/clock tracks should be kept well away from analogue inputs and outputs.                        | (h) The source impedance to the Encoder Input pin must be less than 100Ω, Output Idle channel noise levels will improve with even lower source impedances. |

## Package Outlines

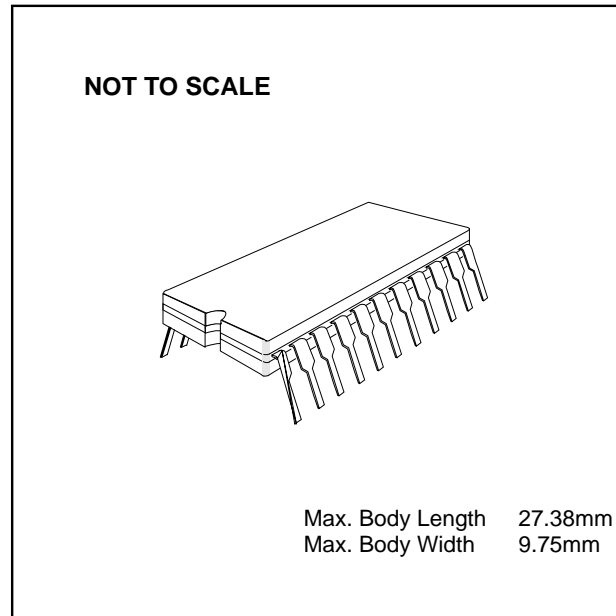
The FX629 is available in the package style outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.

Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

## Handling Precautions

The FX629 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

**FX629J**    22-pin cerdip DIL    (J3)



## Ordering Information

**FX629J**    22-pin cerdip DIL    (J3)

CML does not assume any responsibility for the use of any circuitry described. No circuit patent licences are implied and CML reserves the right at any time without notice to change the said circuitry.