

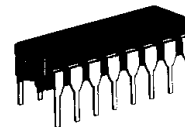
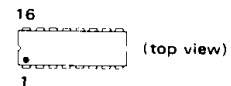
# MC8T14 MC8T24

## TRIPLE LINE RECEIVERS WITH HYSTERESIS

... specifically designed to meet the input/output specifications for IBM 360/370 Systems (IBM specification GA 22-6974-0). Each receiver incorporates hysteresis to provide high noise immunity and also high input impedance to minimize loading on the related driver.

- Each Channel Can Be Independently Strobed
- High Speed —  $t_{PLH} = t_{PHL} = 20 \text{ ns}$
- Input Gating Provided on Each Line
- Operates on a Single +5.0 V Power Supply
- Fully Compatible with MTTL or MDTL Logic Systems
- Input Hysteresis Results in High Noise Immunity

## TRIPLE LINE RECEIVERS WITH HYSTERESIS SILICON MONOLITHIC INTEGRATED CIRCUIT

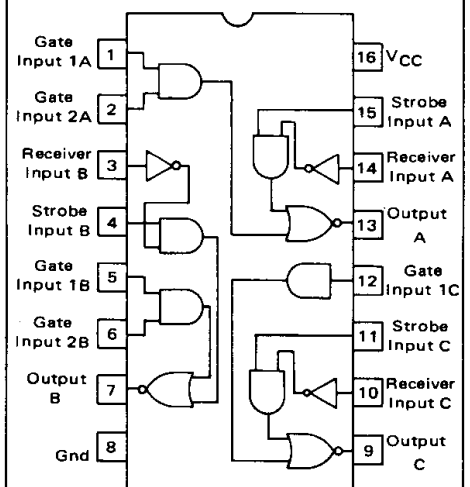


**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648

### PIN CONNECTIONS

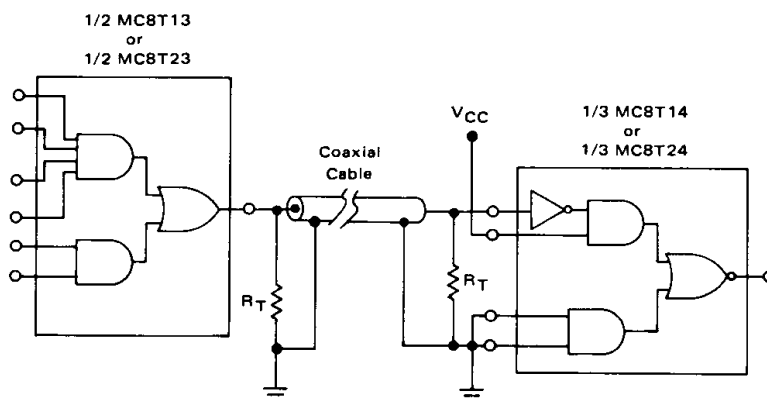


### TRUTH TABLE

Receiver	Inputs			Output
	Strobe	Gate 1	Gate 2	
X	X	H	H	L
L	H	X	X	L
H	X	L	X	H
X	L	L	X	H
H	X	X	L	H
X	L	X	L	H

Where:  
L = Low Logic State  
H = High Logic State  
X = Don't Care

### TYPICAL APPLICATION



# MC8T14,MC8T24

## MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	7.0	Vdc
Receiver Input Voltage (V <sub>CC</sub> = 0)	V <sub>I(R)</sub>	7.0 6.0	Vdc
Strobe or Gate Input Voltage	V <sub>I(S) or (G)</sub>	5.5	Vdc
Output Voltage	V <sub>O</sub>	7.0	Vdc
Output Current	I <sub>O</sub>	±100	mA
Power Dissipation (Package Limitation)	P <sub>D</sub>		
Ceramic Package Derate above 25°C		1000 6.7	mW mW/°C
Plastic Package Derate above 25°C		830 6.7	mW mW/°C
Junction Temperature	T <sub>J</sub>		°C
Ceramic Package		175	
Plastic Package		150	
Operating Ambient Temperature Range	T <sub>A</sub>	0 to +75	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C

## ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 ≤ V<sub>CC</sub> ≤ 5.25 V and 0°C ≤ T<sub>A</sub> ≤ 75°C)

Characteristic	Symbol	MC8T14			MC8T24			Unit
		Min	Typ	Max	Min	Typ	Max	
Gate or Strobe Input Voltage – High Logic State	V <sub>IH(G) or (S)</sub>	2.0	–	–	2.0	–	–	V
Gate or Strobe Input Voltage – Low Logic State	V <sub>IL(G) or (S)</sub>	–	–	0.8	–	–	0.8	V
Receiver Input Voltage – High Logic State	V <sub>IH(R)</sub>	2.0	–	–	1.7	–	–	Vdc
Receiver Input Voltage – Low Logic State	V <sub>IL(R)</sub>	–	–	0.8	–	–	0.7	Vdc
Receiver Input Hysteresis (1) (V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C, V <sub>IL(G)</sub> = 0, V <sub>IH(S)</sub> = 4.5 V)	V <sub>H(R)</sub>	0.3	0.5	–	0.2	0.4	–	V
Input Clamp Voltage (V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C, I <sub>I</sub> = -12 mA) (Strobe or Gate Inputs)	V <sub>IC(G) or (S)</sub>	–	–	1.5	–	–	1.5	V
Input Breakdown Voltage (V <sub>CC</sub> = 5.0 V, I <sub>I</sub> = 10 mA) (Strobe or Gate Inputs)	V <sub>I(G) or (S)</sub>	5.5	–	–	5.5	–	–	V
Receiver Input Current – High Logic State (V <sub>IH(R)</sub> = 3.8 V) (V <sub>IH(R)</sub> = 3.11 V) (V <sub>IH(R)</sub> = 7.0 V) (V <sub>IH(R)</sub> = 6.0 V, V <sub>CC</sub> = 0 V)	I <sub>IH(R)</sub>	–	–	0.17	–	–	–	mA
Gate or Strobe Input Current – High Logic State (V <sub>IH(S)</sub> = 4.5 V, V <sub>IH(R)</sub> = 3.11 V) (V <sub>IH(G)</sub> = 4.5 V)	I <sub>IH(G) or (S)</sub>	–	–	40	–	–	40	μA
Gate or Strobe Input Current – Low Logic State (V <sub>IL(G) or (S)</sub> = 0.4 V, V <sub>IL(R)</sub> = 0 V)	I <sub>IL(G) or (S)</sub>	-0.1	–	-1.6	-0.1	–	-1.6	mA
Output Voltage – High Logic State (V <sub>IH(R)</sub> = 2.0 V, V <sub>IH(S)</sub> = 2.0 V, V <sub>IL(G)</sub> = 0.8 V, I <sub>OH</sub> = -800 μA) (V <sub>IH(R)</sub> = 0.8 V, V <sub>IL(S)</sub> = 0.8 V, V <sub>IL(G)</sub> = 0.8 V, I <sub>OH</sub> = -800 μA) (V <sub>IH(R)</sub> = 1.7 V, V <sub>IH(S)</sub> = 2.0 V, V <sub>IL(G)</sub> = 0.8 V, I <sub>OH</sub> = -800 μA) (V <sub>IH(R)</sub> = 0.7 V, V <sub>IL(S)</sub> = 0.8 V, V <sub>IL(G)</sub> = 0.8 V, I <sub>OH</sub> = -800 μA)	V <sub>OH</sub>	2.6 2.6	3.5 3.5	– –	– –	– –	– –	V
Output Voltage – Low Logic State (V <sub>IL(R)</sub> = 0.8 V, V <sub>IH(S)</sub> = 2.0 V, V <sub>IL(G)</sub> = 0.8 V, I <sub>OL</sub> = 16 mA) (V <sub>IL(R)</sub> = 0.8 V, V <sub>IL(S)</sub> = 0.8 V, V <sub>IH(G)</sub> = 2.0 V, I <sub>OL</sub> = 16 mA) (V <sub>IL(R)</sub> = 0.7 V, V <sub>IH(S)</sub> = 2.0 V, V <sub>IL(G)</sub> = 0.8 V, I <sub>OL</sub> = 16 mA) (V <sub>IL(R)</sub> = 0.7 V, V <sub>IL(S)</sub> = 0.8 V, V <sub>IH(G)</sub> = 2.0 V, I <sub>OL</sub> = 16 mA)	V <sub>OL</sub>	– – – –	– – – –	0.4 0.4 – –	– – – –	– – – –	– – 0.4 0.4	V
Output Short-Circuit Current (2) (V <sub>IH(R)</sub> = 3.8 V, V <sub>IL(G)</sub> = 0 V, V <sub>IL(S)</sub> = 0, V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C) (V <sub>IH(R)</sub> = 3.11 V, V <sub>IL(G)</sub> = 0 V, V <sub>IL(S)</sub> = 0 V, V <sub>CC</sub> = 5.0 V, T <sub>A</sub> = 25°C)	I <sub>OS</sub>	-50 –	– –	-100 –	– -50	– –	– -100	mA
Power Supply Current (V <sub>CC</sub> = 5.25 V, T <sub>A</sub> = 25°C)	I <sub>CC</sub>	–	60	72	–	60	72	mA

(1) The Input Hysteresis is defined as the difference the input voltage at which the output begins to go from the high logic state to the low logic state and the input voltage which causes the output to begin to go from the low logic state to the high logic state.

(2) Only one output may be shorted at a time.

5

# MC8T14, MC8T24

SWITCHING CHARACTERISTICS ( $V_{CC} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Parameter	Symbol	MC8T14, MC8T24			Unit
		Min	Typ	Max	
Propagation Delay Time – Receiver Input to High Logic State Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time Receiver Input to Low Logic State Output	$t_{PHL(R)}$	–	20	30	ns
Propagation Delay Time Strobe Input to High Logic State Output	$t_{PLH(S)}$	–	–	–	ns
Propagation Delay Time Strobe Input to Low Logic State Output	$t_{PHL(S)}$	–	–	–	ns
Propagation Delay Time Gate Input to High Logic State Output	$t_{PLH(G)}$	–	–	–	ns
Propagation Delay Time Gate Input to Low Logic State Output	$t_{PHL(G)}$	–	–	–	ns

FIGURE 1 – RECEIVER PROPAGATION DELAY TIMES  $t_{PLH(R)}$  and  $t_{PHL(R)}$  TEST CIRCUIT AND WAVEFORMS

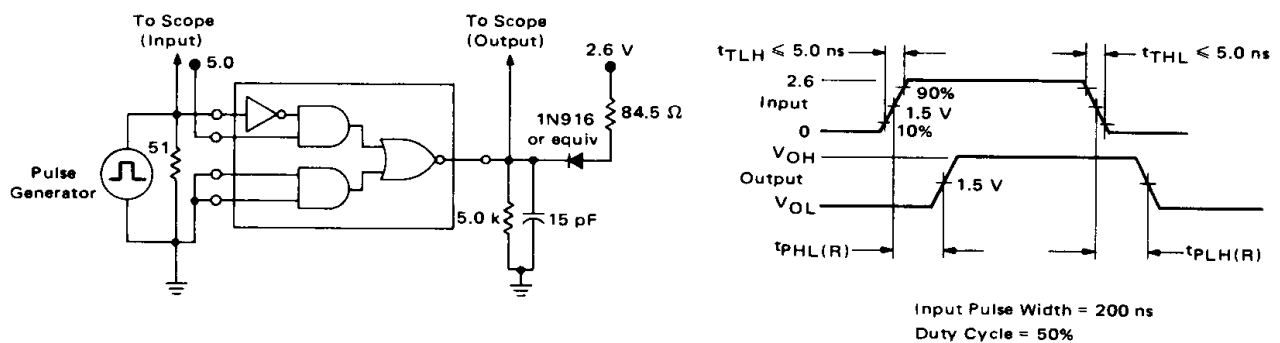
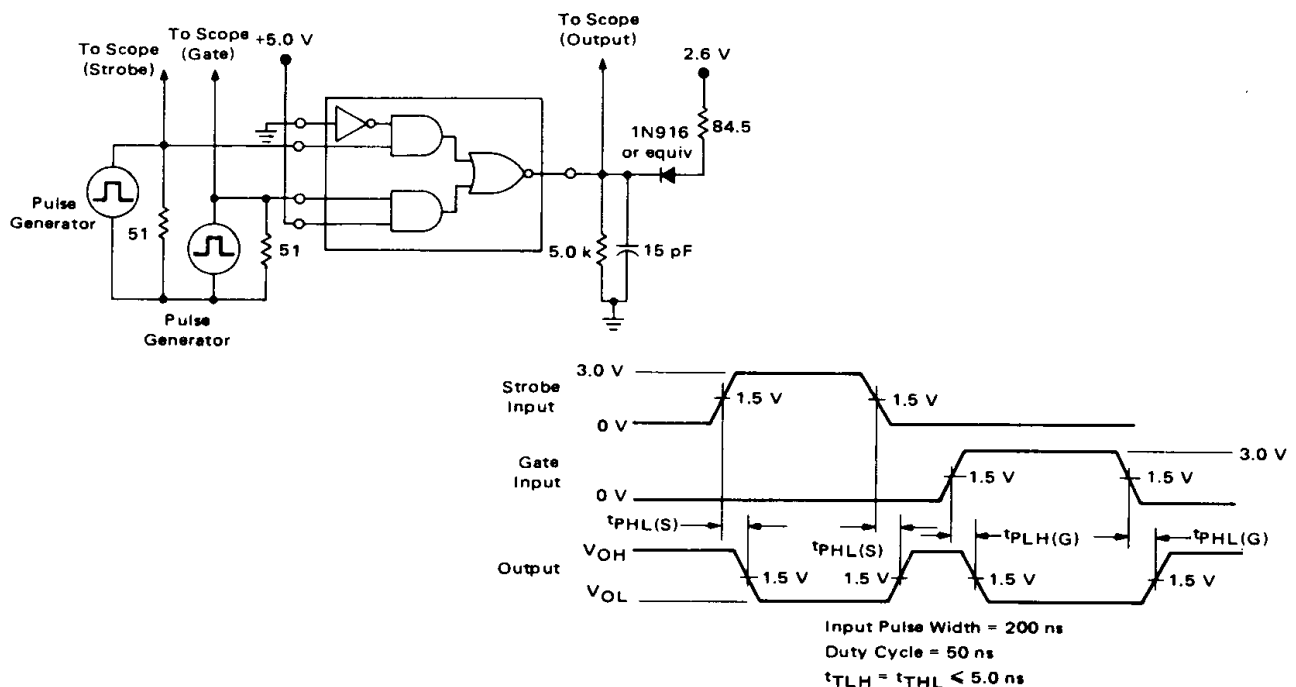
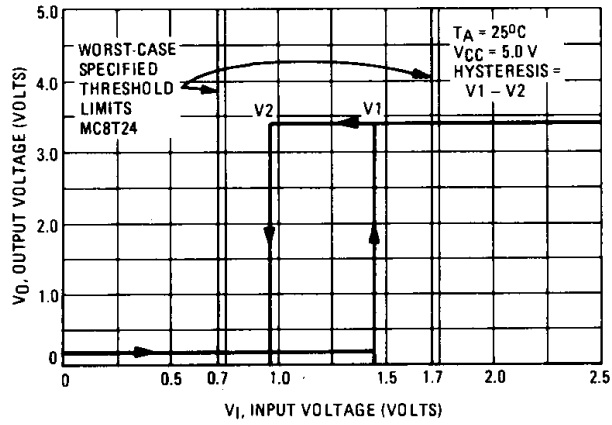


FIGURE 2 – GATE AND STROBE PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS

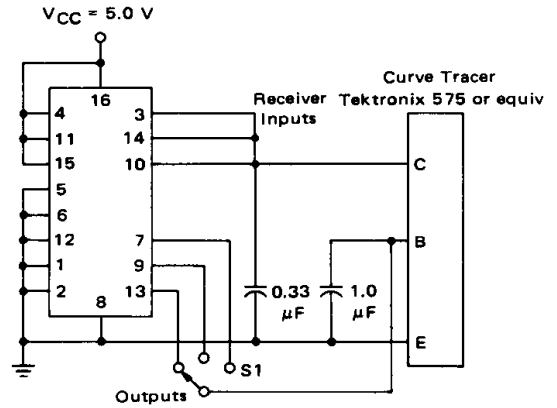


# MC8T14,MC8T24

**FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTIC**



**FIGURE 4 – HYSTERESIS TEST CIRCUIT**



**REPRESENTATIVE CIRCUIT SCHEMATIC**

