

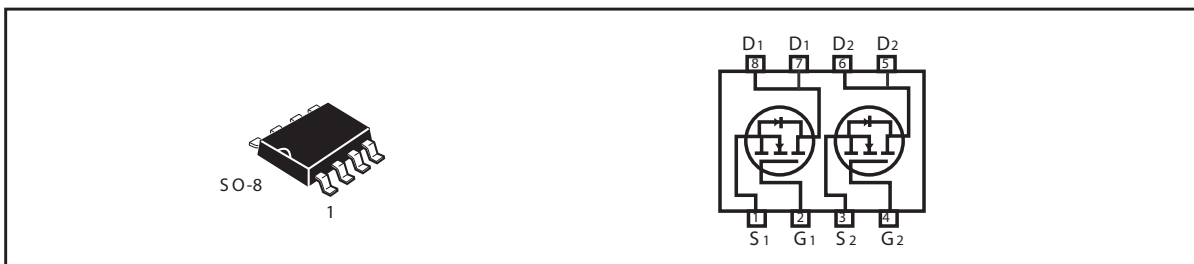


## Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
40V	7A	25 @ V <sub>GS</sub> = 10V 45 @ V <sub>GS</sub> = 4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	40	V	
Gate-Source Voltage	V <sub>GS</sub>	±25	V	
Drain Current-Continuous <sup>a</sup> @ T <sub>a</sub>	I <sub>D</sub>	25°C	7	A
		70°C	5.9	A
-Pulsed <sup>b</sup>	I <sub>DM</sub>	22	A	
Drain-Source Diode Forward Current <sup>a</sup>	I <sub>S</sub>	1.7	A	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>a</sub> = 25°C	2	W
		T <sub>a</sub> =70°C	1.44	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C	

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	R <sub>θJA</sub>	62.5	°C/W
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N-Channel ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	40			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 32V, V <sub>GS</sub> = 0V			1	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±25V, V <sub>DS</sub> = 0V			±100	nA
ON CHARACTERISTICS <sup>b</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA	1	1.8	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6A		20	25	m ohm
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5A		35	45	m ohm
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = 5V, V <sub>GS</sub> = 10V	15			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 6A		8		S
DYNAMIC CHARACTERISTICS <sup>c</sup>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V f = 1.0MHz		947	1231	pF
Output Capacitance	C <sub>OSS</sub>			117	152	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			77	100	pF
Gate resistance	R <sub>g</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V, f = 1.0MHz		2		ohm
SWITCHING CHARACTERISTICS <sup>c</sup>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 20V I <sub>D</sub> = 1 A V <sub>GS</sub> = 10V R <sub>GEN</sub> = 3.3 ohm		16.7	19	ns
Rise Time	t <sub>r</sub>			3.6	5	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			28.7	38	ns
Fall Time	t <sub>f</sub>			10.1	14	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 20V, I <sub>D</sub> = 6A, V <sub>GS</sub> = 10V		18.2	24	nC
		V <sub>DS</sub> = 20V, I <sub>D</sub> = 6A, V <sub>GS</sub> = 4.5V		8.7	12	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 20V, I <sub>D</sub> = 6 A		2.8	4	nC
Gate-Drain Charge	Q <sub>gd</sub>	V <sub>GS</sub> = 4.5V		3.3	5	nC

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## ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_s = 1.7A$		0.78	1.2	V

### Notes

- a. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .
- b. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- c. Guaranteed by design, not subject to production testing.

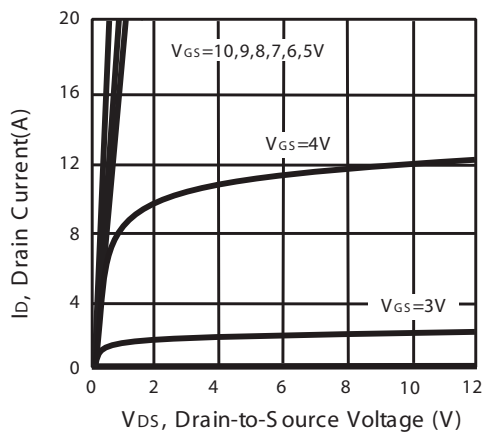


Figure 1. Output Characteristics

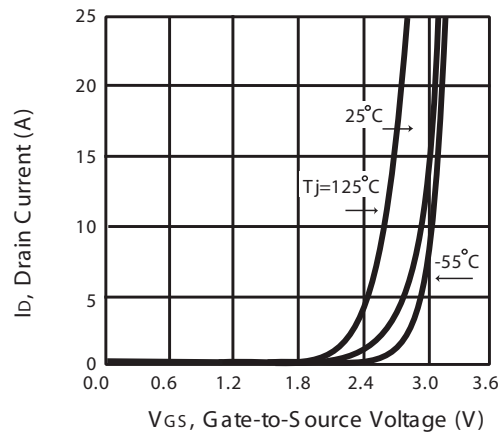


Figure 2. Transfer Characteristics

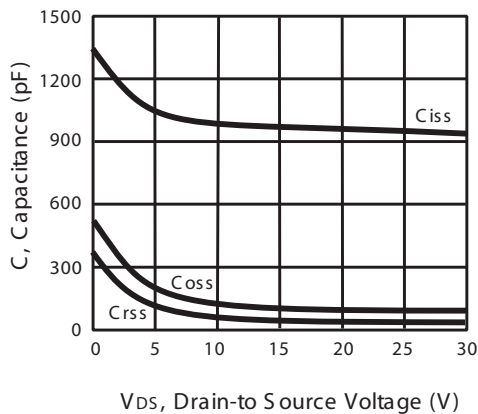


Figure 3. Capacitance

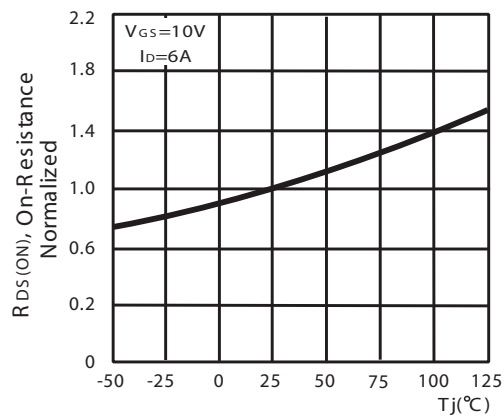
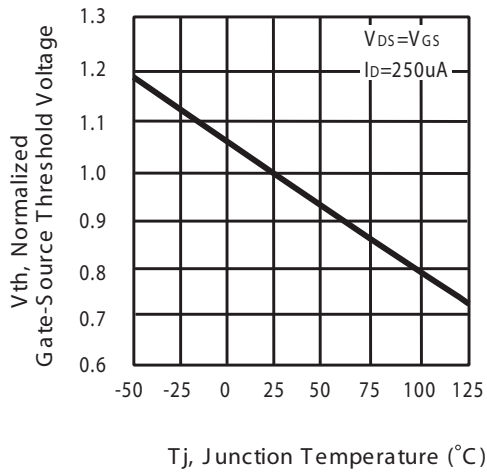


Figure 4. On-Resistance Variation with Temperature

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with Temperature

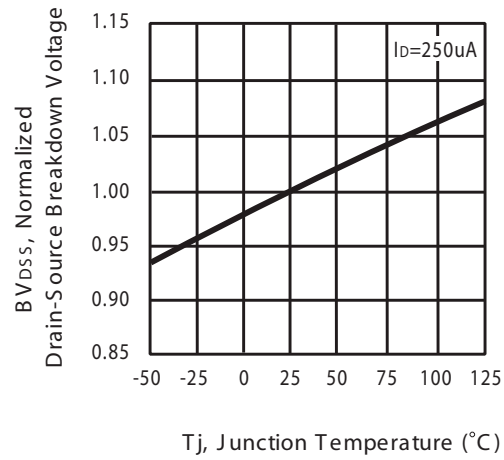


Figure 6. Breakdown Voltage Variation with Temperature

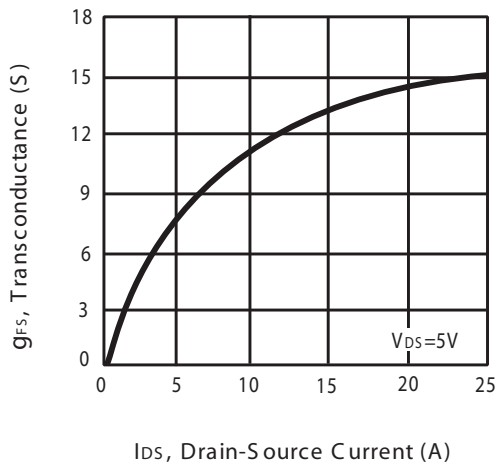


Figure 7. Transconductance Variation with Drain Current

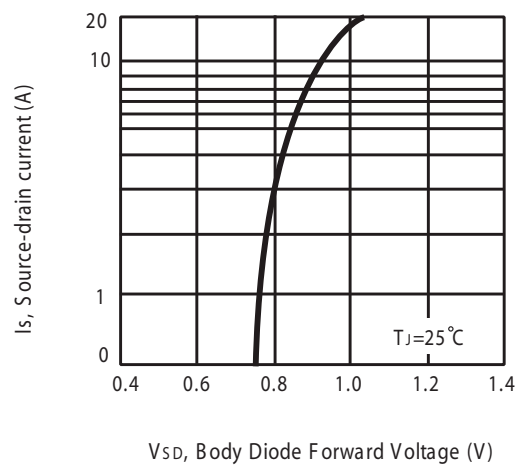


Figure 8. Body Diode Forward Voltage Variation with Source Current

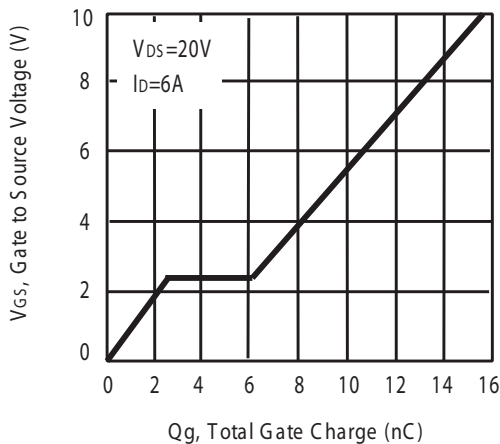


Figure 9. Gate Charge

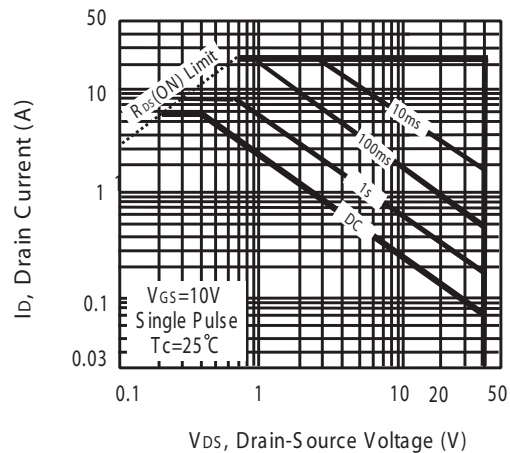


Figure 10. Maximum Safe Operating Area

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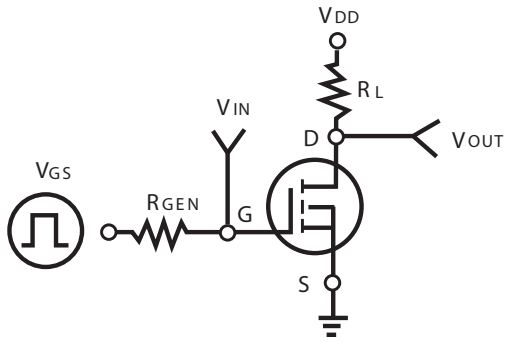


Figure 11. Switching Test Circuit

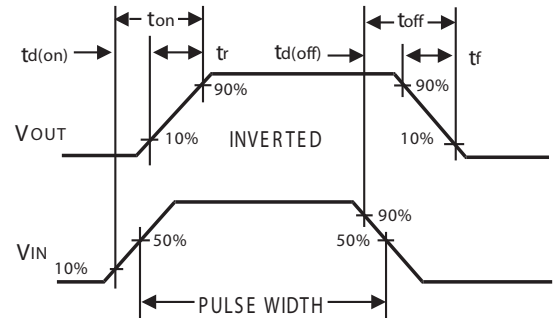
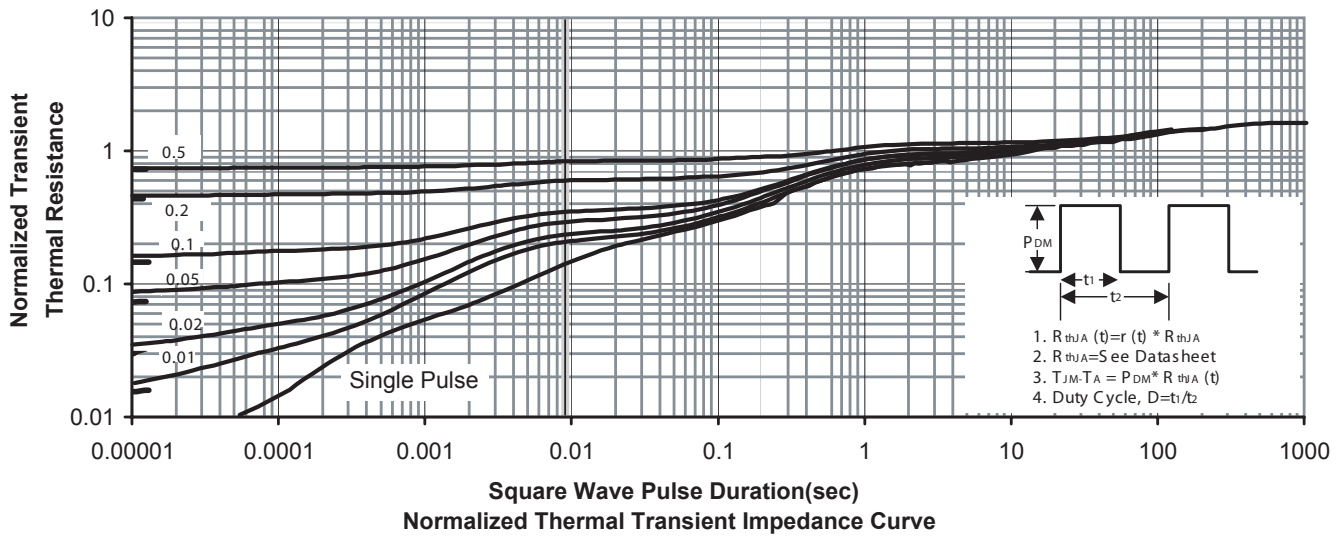


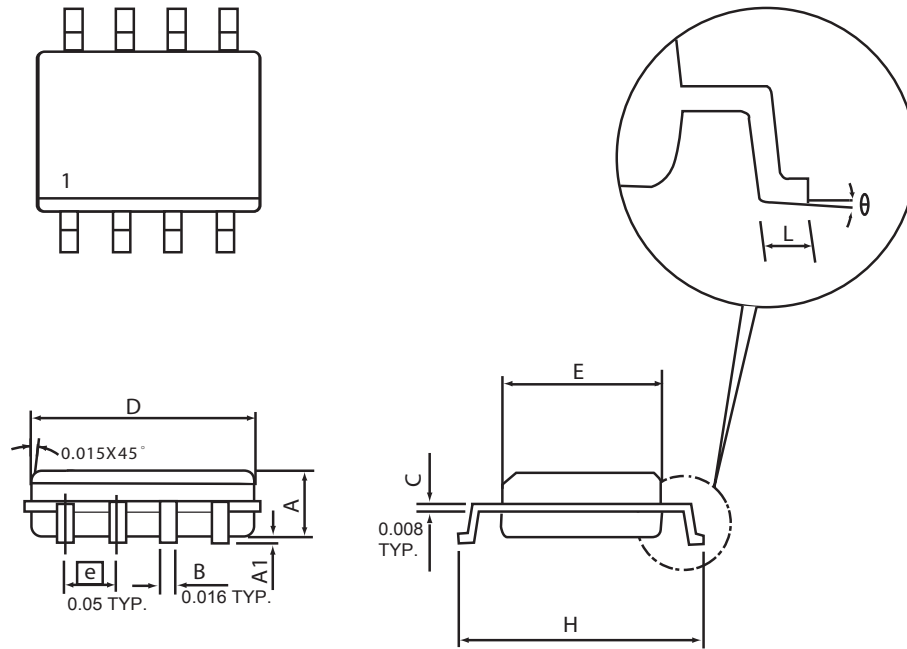
Figure 12. Switching Waveforms



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## PACKAGE OUTLINE DIMENSIONS

SO-8

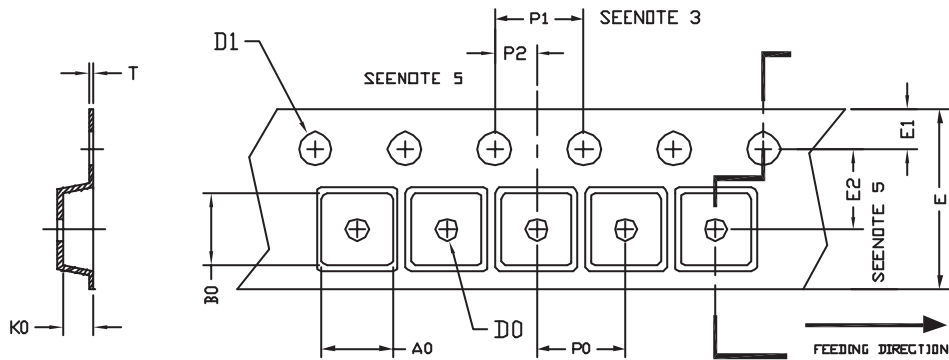


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	4.98	0.189	0.196
E	3.81	3.99	0.150	0.157
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
$\theta$	0°	8°	0°	8°

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## SO-8 Tape and Reel Data

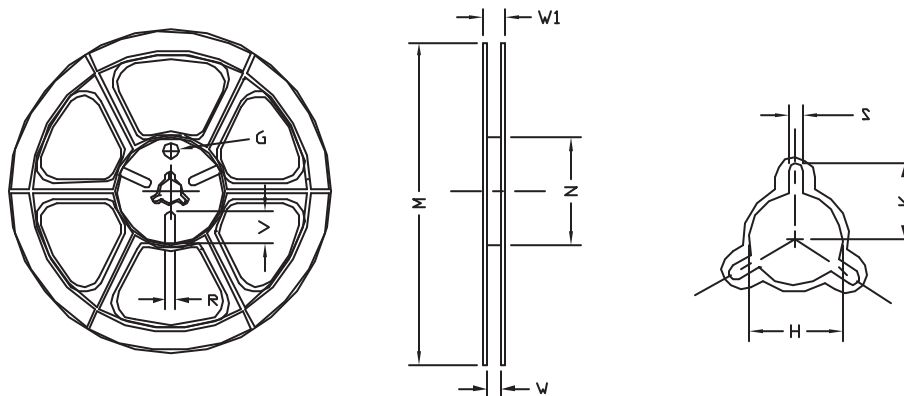
### SO-8 Carrier Tape



unit:mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOP 8N 150mil	6.40	5.20	2.10	$\phi$ 1.5 (MIN)	$\phi$ 1.5 + 0.1 - 0.0	12.0 $\pm$ 0.3	1.75	5.5 $\pm$ 0.05	8.0	4.0	2.0 $\pm$ 0.05	0.3 $\pm$ 0.05

### SO-8 Reel



UNIT:mm

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	$\phi$ 330	330 $\pm$ 1	62 $\pm$ 1.5	12.4 + 0.2	16.8 - 0.4	$\phi$ 12.75 + 0.15	---	2.0 $\pm$ 0.15	---	---	---