MX•COM, INC. MiXed Signal ICs

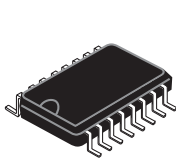
DATABULLETIN

MX631

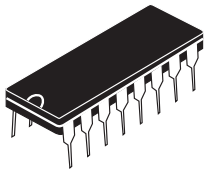
LOW VOLTAGE SPM DETECTOR

Features

- **Detects 12 & 16kHz SPM Frequencies**
- **Low Power (3.0 Volt$_{MIN}$ <1.0mA) Operation**
- **High Speechband Rejection Properties**
- **Tone-Follower and Packet Mode Outputs**
- **Applications**
  - **•Complex and/or Simple Telephone Systems**
  - **•Call-Charge/-Logging Systems**



MX631DW
16-Pin SOIC



MX631P
16-Pin PDIP

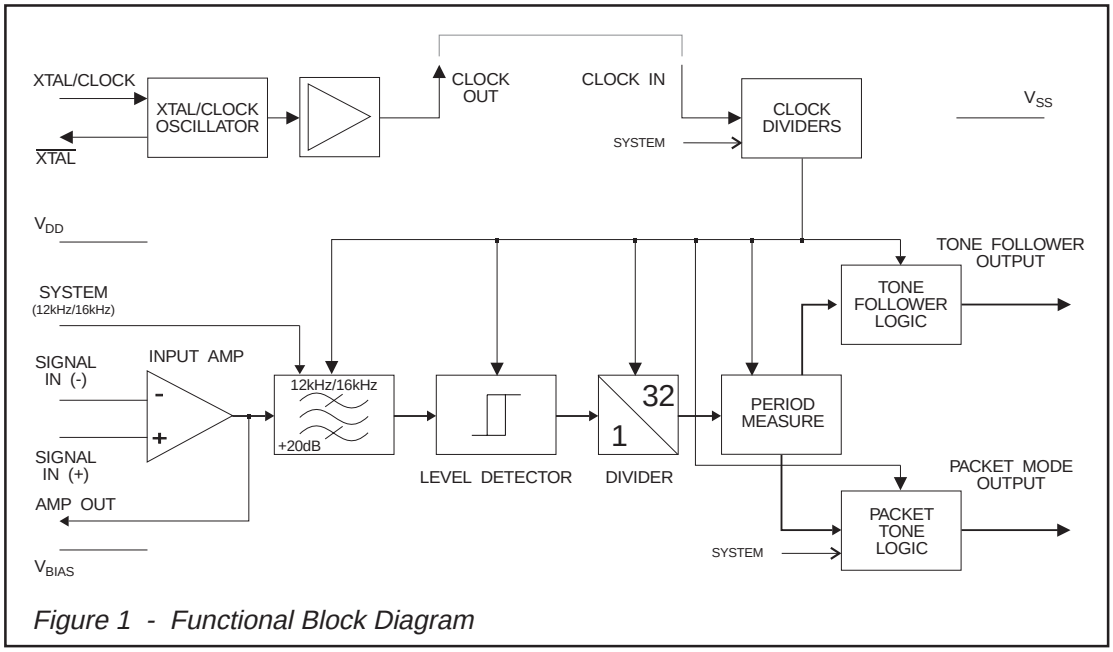


Figure 1 - Functional Block Diagram

Description

The MX631 is a low-power, system-selectable Subscriber Pulse Metering (SPM) detector that indicates the presence of both 12kHz or 16kHz telephone call-charge frequencies on a telephone line.

Deriving its input directly from the telephone line, input amplitude/sensitivities are component adjustable to the user's national 'Must/Must-Not Decode' specifications via an on-chip input amplifier, while the 12kHz and 16kHz frequency limits are accurately defined by the use of an external 3.579545MHz telephone-system Xtal or clock-pulse input.

The MX631, which demonstrates high 12kHz and 16kHz performance in the presence of both voice and noise, can operate from either a single or differential analog signal input from which it will produce two individual logic outputs:

1. Tone Follower Output - A 'tone-following' logic output producing a "Low" level for the period of a correct decode and a "High" level for a bad decode or NOTONE.
2. Packet (Cumulative Tone) Mode Output - To respond and/or de-respond after a cumulative 40ms of good tone (orNOTONE) in any 48ms period. This process will ignore small fluctuations or fades of a valid frequency input and is available for µProcessor 'Wake-Up', Minimum Tone detection, NOTONE indication or transient avoidance.

This system (12kHz/16kHz) selectable integrated circuit, which may be line-powered, is available in 16-pin plastic DIP and SOIC surface mount packages.

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Pin	Function
1	**Xtal/Clock :** The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the Xtal output (see Figure 2). Circuit components are on-chip. Using this mode of clock operation, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is employed to the Clock In pin, this pin must be connected directly to V_{DD} (see Figure 2).
2	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter.
3	**Clock Out:** The buffered output of the on-chip clock oscillator inverter. If a Xtal input is employed this output should be connected directly to the Clock In pin.
4	**Clock In:** The 3.579545MHz clock pulse input to the internal clock-dividers. In the clock pulse input mode the Xtal/Clock input (pin 1) should be connected to V_{DD}. (See Figure 2.)
5	No internal connection, leave open circuit.
6	No internal connection, leave open circuit.
7	**V_{BIAS}:** The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} (see Figure 2).
8	**V_{SS}:** Negative supply (GND).
9 10 11	**Signal In (+):** **Signal In (-):** **Amp Out:** The positive and negative inputs to, and the output from, the input gain adjusting signal amplifier. Refer to Figure 4 for guidance on setting level sensitivities to national specifications, and the selection of gain adjusting components.
12	No internal connection, leave open circuit.
13	**Tone Follower Output:** This output provides a logic “0” (Low) for the period of a detected tone and a logic “1” (High) for NOTONE detection. See Figure 5.
14	**Packet Mode Output:** A logic output that will be available after a cumulation of 40ms of 'good' tone has been received. This packet tone follower will only respond when a tone frequency of sufficient quality has been received for sufficient time, i.e. a cumulation of 40ms in any 48ms; short tone bursts or breaks will be ignored. This output provides a logic “0” (Low) for a detected tone and a logic “1” (High) for NOTONE detection. See Figure 6.
15	**System:** The logic input to select device operation to either 12kHz (logic “1” - High) or 16kHz (logic “0” - Low) SPM systems. This input has an internal 1MΩ pullup resistor (12kHz).
16	**V_{DD}:** Positive supply. A single, stable power supply is required. Critical levels and voltages within the MX631 are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin. Note that if this device is ‘line’ powered, the resulting supply must be stable. See notes on IC Protection from high and spurious line voltages.

Application Information: External Components

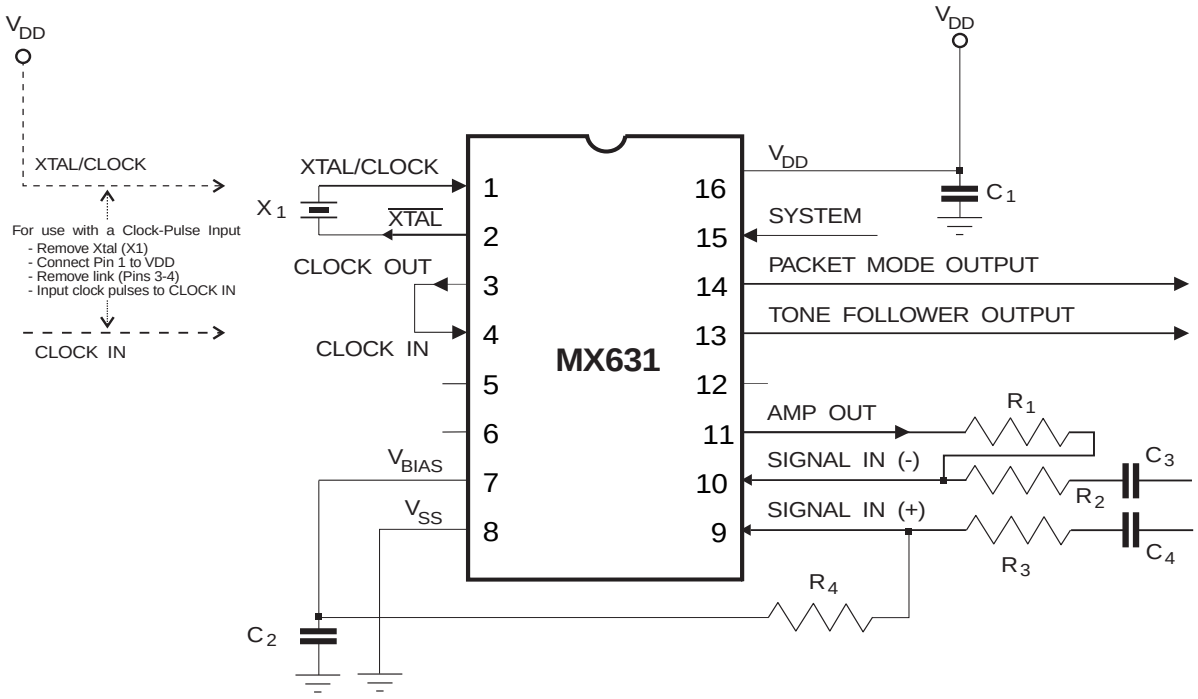


Figure 2 - Recommended External Components - Differential Input Mode

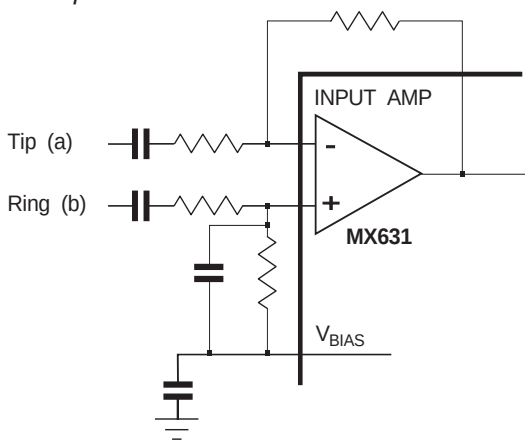
Component	Value
R_1	$R_{FEEDBACK}$
R_2	$R_{IN(-)}$
R_3	$R_{IN(+)}$
R_4	R_{BIAS}
C_1	1.0µF ±20%
C_2	1.0µF ±20%
C_3	$C_{IN(-)}$
C_4	$C_{IN(+)}$
X_1	3.579545MHz

External Components

1. The values of the Input Amp gain components illustrated are calculated using the Input Gain Calculation Graph (Figure 4).
   When calculating input gain components, for correct operation, it is recommended that the values of resistors R_1 and R_4 do not go below 100kΩ.

2. Refer to following pages for advice on IC Protection from high and spurious line voltages.

Differential Input



Common Mode Input

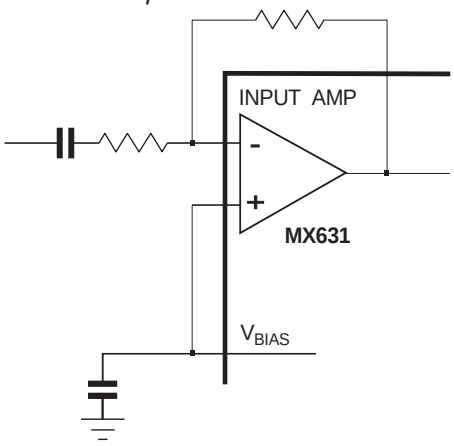


Figure 3 - Example Input Configurations

Application Information .....

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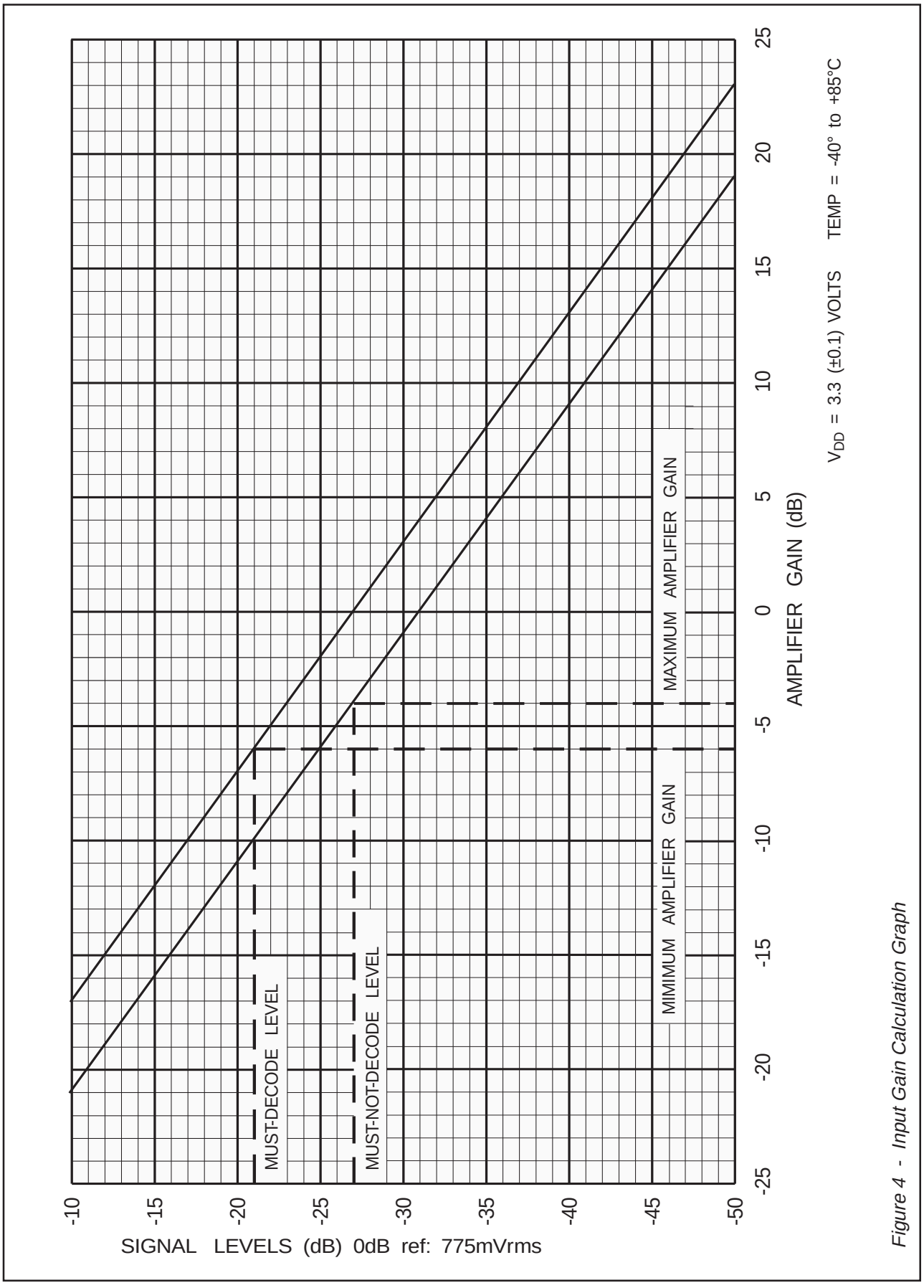

Figure 4 - Input Gain Calculation Graph

Application Information .....

Input Gain Calculation

The input amplifier, with its external circuitry, is provided on-chip to set the sensitivity of the MX631 to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to Figure 4, the following steps will assist in the determination of the required gain/ attenuation.

Step 1

Draw two horizontal lines from the Y-axis (Signal Levels (dB)). The upper line represents your required 'Must' decode level. The lower line represents your required 'Must-Not' decode level.

Step 2

Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis (Amplifier Gain (dB)).

The point where the vertical line meets the X-axis indicates the MINIMUM Input Amp gain required for reliable decoding of valid signals.

Step 3

Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis.

The point where the vertical line meets the X-axis indicates the MAXIMUM allowable Input Amp gain.

Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.

Input Gain Components

The following paragraphs refer to the gain components shown in Figures 2 and 3.

The user should calculate and select external components (R_1, R_2/C_3, R_3/C_4, R_4) to provide an amplifier gain within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain-figure outside these limits.

It is recommended that the designed gain is near the center of the calculated range. The graph in Figure 4 is for calculations for the input gain components for an MX631 using a V_{DD} of 3.3 (±0.1) volts.

Use this area to keep a permanent record of your calculated gains and components

Implementation Notes

Aliasing

Due to the switched-capacitor filters employed in the MX631, be careful to avoid the effects of alias distortion with the external components you choose.

Possible Alias Frequencies:
12kHz Mode= 52kHz
16kHz Mode= 69kHz

If these alias frequencies are liable to cause problems and/or interference, it is recommended that anti-alias capacitors are used across input resistors R_1 and R_4.

Values of anti-alias capacitors should be chosen to provide a highpass cutoff frequency, in conjunction with R_1 (R_4) of approximately 20kHz to 25kHz (12kHz system) or 25kHz to 30kHz (16kHz system).

$$\text{i.e. } C = \frac{1}{2 \times \pi \times f_0 \times R_1}$$

When anti-alias capacitors are used, make allowance for reduced gain at the SPM frequency (12kHz or 16kHz).

Signal Input Protection

Telephone systems may have high d.c. and a.c. voltages present on the line. If the MX631 is part of host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} + 0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the MX631 will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the d.c. voltages plus all expected signal peaks.

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Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} +0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage temperature range	-40°C to +85°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.3V

T_{AMB} = +25 °C

Audio Level 0dB ref: = 775mVrms

Noise Bandwidth = 50kHz

Xtal/Clock or 'Clock In' Frequency = 3.579545MHz

12kHz or 16kHz System Setting

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD}) at 25°C		3.0	-	5.5	V
Supply Current		-	-	1.0	mA
Input Logic "1" (High)		2.3	-	-	V
Input Logic "0" (Low)		-	-	1.0	V
Output Logic "1" (High)		2.9	-	-	V
Output Logic "0" (Low)		-	-	0.4	V
Xtal/Clock or Clock In Frequency		3.558918	-	3.589368	MHz
"High" External Clock Pulse Width		0.1	-	-	µs
"Low" External Clock Pulse Width		0.1	-	-	µs
Input Amp					
D.C. Gain		60.0	-	-	dB
Bandwidth (-3dB open loop)		-	100	-	Hz
Input Impedance		-	1.0	-	MΩ
Logic Impedances					
Input (System)		0.7	-	3.8	MΩ
(Clock In)		10.0	-	-	MΩ
Output		-	14.0	30.0	kΩ
Overall Performance					
12kHz Detect Bandwidth	1	11.820		12.180	kHz
12kHz Not-Detect Frequencies (below 12kHz)	1	-	-	11.520	kHz
12kHz Not-Detect Frequencies (above 12kHz)	1	12.480	-	-	kHz
16kHz Detect Bandwidth	1	15.760		16.240	kHz
16kHz Not-Detect Frequencies (below 16kHz)	1	-	-	15.360	kHz
16kHz Not-Detect Frequencies (above 12kHz)	1	16.640	-	-	kHz
Sensitivity	2	7.8	10.0	15.5	mVp-p
Tone Operation Characteristics					
Signal-to-Noise Requirements (Amp Input)	3,4,5,6	22.0	20.0	-	dB
Signal-to-Voice Requirements (Amp Input)	3,4,5,7	-36.0	-40.0	-	dB
Signal-to-Voice Requirements (Amp Output)	5,6	-25.0	-	-29.0	dB
Tone Follower Output					
Response and De-Response Times	1,8	-	-	10.0	ms
Packet Mode Output					
Response and De-Response Times	1,8	40.0	-	48.0	ms

Characteristics Notes

1. With adherence to Signal-to-Voice and Signal-to Noise specifications.
2. With Input Amp gain setting: $15.5dB_{MIN}$/$19.5dB_{MAX}$.
3. Common Mode SPM and balanced voice signal.
4. Immune to false responses.
5. Immune to false de-responses
6. With SPM and voice signal amplitudes balanced; To avoid false de-responses due to saturation, the peak-to-peak voice+noise level at the output of the Input Amp (12/16kHz Filter Input) should be no greater than the dynamic range of the device.
7. Maximum voice frequencies = 3.4kHz
8. Response, De-Response and Power-up Response Timing.

Application Information .....

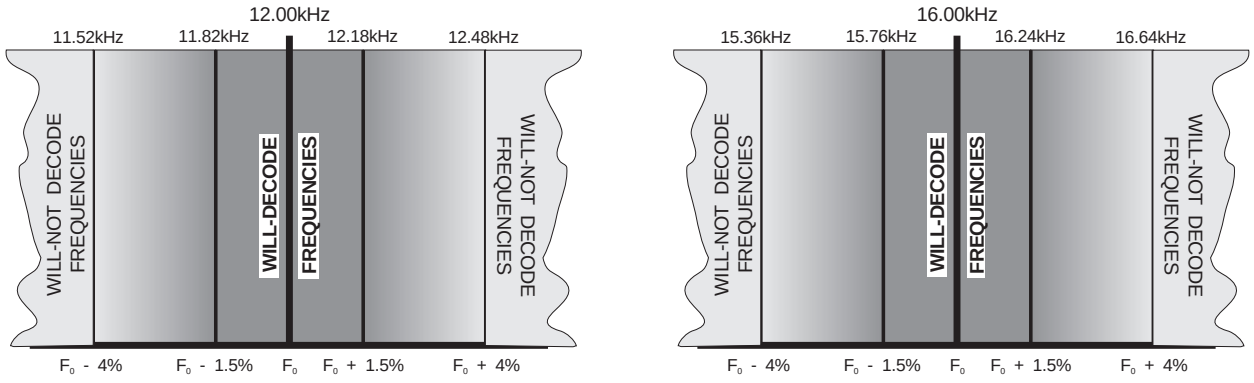


Figure 5 - Will/Will-Not Decode Frequencies

System Timing

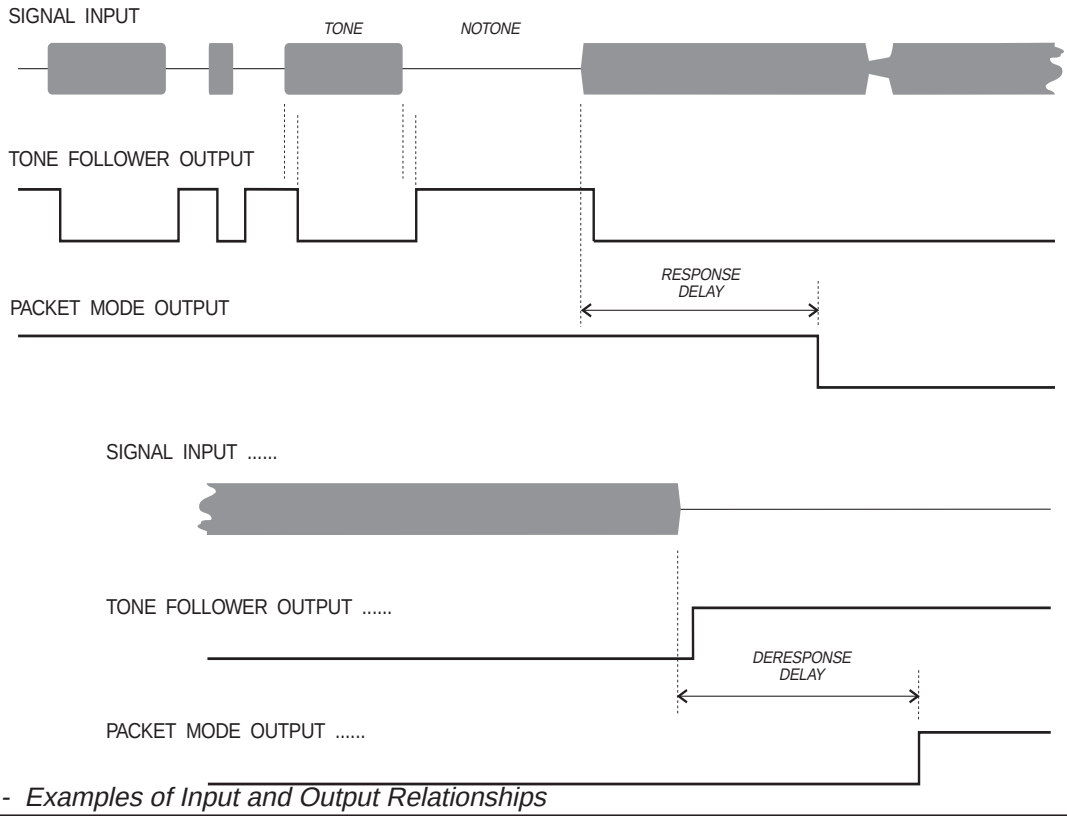
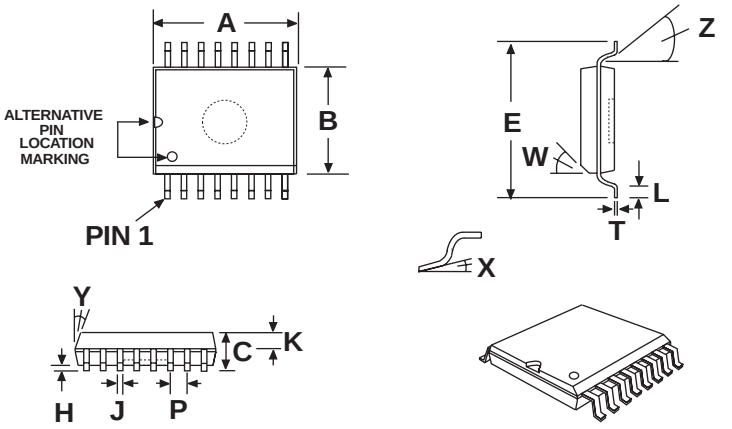


Figure 6 - Examples of Input and Output Relationships

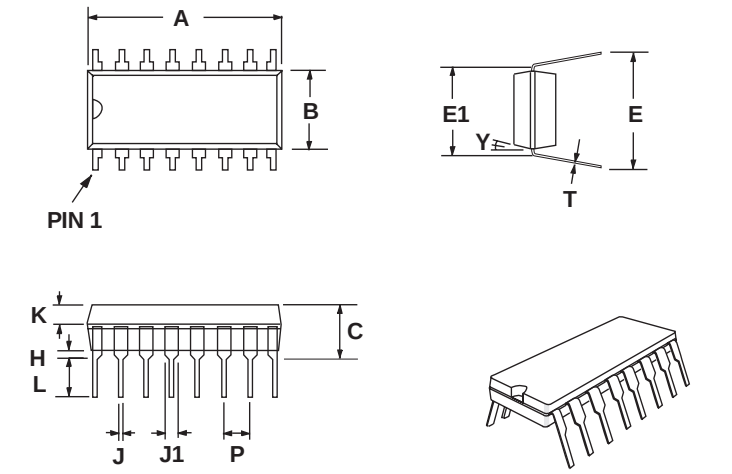


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure7: 16-pin SOIC Mechanical Outline: order as part no. MX631DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure7: 16-pin PDIP Mechanical Outline: order as part no. MX631P

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CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the **'MX-COM'** textual logo is being replaced by a **'CML'** textual logo.

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