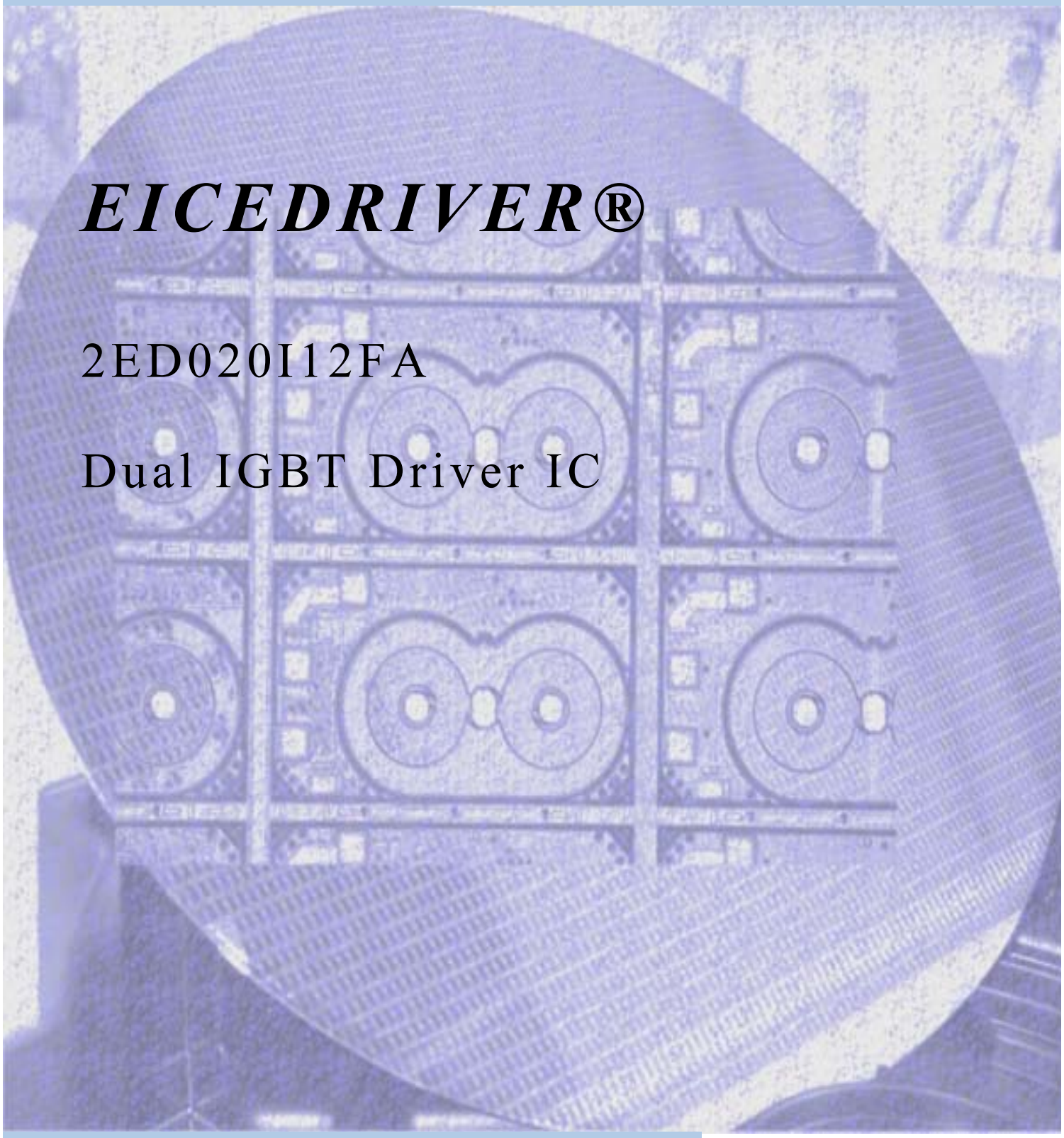

EICEDRIVER®

2ED020I12FA

Dual IGBT Driver IC

Power Management & Drives

Never stop thinking.

2ED020I12FA

Revision History:	**2010-09-20**	Version 1.2
Previous Version:	1.1	

Page	Subjects (major changes since 1.1)

Edition 2010-09-20

Published by Infineon Technologies AG,
Campeon 1-12,
85579 Neubiberg, Germany

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Dual IGBT Driver IC

Product Highlights

- **Coreless transformer isolated driver**
- **Galvanic Insulation**
- **Integrated protection features**
- **Suitable for operation at high ambient temperature**
- **Automotive Qualified (pending)**

Features

- Dual channel isolated IGBT Driver
- For 600V/1200V IGBTs
- 2A rail-to-rail output
- Vcesat-detection
- Active Miller Clamp

Typical Application

- AC and Brushless DC Motor Drives
- High Voltage DC/DC-Converter
- UPS-Systems
- Welding

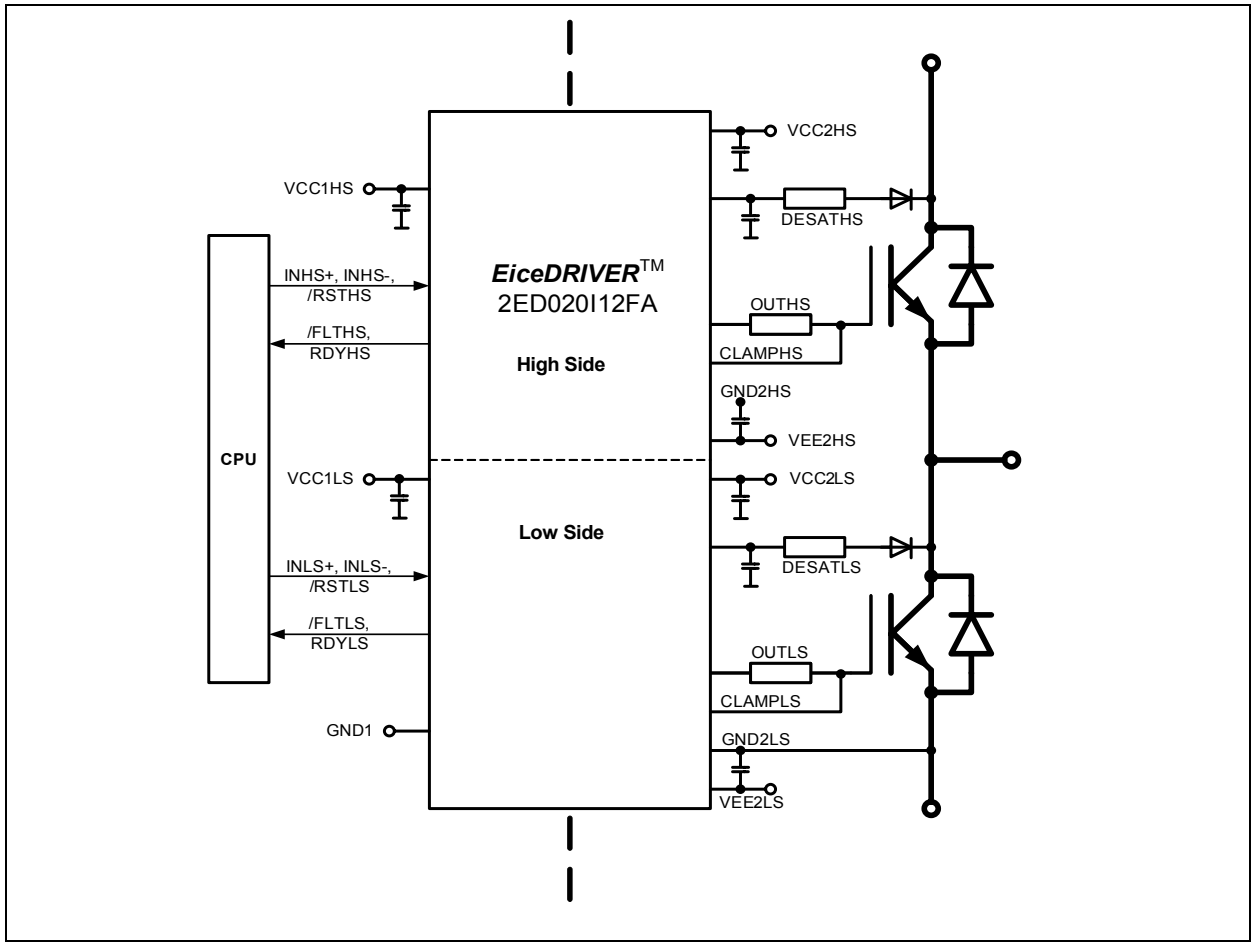

Figure 1: Typical Application

Type		Gate drive current	Package
2ED020I12FA		+/- 2A	PG-DSO-36/32-1

1 Block Diagram and Application

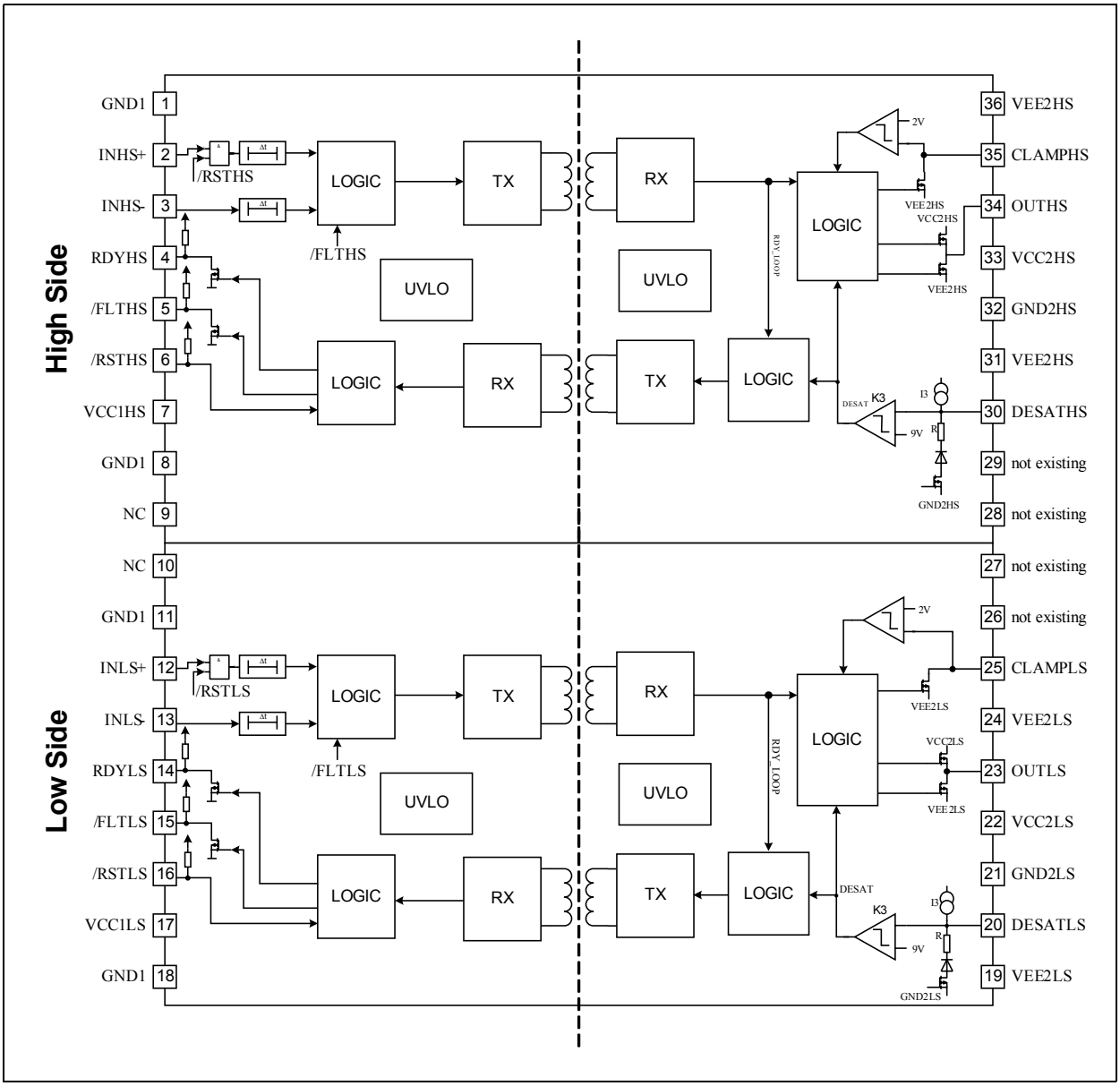

Figure 1: Block Diagram 2ED020I12FA

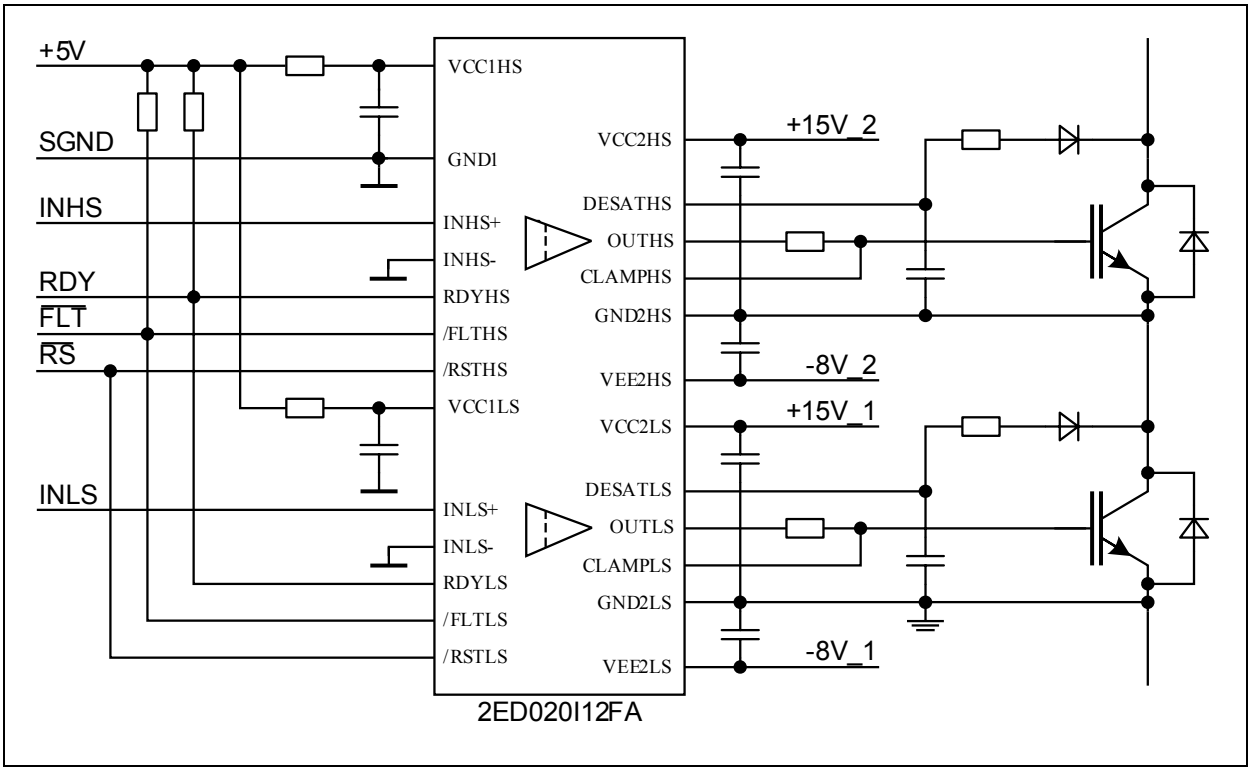

Figure 2: Application Example

2 Functional Description

2.1 Introduction

The 2ED020I12FA is an advanced IGBT dual gate driver that can be also used for driving power MOS devices. Control and protection functions are included to make possible the design of high reliability systems.

The device consists of two galvanic separated driver. The input can be directly connected to a standard 5V DSP or microcontroller with CMOS in/output and the output driver are connected to the high side and low side switch.

The rail-to-rail driver outputs enables the user to provide easy clamping of the IGBTs gate voltage during short circuit of the IGBT. So an increase of short circuit current due to the feedback via the Miller capacitance can be avoided. Further, a rail-to-rail output reduces power dissipation.

The device also includes IGBT desaturation protection with FAULT status outputs.

Two READY status outputs reports if the device is supplied and operates correctly.

2.2 Internal Protection Features

2.2.1 Undervoltage Lockout (UVLO)

To ensure correct switching of IGBTs the device is equipped with undervoltage lockout for all driver outputs as well as for input section.

If the power supply voltage V_{VCC1xx} of the input section drops below V_{UVLOL1} a turn-off signal is sent to the output driver before power-down. The IGBT is switched off and the signals at INxx+ and INxx- are ignored as long as V_{VCC1xx} reaches the power-up voltage V_{UVLOH1} .

If the power supply voltage V_{VCC2xx} of the output driver goes down below V_{UVLOL2} the IGBT is switched off and signals from the input chip are ignored as long as V_{VCC2xx} reaches the power-up voltage V_{UVLOH2} . VEE2 is not monitored, otherwise negative supply voltage range from 0V to -12V would not be possible.

2.2.2 READY status output

The READY outputs shows the status of three internal protection features.

- UVLO of the input chip
- UVLO of the output chip after a short delay
- Internal signal transmission

It is not necessary to reset the READY signal since its state only depends on the status of the former protection signals.

2.2.3 Watchdog Timer

During normal operation the internal signal transmission is monitored by a watchdog timer. If the transmission fails for a given time, the IGBT is switched off and the READY output reports an internal error.

2.2.4 Active Shut-Down

The Active Shut-Down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply.

2.3 Non-Inverting and Inverting Inputs

There are two possible input modes to control the IGBT. At non-inverting mode INxx+ controls the driver output while INxx- is set to low. At inverting mode INxx- controls the driver output while INxx+ is set to high. A minimum input pulse width is defined to filter occasional glitches.

2.4 Driver Outputs

The output driver sections uses only MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the drivers supply is stable. Due to the low internal voltage drop, switching behaviour of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

2.5 External Protection Features

2.5.1 Desaturation Protection

A desaturation protection ensures the protection of the IGBT at short circuit. When the DESAT voltage goes up and reaches 9V, the output is driven low. Further, the FAULT output is activated. A programmable blanking time is used to allow enough time for IGBT saturation. Blanking time is provided by a highly precise internal current source and an external capacitor.

2.5.2 Short Circuit Clamping

During short circuit the IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to OUTxx limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10us may be fed back to the supply through one of this paths. If higher currents are expected or a tighter clamping is desired external Schottky diodes may be added.

2.6 RESET

The reset inputs have two functions.

Firstly, /RSTxx is in charge of setting back the FAULT output. If /RSTxx is low longer than a given time , /FLTxx will be reseted at the rising edge of /RSTxx; otherwise, it will remain unchanged. Moreover, it works as enable/shutdown of the input logic.

3 Pin Configuration and Functionality

3.1 Pin Configuration

Pin	Symbol	Function
1	GND1	Signal ground input side
2	INHS+	Non inverted driver input high side
3	INHS-	Inverted driver input high side
4	RDYHS	Ready output high side
5	/FLTHS	Inverted fault output high side
6	/RSTHS	Inverted reset input high side
7	VCC1HS	Positive power supply input high side
8	GND1	Signal ground input side
9	NC	Not used, internally connected to Pin 10
10	NC	Not used, internally connected to Pin 9
11	GND1	Signal ground input side
12	INLS+	Non inverted driver input low side
13	INLS-	Inverted driver input lowside
14	RDYLS	Ready output low side
15	/FLTLS	Inverted fault output low side
16	/RSTLS	Inverted reset input low side
17	VCC1LS	Positive power supply input low side
18	GND1LS	Signal ground input side
19	VEE2LS	Negative power supply low side driver
20	DESATLS	Desaturation protection low side driver
21	GND2LS	Signal ground low side driver
22	VCC2LS	Power supply low side driver
23	OUTLS	Output low side driver
24	VEE2LS	Negative power supply low side driver
25	CLAMPLS	Miller clamping low side driver
26		Pin not existing, cut out
27		Pin not existing, cut out
28		Pin not existing, cut out
29		Pin not existing, cut out
30	DESATHS	Desaturation protection high side driver
31	VEE2HS	Negative power supply high side driver
32	GND2HS	Signal ground high side driver
33	VCC2HS	Power supply high side driver
34	OUTHS	Output high side driver
35	CLAMPHS	Miller clamping high side driver
36	VEE2HS	Negative power supply high side driver

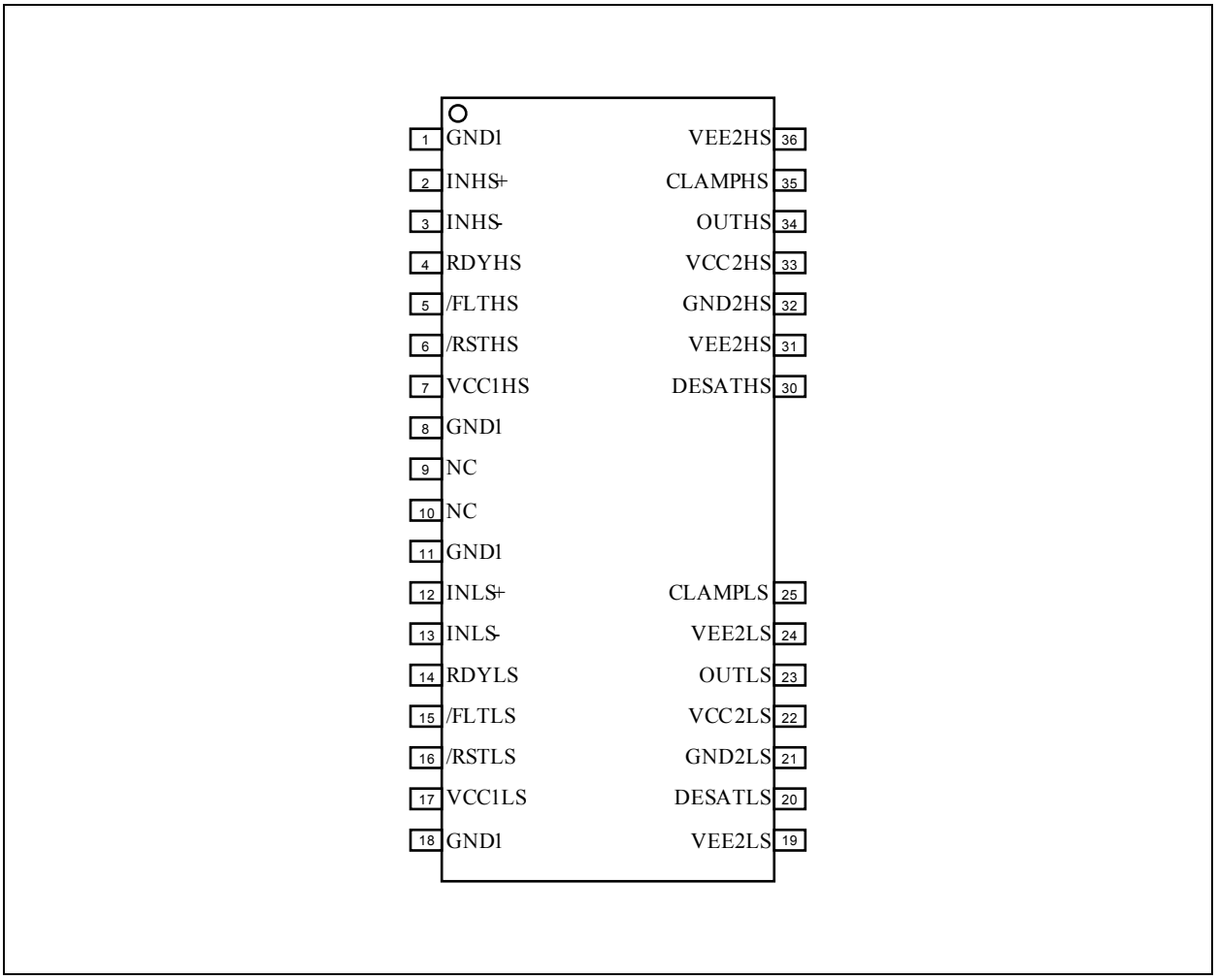

Figure 3: PG-DSO 36/32-1/32-1 (top view)

3.2 Pin Functionality

GND1

Common ground connection of the input side.

INHS+ Non-inverting driver input (High side)

INHS+ control signal for the driver output if INHS- is set to low. (The IGBT is on if INHS+ = high and INHS- = low)

A minimum pulse width is defined to make the IC robust against glitches at IN+. An internal Pull-Down-Resistor ensures IGBT Off-State.

INHS- Inverting driver input (High side)

INHS- control signal for driver output if INHS+ is set to high. (IGBT is on if INHS- = low and INHS+ = high)

A minimum pulse width is defined to make the IC robust against glitches at INHS-. An internal Pull-Up-Resistor ensures IGBT Off-State.

/RSTHS (Reset input High side)

Function 1: Enable/shutdown of the input chip. (The IGBT is off if /RSTHS = low). A minimum pulse width is defined to make the IC robust against glitches at INHS-.

Function 2: Resets the DESAT-FAULT-state of the chip if /RSTHS is low for a time T_{RST}. An internal Pull-Up-Resistor is used to ensure /FLTHS status output.

/FLTHS (Fault output High side)

Open-drain output to report a desaturation error of the IGBT (/FLTHS is low if desaturation occurs)

RDYHS (Ready status High side)

Open-drain output to report the correct operation of the device. (RDYHS = high if both chips are above the UVLO level and the internal chip transmission is faultless)

VCC1HS (High side)

5V power supply of the input chip

VEE2HS (High side)

Negative power supply pins of the output chip. If no negative supply voltage is available, both pins have to be connected to GND2HS.

DESATHS (Desaturation High side)

Monitoring of the IGBT saturation voltage (V_{CE}) to detect desaturation caused by short circuits. If OUT is high, V_{CE} is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an external capacitor.

CLAMPHS (Clamping)

Ties the gate voltage to ground after the IGBT has been switched off at a defined voltage to avoid a parasitic switch-on of the IGBT.During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2V (related to VEE2HS).

GND2HS (High side)

Reference ground of the output chip.

OUTHS (Driver output High side)

Output pin to drive an IGBT. The voltage is switched between VEE2HS and VCC2HS. In normal operating mode Vout is controlled by INHS+, INHS- and /RSTHS. During error mode (UVLO, internal error or DESATHS Vout is set to VEE2HS independent of the input control signals.

VCC2HS (High side)

Positive power supply pin of the output side.

GND1LS (Low side)

Ground connection of the input side.

INLS+ Non-inverting driver input (Low side)

INLS+ control signal for the driver output if INLS- is set to low. (The IGBT is on if INLS+ = high and INLS- = low)

A minimum pulse width is defined to make the IC robust against glitches at IN+. An internal Pull-Down-Resistor ensures IGBT Off-State.

INLS- Inverting driver input (Low side)

INLS- control signal for driver output if INLS+ is set to high. (IGBT is on if INLS- = low and INLS+ = high)

A minimum pulse width is defined to make the IC robust against glitches at INLS-. An internal Pull-Up-Resistor ensures IGBT Off-State.

/RSTLS (Reset input Low side)

Function 1: Enable/shutdown of the input chip. (The IGBT is off if /RSTLS = low). A minimum pulse width is defined to make the IC robust against glitches at INLS-.

Function 2: Resets the DESAT-FAULT-state of the chip if /RSTLS is low for a time T_{RST}. An internal Pull-Up-Resistor is used to ensure /FLTLS status output.

/FLTLS (Fault output Low side)

Open-drain output to report a desaturation error of the IGBT (/FLTLS is low if desaturation occurs)

RDYLS (Ready status Low side)

Open-drain output to report the correct operation of the device. (RDYLS = high if both chips are above the UVLO level and the internal chip transmission is faultless)

VCC1LS (Low side)

5V power supply of the input chip

VEE2LS (Low side)

Negative power supply pins of the output chip. If no negative supply voltage is available, both pins have to be connected to GND2LS.

DESATLS (Desaturation Low side)

Monitoring of the IGBT saturation voltage (V_{CE}) to detect desaturation caused by short circuits. If OUT is high, V_{CE} is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an external capacitor.

CLAMPLS (Clamping)

Ties the gate voltage to ground after the IGBT has been switched off at a defined voltage to avoid a parasitic switch-on of the IGBT.During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2V (related to VEE2LS).

GND2LS (Low side)

Reference ground of the output chip.

OUTLS (Driver output Low side)

Output pin to drive an IGBT. The voltage is switched between VEE2LS and VCC2LS. In normal operating mode Vout is controlled by INLS+, INLS- and /RSTLS. During error mode (UVLO, internal error or DESATLS Vout is set to VEE2LS independent of the input control signals.

VCC2LS (Low side)

Positive power supply pin of the output side.

4 Electrical Parameters

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1. The specification for all driver signals is valid for HS and LS with out special notic, e.g. IN+ covers INHS+ as well as INLS+. The signals from driver output side are measured with respect to their specific GND2HS or GND2LS.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Positive power supply output side	V_{VCC2}	-0.3	20	V	1)
Negative power supply output side	V_{VEE2}	-12	0.3	V	1)
Maximum power supply voltage output side (V_{VCC2}-V_{VEE2})	V_{max2}	—	28	V	
Gate driver output	V_{OUT}	V_{VEE2}-0.3	V_{max2}+0.3	V	
Gate driver high output maximum current	I_{OUT}		2.4	A	t = 2µs
Gate driver low output maximum current	I_{OUT}		2.4	A	t = 2µs
Maximum short circuit clamping time	t_{CLP}	—	10	us	$I_{CLAMP/OUT}$ = 500mA
Positive power supply input side	V_{VCC1}	-0.3	6.5	V	
Logic input voltages (IN+,IN-,$\overline{RST}$)	$V_{LogicIN}$	-0.3	6.5	V	
Opendrain Logic output voltage ($\overline{FLT}$)	$V_{\overline{FLT}}$	-0.3	6.5	V	
Opendrain Logic output voltage (RDY)	V_{RDY}	-0.3	6.5	V	
Opendrain Logic output current ($\overline{FAULT}$)	$I_{\overline{FLT}}$	—	10	mA	
Opendrain Logic output current (RDY)	I_{RDY}	—	10	mA	
Pin DESAT voltage	V_{DESAT}	-0.3	V_{VCC2} +0.3		1) V_{VEE2} = -8V
Junction temperature	T_J	-40	150	°C	
Storage temperature	T_S	-55	150	°C	
Power dissipation, per input part	$P_{D, IN}$	—	100	mW	2)@TA = 25°
Power dissipation, per output part	$P_{D, OUT}$	—	400	mW	2)@TA = 25°
Power dissipation, total	$P_{D, tot}$	—	1000	mW	2)@TA = 25°
Thermal resistance (Input part)	$R_{THJA,IN}$	—	375	K/W	2)@TA = 25°C, P_{D, IN_HS+LS} = 200mW, P_{D, OUT_HS+LS} = 800mW

Thermal resistance (Output part)	$R_{THJA,OUT}$	—	110	K/W	[2]@TA = 25°C, P_{D, IN_HS+LS} = 200mW, P_{D, OUT_HS+LS} = 800mW
ESD Capability	V_{ESD}	—	tbd	kV	Human Body Model[3]

1) With respect to GND2.

2) IC power dissipation is derated linearly at 12mW/°C above 65°C. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

3) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor).

4.2 Operating Parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1. The specification for all driver signals is valid for HS and LS with out special notic, e.g. IN+ covers INHS+ as well as INLS+. The signals from driver output side are measured with respect to their specific GND2HS or GND2LS

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Positive power supply output side	V_{VCC2}	13	20	V	1)
Negative power supply output side	V_{VEE2}	-12	0	V	1)
Maximum power supply voltage output side (V_{VCC2}-V_{VEE2})	V_{max2}	—	28	V	
Positive power supply input side	V_{VCC1}	4.5	5.5	V	
Logic input voltages (IN+,IN-,$\overline{RST}$)	$V_{LogicIN}$	-0.3	5.5	V	
Pin DESAT voltage	V_{DESAT}	-0.3	V_{VCC2}	V	1)
Ambient temperature	T_A	-40	125	°C	
Common mode transient immunity2)	$\|\Delta V_{ISO}/dt\|$	—	50	kV/µs	@ 500V

1) With respect to GND2.

2) The parameter is not subject to production test - verified by design/characterization

4.3 Recommended Operating Parameters

Note: Unless otherwise noted all parameters refer to GND1. The specification for all driver signals is valid for HS and LS with out special notic, e.g. IN+ covers INHS+ as well as INLS+. The signals from driver output side are measured with respect to their specific GND2HS or GND2LS

Parameter	Symbol	Values	Unit	Remarks
Positive power supply output side	V_{VCC2}	15	V	1)
Negative power supply output side	V_{VEE2}	-8	V	1)
Positive power supply input side	V_{VCC1}	5	V	

1) With respect to GND2.

4.4 Electrical Characteristics

Note: The electrical characteristics involve the spread of values for the supply voltages, load and junction temperatures given below. Typical values represent the median values, which are related to production processes at T = 25°C. Unless otherwise noted all voltages are given with respect to GND. The specification for all driver signals is valid for HS and LS with out special notic, e.g. IN+ covers INHS+ as well as INLS+. The signals from driver output side are measured with respect to their specific GND2HS or GND2LS

4.4.1 Voltage Supply.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
UVLO Threshold Input Chip	V_{UVLOH1}	—	4.1	4.3	V	
	V_{UVLOL1}	3.5	3.8	—	V	
UVLO Hysteresis Input Chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS1}	0.15	—	—	V	
UVLO Threshold Output Chip	V_{UVLOH2}	—	12.0	12.6	V	
	V_{UVLOL2}	10.4	11.0	—	V	
UVLO Hysteresis Output Chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS2}	0.7	0.9	—	V	
Quiescent Current Input Chip	I_{Q1}	—	7	9	mA	V_{VCC1} =5V IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High
Quiescent Current Output Chip	I_{Q2}	—	4	6	mA	V_{VCC2} =15V V_{VEE2} =-8V IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High

4.4.2 Logic Input and Output

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
IN+,IN-, $\overline{RST}$ Low Input Voltage	V_{IN+L}, V_{IN-L}, $V_{\overline{RST}L}$	—	—	1.5	V	
IN+,IN-, $\overline{RST}$ High Input Voltage	V_{IN+H}, V_{IN-H} $V_{\overline{RST}H}$	3.5	—	—	V	
IN-, $\overline{RST}$ Input Current	I_{IN-}, $I_{\overline{RST}}$	—	100	400	uA	V_{IN-}=GND1 $V_{\overline{RST}}$=GND1
IN+ Input Current	I_{IN+},	—	100	400	uA	V_{IN+}=VCC1
RDY,$\overline{FLT}$ Pull Up Current	I_{PRDY}, $I_{\overline{PFLT}}$	—	100	400	uA	V_{RDY}=GND1 $V_{\overline{FLT}}$=GND1
Input Pulse Suppression IN+, IN-	T_{MININ+}, T_{MININ-}	30	40	—	ns	
Input Pulse Suppression $\overline{RST}$ for ENABLE/SHUTDOWN	T_{MINRST}	30	40	—	ns	
Pulse Width $\overline{RST}$ for Reseting $\overline{FLT}$	T_{RST}	800	—	—	ns	

$\overline{\text{FLT}}$ Low Voltage	V_{FLTL}	—	—	300	mV	$I_{SINK(\overline{FLT})}$ = 5mA
RDY Low Voltage	V_{RDYL}	—	—	300	mV	$I_{SINK(RDY)}$ = 5mA

4.4.3 Gate Driver

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
High Level Output Voltage	V_{OUTH1}	V_{CC2}-1.2	V_{CC2}-0.8	—	V	I_{OUTH} = -20mA
	V_{OUTH2}	V_{CC2}-2.5	V_{CC2}-2	—	V	I_{OUTH} = -200mA
	V_{OUTH3}	V_{CC2}-9	V_{CC2}-5	—	V	I_{OUTH} = -1A
	V_{OUTH4}		V_{CC2}-10	—	V	I_{OUTH} = -2A
High Level Output Peak Current	I_{OUTH}	-1.5	-2	—	A	IN+ = High, IN- = Low; OUT = High
Low Level Output Voltage	V_{OUTL1}	—	V_{VEE2}+0.04	V_{VEE2}+0.09	V	I_{OUTL} = 20mA
	V_{OUTL2}	—	V_{VEE2}+0.3	V_{VEE2}+0.85	V	I_{OUTL} = 200mA
	V_{OUTL3}	—	V_{VEE2}+2.1	V_{VEE2}+5.0	V	I_{OUTL} = 1A
	V_{OUTL4}	—	V_{VEE2}+7	—	V	I_{OUTL} = 2A
Low Level Output Peak Current	I_{OUTL}	1,5	2	—	A	IN+ = Low, IN- = Low; OUT = Low, V_{VCC2} =15V, V_{VEE2} =-8V

4.4.4 Short Circuit Clamping

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Clamping voltage (OUT) (V_{OUT}-V_{VCC2})	V_{CLPout}	—	0.8	1.3	V	IN+=High, IN-=Low, OUT=High I_{OUT} = 500mA (pulse test,t_{CLPmax}=10us)

4.4.5 Dynamic Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Input IN+ to output propagation delay ON	T_{PDON}	150	170	190	ns	V_{VCC2} =15V,V_{VEE2} =-8V C_{LOAD}= 100pF V_{IN+}=50%, V_{OUT}=50% @ 25°C
Input IN+ to output propagation delay OFF	T_{PDOFF}	145	165	185	ns	
Input IN+ to output propagation delay distortion (T_{PDOFF} - T_{PDON})	T_{PDISTO}	-35	-5	25	ns	
Input IN+ to output propagation delay ON variation due to temp	T_{PDONt}	160	190	220	ns	V_{VCC2} =15V,V_{VEE2} =-8V C_{LOAD}= 100pF V_{IN+}=50%, V_{OUT}=50% @ 125°C
Input IN+ to output propagation delay OFF variation due to temp	T_{PDOFFt}	165	195	225	ns	
Input IN+ to output propagation delay distortion (T_{PDOFF} - T_{PDON})	$T_{PDISTOt}$	-25	5	35	ns	

Input IN+ to output propagation delay ON variation due to temp	T_{PDONt}	135	165	195	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 100pF V_{IN+}=50%, V_{OUT}=50% @ -40°C
Input IN+ to output propagation delay OFF variation due to temp	T_{PDOFFt}	120	150	180	ns	
Input IN+ to output propagation delay distortion (T_{PDOFF} - T_{PDON})	$T_{PDISTOt}$	-45	-15	15	ns	
Input IN- to output propagation delay ON	T_{PDON}	135	155	750	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 100pF V_{IN+}=50%, V_{OUT}=50% @ 25°C
Input IN- to output propagation delay OFF	T_{PDOFF}	145	165	185	ns	
Input IN- to output propagation delay distortion (T_{PDOFF} - T_{PDON})	T_{PDISTO}	-565	10	40	ns	
Input IN- to output propagation delay ON variation due to temp	T_{PDONt}	140	170	990	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 100pF V_{IN-}=50%, V_{OUT}=50% @ 125°C
Input IN- to output propagation delay OFF variation due to temp	T_{PDOFFt}	165	195	225	ns	
Input IN- to output propagation delay distortion (T_{PDOFF} - T_{PDON})	$T_{PDISTOt}$	-770	25	55	ns	
Input IN- to output propagation delay ON	T_{PDON}	120	150	990	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 100pF V_{IN-}=50%, V_{OUT}=50% @ -40°C
Input IN- to output propagation delay OFF	T_{PDOFF}	120	150	180	ns	
Input IN- to output propagation delay distortion (T_{PDOFF} - T_{PDON})	T_{PDISTO}	-810	0	30	ns	
Rise Time	T_{RISE}	10	30	60	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 1nF VL 10% ,VH 90%
		200	400	800	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 34nF VL 10% ,VH 90%
Fall Time	T_{FALL}	10	50	90	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 1nF VL 10% ,VH 90%
		200	350	600	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 34nF VL 10% ,VH 90%

4.4.6 Desaturation protection

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Blanking Capacitor Charge Current	I_{DESATC}	450	500	550	uA	V_{VCC2}=15V,V_{VEE2}=-8V V_{DESAT}=2V
Blanking Capacitor Discharge Current	I_{DESATD}	10	13	—	mA	V_{VCC2}=15V,V_{VEE2}=-8V V_{DESAT}=6V
Desaturation Reference Level	V_{DESAT}	8.3	9	9.5	V	V_{VCC2}=15V
Desaturation Filter Time	$T_{DESATleb}$	-	250	-	ns	V_{VCC2}=15V,V_{VEE2}=-8V V_{DESAT}=9V
Desaturation Sense to OUT Low Delay	$T_{DESATOUT}$	—	350	410	ns	V_{OUT}=90% C_{LOAD}= 1nF
Desaturation Sense to FLT Low Delay	$T_{DESATFLT}$	—		2.25	us	$V_{\overline{FLT}}$=10%; $I_{\overline{FLT}}$=5mA
Desaturation Low Voltage	V_{DESATL}	0.4	0.6	0.95	V	IN+=Low, IN-=Low, OUT=Low
Leading edge blanking	$T_{DESATleb}$	-	400	-	ns	not subject of production test

4.4.7 Active Shut Down

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Active Shut Down Voltage	V_{ACTSD} [1)]	—	—	4	V	I_{OUT}=-200mA, V_{CC2} open

1) With reference to VEE2

5 Insulation Characteristics

5.1 Complies with DIN EN 60747-5-2 (VDE 0884 Teil 2): 2003-01. Basic Insulation

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1 for rated mains voltage ≤ 150 V_{RMS} for rated mains voltage ≤ 300 V_{RMS} for rated mains voltage ≤ 600 V_{RMS}		 I-IV I-III I-II	
Climatic Classification		55/105/21	
Pollution Degree (EN 60664-1)		2	
Minimum External Clearance between input and driver section	CLR	8	mm
Minimum External Creepage between input and driver section	CPG	8	mm
Minimum External Clearance between HS- and LS-driver output		tbd	mm
Minimum External Creepage between HS- and LS-driver output		2.81	mm
Minimum Comparative Tracking Index	CTI	175	
Maximum Repetitive Insulation Voltage	V_{IORM}	1420	V_{PEAK}
Highest Allowable Overvoltage	V_{IOTM}	6000	V_{PEAK}
Maximum Surge Insulation Voltage	V_{IOSM}	6000	V

5.2 Complies with UL 1577

Description	Symbol	Characteristic	Unit
Insulation Withstand Voltage / 1min	V_{ISO}	3750	V_{rms}
Insulation Test Voltage / 1sec	V_{ISO}	4500	V_{rms}

5.3 Reliability

For Qualification Report please contact your local Infineon Technologies office.

6 Timing Diagramms

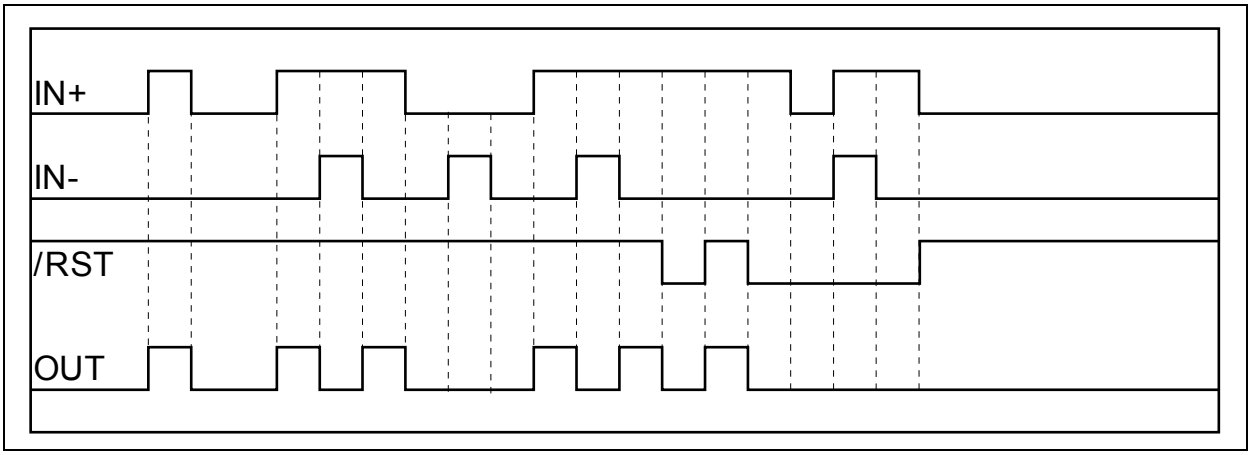

Figure 4: Typical Switching Behavior

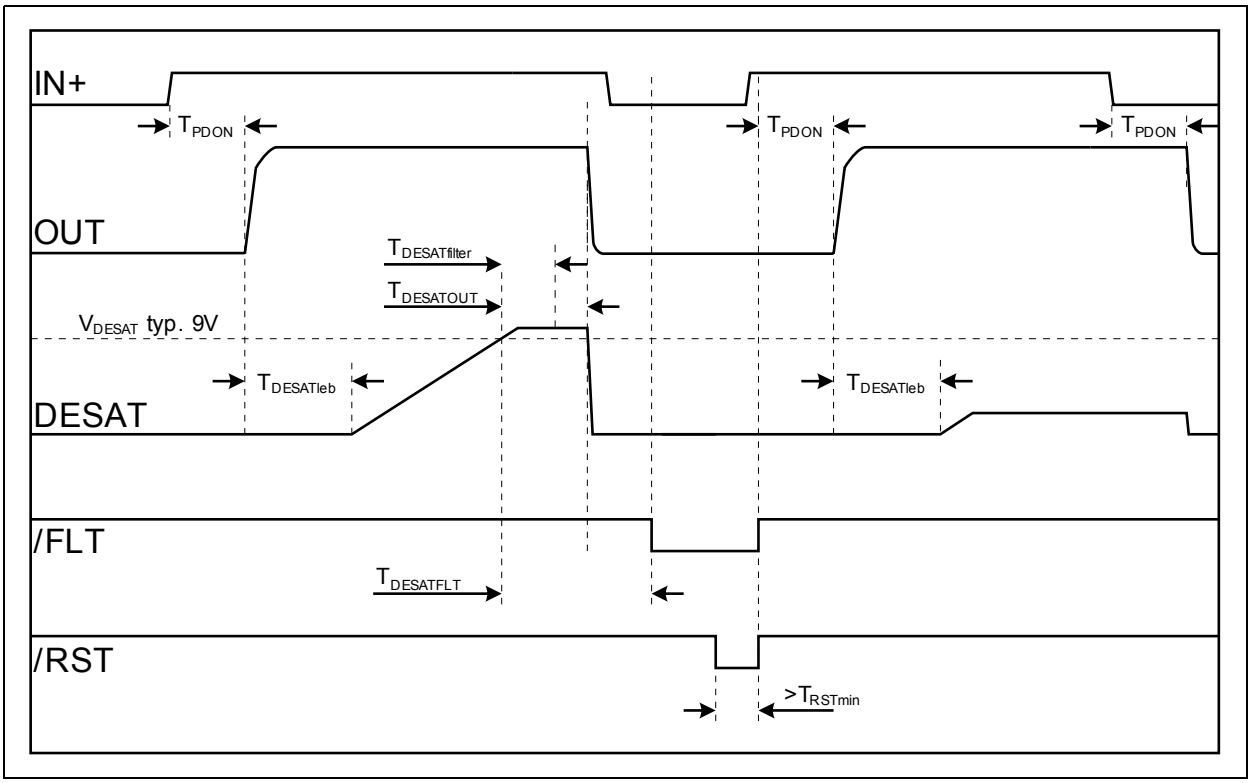

Figure 5: DESAT Switch-Off Behavior

7 Package Outlines

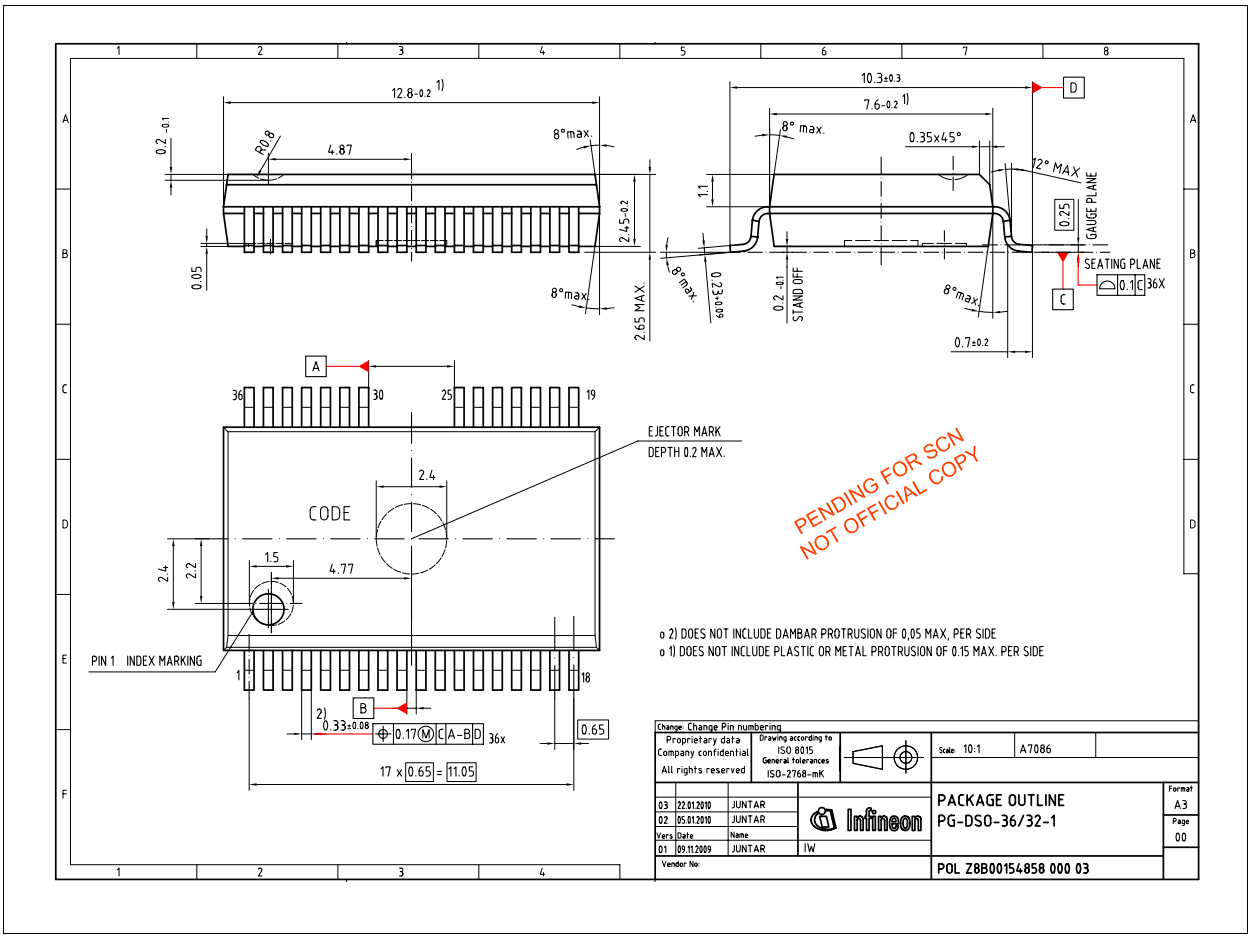

Figure 6: PG-DSO 36/32-1

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