National Semiconductor

November 1999

MAX660
Switched Capacitor Voltage Converter

General Description

The MAX660 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.5V to 5.5V to the corresponding negative voltage. The MAX660 uses two low cost capacitors to provide 100 mA of output current without the cost, size, and EMI related to inductor based converters. With an operating current of only 120 µA and operating efficiency greater than 90% at most loads, the MAX660 provides ideal performance for battery powered systems. The MAX660 may also be used as a positive voltage doubler.

The oscillator frequency can be lowered by adding an external capacitor to the OSC pin. Also, the OSC pin may be used to drive the MAX660 with an external clock. A frequency control (FC) pin selects the oscillator frequency of 10 kHz or 80 kHz.

Features

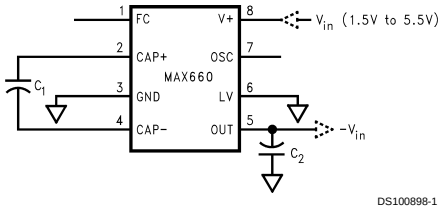
- Inverts or doubles input supply voltage
- Narrow SO-8 Package
- 6.5Ω typical output resistance
- 88% typical conversion efficiency at 100 mA
- Selectable oscillator frequency: 10 kHz/80 kHz

Applications

- Laptop computers
- Cellular phones
- Medical instruments
- Operational amplifier power supplies
- Interface power supplies
- Handheld instruments

Typical Application Circuits

Voltage Inverter



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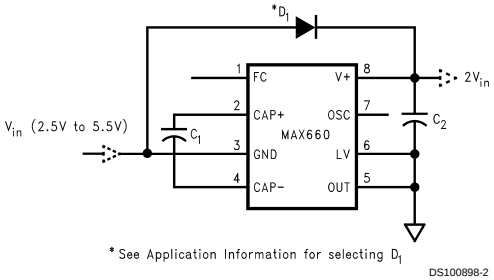
Positive Voltage Doubler



* See Application Information for selecting D_1

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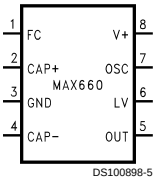
Connection Diagram

8-Lead SO



DS100898-5

Top View

Ordering Information

Order Number	Top Mark	Package	Supplied as
MAX660M	Date Code MAX660M	M08A	Rail (95 units/rail)
MAX660MX	Date Code MAX660M	M08A	Tape and Reel (2500 units/rail)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V+ to GND, or GND to OUT)	6V
LV	(OUT − 0.3V) to (GND + 3V)
FC, OSC	The least negative of (OUT − 0.3V) or (V+ − 6V) to (V+ + 0.3V)
V+ and OUT Continuous Output Current	120 mA
Output Short-Circuit Duration to GND (Note 2)	1 sec.
Power Dissipation (T_A = 25˚C) (Note 3)	735 mW
T_J Max (Note 3)	150˚C
θ_{JA} (Note 3)	170˚C/W
Operating Junction Temp. Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 10 seconds)	300˚C
ESD Rating	2 kV

Electrical Characteristics

Limits in standard typeface are for T_J = 25˚C, and limits in **boldface** type apply over the full operating temperature range. Unless otherwise specified: V+ = 5V, FC = Open, C_1 = C_2 = 150 µF. (Note 4)

Symbol	Parameter	Condition		Min	Typ	Max	Units
V+	Supply Voltage	R_L = 1k	Inverter, LV = Open (Note 5)	**3.5**		**5.5**	V
			Inverter, LV = GND	**1.5**		**5.5**	
			Doubler, LV = OUT	**2.5**		**5.5**	
I_Q	Supply Current	No Load	FC = Open		0.12	**0.5**	mA
		LV = Open	FC = V+		1	**3**	
I_L	Output Current	$T_A \leq +85˚C$, OUT ≤ −4V		**100**			mA
		$T_A > +85˚C$, OUT ≤ −3.8V		**100**			
R_{OUT}	Output Resistance (Note 6)	I_L = 100 mA	$T_A \leq +85˚C$		6.5	**10**	Ω
			$T_A > +85˚C$			**12**	
F_{OSC}	Oscillator Frequency	OSC = Open	FC = Open	**5**	10		kHz
			FC = V+	**40**	80		
I_{OSC}	OSC Input Current	FC = Open			±2		µA
		FC = V+			±16		
P_{EFF}	Power Efficiency	R_L (1k) between V^+ and OUT		**96**	98		%
		R_L (500Ω) between GND and OUT		**92**	96		
		I_L = 100 mA to GND			88		
V_{OEFF}	Voltage Conversion Efficiency	No Load		**99**	99.96		%

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above 85˚C, OUT must not be shorted to GND or V+, or device may be damaged.

Note 3: The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/\theta_{JA}$, where T_{JMax} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package.

Note 4: In the test circuit, capacitors C_1 and C_2 are 0.2Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.

Note 5: The minimum limit for this parameter is different from the limit of 3.0V for the industry-standard “660” product. For inverter operation with supply voltage below 3.5V, connect the LV pin to GND.

Note 6: Specified output resistance includes internal switch resistance and capacitor ESR.

Test Circuit

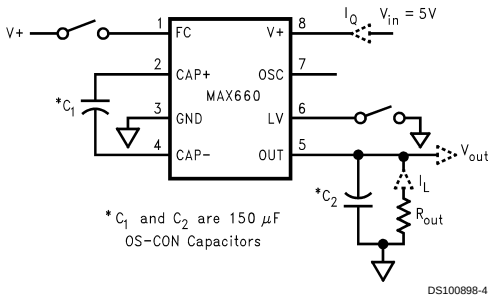
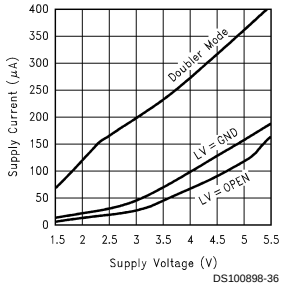


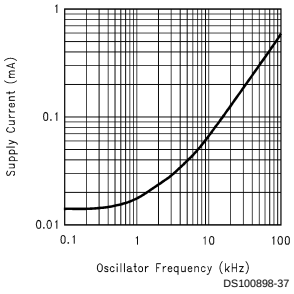
FIGURE 1. MAX660 Test Circuit

Typical Performance Characteristics (Circuit of *Figure 1*)

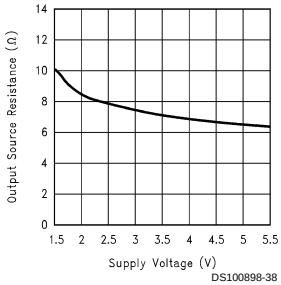
Supply Current vs Supply Voltage



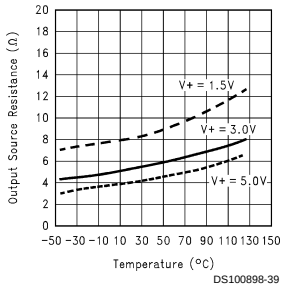
Supply Current vs Oscillator Frequency



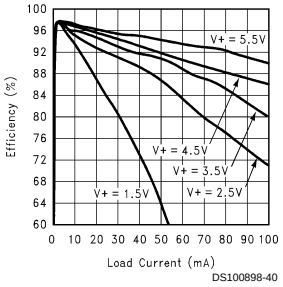
Output Source Resistance vs Supply Voltage



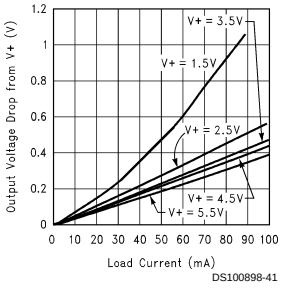
Output Source Resistance vs Temperature



Efficiency vs Load Load Current

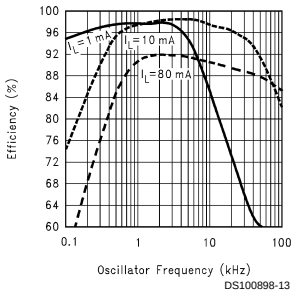


Output Voltage Drop vs Load Current



Typical Performance Characteristics (Circuit of *Figure 1*) (Continued)

Efficiency vs Oscillator Frequency



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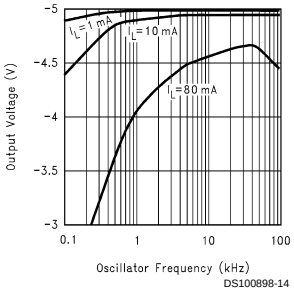
Output Voltage vs Oscillator Frequency



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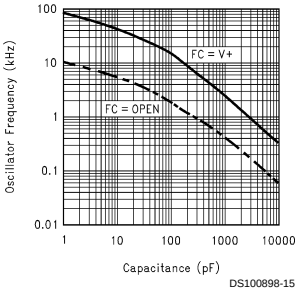
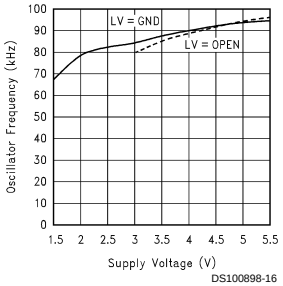
Oscillator Frequency vs External Capacitance



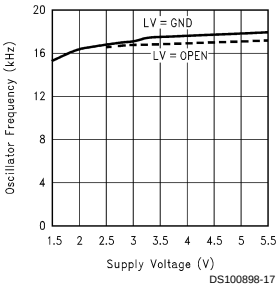
DS100898-15

Oscillator Frequency Supply Voltage (FC = V+)



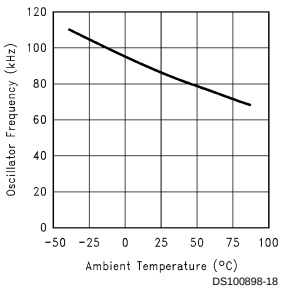
DS100898-16

Oscillator Frequency vs Supply Voltage (FC = Open)



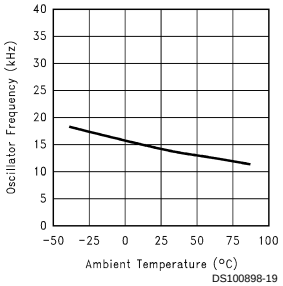
DS100898-17

Oscillator Frequency vs Temperature (FC = V+)



DS100898-18

Oscillator Frequency vs Temperature (FC = Open)



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Pin Description

Pin	Name	Function	
		Voltage Inverter	Voltage Doubler
1	FC	Frequency control for internal oscillator: FC = open, f_{OSC} = 10 kHz (typ); FC = V+, f_{OSC} = 80 kHz (typ); FC has no effect when OSC pin is driven externally.	Same as inverter.
2	CAP+	Connect this pin to the positive terminal of charge-pump capacitor.	Same as inverter.
3	GND	Power supply ground input.	Power supply positive voltage input.
4	CAP−	Connect this pin to the negative terminal of charge-pump capacitor.	Same as inverter.
5	OUT	Negative voltage output.	Power supply ground input.
6	LV	Low-voltage operation input. Tie LV to GND when input voltage is less than 3.5V. Above 3.5V, LV can be connected to GND or left open. When driving OSC with an external clock, LV must be connected to GND.	LV must be tied to OUT.
7	OSC	Oscillator control input. OSC is connected to an internal 15 pF capacitor. An external capacitor can be connected to slow the oscillator. Also, an external clock can be used to drive OSC.	Same as inverter except that OSC cannot be driven by an external clock.
8	V+	Power supply positive voltage input.	Positive voltage output.

Circuit Description

The MAX660 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. *Figure 2* illustrates the voltage conversion scheme. When S_1 and S_3 are closed, C_1 charges to the supply voltage V+. During this time interval switches S_2 and S_4 are open. In the second time interval, S_1 and S_3 are open and S_2 and S_4 are closed, C_1 is charging C_2. After a number of cycles, the voltage across C_2 will be pumped to V+. Since the anode of C_2 is connected to ground, the output at the cathode of C_2 equals −(V+) assuming no load on C_2, no loss in the switches, and no ESR in the capacitors. In reality, the charge transfer efficiency depends on the switching frequency, the on-resistance of the switches, and the ESR of the capacitors.

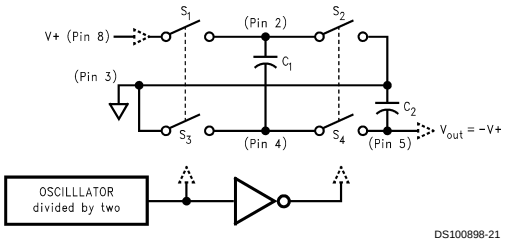


FIGURE 2. Voltage Inverting Principle

Application Information

SIMPLE NEGATIVE VOLTAGE CONVERTER

The main application of MAX660 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in the Typical Application Circuits. The range of the input supply voltage is 1.5V to 5.5V. For a supply voltage less than 3.5V, the LV pin must be connected to ground to bypass the internal regulator circuitry. This gives the best performance in low voltage applications. If the supply voltage is greater than 3.5V, LV may be connected to ground or left open. The choice of leaving LV open simplifies the direct substitution of the MAX660 for the LMC7660 Switched Capacitor Voltage Converter.

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistor. The voltage source equals −(V+). The output resistance R_{out} is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of C_1 and C_2. A good approximation is:

$$R_{out} \cong 2R_{SW} + \frac{2}{f_{osc} \times C_1} + 4\,ESR_{C1} + ESR_{C2}$$

where R_{SW} is the sum of the ON resistance of the internal MOS switches shown in *Figure 2*.

High value, low ESR capacitors will reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the $2/(f_{osc} \times C_1)$ term. Once this term is trivial compared with R_{SW} and ESRs, further increasing in oscillator frequency and capacitance will become ineffective.

The peak-to-peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor C_2:

Application Information (Continued)

$$V_{ripple} = \frac{I_L}{f_{osc} \times C_2} + 2 \times I_L \times ESR_{C2}$$

Again, using a low ESR capacitor will result in lower ripple.

POSITIVE VOLTAGE DOUBLER

The MAX660 can operate as a positive voltage doubler (as shown in the Typical Application Circuits). The doubling function is achieved by reversing some of the connections to the device. The input voltage is applied to the GND pin with an allowable voltage from 2.5V to 5.5V. The V+ pin is used as the output. The LV pin and OUT pin must be connected to ground. The OSC pin can not be driven by an external clock in this operation mode. The unloaded output voltage is twice of the input voltage and is not reduced by the diode D_1's forward drop.

The Schottky diode D_1 is only needed for start-up. The internal oscillator circuit uses the V+ pin and the LV pin (connected to ground in the voltage doubler circuit) as its power rails. Voltage across V+ and LV must be larger than 1.5V to insure the operation of the oscillator. During start-up, D_1 is used to charge up the voltage at V+ pin to start the oscillator; also, it protects the device from turning-on its own parasitic diode and potentially latching-up. Therefore, the Schottky diode D_1 should have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning-on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

SPLIT V+ IN HALF

Another interesting application shown in the Basic Application Circuits is using the MAX660 as a precision voltage divider. Since the off-voltage across each switch equals $V_{IN}/2$, the input voltage can be raised to +11V.

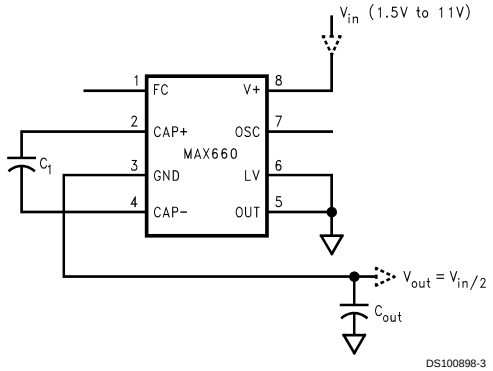


FIGURE 3. Splitting V_{IN} in Half

CHANGING OSCILLATOR FREQUENCY

The internal oscillator frequency can be selected using the Frequency Control (FC) pin. When FC is open, the oscillator frequency is 10 kHz; when FC is connected to V+, the frequency increases to 80 kHz. A higher oscillator frequency allows smaller capacitors to be used for equivalent output resistance and ripple, but increases the typical supply current from 0.12 mA to 1 mA.

The oscillator frequency can be lowered by adding an external capacitor between OSC and GND. (See Typical Performance Characteristics.) Also, in the inverter mode, an external clock that swings within 100 mV of V+ and GND can be used to drive OSC. Any CMOS logic gate is suitable for driving OSC. LV must be grounded when driving OSC. The maximum external clock frequency is limited to 150 kHz.

The switching frequency of the converter (also called the charge pump frequency) is half of the oscillator frequency.

Note: OSC cannot be driven by an external clock in the voltage-doubling mode.

TABLE 1. MAX660 Oscillator Frequency Selection

FC	OSC	Oscillator
Open	Open	10 kHz
V+	Open	80 kHz
Open or V+	External Capacitor	See Typical Performance Characteristics
N/A	External Clock **(inverter mode only)**	External Clock Frequency

CAPACITOR SELECTION

As discussed in the *Simple Negative Voltage Converter* section, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_L^2 R_L}{I_L^2 R_L + I_L^2 R_{out} + I_Q(V+)}$$

Where $I_Q(V+)$ is the quiescent power loss of the IC device, and $I_L^2 R_{OUT}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

Since the switching current charging and discharging C_1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C_1 is multiplied by four in the output resistance. The output capacitor C_2 is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. However, the ESR of C_2 directly affects the output voltage ripple. Therefore, low ESR capacitors (*Table 2*) are recommended for both capacitors to maximize efficiency, reduce the output voltage drop and voltage ripple. For convenience, C_1 and C_2 are usually chosen to be the same.

The output resistance varies with the oscillator frequency and the capacitors. In *Figure 4*, the output resistance vs. oscillator frequency curves are drawn for three different tantalum capacitors. At very low frequency range, capacitance plays the most important role in determining the output resistance. Once the frequency is increased to some point (such as 20 kHz for the 150 µF capacitors), the output resistance is dominated by the ON resistance of the internal switches and the ESRs of the external capacitors. A low value, smaller size capacitor usually has a higher ESR compared with a bigger size capacitor of the same type. For lower ESR, use ceramic capacitors.

Application Information (Continued)

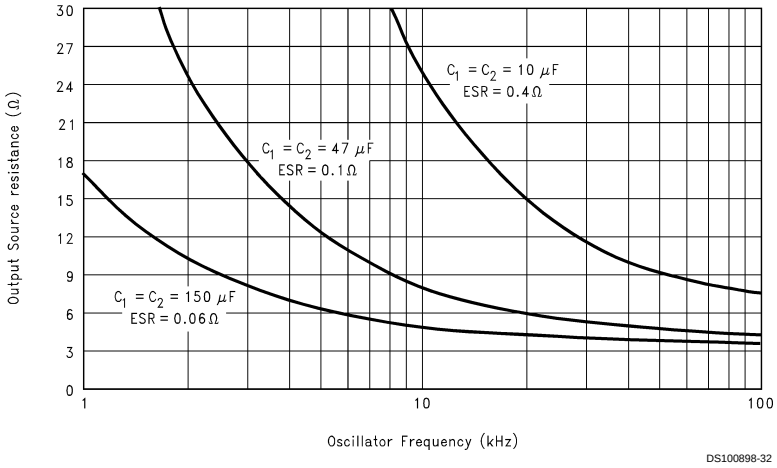


FIGURE 4. Output Source Resistance vs Oscillator Frequency

TABLE 2. Low ESR Capacitor Manufacturers

Manufacturer	Phone	FAX	Capacitor Type
Nichicon Corp.	(708)-843-7500	(708)-843-2798	PL, PF series, through-hole aluminum electrolytic
AVX Corp.	(803)-448-9411	(803)-448-1943	TPS series, surface-mount tantalum
Sprague	(207)-324-4140	(207)-324-7223	593D, 594D, 595D series, surface-mount tantalum
Sanyo	(619)-661-6835	(619)-661-1055	OS-CON series, through-hole aluminum electrolytic

Other Applications

PARALLELING DEVICES

Any number of MAX660s can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor C_1, while only one output capacitor C_{out} is needed as shown in *Figure 5*. The composite output resistance is:

$$R_{out} = \frac{R_{out}\ of\ each\ MAX660}{Number\ of\ Devices}$$

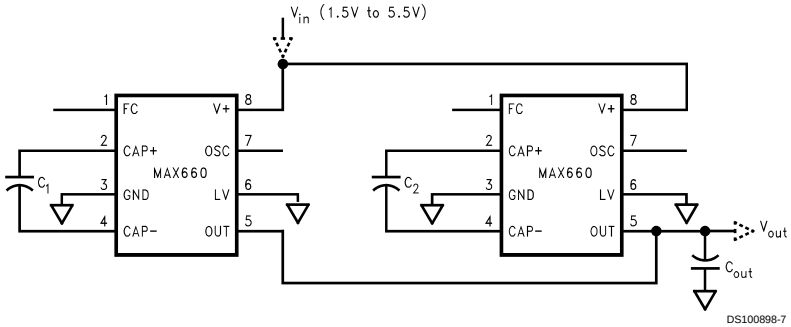


FIGURE 5. Lowering Output Resistance by Paralleling Devices

CASCADING DEVICES

Cascading the is an easy way to produce a greater negative voltage (as shown in *Figure 6*). If n is the integer representing the number of devices cascaded, the unloaded output voltage V_{out} is ($-nV_{in}$). The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = nR_{out\_1} + \frac{n}{2}R_{out\_2} + \ldots + R_{out\_n}$$

Other Applications (Continued)

A three-stage cascade circuit shown in *Figure 7* generates $-3V_{in}$, from V_{in}.

Cascading is also possible when devices are operating in doubling mode. In *Figure 8*, two devices are cascaded to generate $3V_{in}$.

An example of using the circuit in *Figure 7* or *Figure 8* is generating +15V or −15V from a +5V input.

Note that the number of n is practically limited since the increasing of n significantly reduces the efficiency and increases the output resistance and output voltage ripple.

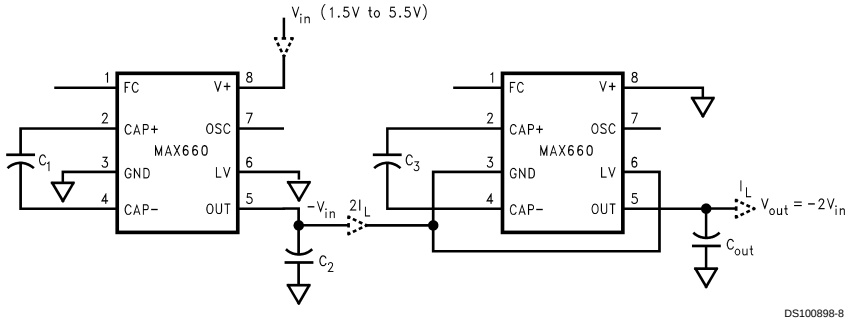


FIGURE 6. Increasing Output Voltage by Cascading Devices

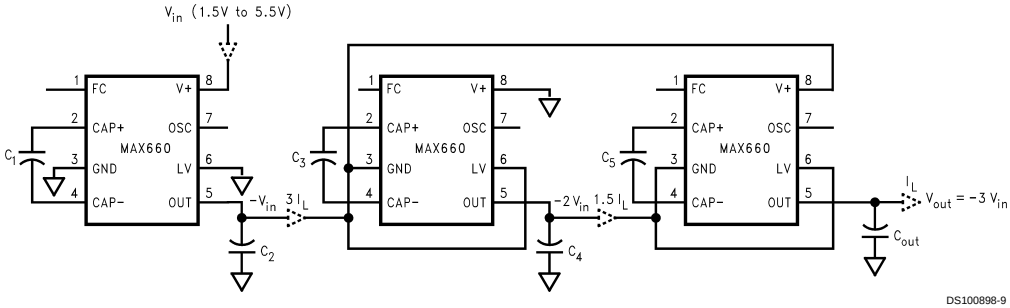


FIGURE 7. Generating $-3V_{in}$ from $+V_{in}$

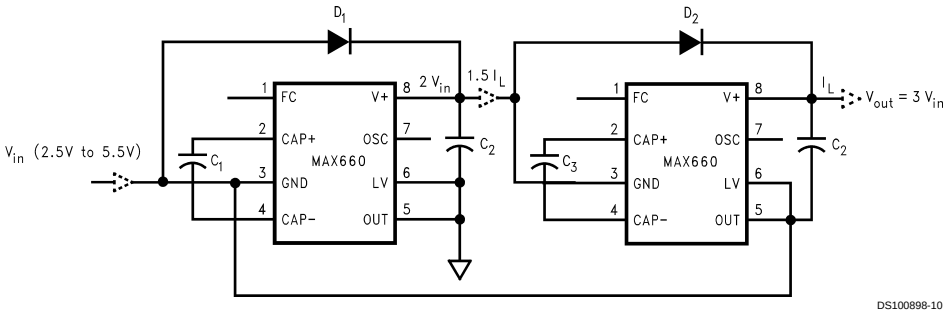


FIGURE 8. Generating $+3V_{in}$ from $+V_{in}$

REGULATING V_{out}

It is possible to regulate the output of the MAX660 by use of a low dropout regulator (such as LP2951). The whole converter is depicted in *Figure 9*. This converter can give a regulated output from −1.5V to −5.5V by choosing the proper resistor ratio:

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

where V_{ref} = 1.235V.

Other Applications (Continued)

The error flag on pin 5 of the LP2951 goes low when the regulated output at pin 4 drops by about 5%. The LP2951 can be shut-down by taking pin 3 high.

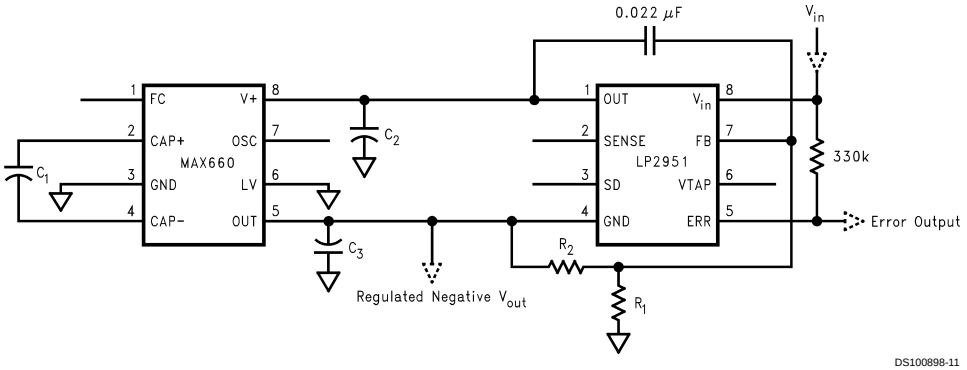


FIGURE 9. Combining MAX660 with LP2951 to Make a Negative Adjustable Regulator

Also, as shown in *Figure 10* by operating MAX660 in voltage doubling mode and adding a linear regulator (such as LP2981) at the output, we can get +5V output from an input as low as +3V.

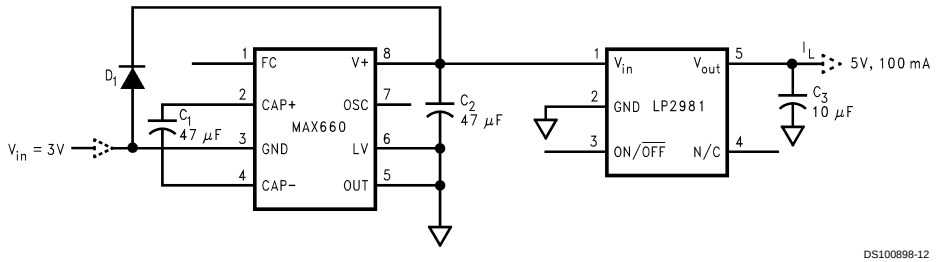


FIGURE 10. Generating +5V from +3V Input Voltage

Other Applications (Continued)

OTHER SWITCHED-CAPACITOR CONVERTERS

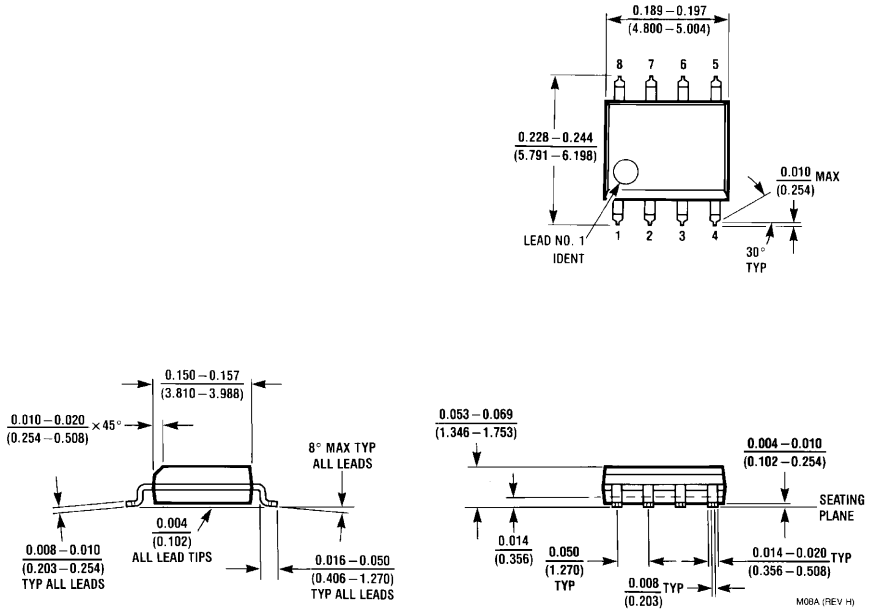
Please refer to *Table 3*, which shows National's Switched-Capacitor Converter products.

TABLE 3. Switched-Capacitor Converters

	LM2664	LM2665	LM3350	LM3351	MAX660
Package	SOT23-6	SOT23-6	Mini SO-8	Mini SO-8	SO-8
Supply Current (typ., mA)	0.22	0.22	3.75	1.1	0.12 at 10kHz, 1.0 at 80kHz
Output Ω (typ.)	12	12	4.2	4.2	6.5
Oscillator (kHz)	80	80	800	200	10, 80
Input (V)	1.8 to 5.5	1.8 to 5.5	2.5 to 6.25	2.5 to 6.25	1.8 to 5.5
Output Mode(s)	Invert	Double	3/2, 2/3	3/2, 2/3	Invert, Double

	LM2660	LM2661	LM2662	LM2663
Package	Mini SO-8, SO-8	Mini SO-8, SO-8	SO-8	SO-8
Supply Current (typ., mA)	0.12 at 10kHz, 1.0 at 80kHz	1.0	0.3 at 10kHz, 1.3 at 70kHz	1.3
Output Ω (typ.)	6.5	6.5	3.5	3.5
Oscillator (kHz)	10, 80	80	10, 70	70
Input (V)	1.8 to 5.5	1.8 to 5.5	1.8 to 5.5	1.8 to 5.5
Output Mode(s)	Invert, Double	Invert, Double	Invert, Double	Invert, Double

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead SO (M)
Order Number MAX660M
NS Package Number M08A

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