National Semiconductor

January 1999

LM2662/LM2663
Switched Capacitor Voltage Converter

General Description

The LM2662/LM2663 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.5V to 5.5V to the corresponding negative voltage. The LM2662/LM2663 uses two low cost capacitors to provide 200 mA of output current without the cost, size, and EMI related to inductor based converters. With an operating current of only 300 µA and operating efficiency greater than 90% at most loads, the LM2662/LM2663 provides ideal performance for battery powered systems. The LM2662/LM2663 may also be used as a positive voltage doubler.

The oscillator frequency can be lowered by adding an external capacitor to the OSC pin. Also, the OSC pin may be used to drive the LM2662/LM2663 with an external clock. For LM2662, a frequency control (FC) pin selects the oscillator frequency of 20 kHz or 150 kHz. For LM2663, an external shutdown (SD) pin replaces the FC pin. The SD pin can be used to disable the device and reduce the quiescent current to 10 µA. The oscillator frequency for LM2663 is 150 kHz.

Features

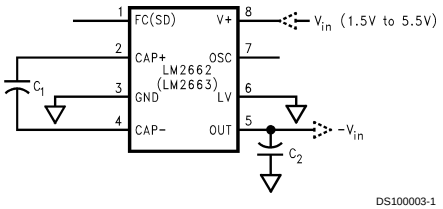
- Inverts or doubles input supply voltage
- Narrow SO-8 Package
- 3.5Ω typical output resistance
- 86% typical conversion efficiency at 200 mA
- (LM2662) selectable oscillator frequency: 20 kHz/150 kHz
- (LM2663) low current shutdown mode

Applications

- Laptop computers
- Cellular phones
- Medical instruments
- Operational amplifier power supplies
- Interface power supplies
- Handheld instruments

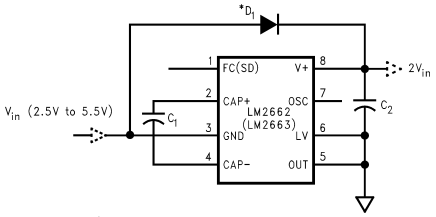
Basic Application Circuits

Voltage Inverter



DS100003-1

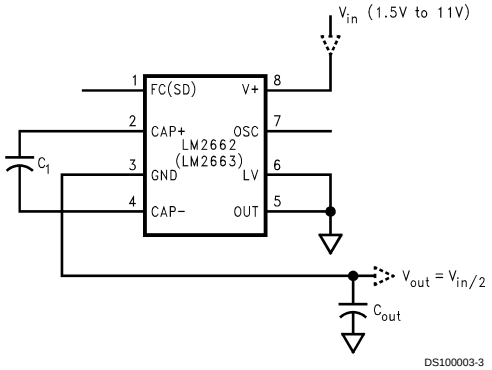
Positive Voltage Doubler



* See Application Information for selecting D_1

DS100003-2

Splitting V_{IN} in Half



DS100003-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V+ to GND, or GND to OUT)	6V
LV	(OUT − 0.3V) to (GND + 3V)
FC, OSC, SD	The least negative of (OUT − 0.3V) or (V+ − 6V) to (V+ + 0.3V)
V+ and OUT Continuous Output Current	250 mA
Output Short-Circuit Duration to GND (Note 2)	1 sec.
Power Dissipation (T_A = 25˚C) (Note 3)	735 mW
T_J Max (Note 3)	150˚C
θ_{JA} (Note 3)	170˚C/W
Operating Junction Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 10 seconds)	300˚C
ESD Rating	2 kV

Electrical Characteristics

Limits in standard typeface are for T_J = 25˚C, and limits in **boldface** type apply over the full operating temperature range. Unless otherwise specified: V+ = 5V, FC = Open, C_1 = C_2 = 47 µF.(Note 4)

Symbol	Parameter	Condition		Min	Typ	Max	Units
V+	Supply Voltage	R_L = 1k	Inverter, LV = Open	**3.5**		**5.5**	V
			Inverter, LV = GND	**1.5**		**5.5**	
			Doubler, LV = OUT	**2.5**		**5.5**	
I_Q	Supply Current	No Load, LV = Open	FC = V+ (LM2662), SD = Ground (LM2663)		1.3	**4**	mA
			FC = Open		0.3	**0.8**	
I_{SD}	Shutdown Supply Current (LM2663)				10		µA
V_{SD}	Shutdown Pin Input Voltage (LM2663)	Shutdown Mode		**2.0**	(Note 5)		V
		Normal Operation				**0.3**	
I_L	Output Current			**200**			mA
R_{OUT}	Output Resistance (Note 6)	I_L = 200 mA			3.5	**7**	Ω
f_{OSC}	Oscillator Frequency (Note 7)	OSC = Open	FC = Open	**7**	20		kHz
			FC = V+	**55**	150		
f_{SW}	Switching Frequency (Note 8)	OSC = Open	FC = Open	**3.5**	10		kHz
			FC = V+	**27.5**	75		
I_{OSC}	OSC Input Current	FC = Open			±2		µA
		FC = V+			±10		
P_{EFF}	Power Efficiency	R_L (500) between V^+ and OUT		**90**	96		%
		I_L = 200 mA to GND			86		
V_{OEFF}	Voltage Conversion Efficiency	No Load		**99**	99.96		%

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above 85˚C, OUT must not be shorted to GND or V+, or device may be damaged.

Note 3: The maximum allowable power dissipation is calculated by using $P_{DMax} = (T_{JMax} - T_A)/\theta_{JA}$, where T_{JMax} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package.

Note 4: In the test circuit, capacitors C_1 and C_2 are 47 µF, 0.2Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.

Note 5: In doubling mode, when $V_{out} > 5V$, minimum input high for shutdown equals $V_{out} - 3V$.

Note 6: Specified output resistance includes internal switch resistance and capacitor ESR.

Note 7: For LM2663, the oscillator frequency is 150 kHz.

Note 8: The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$.

Test Circuits

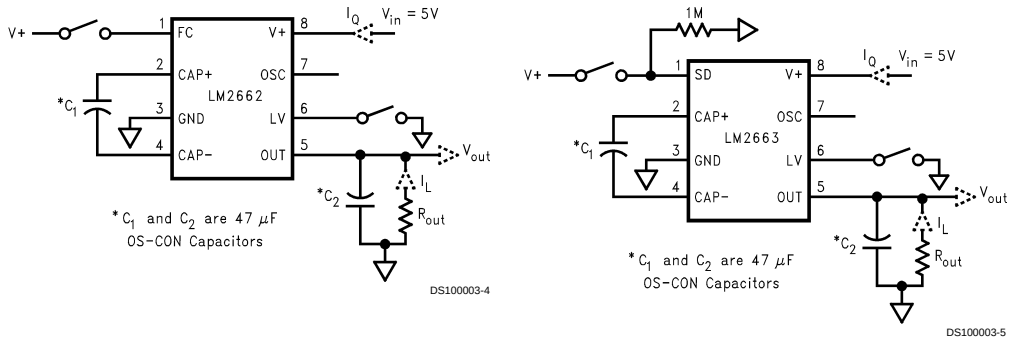
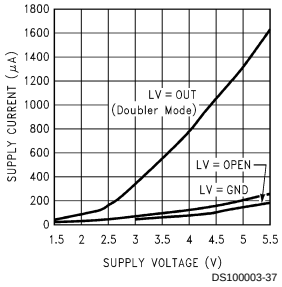


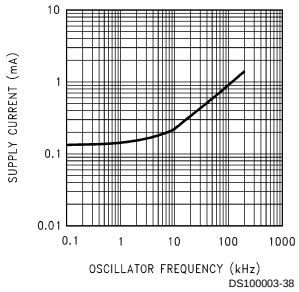
FIGURE 1. LM2662 and LM2663 Test Circuits

Typical Performance Characteristics (Circuit of *Figure 1*)

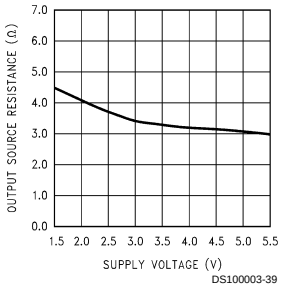
Supply Current vs Supply Voltage



Supply Current vs Oscillator Frequency

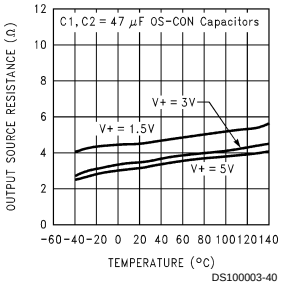


Output Source Resistance vs Supply Voltage



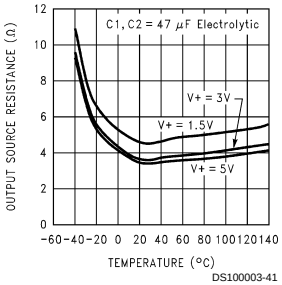
Typical Performance Characteristics (Circuit of *Figure 1*) (Continued)

Output Source Resistance vs Temperature



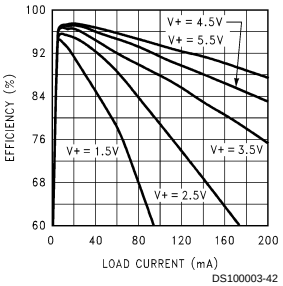
DS100003-40

Output Source Resistance vs Temperature



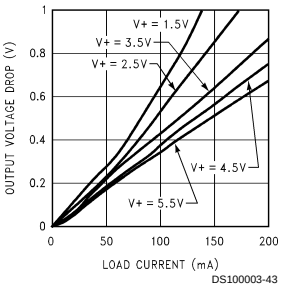
DS100003-41

Efficiency vs Load Current



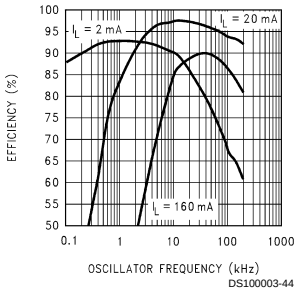
DS100003-42

Output Voltage Drop vs Load Current



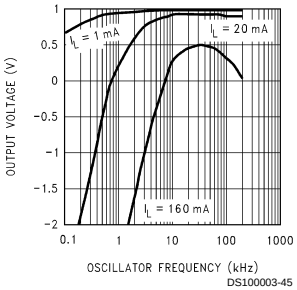
DS100003-43

Efficiency vs Oscillator Frequency



DS100003-44

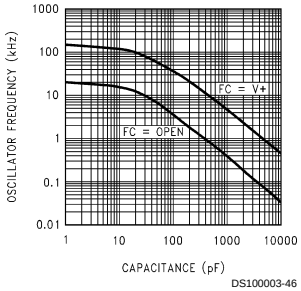
Output Voltage vs Oscillator Frequency



DS100003-45

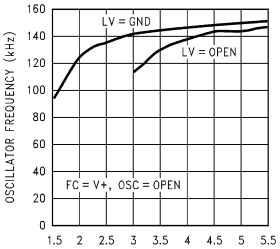
Typical Performance Characteristics (Circuit of *Figure 1*) (Continued)

Oscillator Frequency vs External Capacitance



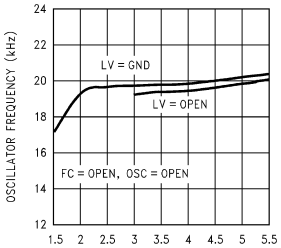
DS100003-46

Oscillator Frequency vs Supply Voltage



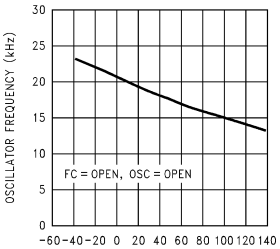
DS100003-47

Oscillator Frequency vs Supply Voltage



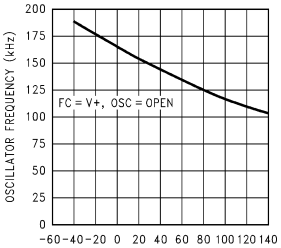
DS100003-48

Oscillator Frequency vs Temperature



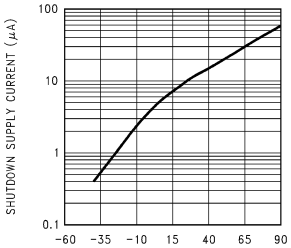
DS100003-49

Oscillator Frequency vs Temperature



DS100003-50

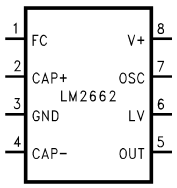
Shutdown Supply Current vs Temperature (LM2663 Only)



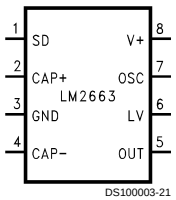
DS100003-51

Connection Diagrams

8-Lead SO (M)



DS100003-20



DS100003-21

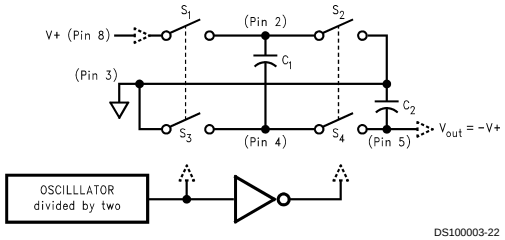
Top View
Order Number LM2662M, LM2663M
See NS Package Number M08A

Pin Description

Pin	Name	Function	
		Voltage Inverter	**Voltage Doubler**
1	FC (LM2662)	Frequency control for internal oscillator: FC = open, f_{OSC} = 20 kHz (typ); FC = V+, f_{OSC} = 150 kHz (typ); FC has no effect when OSC pin is driven externally.	Same as inverter.
1	SD (LM2663)	Shutdown control pin, tie this pin to the ground in normal operation.	Same as inverter.
2	CAP+	Connect this pin to the positive terminal of charge-pump capacitor.	Same as inverter.
3	GND	Power supply ground input.	Power supply positive voltage input.
4	CAP−	Connect this pin to the negative terminal of charge-pump capacitor.	Same as inverter.
5	OUT	Negative voltage output.	Power supply ground input.
6	LV	Low-voltage operation input. Tie LV to GND when input voltage is less than 3.5V. Above 3.5V, LV can be connected to GND or left open. When driving OSC with an external clock, LV must be connected to GND.	LV must be tied to OUT.
7	OSC	Oscillator control input. OSC is connected to an internal 15 pF capacitor. An external capacitor can be connected to slow the oscillator. Also, an external clock can be used to drive OSC.	Same as inverter except that OSC cannot be driven by an external clock.
8	V+	Power supply positive voltage input.	Positive voltage output.

Circuit Description

The LM2662/LM2663 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. *Figure 2* illustrates the voltage conversion scheme. When S_1 and S_3 are closed, C_1 charges to the supply voltage V+. During this time interval switches S_2 and S_4 are open. In the second time interval, S_1 and S_3 are open and S_2 and S_4 are closed, C_1 is charging C_2. After a number of cycles, the voltage across C_2 will be pumped to V+. Since the anode of C_2 is connected to ground, the output at the cathode of C_2 equals −(V+) assuming no load on C_2, no loss in the switches, and no ESR in the capacitors. In reality, the charge transfer efficiency depends on the switching frequency, the on-resistance of the switches, and the ESR of the capacitors.



DS100003-22

FIGURE 2. Voltage Inverting Principle

Application Information

SIMPLE NEGATIVE VOLTAGE CONVERTER

The main application of LM2662/LM2663 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in the Basic Application Circuits. The range of the input supply voltage is 1.5V to 5.5V. For a supply voltage less than 3.5V, the LV pin must be connected to ground to bypass the internal regulator circuitry. This gives the best performance in low voltage applications. If the supply voltage is greater than 3.5V, LV may be connected to ground or left open. The choice of leaving LV open simplifies the direct substitution of the LM2662/LM2663 for the LMC7660 Switched Capacitor Voltage Converter.

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistor. The voltage source equals −(V+). The output resistance R_{out} is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of C_1 and C_2. Since the switching current charging and discharging C_1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C_1 is multiplied by four in the output resistance. The output capacitor C_2 is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation is:

$$R_{out} \cong 2R_{SW} + \frac{2}{f_{osc} \times C_1} + 4\,ESR_{C1} + ESR_{C2}$$

where R_{SW} is the sum of the ON resistance of the internal MOS switches shown in *Figure 2*.

High value, low ESR capacitors will reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the $2/(f_{osc} \times C_1)$ term. Once this term is trivial compared with R_{SW} and ESRs, further increasing in oscillator frequency and capacitance will become ineffective.

The peak-to-peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor C_2:

$$V_{ripple} = \frac{I_L}{f_{osc} \times C_2} + 2 \times I_L \times ESR_{C2}$$

Again, using a low ESR capacitor will result in lower ripple.

POSITIVE VOLTAGE DOUBLER

The LM2662/LM2663 can operate as a positive voltage doubler (as shown in the Basic Application Circuits). The doubling function is achieved by reversing some of the connections to the device. The input voltage is applied to the GND pin with an allowable voltage from 2.5V to 5.5V. The V+ pin is used as the output. The LV pin and OUT pin must be connected to ground. The OSC pin can not be driven by an external clock in this operation mode. The unloaded output voltage is twice of the input voltage and is not reduced by the diode D_1's forward drop.

The Schottky diode D_1 is only needed for start-up. The internal oscillator circuit uses the V+ pin and the LV pin (connected to ground in the voltage doubler circuit) as its power rails. Voltage across V+ and LV must be larger than 1.5V to insure the operation of the oscillator. During start-up, D_1 is used to charge up the voltage at V+ pin to start the oscillator; also, it protects the device from turning-on its own parasitic diode and potentially latching-up. Therefore, the Schottky diode D_1 should have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning-on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

SPLIT V+ IN HALF

Another interesting application shown in the Basic Application Circuits is using the LM2662/LM2663 as a precision voltage divider. Since the off-voltage across each switch equals $V_{IN}/2$, the input voltage can be raised to +11V.

CHANGING OSCILLATOR FREQUENCY

For the LM2662, the internal oscillator frequency can be selected using the Frequency Control (FC) pin. When FC is open, the oscillator frequency is 20 kHz; when FC is connected to V+, the frequency increases to 150 kHz. A higher oscillator frequency allows smaller capacitors to be used for equivalent output resistance and ripple, but increases the typical supply current from 0.3 mA to 1.3 mA.

The oscillator frequency can be lowered by adding an external capacitor between OSC and GND (See typical performance characteristics). Also, in the inverter mode, an external clock that swings within 100 mV of V+ and GND can be used to drive OSC. Any CMOS logic gate is suitable for driving OSC. LV must be grounded when driving OSC. The maximum external clock frequency is limited to 150 kHz.

The switching frequency of the converter (also called the charge pump frequency) is half of the oscillator frequency.

Note: OSC cannot be driven by an external clock in the voltage-doubling mode.

TABLE 1. LM2662 Oscillator Frequency Selection

FC	OSC	Oscillator
Open	Open	20 kHz
V+	Open	150 kHz
Open or V+	External Capacitor	See Typical Performance Characteristics
N/A	External Clock **(inverter mode only)**	External Clock Frequency

TABLE 2. LM2663 Oscillator Frequency Selection

OSC	Oscillator
Open	150 kHz
External Capacitor	See Typical Performance Characteristics
External Clock **(inverter mode only)**	External Clock Frequency

SHUTDOWN MODE

For the LM2663, a shutdown (SD) pin is available to disable the device and reduce the quiescent current to 10 µA. Applying a voltage greater than 2V to the SD pin will bring the device into shutdown mode. While in normal operating mode, the SD pin is connected to ground.

Application Information (Continued)

CAPACITOR SELECTION

As discussed in the *Simple Negative Voltage Converter* section, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_L^2 R_L}{I_L^2 R_L + I_L^2 R_{out} + I_Q(V+)}$$

Where $I_Q(V+)$ is the quiescent power loss of the IC device, and $I_L^2 R_{OUT}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

Low ESR capacitors (*Table 3*) are recommended for both capacitors to maximize efficiency, reduce the output voltage drop and voltage ripple. For convenience, C_1 and C_2 are usually chosen to be the same.

The output resistance varies with the oscillator frequency and the capacitors. In *Figure 3*, the output resistance vs. oscillator frequency curves are drawn for four difference capacitor values. At very low frequency range, capacitance plays the most important role in determining the output resistance. Once the frequency is increased to some point (such as 100 kHz for the 47 µF capacitors), the output resistance is dominated by the ON resistance of the internal switches and the ESRs of the external capacitors. A low value, smaller size capacitor usually has a higher ESR compared with a bigger size capacitor of the same type. Ceramic capacitors can be chosen for their lower ESR. As shown in *Figure 3*, in higher frequency range, the output resistance using the 10 µF ceramic capacitors is close to these using higher value tantalum capacitors.

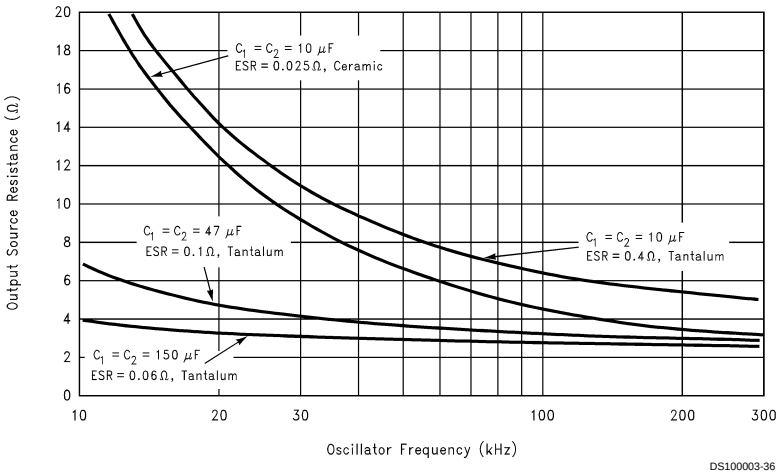


FIGURE 3. Output Source Resistance vs Oscillator Frequency

TABLE 3. Low ESR Capacitor Manufacturers

Manufacturer	Phone	Capacitor Type
Nichicon Corp.	(708)-843-7500	PL, PF series, through-hole aluminum electrolytic
AVX Corp.	(803)-448-9411	TPS series, surface-mount tantalum
Sprague	(207)-324-4140	593D, 594D, 595D series, surface-mount tantalum
Sanyo	(619)-661-6835	OS-CON series, through-hole aluminum electrolytic
Murata	(800)-831-9172	Ceramic chip capacitors
Taiyo Yuden	(800)-348-2496	Ceramic chip capacitors
Tokin	(408)-432-8020	Ceramic chip capacitors

Other Applications

PARALLELING DEVICES

Any number of LM2662s (or LM2663s) can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor C_1, while only one output capacitor C_{out} is needed as shown in *Figure 4*. The composite output resistance is:

$$R_{out} = \frac{R_{out} \text{ of each LM2662 (or LM2663)}}{\text{Number of Devices}}$$

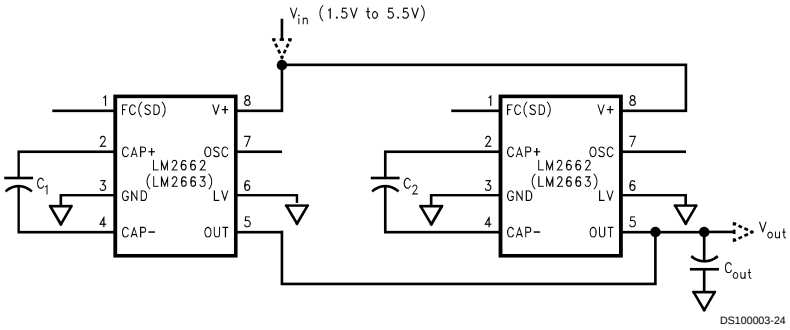


FIGURE 4. Lowering Output Resistance by Paralleling Devices

CASCADING DEVICES

Cascading the LM2662s (or LM2663s) is an easy way to produce a greater negative voltage (as shown in *Figure 5*). If n is the integer representing the number of devices cascaded, the unloaded output voltage V_{out} is ($-nV_{in}$). The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = nR_{out\_1} + \frac{n}{2}R_{out\_2} + \ldots + R_{out\_n}$$

A three-stage cascade circuit shown in *Figure 6* generates $-3V_{in}$, from V_{in}.

Cascading is also possible when devices are operating in doubling mode. In *Figure 7*, two devices are cascaded to generate $3V_{in}$.

An example of using the circuit in *Figure 6* or *Figure 7* is generating +15V or −15V from a +5V input.

Note that, the number of n is practically limited since the increasing of n significantly reduces the efficiency and increases the output resistance and output voltage ripple.

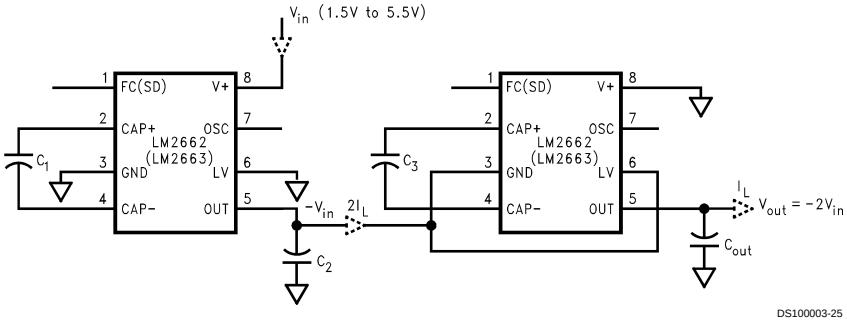


FIGURE 5. Increasing Output Voltage by Cascading Devices

Other Applications (Continued)

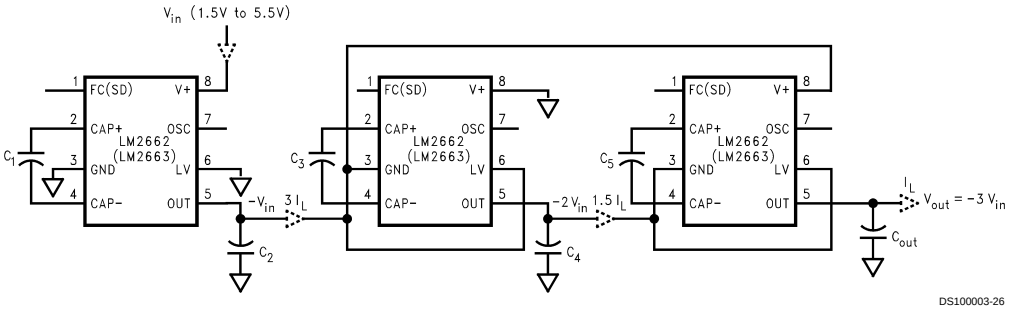


FIGURE 6. Generating $-3V_{in}$ from $+V_{in}$

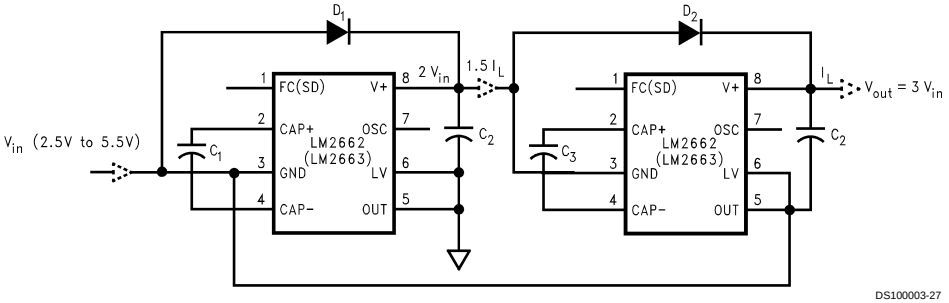


FIGURE 7. Generating $+3V_{in}$ from $+V_{in}$

REGULATING V_{out}

It is possible to regulate the output of the LM2662/LM2663 by use of a low dropout regulator (such as LP2986). The whole converter is depicted in *Figure 8*. This converter can give a regulated output from −1.5V to −5.5V by choosing the proper resistor ratio:

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{100k}\right)$$

where, $V_{ref} = 1.23V$

The error flag on pin 7 of the LP2986 goes low when the regulated output at pin 5 drops by about 5% below nominal. The LP2986 can be shutdown by taking pin 8 low. The less than 1 µA quiescent current in the shutdown mode is favorable for battery powered applications.

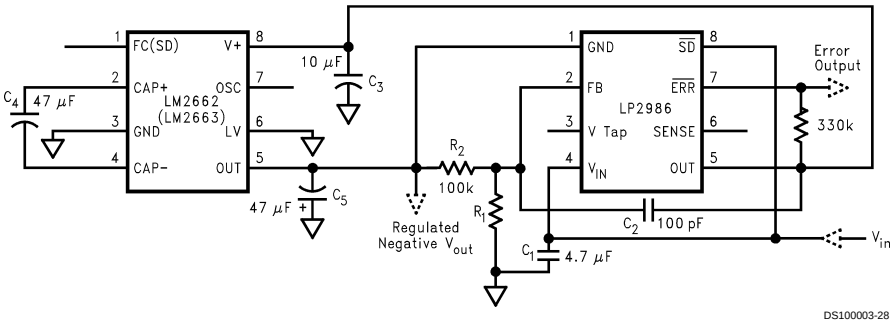


FIGURE 8. Combining LM2662/LM2663 with LP2986 to Make a Negative Adjustable Regulator

Other Applications (Continued)

Also, as shown in *Figure 9* by operating the LM2662/LM2663 in voltage doubling mode and adding a low dropout regulator (such as LP2986) at the output, we can get +5V output from an input as low as +3.3V.

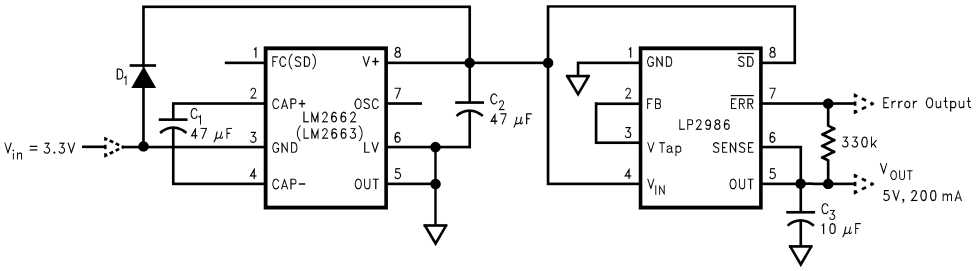
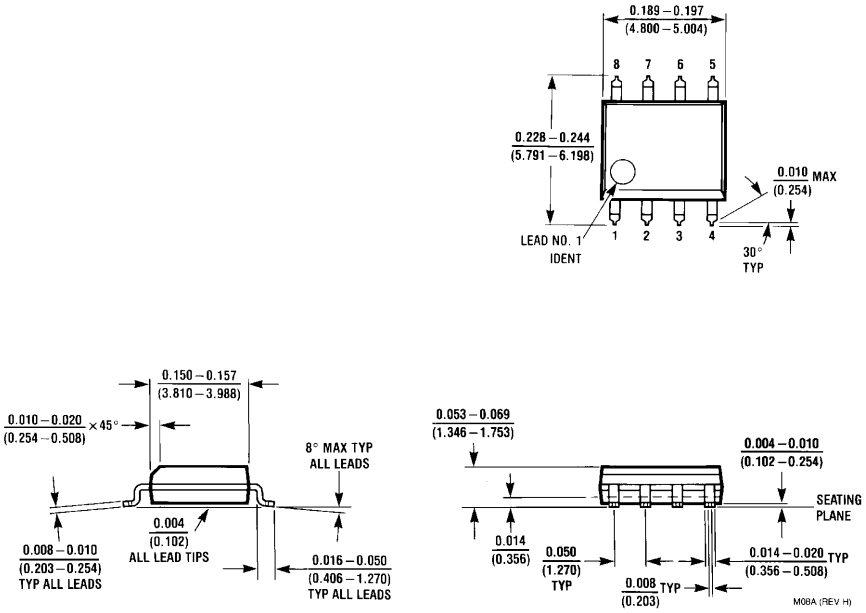


FIGURE 9. Generating +5V from +3.3V Input Voltage

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead SO (M)
Order Number LM2662M or LM2663M
NS Package Number M08A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507