The RF Line

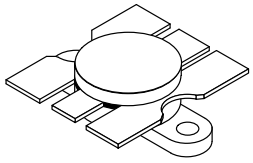
NPN Silicon RF Power Transistor

. . . designed for 12.5 Volt UHF large–signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics —
  Output Power = 15 Watts
  Minimum Gain = 7.8 dB
  Efficiency = 55%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Built–In Matching Network for Broadband Operation
- Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 16–Volt High Line and Overdrive
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

MRF641

**15 W, 470 MHz
CONTROLLED Q
RF POWER
TRANSISTOR
NPN SILICON**



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	43.7 0.25	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.0	°C/W

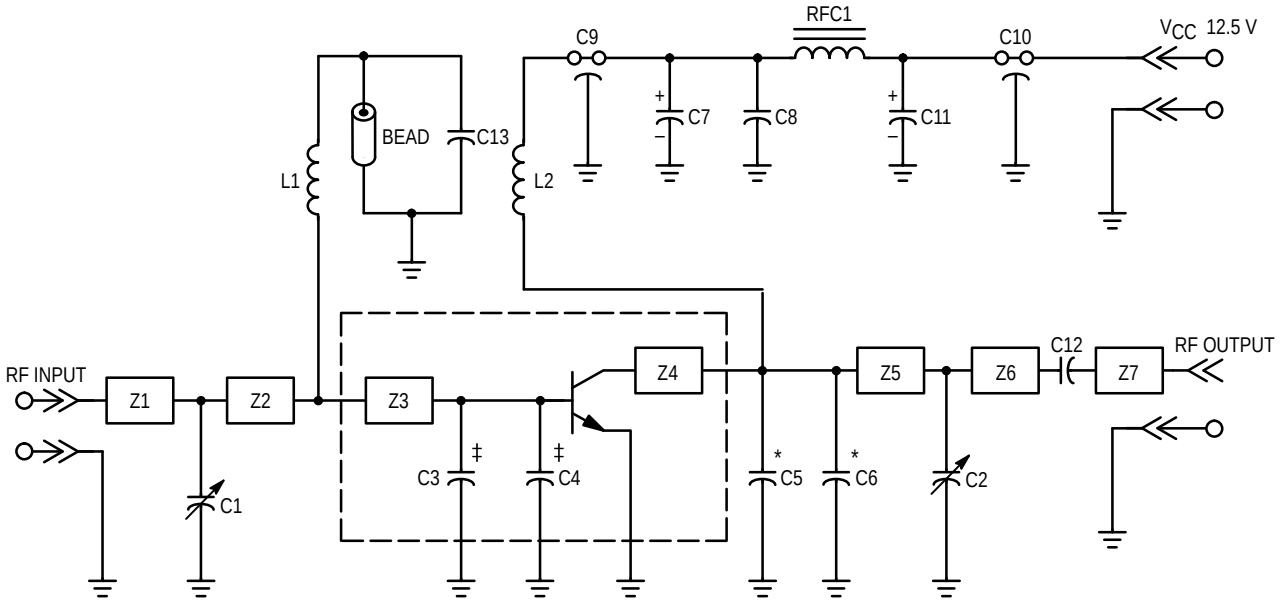
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5.0	mAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	30	70	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	40	60	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 470 MHz)	G_{pe}	7.8	8.5	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 470 MHz)	η	55	60	—	%
Output Mismatch Stress (V_{CC} = 16 Vdc, P_{in} = 3.0 W, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ	No Degradation in Output Power			



PARTS

Z1 — 1.225″ x 0.187″ Microstrip
Z2 — 0.884″ x 0.187″ Microstrip
Z3 — Capacitor Block (Base)
Z4 — Collector Block
Z5 — 1.1″ x 0.187″ Microstrip
Z6 — 0.433″ x 0.187″ Microstrip
Z7 — 0.4″ x 0.187″ Microstrip

Dotted Area — Capacitor Assembly

C1, C2 — 0.8–10 pF Johanson
C3, C4 — 24 pF Chip Caps 100 mils ATC
C5, C6 — 22 pF Chip Caps 100 mils ATC
C12 — 220 pF Chip Cap 100 mils ATC
C7, C11 — 1.0 μF Tantalum 35 Vdc
C9, C10 — 680 pF Feedthrough Allen–Bradley
C13 — 200 pF UNELCO
C8 — 0.1 μF, 50 V Erie Red Cap
RFC1 — VK 200 — 104B Ferrite Choke
L1 — 4 Turns 0.2″ Dia. #16 AWG
L2 — 9 Turns 0.15″ Dia. #16 AWG

Bead — Ferroxcube 56–590–65–35EB

NOTES

*C5, C6, are mounted as close to the capacitor assembly as possible.
‡‡C3, C4 are mounted in the capacitor assembly.
Board — 62.5 mil Glass Teflon, ε_r = 2.55.

Figure 1. Test Circuit Schematic

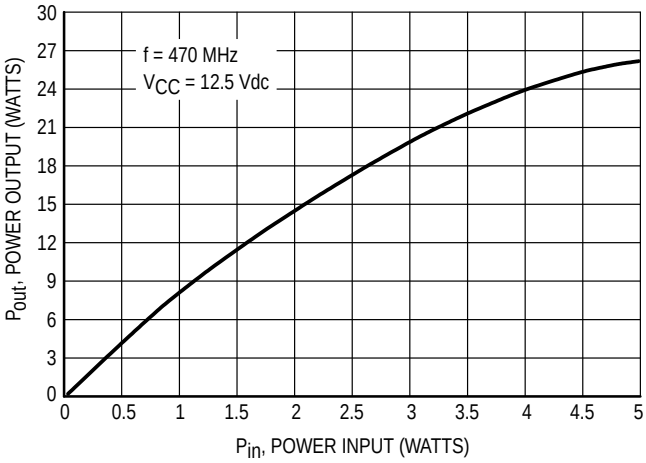


Figure 2. Power Output versus Power Input

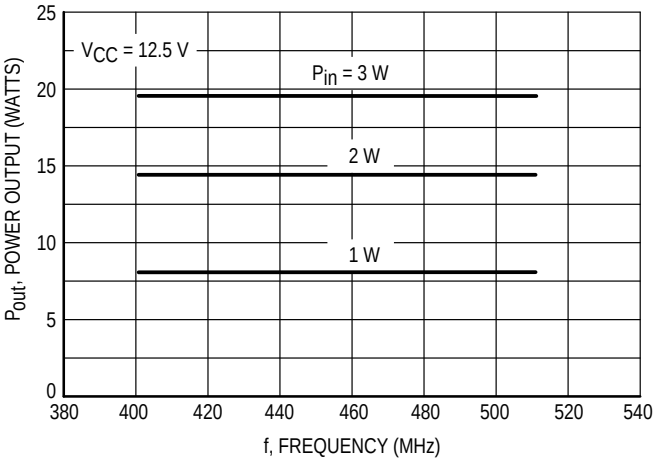


Figure 3. Power Output versus Frequency

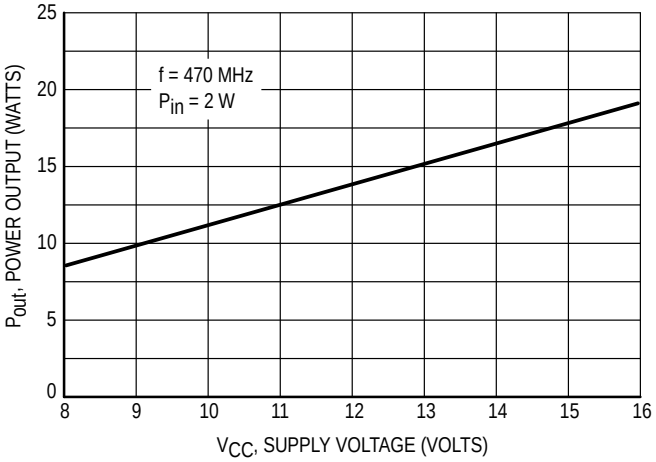


Figure 4. Power Output versus Supply Voltage

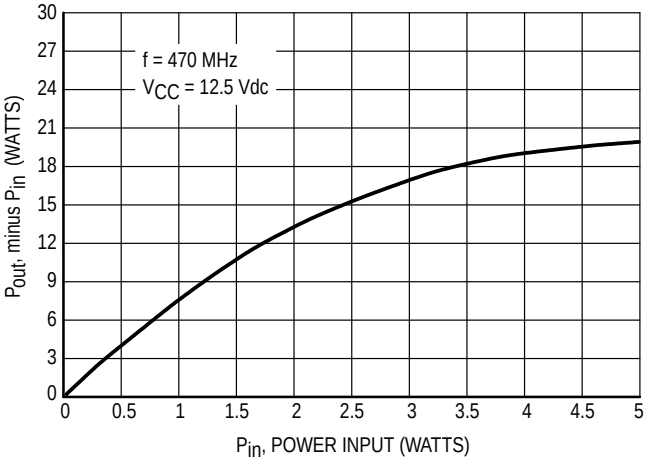
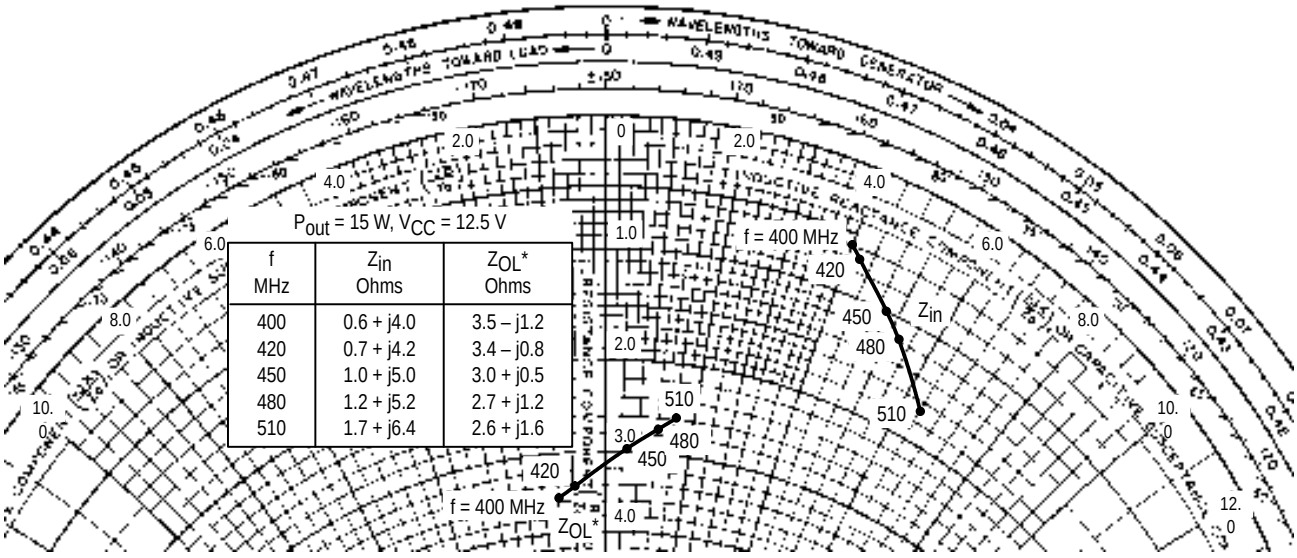


Figure 5. Power Saturation Profile

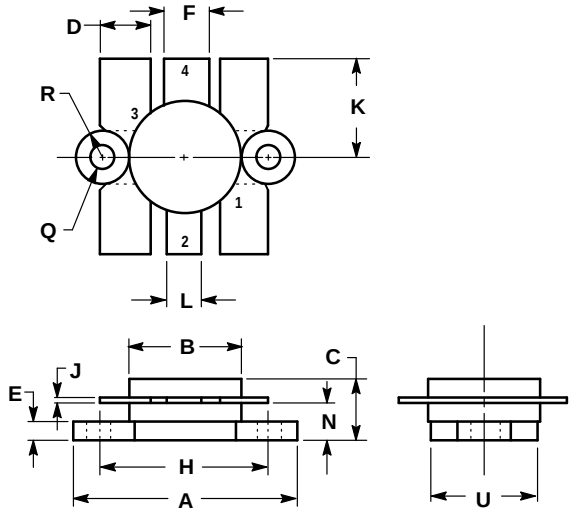


f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	0.6 + j4.0	3.5 – j1.2
420	0.7 + j4.2	3.4 – j0.8
450	1.0 + j5.0	3.0 + j0.5
480	1.2 + j5.2	2.7 + j1.2
510	1.7 + j6.4	2.6 + j1.6

Z_{OL}* = Conjugate of the load impedance into which the device output operates at a given power, η, and frequency.

Figure 6. Series Equivalent Input–Output Impedance

PACKAGE DIMENSIONS



NOTES:
1. FLANGE IS ISOLATED IN ALL STYLES.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	24.38	25.14	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.58	0.210	0.220
E	2.16	3.04	0.085	0.120
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.17	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.31	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130
U	11.94	12.57	0.470	0.495

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

CASE 316–01
ISSUE D

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.