FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21349-1E

ASSP

Single Serial Input PLL Frequency Synthesizer

On-Chip prescaler

MB15C03

■ DESCRIPTION

The Fujitsu MB15C03 is a serial input Phase Locked Loop (PLL) frequency synthesizer with a prescaler. A 64/65 division is available for the prescaler that enables pulse swallow operation.

This operates with a supply voltage of 1.0 V (min.).

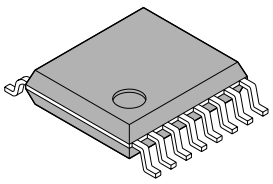
MB15C03 is suitable for mobile communications, such as paging systems.

■ FEATURES

- Frequency operation 90 MHz @V_{DD} = 1.0 to 1.5V
  120 MHz @V_{DD} = 1.2 to 1.5V
- Separate power supply : V_{DD} = 1.0 to 1.5 V (for overall system)
  V_P = 2.0V to 3.5V (for a charge pump)
- Power saving function
- Pulse swallow function: 64/65
- Serial input 14-bit programmable reference divider: R = 5 to 16,383
- Serial input 18-bit programmable divider consisting of:
  - Binary 6-bit swallow counter: 0 to 63
  - Binary 12-bit programmable counter: 5 to 4,095
- Wide operating temperature: Ta = –20 to +60°C
- Plastic 16-pin SSOP package (FPT-16P-M05)

■ PACKAGE

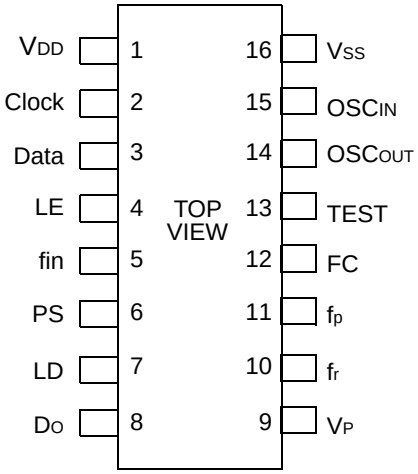
16-pin, plastic SSOP



(FPT-16P-M05)

This device contains circuitry to protect the inputs against damage due to high static voltages or electroc fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

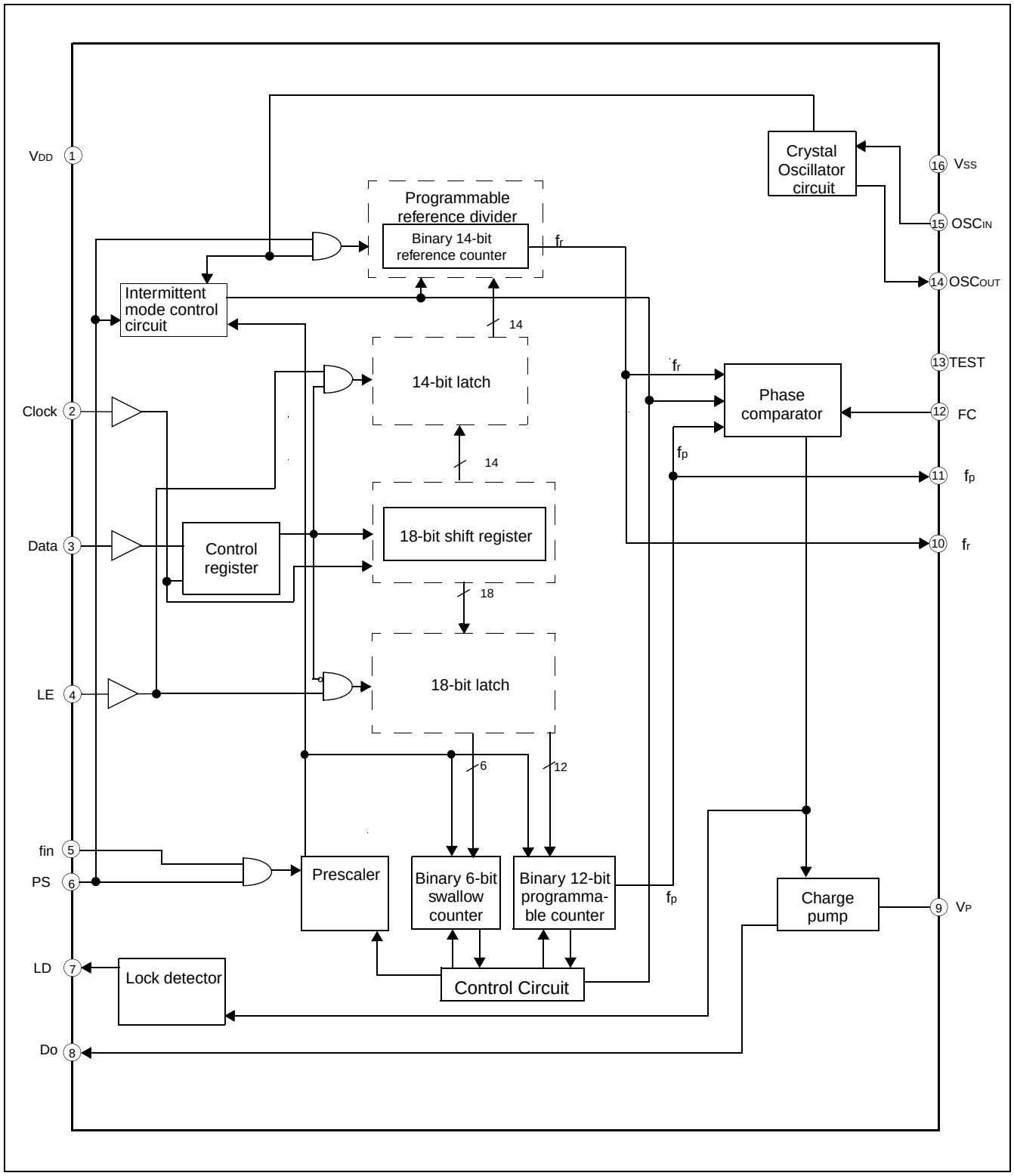
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O	System	Descriptions
1	V_{DD}	—	1 V	Power supply voltage
2	Clock	I	1 V	Clock input for the shift register. Data is shifted into the shift register on the rising edge of the clock.
3	Data	I	1 V	Serial data input using binary code.
4	LE	I	1 V	Load enable signal input When LE is high, the data in the shift register is transferred to a latch, according to the control bit in the serial data.
5	fin	I	1 V	Prescaler input. A bias circuit and amplifier are at input port. Connection with an external VCO should be done by AC coupling.
6	PS	I	1 V	Power saving mode control. This pin must be set at “L” at Power-ON. PS = “H” ; Normal mode PS = “L” ; Power saving mode
7	LD	O	1 V	Lock detector signal output. When a PLL is locking, LD outputs “H”. When a PLL is not locking, LD outputs “L”.
8	D_O	O	3 V	Charge pump output. Phase of the charge pump can be reversed by FC input. The D_O output may be inverted by FC input. The relationships between the programmable reference divider output(fr) and the programmable divider output(f_p) are shown below; $f_r > f_p$: “H” level (FC= “L”), “L” level (FC= “H”) $f_r = f_p$: High impedance $f_r < f_p$: “L” level (FC= “L”), “H” level (FC= “H”)
9	V_P	—	3 V	Power supply for the charge pump.
10	f_r	O	1 V	Programmable reference counter output (f_r) monitoring pin.
11	f_p	O	1 V	Programmable counter output (f_p) monitoring pin.
12	FC	I	1 V	Phase comparator input select pin.
13	TEST	I	1 V	Test mode select pin. (Pull down resistor) Setting this pin to “H”, test mode becomes available. Please set this pin to ground or open usually.
14	OSC_{OUT}	O	1 V	Oscillator output. Connection for an external crystal.
15	OSC_{IN}	I	1 V	Programmable reference divider input. Oscillator input. Clock can be input to OSC_{IN} from outside. In the case, please leave OSC_{OUT} pin open and make connection with OSC_{IN} as AC coupling.
16	V_{SS}	—	—	Ground.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remark
		Min.	Max.		
Power supply voltage	V_{DD}	GND –0.5	+2.0	V	
	V_P	GND –0.5	+5.0	V	
Input voltage	V_{IN}	GND –0.5	V_{DD} +0.5	V	
Output voltage	V_{OUT}	GND –0.5	V_{DD} +0.5	V	
	V_{OUTP}	GND –0.5	V_P +0.5	V	
Output current	I_{OUT}	–10	+10	mA	
Operating temperature	Ta	–20	+60	°C	
Storage temperature	T_{stg}	–40	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{DD}	1.0 1.2	— —	1.5 1.5	V	For 90 MHz For 120 MHz
	V_P	2.0	—	3.5	V	
Input voltage	V_{IN}	GND	—	V_{DD}	V	
Operating temperature	Ta	–20	—	+60	°C	

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

Handling Precautions

- This device should be transported and stores in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

(For 90 MHz: V_{DD} = 1.0 V to 1.5 V, V_P = 2.0 V to 3.5 V, Ta = –20°C to +60°C)
(For 120 MHz: V_{DD} = 1.2 V to 1.5 V, V_P = 2.0 V to 3.5 V, Ta = –20°C to +60°C)

Parameter			Symbol	Condition	Value			Unit
					Min.*3	Typ.*4	Max.	
Supply current		Active Mode	I_{DD}*1	(V_{DD} = 1.0 V/ 90 MHz) (V_{DD} = 1.2 V/ 120 MHz)	— —	0.5 0.7	1.0 1.4	mA
Power saving current		Power saving mode	I_{DDS}*2	(V_{DD} = 1.0 V) (V_{DD} = 1.2 V)	— —	10 15	100 120	µA
Operating frequency		fin	fin	(V_{DD} = 1.0 V to 1.5 V) (V_{DD} = 1.2 V to 1.5 V)	10 10	— —	90 120	MHz
		OSC_{IN}	f_{OSC}	—	5	–	20	MHz
Input sensitivity	fin		Vfin	—	–4.0	–	–	dBm
	OSC_{IN}		V_{OSC}	—	–4.0	–	–	dBm
Input voltage	Except for fin and OSC_{IN}	“H” level	V_{IH}	—	V_{DD} – 0.2	–	–	V
		“L” level	V_{IL}	—	–	–	0.2	
Input current	Except for fin, OSC_{IN} and TEST	“H” level	I_{IH}	V_{IN} = V_{DD}	–	–	+1.0	µA
		“L” level	I_{IL}	V_{IN} = GND	–1.0	–	–	
Output voltage	Except for OSC_{OUT}	“H” level	V_{OH}	I_{OH} = –0.3 mA	V_{DD} – 0.2	–	–	V
		“L” level	V_{OL}	I_{OL} = 0.3 mA	–	–	0.2	
	D_O	“H” level	V_{OHP}	I_{OHP} = –1.0 mA	V_P – 0.2	–	–	V
		“L” level	V_{OLP}	I_{OLP} = 1.0 mA	–	–	0.2	
High impedance cutoff current	D_O		I_{off}	V_{OUT} = GND to V_P	–100	–	100	nA

*1: Conditions; fin = 90MHz or 120MHz, 16.0MHz crystal between OSC_{IN} and OSC_{OUT}, Inputs except for fin, OSC_{IN} and TEST are grounded, Outputs are opened.

*2: Conditions; PS = Low, Inputs are grounded except for fin, OSC_{IN} and TEST. Outputs are opened.

*3: Condition; Ta = 25°C

*4: Condition; Ta = –20°C to +60°C

■ FUNCTIONAL DESCRIPTIONS

1. Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 12-bit programmable counter (5 to 4,095)
- A : Preset divide ratio of binary 6-bit swallow counter (0 to 63)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)
- M : Preset modulus of dual modulus prescaler (64)

2. Circuit Description

(1) Intermittent operation

The intermittent operation of the MB15C03 refers to the process of activating and deactivating its internal circuit thus saving power dissipation otherwise consumed by the circuit. If the circuit is simply restarted from the power saving state, however, the phase relation between the reference frequency (f_r) and the programmable frequency (f_p), which are the input to the phase comparator, is not stable even when they are of the same value. This may cause the phase comparator to generate an excessively large error signal, resulting in an out-of-synth lock frequency.

To preclude the occurrence of this problem, the MB15C03 has an intermittent mode control circuit which forces the frequencies into phase with each other when the IC is reactivated, thus minimizing the error signal and resultant lock frequency fluctuations. The intermittent mode control circuit is controlled by the PS pin. Setting pin PS high provides the normal operation mode and setting the pin low provides the power saving mode. The MB15C03 behavior in the active and power saving modes is summarized below.

Active mode (PS = “H”)
All MB15C03 circuits are active and provide the normal operation.

Power saving mode (PS = “L”)
The MB15C03 stops any circuits that consume power heavily as well as cause little inconvenience when deactivated and enters the low-power dissipation state. D_O and LD pins take the same state as when the PLL is locked. D_O pin becomes a high-impedance state.

Applying the intermittent operation by alternating the active and power saving modes, and also forcing the phases of f_r and f_p to synchronize when it switches from stand by to active modes, the MB15C03 can keep the power dissipation of its entire circuitry to the minimum.

(2) Programmable divider

The f_{VCO} input through fin pin is divided by the programmable divider and then output to the phase comparator as f_p. It consists of a dual modulus prescaler, a 6-bit binary swallow counter, a 12-bit binary programmable counter, and a controller which controls the divide ratio of the prescaler.

Divide ratio range:

Prescaler : M = 64, M + 1 = 65
Swallow counter : A = 0 to 63
Programmable counter : N = 5 to 4095

The MB15C03 uses the pulse swallow method; consequently, the divide rations of the swallow and programmable counters must satisfy the relationship N > A.

The total divide ratio of the programmable divider is calculated as follows:

Total divide ratio = (M+1) x A + M x (N-A) = M x N + A = 64 x N + A

When N is set within $5 \leq N \leq 63$, the possible divide ratio A of the swallow counter can take values $0 \leq A \leq N-1$ because N must be greater than A. For example, $0 \leq A \leq 19$ is allowed when N = 20 but $20 \leq A \leq 63$ is not allowed in that case. Consequently, $N \geq 64$ must be satisfied for the total divider to be set within $0 \leq A \leq 63$.

The f_p and fin have the following relation:

$f_p = fin / (64 \times N + A)$

(3) Programmable reference divider

The programmable reference divider divides the reference oscillation frequency (f_{OSC}) from the crystal oscillator connected between OSC_{IN} and OSC_{OUT} pins or from the external oscillator input taken in directly through OSC_{IN}, pin and then, sends the resultant f_r to the phase comparator. It consists of a 14-bit binary programmable reference counter. When the output from the external oscillator is to be input directly to OSC_{IN} pin, the connection must be AC coupled and OSC_{OUT} pin is left open. Also, to prevent OSC_{OUT} from malfunctioning, its traces on the printed circuit board must be kept minimal or eliminated entirely; whenever possible, it must be free of any form of load.

The following divider is used:

Programmable reference counter : R = 5 to 16383

The f_r and f_{OSC} have the following relation:

$f_r = f_{OSC} / R$

(4) Phase comparator

The phase comparator detects the phase difference between the outputs f_r and f_p from the dividers and generates an error signal that is proportional to phase difference. The outputs from the phase comparator include D_O which takes on one of the three states, namely, “L” (low), “H” (high), and “Z” (high impedance), and is sent to the LPF LD which indicates the PLL lock or unlock states.

(a) Phase comparator

The phase comparator detects the phase error between f_r and f_p, then generates an error signal that is proportional to the phase error. The roles of the f_r and f_p supplied to the phase comparator may be reversed by switching the logical input level of pin FC. This inverts the logical level of the D_O output. The logical level of D_O output may be selected according to the characteristics of the external LPF and the VCO. (Refer to Table 1.)

Table.1 Phass comparator inputs/output relationships

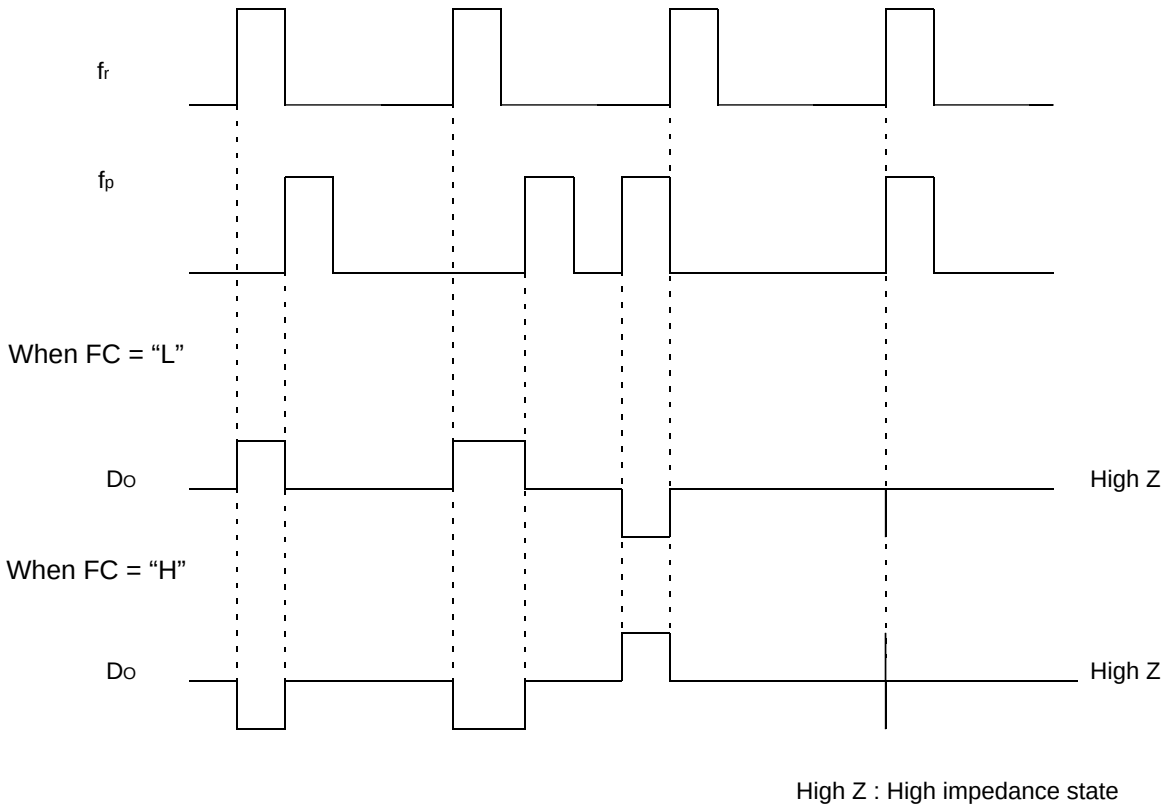
FC	"L"	"H"
$f_r > f_p$	H	L
$f_r = f_p$	Z	Z
$f_r < f_p$	L	H

(b) Phase comparator input/output waveforms

The phase comparator outputs logic levels summarized in Table 1, according to the phase error between f_r and f_p.

The pulse width of the phase comparator outputs are identical and equal to the phase error between f_r and f_p as shown in Figure 1.

Figure 1 Phase comparator input/output waveforms

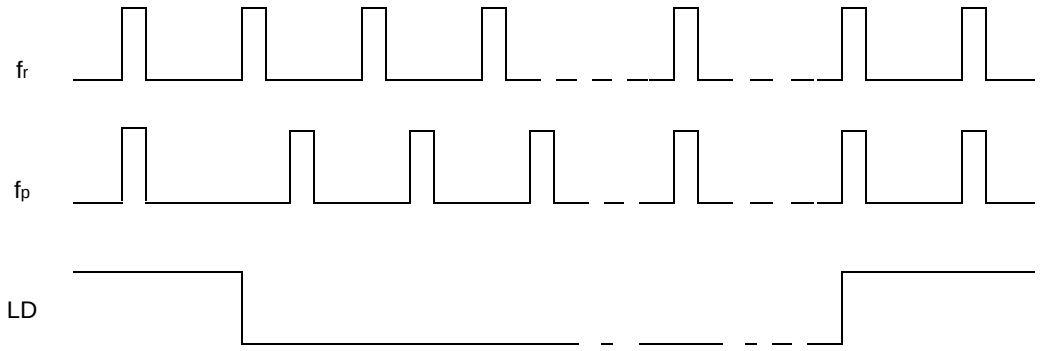


High Z : High impedance state

(c) Lock detector

The lock detector detects the lock and unlock states of the PLL. The lock detector outputs “H” when the PLL enters the lock state and outputs “L” when the PLL enters the unlock state as shown in Figure 2. When PS = “L”, the lock detector outputs “H” compulsorily.

Figure 2 Phase comparator input/output waveforms (lock detector)



3. Setting the Divide Ratio

(1) Serial data format

The format of the serial data is shown is Figure 3. The serial data is composed of control bits and divide ratio setting data. The contorl bits select the programmable divider or programmable reference divider.

In case of the programmable divider, serial data consists of 18 bits (6 bits for the swallow counter and 12 bits for the programmable counter) and control bits as shown in Figure 3.1. In case of the programmable reference divider, the serial data consists of 14 bits and 2 control bits as shown in Figure 3.2.

The control bits are set to: C0 = C1= 0 for the programmable divider
C0 = 0, C1 = 1 for the programmable reference divider.

Figure 3 Serial data format

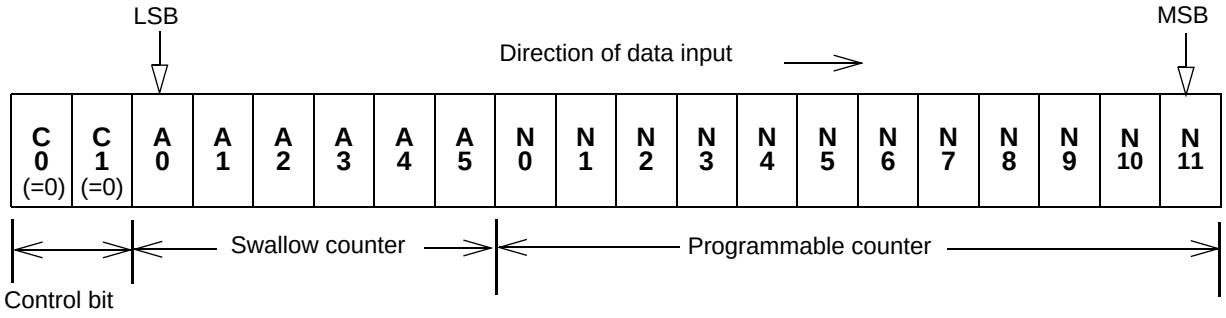


Figure 3.1 Divide ratio for the programmable divider

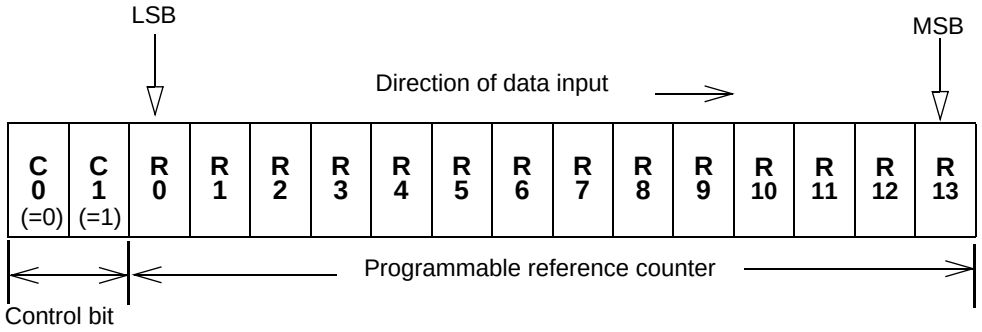
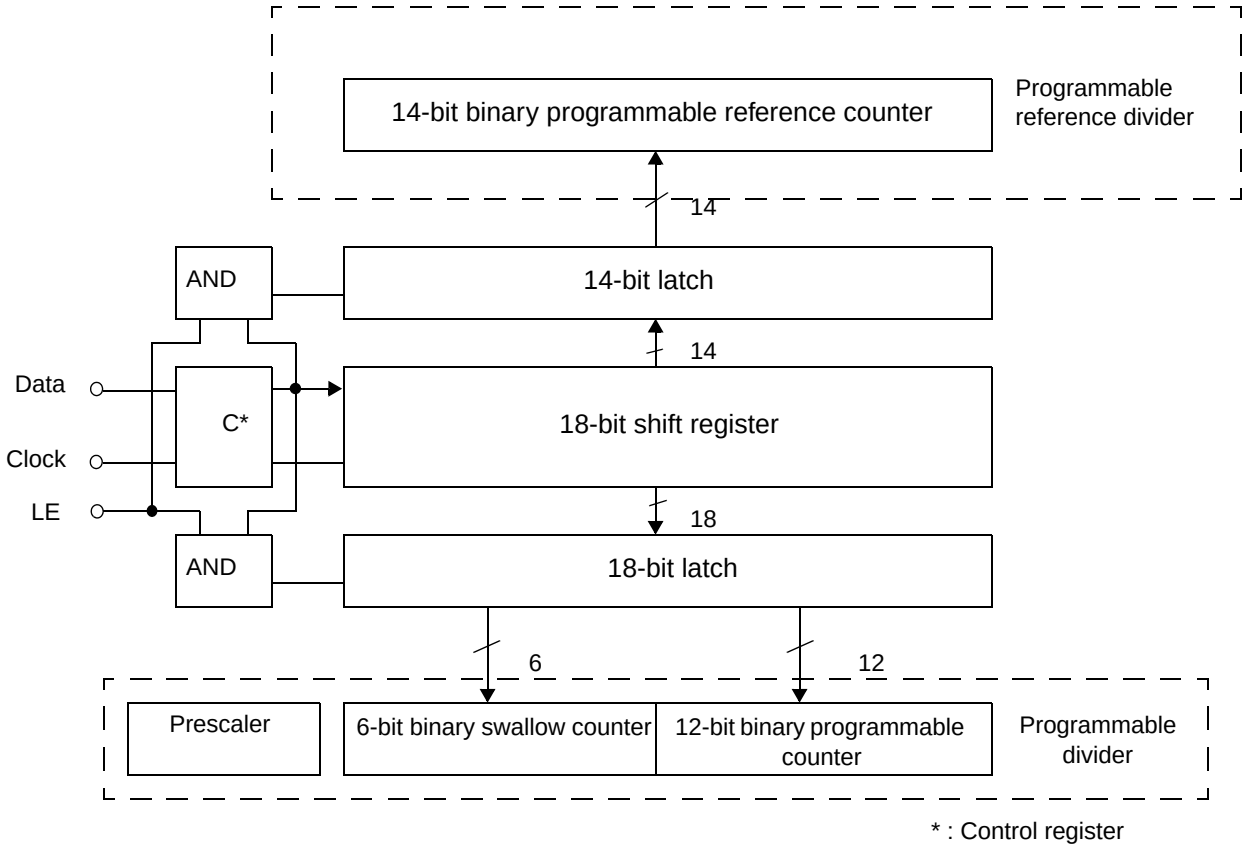


Figure 3.2 Divide ratio for the programmable reference divider

(2) The flow of serial data

Serial data is received via data pin in synchronization with the clock input and loaded into shift register which contains the divide ratio setting data and into the control register which contains the control bit. The logical product (through the AND gate in Figure 4) of LE and the control register output (i.e., control bit) is fed to the enable input of the latches. Accordingly, when LE is set high, the latch for the divider identitied by the control bit is enabled and the divide ratio data from the shift register is loaded into the selected counter(s).

Figure 4 The flow of serial data



(3) Setting the divide ratio for the programmable divider

Columns A0 to A5 of Table.2.1 represent the divide ratio of the swallow counter and columns N0 to N11 of Table.2.2 represent the divide ratio of programmable counter. The control bit is set to 0.

Table. 2 Divide ratio for the programmable divider

Table.2.1 Swallow counter divider A

Divide ratio (A)	A 0	A 1	A 2	A 3	A 4	A 5
0	0	0	0	0	0	0
1	1	0	0	0	0	0
•	•	•	•	•	•	•
63	1	1	1	1	1	1

Table.2.2 Programmable counter divider N

Divide ratio (N)	N 0	N 1	N 2	N 3	N 4	N 5	N 6	N 7	N 8	N 9	N 10	N 11
5	1	0	1	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

Note: Less than 5 is prohibited.

(4) Setting the divide ratio for the programmable reference divider

Columns R0-R13 of Table 3 represent the divide ratio of the programmable reference counter. The control bit is set to 1.

Table.3 Divide ratio for the programmable reference divider

Divide ratio (R)	R 0	R 1	R 2	R 3	R 4	R 5	R 6	R 7	R 8	R 9	R 10	R 11	R 12	R 13
5	1	0	1	0	0	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Less than 5 is prohibited.

(5) Setting data input timing

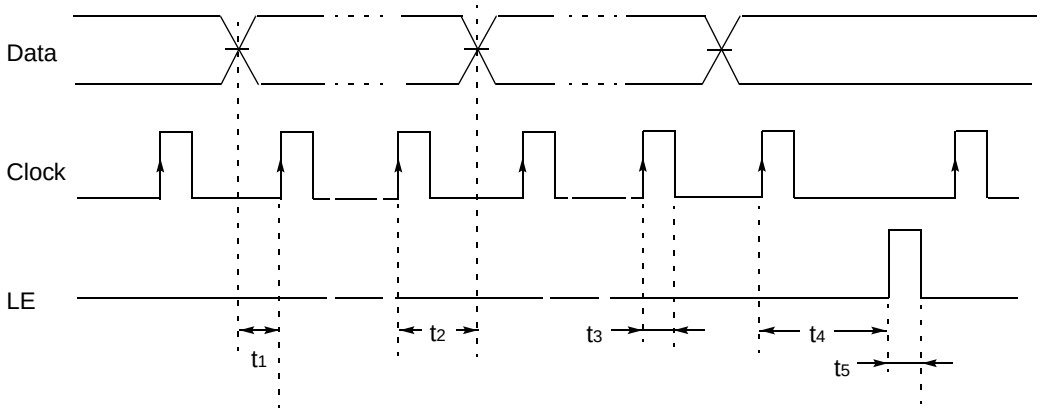
The MB15C03 uses 20 bits of serial data for the programmable divider and 16 bits for the programmable reference divider. When more bits of serial data than defined for the target divider are received, only the last valid serial data bits are effective.

To set the divide ratio for the MB15C03 dividers, it is necessary to supply the Data, Clock, and LE signals at the timing shown in Figure 5.

t_1 (≥ 0.5 µs): Data setup time t_2 (≥ 0 5 µs): Data hold time t_3 (≥ 0.5 µs): Clock pulse width

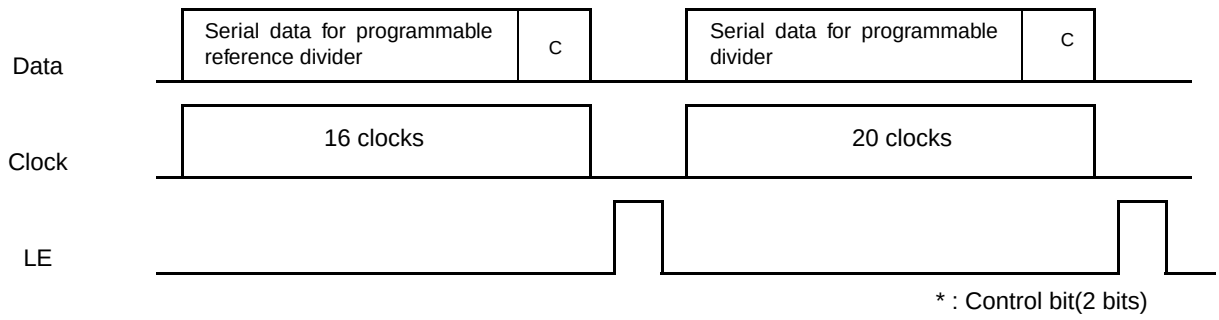
t_4 (≥ 0.5 µs): LE setup time to the rising edge of last clock t_5 (≥ 0.5 µs): LE pulse width

Figure 5 Serial data input timing



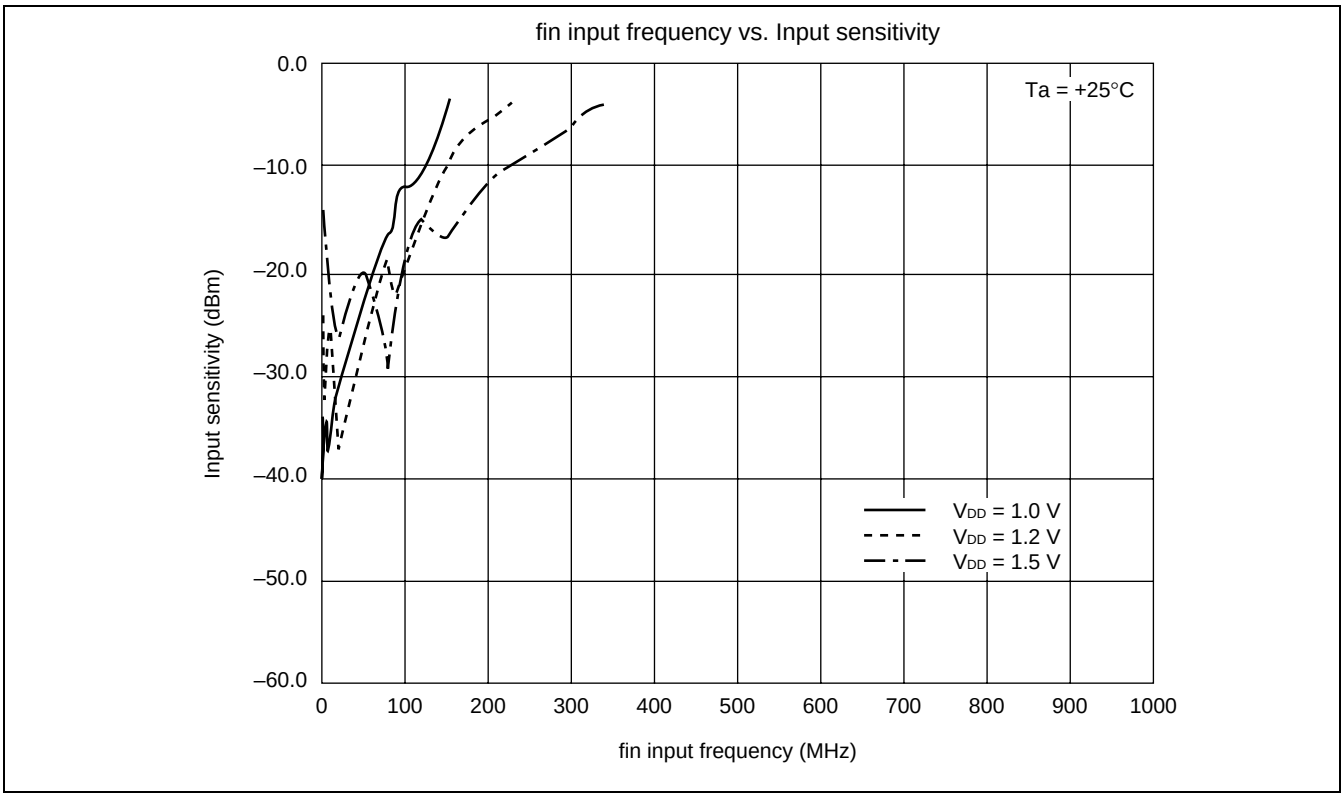
Since the divide rations are unpredictable when the MB15C03 is turned on, it is necessary to initialize the divide ratio for both dividers at power-on time. As shown in Figure 6, after setting the divide ratio for one of the dividers (e.g., programmable reference divider), set LE to “H” level before setting the divide ratio for the other divider (e.g., programmable divider). To change the divide ratio of one of the dividers after initialization, input the serial data only for that divider (the divide ratio for the other divider is preserved).

Figure 6 Inputting serial data (Setting divisors)

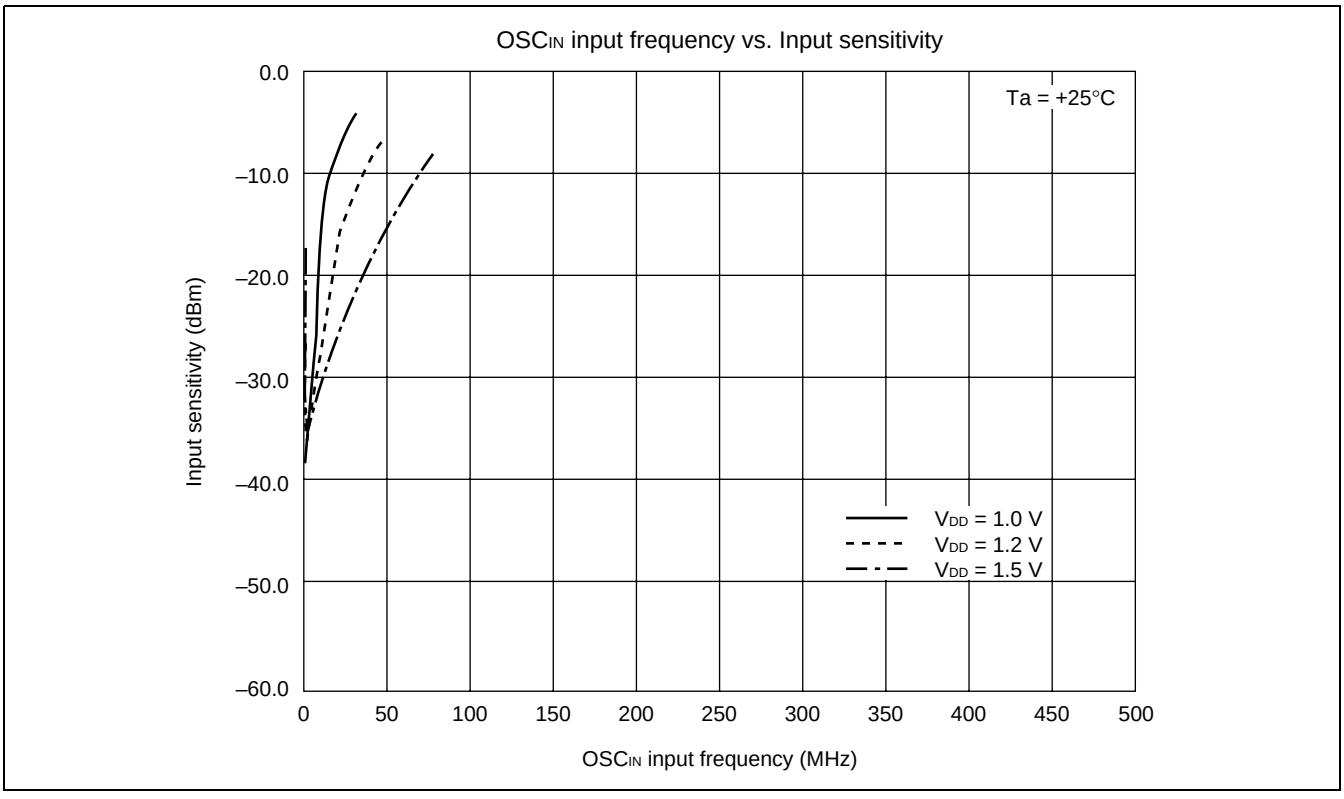


■ TYPICAL CHARACTERISTIC CURVES

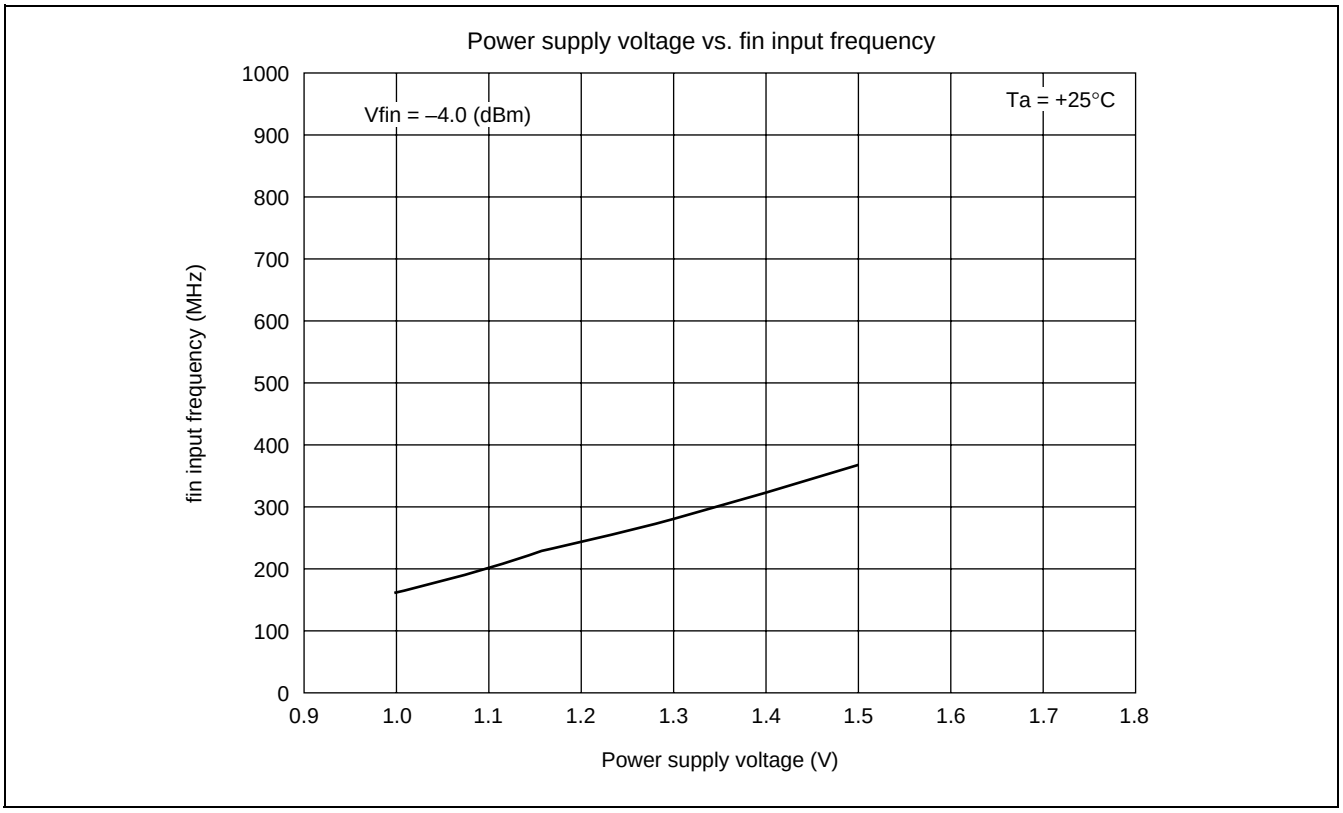
1. fin Input Sensitivity Characteristics



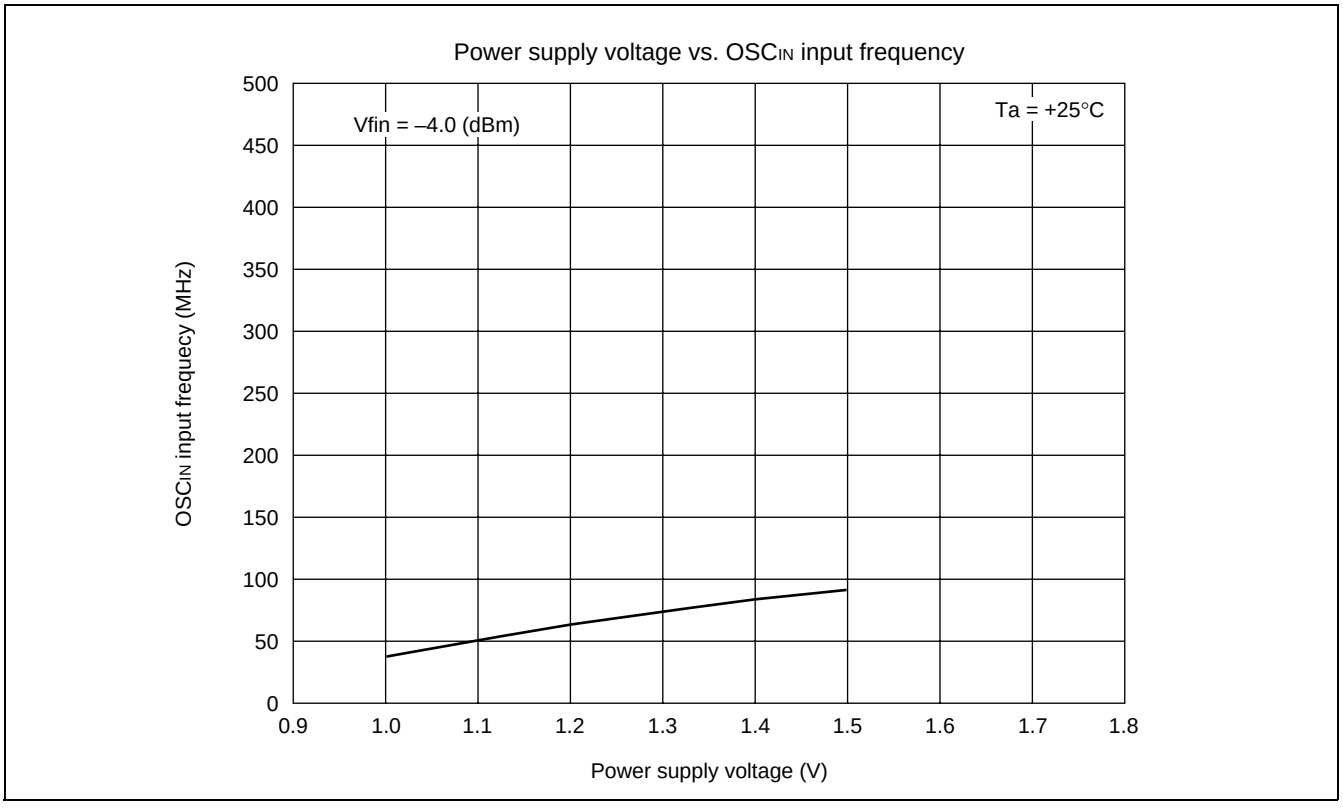
2. OSCIN Input Sensitivity Characteristics



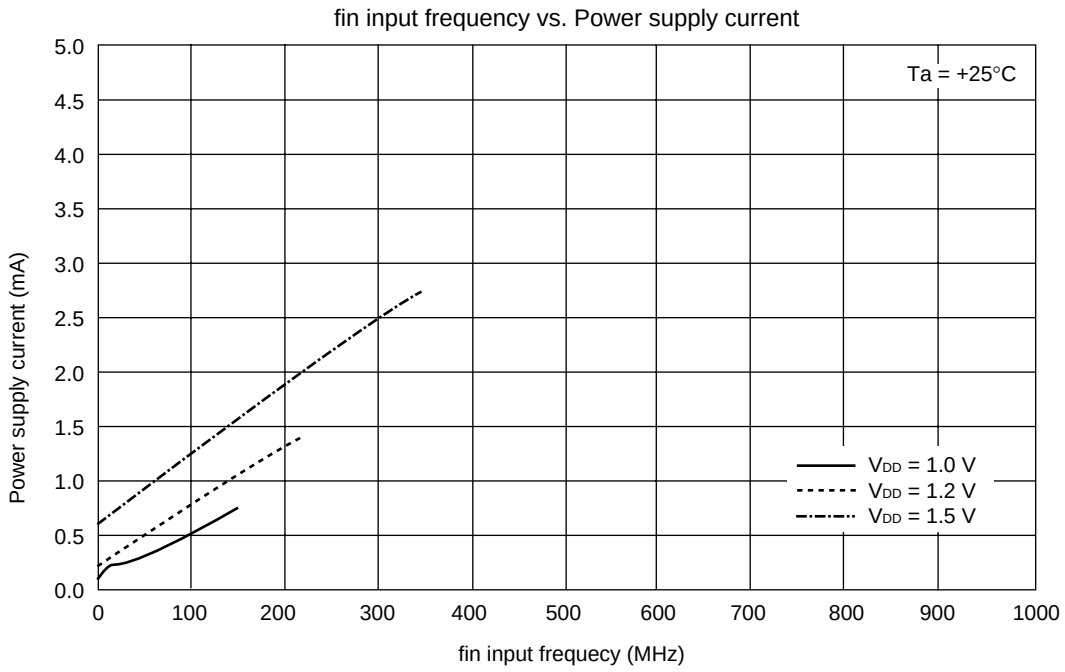
3. fin Power Supply Voltage Dependency

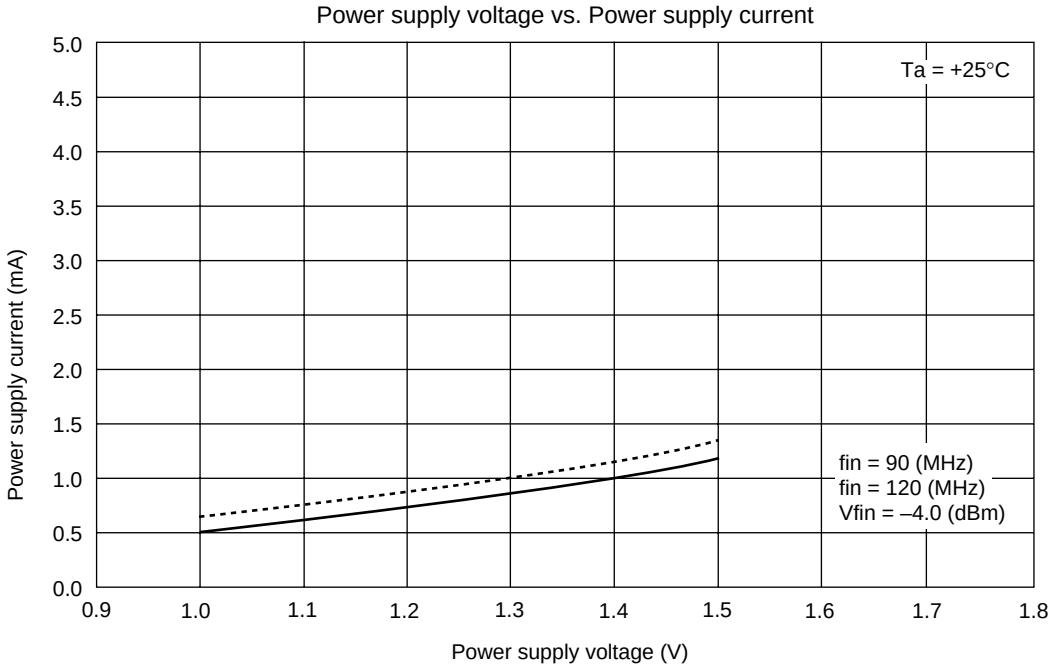


4. OSC_{IN} Power Supply Voltage Dependency

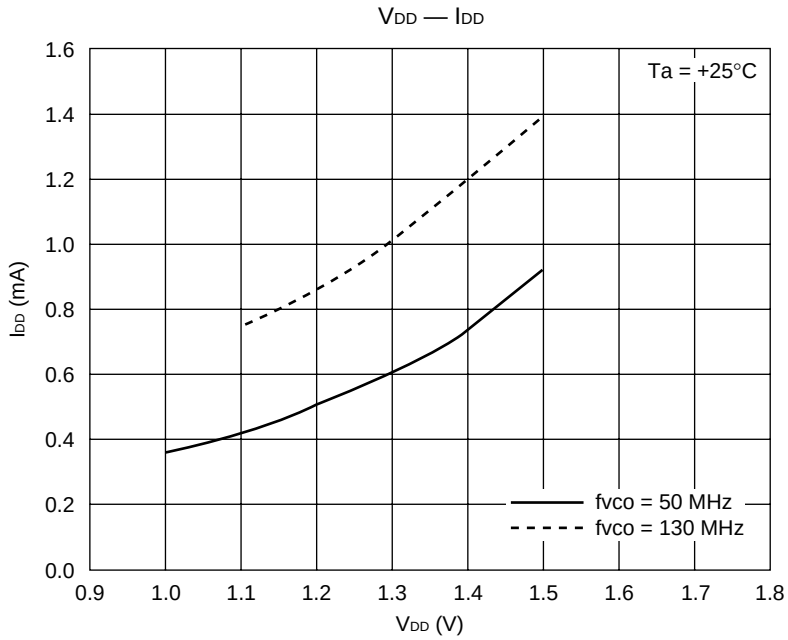


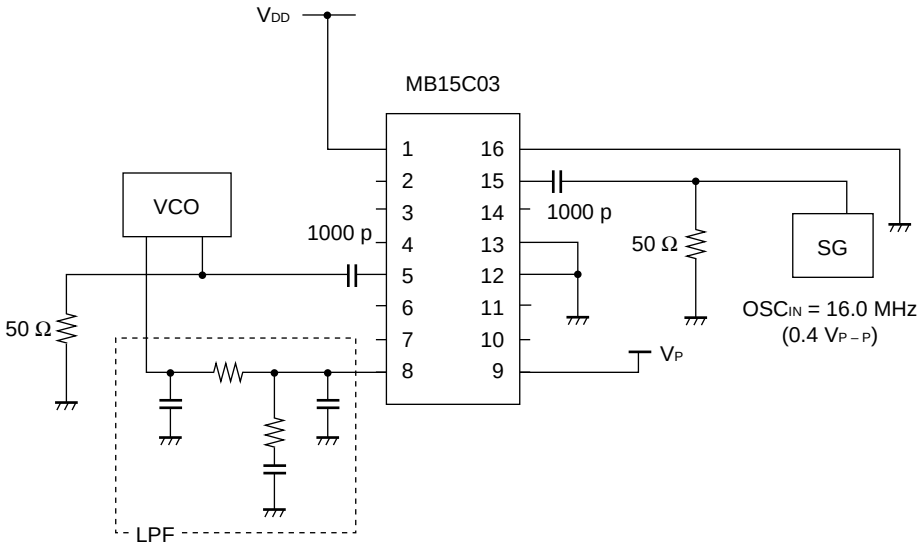
5. Power Supply Current Characteristics



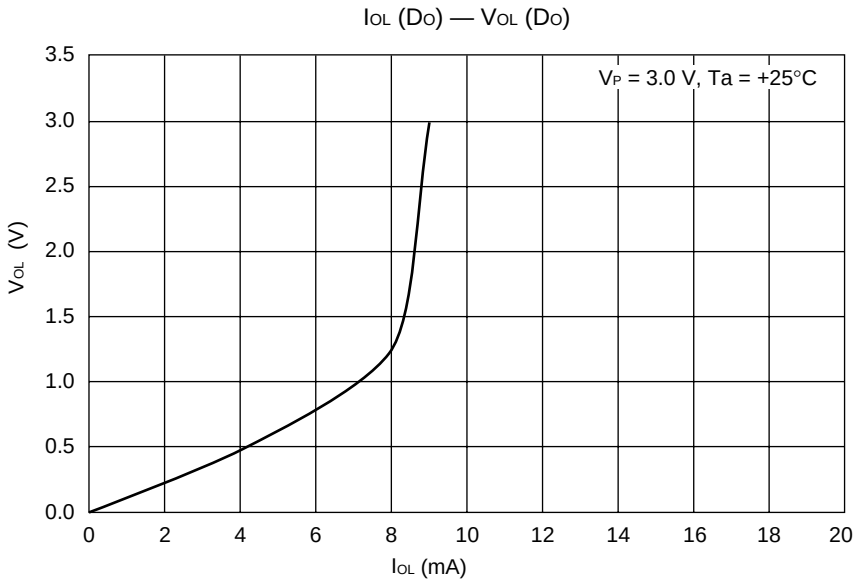


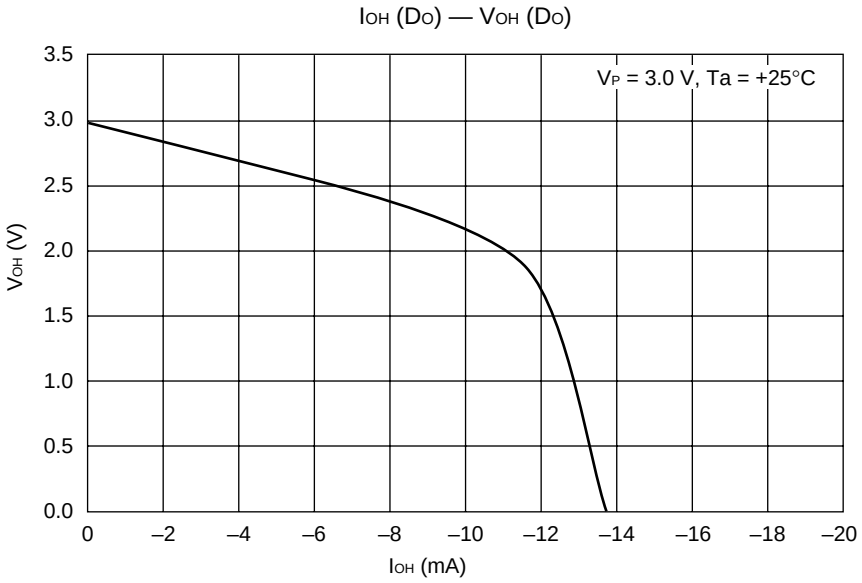
6. I_{DD} (Lock) Power Supply Voltage Dependency



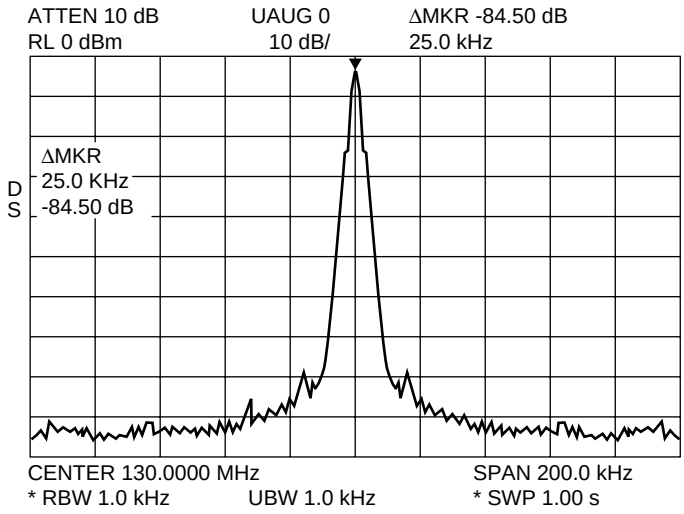


7. D_O (Chargepump) Power Supply Voltage Dependency

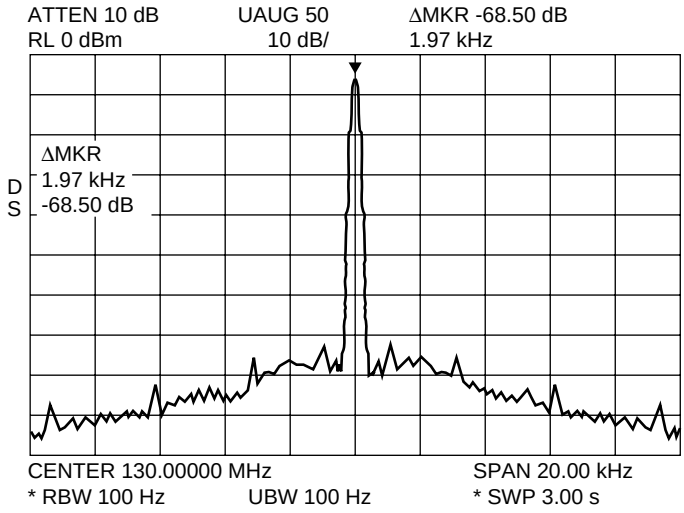




8. Spectrum Waveforms

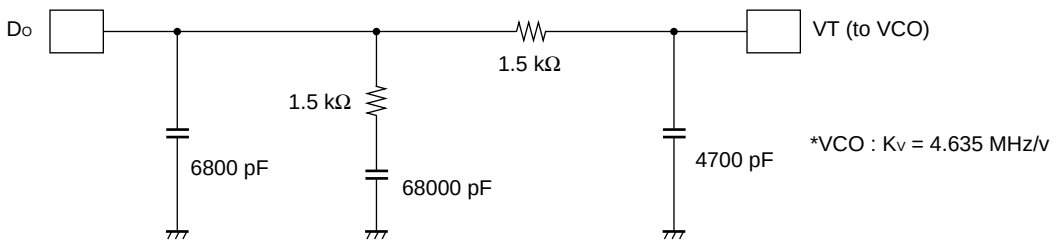


- LOCK Frequency: 130.0 MHz (fr = 25 kHz)
- V_{DD} = 1.2 V, V_p = 3.0 V
  Ta = +25˚C



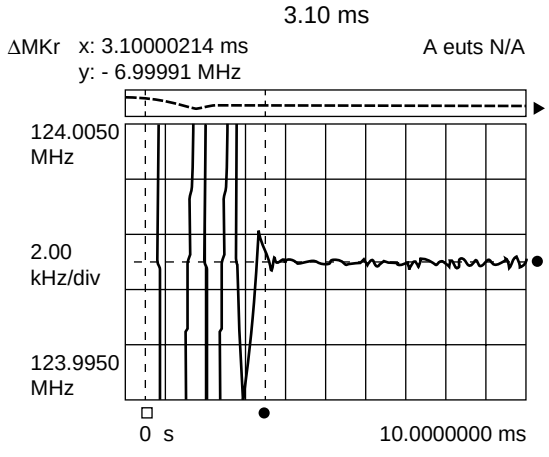
- LOCK Frequency: 130.0 MHz (fr = 25 KHz)
- V_{DD} = 1.2 V, V_p = 3.0 V
  Ta = +25˚C

- Mesurement circuit

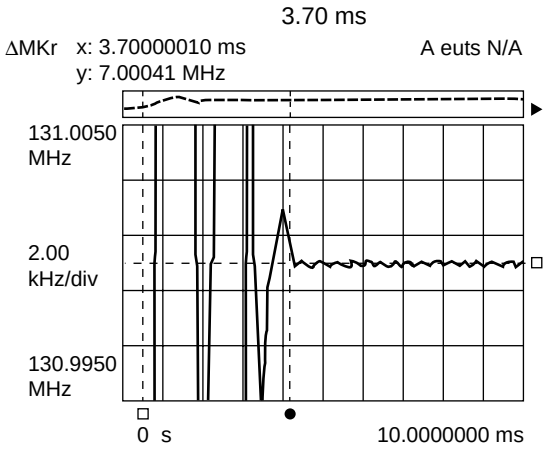


9. Lock-up Time

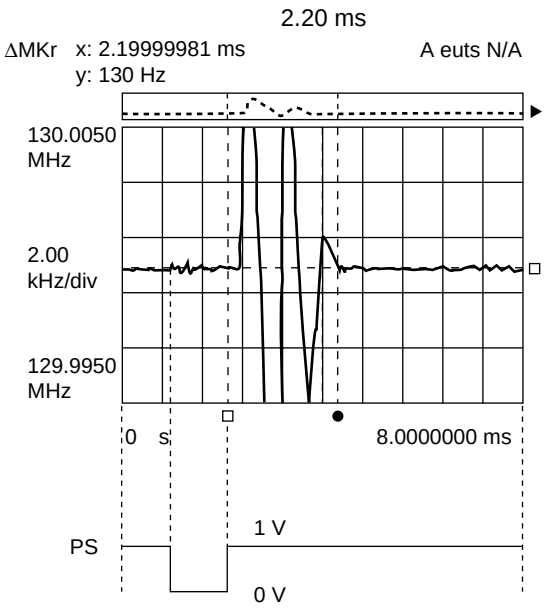
• LOCK Frequency: 131.0 MHz to 124.0 MHz
(fr = 25 kHz)
• V_{DD} = 1.2 V, V_P = 3.0 V, Ta = +25˚C
131.0 MHz → 124.0 MHz, within ±1 kHz



• LOCK Frequency: 124.0 MHz to 131.0 MHz
(fr = 25 KHz)
• V_{DD} = 1.2 V, V_P = 3.0 V, Ta = +25˚C
124.0 MHz → 131.0 MHz, within ±1 kHz



• LOCK Frequency: 130.0 MHz (fr = 25 kHz)
• V_{DD} = 1.2 V, V_P = 3.0 V, Ta = +25˚C
PS ON → 130.0 MHz, within ±1 kHz



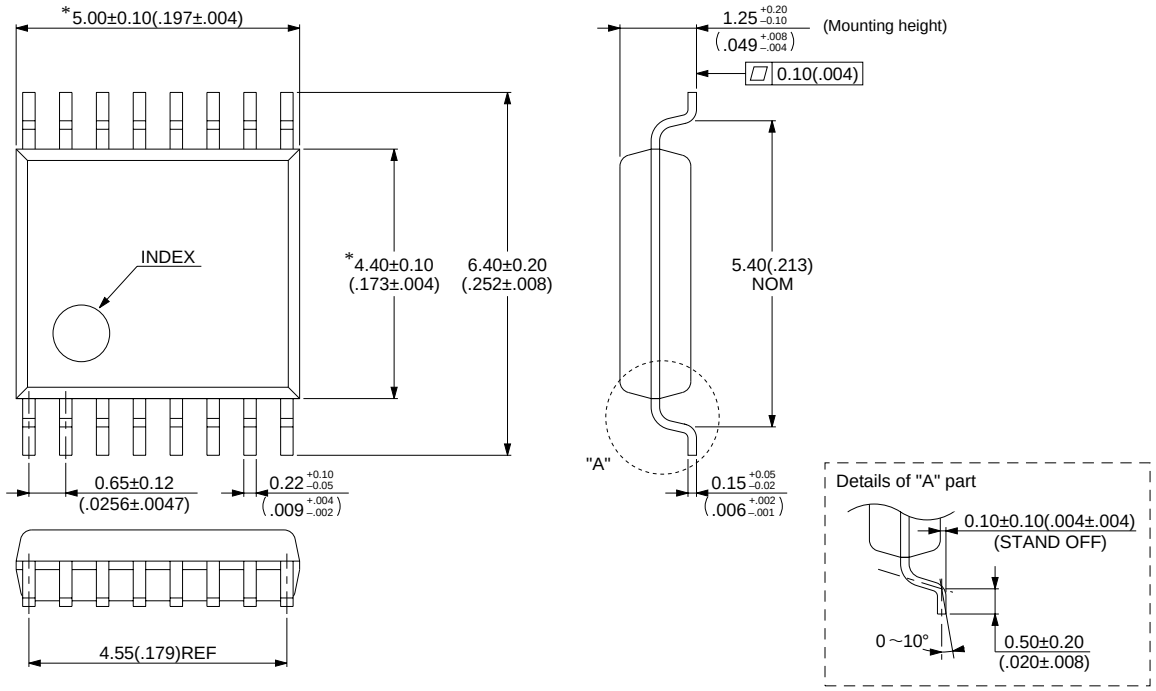
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15C03PFV	16-pin, Plastic SSOP (FPT-16P-M05)	

■ PACKAGE DIMENSION

16-pin, plastic SSOP
(FPT-16P-M05)

* : These dimensions do not include resin protrusion.



Dimensions in mm (inches)

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