

# 32-bit RISC Microcontroller

CMOS

## FR30 MB91101 Series

### MB91101/MB91101A

#### DESCRIPTION

The MB91101 and MB91101A are a standard single-chip microcontroller constructed around the 32-bit RISC CPU (FR\* family) core with abundant I/O resources and bus control functions optimized for high-performance/high-speed CPU processing for embedded controller applications. To support the vast memory space accessed by the 32-bit CPU, the MB91101 and MB91101A normally operate in the external bus access mode and executes instructions on the internal 1 Kbyte cache memory and 2 Kbytes RAM for enhanced performance.

The MB91101 and MB91101A are optimized for applications requiring high-performance CPU processing such as navigation systems, high-performance FAXs and printer controllers.

\*: FR Family stands for FUJITSU RISC controller.

#### FEATURES

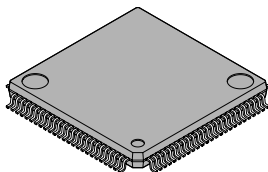
##### FR CPU

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Operating clock frequency: Internal 50 MHz/external 25 MHz (PLL used at source oscillation 12.5 MHz)
- General purpose registers: 32 bits × 16
- 16-bit fixed length instructions (basic instructions), 1 instruction/1 cycle
- Memory to memory transfer, bit processing, barrel shifter processing: Optimized for embedded applications
- Function entrance/exit instructions, multiple load/store instructions of register contents, instruction systems supporting high level languages

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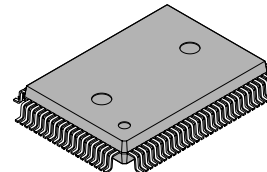
#### PACKAGES

100-pin Plastic LQFP



(FPT-100P-M05)

100-pin Plastic QFP



(FPT-100P-M06)

The Fujitsu logo, consisting of the word "FUJITSU" in a bold, sans-serif font with a stylized infinity symbol above the letter "I".

# MB91101/MB91101A

- Register interlock functions, efficient assembly language coding
- Branch instructions with delay slots: Reduced overhead time in branch executions
- Internal multiplier/supported at instruction level
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupt (push PC and PS): 6 cycles, 16 priority levels

## External bus interface

- Clock doubler: Internal 50 MHz, external bus 25 MHz operation
- 25-bit address bus (32 Mbytes memory space)
- 8/16-bit data bus
- Basic external bus cycle: 2 clock cycles
- Chip select outputs for setting down to a minimum memory block size of 64 Kbytes: 6
- Interface supported for various memory technologies
  - DRAM interface (area 4 and 5)
- Automatic wait cycle insertion: Flexible setting, from 0 to 7 for each area
- Unused data/address pins can be configured as input/output ports.
- Little endian mode supported (Select 1 area from area 1 to 5)

## DRAM interface

- 2 banks independent control (area 4 and 5)
- Normal mode (double CAS DRAM)/high-speed page mode (single CAS DRAM)/Hyper DRAM
- Basic bus cycle: Normally 5 cycles, 2-cycle access possible in high-speed page mode
- Programmable waveform: Automatic 1-cycle wait insertion to RAS and CAS cycles
- DRAM refresh
  - CBR refresh (interval time configurable by 6-bit timer)
  - Self-refresh mode
- Supports 8/9/10/12-bit column address width
- 2CAS/1WE, 2WE/1CAS selective

## Cache memory

- 1-Kbyte instruction cache memory
- 32 block/way, 4 entry(4 word)/block
- 2 way set associative
- Lock function: For specific program code to be resident in cache memory

## DMA controller (DMAC)

- 8 channels
- Transfer incident/external pins/internal resource interrupt requests
- Transfer sequence: Step transfer/block transfer/burst transfer/continuous transfer
- Transfer data length: 8 bits/16 bits/32 bits selective
- NMI/interrupt request enables temporary stop operation.

## UART

- 3 independent channels
- Full-duplex double buffer
- Data length: 7 bits to 9 bits (non-parity), 6 bits to 8 bits (parity)
- Asynchronous (start-stop system), CLK-synchronized communication selective
- Multi-processor mode
- Internal 16-bit timer (U-TIMER) operating as a proprietary baud rate generator: Generates any given baud rate
- External clock can be used as a transfer clock.
- Error detection: Parity, frame, overrun

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## 10-bit A/D converter (successive approximation conversion type)

- 10-bit resolution, 4 channels
- Successive approximation type: Conversion time of 5.6  $\mu$ s at 25 MHz
- Internal sample and hold circuit
- Conversion mode: Single conversion/scanning conversion/repeated conversion/stop conversion selective
- Start: Software/external trigger/internal timer selective

## 16-bit reload timer

- 3 channels
- Internal clock: 2 clock cycle resolution, divide by 2/8/32 selective

## Other interval timers

- 16-bit timer: 3 channels (U-TIMER)
- PWM timer: 4 channels
- Watchdog timer: 1 channel

## Bit search module

First bit transition "1" or "0" from MSB can be detected in 1 cycle.

## Interrupt controller

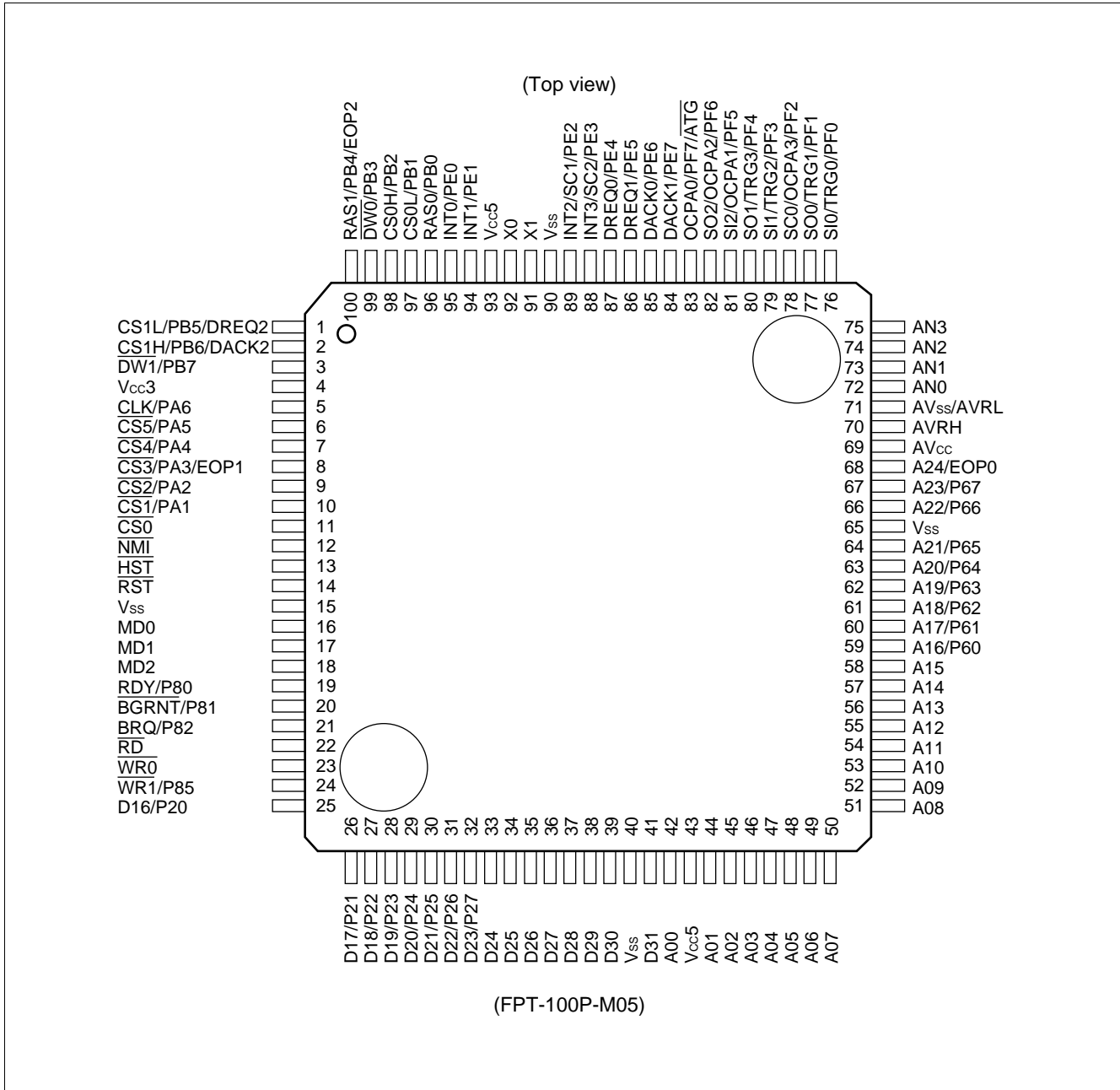
- External interrupt input: Non-maskable interrupt ( $\overline{\text{NMI}}$ ), normal interrupt  $\times 4$  (INT0 to INT3)
- Internal interrupt incident: UART, DMA controller (DMAC), A/D converter, U-TIMER and delayed interrupt module
- Priority levels of interrupts are programmable except for non-maskable interrupt (in 16 steps).

## Others

- Reset cause: Power-on reset/hardware standby/watchdog timer/software reset/external reset
- Low-power consumption mode: Sleep mode/stop mode
- Clock control
  - Gear function: Operating clocks for CPU and peripherals are independently selective.  
Gear clock can be selected from 1/1, 1/2, 1/4 and 1/8 (or 1/2, 1/4, 1/8 and 1/16).  
However, operating frequency for peripherals is less than 25 MHz.
- Packages: LQFP-100 and QFP-100
- CMOS technology (0.35  $\mu$ m)
- Power supply voltage
  - 5 V: CPU power supply 5.0 V  $\pm$ 10% (internal regulator)  
A/D power supply 2.7 V to 3.6 V
  - 3 V: CPU power supply 2.7 V to 3.6 V (without internal regulator)  
A/D power supply 2.7 V to 3.6 V

# MB91101/MB91101A

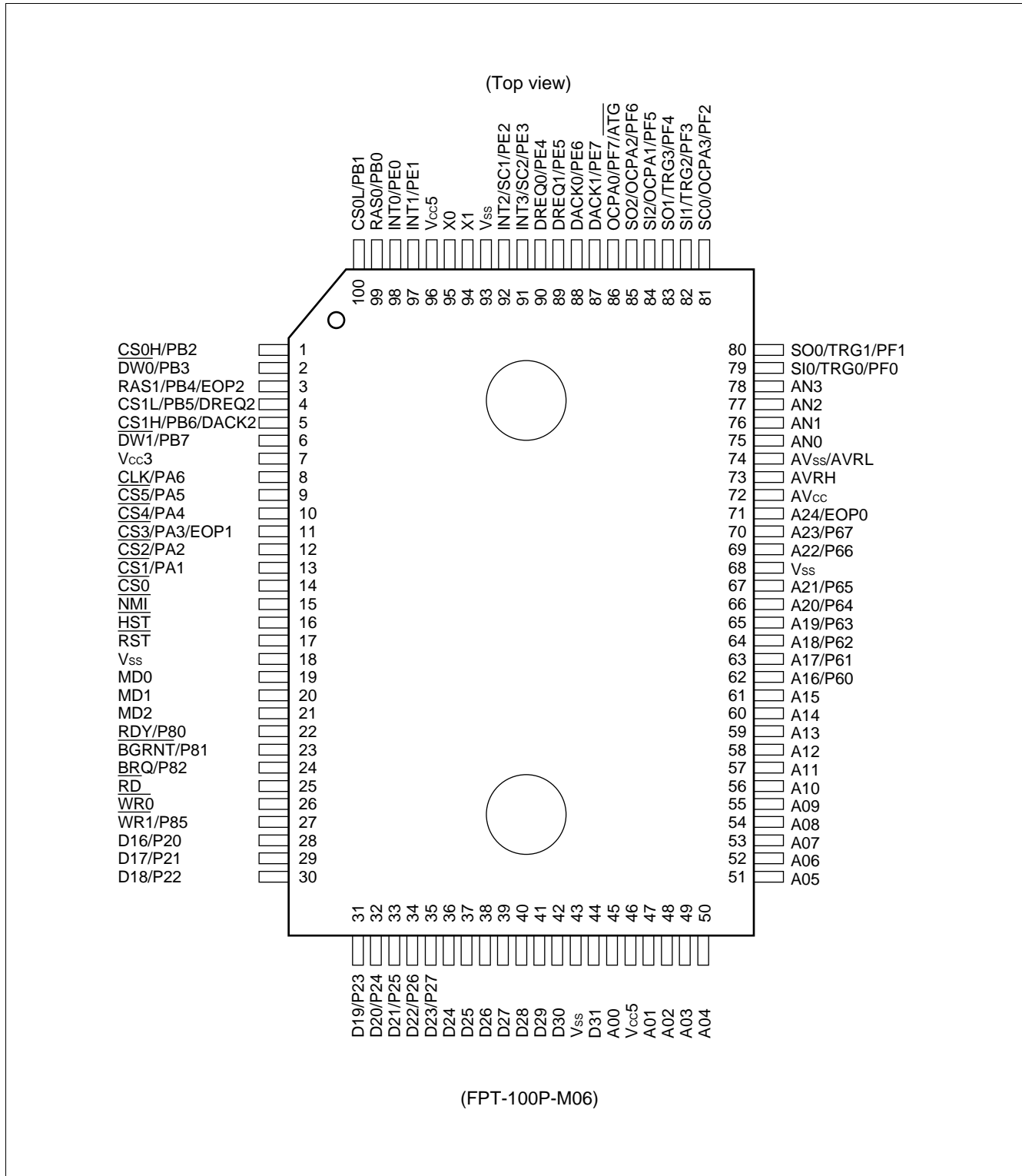
## ■ PIN ASSIGNMENT



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# MB91101/MB91101A

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# MB91101/MB91101A

## ■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Description									
LQFP*1	QFP*2												
25 to 32	28 to 35	D16 to D23	C	Bit 16 to bit 23 of external data bus									
		P20 to P27		Can be configured as I/O ports when external data bus width is set to 8-bit.									
33 to 39, 41	36 to 42, 44	D24 to D30, D31	C	Bit 24 to bit 31 of external data bus									
42, 44 to 58	45, 47 to 61	A00, A01 to A15	F	Bit 00 to bit 15 of external address bus									
59 to 64, 66, 67	62 to 67, 69, 70	A16 to A21, A22, A23	F	Bit 16 to bit 23 of external address bus									
		P60 to P65, P66, P67		Can be configured as I/O ports when not used as address bus.									
68	71	A24	L	Bit 24 of external address bus									
		EOP0		Can be configured as DMAC EOP output (ch. 0) when DMAC EOP output is enabled.									
19	22	RDY	C	External ready input Inputs "0" when bus cycle is being executed and not completed.									
		P80		Can be configured as a port when RDY is not used.									
20	23	$\overline{\text{BGRNT}}$	F	External bus release acknowledge output Outputs "L" level when external bus is released.									
		P81		Can be configured as a port when $\overline{\text{BGRNT}}$ is not used.									
21	24	BRQ	C	External bus release request input Inputs "1" when release of external bus is required.									
		P82		Can be configured as a port when BRQ is not used.									
22	25	$\overline{\text{RD}}$	L	Read strobe output pin for external bus									
23	26	$\overline{\text{WR0}}$	L	Write strobe output pin for external bus Relation between control signals and effective byte locations is as follows:									
24	27	$\overline{\text{WR1}}$	F	<table border="1"> <thead> <tr> <th></th> <th>16-bit bus width</th> <th>8-bit bus width</th> </tr> </thead> <tbody> <tr> <td>D15 to D08</td> <td><math>\overline{\text{WR0}}</math></td> <td><math>\overline{\text{WR0}}</math></td> </tr> <tr> <td>D07 to D00</td> <td><math>\overline{\text{WR1}}</math></td> <td>(I/O port enabled)</td> </tr> </tbody> </table>		16-bit bus width	8-bit bus width	D15 to D08	$\overline{\text{WR0}}$	$\overline{\text{WR0}}$	D07 to D00	$\overline{\text{WR1}}$	(I/O port enabled)
					16-bit bus width	8-bit bus width							
D15 to D08	$\overline{\text{WR0}}$	$\overline{\text{WR0}}$											
D07 to D00	$\overline{\text{WR1}}$	(I/O port enabled)											
P85	WR1 is High-Z during resetting. Attach an external pull-up resistor when using at 16-bit bus width. Can be configured as a port when $\overline{\text{WR1}}$ is not used.												

\*1: FPT-100P-M05

\*2: FPT-100P-M06

(Continued)

# MB91101/MB91101A

Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
11	14	$\overline{CS0}$	L	Chip select 0 output ("L" active)
10	13	$\overline{CS1}$	F	Chip select 1 output ("L" active)
		PA1		Can be configured as a port when $\overline{CS1}$ is not used.
9	12	$\overline{CS2}$	F	Chip select 2 output ("L" active)
		PA2		Can be configured as a port when $\overline{CS2}$ is not used.
8	11	$\overline{CS3}$	F	Chip select 3 output ("L" active)
		PA3		Can be configured as a port when $\overline{CS3}$ and EOP1 are not used.
		EOP1		EOP output pin for DMAC (ch. 1) This function is available when EOP output for DMAC is enabled.
7	10	$\overline{CS4}$	F	Chip select 4 output ("L" active)
		PA4		Can be configured as a port when $\overline{CS4}$ is not used.
6	9	$\overline{CS5}$	F	Chip select 5 output ("L" active)
		PA5		Can be configured as a port when $\overline{CS5}$ is not used.
5	8	CLK	F	System clock output Outputs clock signal of external bus operating frequency.
		PA6		Can be configured as a port when CLK is not used.
96	99	RAS0	F	RAS output for DRAM bank 0 Refer to the DRAM interface for details.
		PB0		Can be configured as a port when RAS0 is not used.
97	100	CS0L	F	CASL output for DRAM bank 0 Refer to the DRAM interface for details.
		PB1		Can be configured as a port when CS0L is not used.
98	1	CS0H	F	CASH output for DRAM bank 0 Refer to the DRAM interface for details.
		PB2		Can be configured as a port when CS0H is not used.
99	2	$\overline{DW0}$	F	$\overline{WE}$ output for DRAM bank 0 ("L" active) Refer to the DRAM interface for details.
		PB3		Can be configured as a port when $\overline{DW0}$ is not used.
100	3	RAS1	F	RAS output for DRAM bank 1 Refer to the DRAM interface for details.
		PB4		Can be configured as a port when RAS1 and EOP2 are not used.
		EOP2		DMAC EOP output (ch. 2) This function is available when DMAC EOP output is enabled.

\*1: FPT-100P-M05

\*2: FPT-100P-M06

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# MB91101/MB91101A

Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
1	4	CS1L	F	CASL output for DRAM bank 1 Refer to the DRAM interface for details.
		PB5		Can be configured as a port when CS1L and DREQ2 are not used.
		DREQ2		External transfer request input pin for DMA This pin is used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
2	5	CS1H	F	CASH output for DRAM bank 1 Refer to the DRAM interface for details.
		PB6		Can be configured as a port when CS1H and DACK2 are not used.
		DACK2		External transfer request acknowledge output pin for DMAC (ch. 2) This function is available when transfer request output for DMAC is enabled.
3	6	$\overline{DW1}$	F	$\overline{WE}$ output for DRAM bank 1 ("L" active) Refer to the DRAM interface for details.
		PB7		Can be configured as a port when $\overline{DW1}$ is not used.
16 to 18	19 to 21	MD0 to MD2	G	Mode pins 0 to 2 MCU basic operation mode is set by these pins. Directly connect these pins with $V_{CC}$ or $V_{SS}$ for use.
92	95	X0	A	Clock (oscillator) input
91	94	X1	A	Clock (oscillator) output
14	17	$\overline{RST}$	B	External reset input
13	16	$\overline{HST}$	H	Hardware standby input ("L" active)
12	15	$\overline{NMI}$	H	NMI (non-maskable interrupt pin) input ("L" active)
95, 94	98, 97	INT0, INT1	F	External interrupt request input pins These pins are used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
		PE0, PE1		Can be configured as I/O ports when INT0, INT1 are not used.
89	92	INT2	F	External interrupt request input pin This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		SC1		Clock I/O pin for UART1 Clock output is available when clock output of UART1 is enabled.
		PE2		Can be configured as the I/O port when INT2 and SC1 are not used. This function is available when UART1 clock output is disabled.

\*1: FPT-100P-M05

\*2: FPT-100P-M06

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Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
88	91	INT3	F	External interrupt request input pin This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		SC2		UART2 clock I/O pin Clock output is available when UART2 clock output is enabled.
		PE3		Can be configured as the I/O port when INT3 and SC2 are not used. This function is available when UART2 clock output is disabled.
87, 86	90, 89	DREQ0, DREQ1	F	External transfer request input pins for DMA These pins are used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
		PE4, PE5		Can be configured as I/O ports when DREQ0, DREQ1 are not used.
85	88	DACK0	F	External transfer request acknowledge output pin for DMAC (ch. 0) This function is available when transfer request output for DMAC is enabled.
		PE6		Can be configured as the I/O port when DACK0 is not used. This function is available when transfer request acknowledge output for DMAC or DACK0 output is disabled.
84	87	DACK1	F	External transfer request acknowledge output pin for DMAC (ch. 1) This function is available when transfer request output for DMAC is enabled.
		PE7		Can be configured as the I/O port when DACK1 is not used. This function is available when transfer request output for DMAC or DACK1 output is disabled.
76	79	SI0	F	UART0 data input pin This pin is used for input during UART0 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		TRG0		PWM timer external trigger input pin This pin is used for input during PWM timer external trigger is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		PF0		Can be configured as the I/O port when SI0 and TRG0 are not used.

\*1: FPT-100P-M05

\*2: FPT-100P-M06

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# MB91101/MB91101A

Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
77	80	SO0	F	UART0 data output pin This function is available when UART0 data output is enabled.
		TRG1		PWM timer external trigger input pin This function is available when serial data output of PF1, UART0 are disabled.
		PF1		Can be configured as the I/O port when SO0 and TRG1 are not used. This function is available when serial data output of UART0 is disabled.
78	81	SC0	F	UART0 clock I/O pin Clock output is available when UART0 clock output is enabled.
		OCPA3		PWM timer output pin This function is available when PWM timer output is enabled.
		PF2		Can be configured as the I/O port when SC0 and OCPA3 are not used. This function is available when UART0 clock output is disabled.
79	82	SI1	F	UART1 data input pin This pin is used for input during UART1 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		TRG2		PWM timer external trigger input pin This pin is used for input during PWM timer external trigger is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		PF3		Can be configured as the I/O port when SI1 and TRG2 are not used.
80	83	SO1	F	UART1 data output pin This function is available when UART1 data output is enabled.
		TRG3		PWM timer external trigger input pin This function is available when PF4, UART1 data outputs are disabled.
		PF4		Can be configured as the I/O port when SO1 and TRG3 are not used. This function is available when UART1 data output is disabled.
81	84	SI2	F	UART2 data input pin This pin is used for input during UART2 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		OCPA1		PWM timer output pin This function is available when PWM timer output is enabled.
		PF5		Can be configured as the I/O port when SI2 and OCPA1 are not used.

\*1: FPT-100P-M05

\*2: FPT-100P-M06

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Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
82	85	SO2	F	UART2 data output pin This function is available when UART2 data output is enabled.
		OCPA2		PWM timer output pin This function is available when PWM timer output is enabled.
		PF6		Can be configured as the I/O port when SO2 and OCPA2 are not used. This function is available when UART2 data output is disabled.
83	86	OCPA0	F	PWM timer output pin This function is available when PWM timer output is enabled.
		PF7		Can be configured as the I/O port when OCPA0 and $\overline{ATG}$ are not used. This function is available when PWM timer output is disabled.
		$\overline{ATG}$		External trigger input pin for A/D converter This pin is used for input when external trigger is selected to cause A/D converter operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
72 to 75	75 to 78	AN0 to AN3	D	Analog input pins of A/D converter
69	72	AV <sub>CC</sub>	—	Power supply pin (V <sub>CC</sub> ) for A/D converter
70	73	AVRH	—	Reference voltage input (high) for A/D converter Make sure to turn on and off this pin with potential of AVRH or more applied to AV <sub>CC</sub> .
71	74	AV <sub>SS</sub> / AVRL	—	Power supply pin (V <sub>SS</sub> ) for A/D converter and reference voltage input pin (low)
43, 93	46, 96	V <sub>CC5</sub>	—	5 V power supply pin (V <sub>CC</sub> ) for digital circuit Always two pins must be connected to the power supply (connect to 3 V power supply when operating at 3 V).
4	7	V <sub>CC3</sub>	—	Bypass capacitor pin for internal capacitor. Also connect this pin to 3 V power supply when operating at 3 V.
15, 40, 65, 90	18, 43, 68, 93	V <sub>SS</sub>	—	Earth level (V <sub>SS</sub> ) for digital circuit

\*1: FPT-100P-M05

\*2: FPT-100P-M06

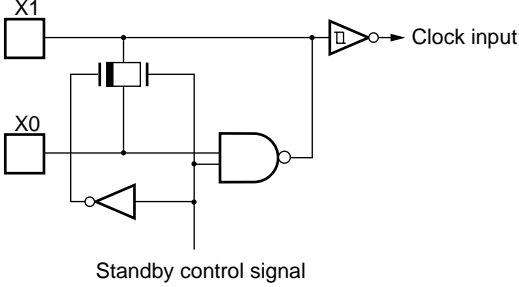
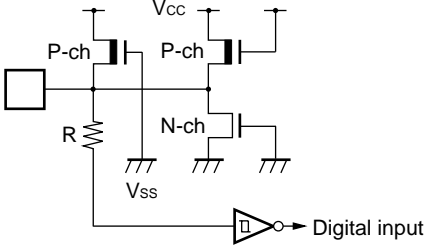
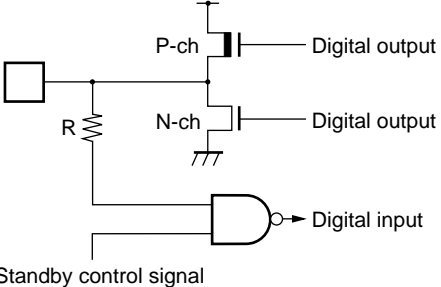
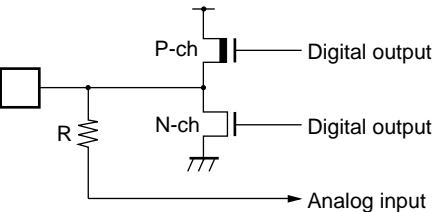
Note: In most of the above pins, I/O ports and resource I/O are multiplexed, e.g. P82 and BRQ. In case of conflict between output of I/O ports and resource I/O, priority is always given to the output of resource I/O.

# MB91101/MB91101A

## ■ DRAM CONTROL PIN

Pin name	Data bus 16-bit mode		Data bus 8-bit mode	Remarks
	2CAS/1WR mode	1CAS/2WR mode	—	
RAS0	Area 4 RAS	Area 4 RAS	Area 4 RAS	Correspondence of “L”, “H” to lower address 1 bit (A0) in data bus 16-bit mode “L”: “0” “H”: “1” CASL: CAS which A0 corresponds to “0” area CASH: CAS which A0 corresponds to “1” area WEL: WE which A0 corresponds to “0” area WEH: WE which A0 corresponds to “1” area
RAS1	Area 5 RAS	Area 5 RAS	Area 5 RAS	
CS0L	Area 4 CASL	Area 4 CAS	Area 4 CAS	
CS0H	Area 4 CASH	Area 4 $\overline{WEL}$	Area 4 CAS	
CS1L	Area 5 CASL	Area 5 CAS	Area 5 CAS	
CS1H	Area 5 CASH	Area 5 $\overline{WEL}$	Area 5 CAS	
$\overline{DW0}$	Area 4 $\overline{WE}$	Area 4 $\overline{WEH}$	Area 4 $\overline{WE}$	
$\overline{DW1}$	Area 5 $\overline{WE}$	Area 5 $\overline{WEH}$	Area 5 $\overline{WE}$	

## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> <li>Oscillation feedback resistance 1 MΩ approx.</li> <li>With standby control</li> </ul>
B		<ul style="list-style-type: none"> <li>CMOS level</li> <li>Hysteresis input</li> <li>Without standby control</li> <li>With pull-up resistance</li> </ul>
C		<ul style="list-style-type: none"> <li>CMOS level I/O</li> <li>With standby control</li> </ul>
D		<ul style="list-style-type: none"> <li>Analog input</li> </ul>

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# MB91101/MB91101A

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Type	Circuit	Remarks
F		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level Hysteresis input With standby control</li> </ul>
G		<ul style="list-style-type: none"> <li>• CMOS level input Without standby control</li> </ul>
H		<ul style="list-style-type: none"> <li>• CMOS level Hysteresis input Without standby control</li> </ul>
L		<ul style="list-style-type: none"> <li>• CMOS level output</li> </ul>

## ■ HANDLING DEVICES

### 1. Preventing Latchup

In CMOS ICs, applying voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  to input/output pin or applying voltage over rating across  $V_{CC}$  and  $V_{SS}$  may cause latchup.

This phenomenon rapidly increases the power supply current, which may result in thermal breakdown of the device. Make sure to prevent the voltage from exceeding the maximum rating.

Take care that the analog power supply ( $AV_{CC}$ ,  $AVRH$ ) and the analog input do not exceed the digital power supply ( $V_{CC}$ ) when the analog power supply turned on or off.

### 2. Treatment of Unused Pins

Unused pins left open may cause malfunctions. Make sure to connect them to pull-up or pull-down resistors.

### 3. External Reset Input

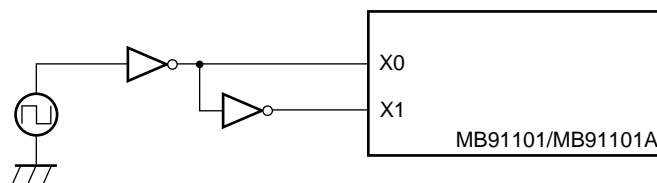
It takes at least 5 machine cycle to input "L" level to the  $\overline{RST}$  pin and to ensure inner reset operation properly.

### 4. Remarks for External Clock Operation

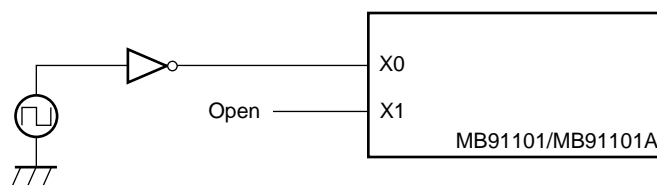
When external clock is selected, supply it to X0 pin generally, and simultaneously the opposite phase clock to X0 must be supplied to X1 pin. However, in this case the stop mode must not be used (because X1 pin stops at "H" output in stop mode).

And it can be used to supply only to X0 pin with 5 V power supply at 12.5 MHz and less than.

#### • Using an external clock



Using an external clock (normal)  
Note: Stop mode (oscillation stop mode) can not be used.



Using an external clock (can be used at 12.5 MHz and less than.)  
(5 V power supply only)

### 5. Power Supply Pins

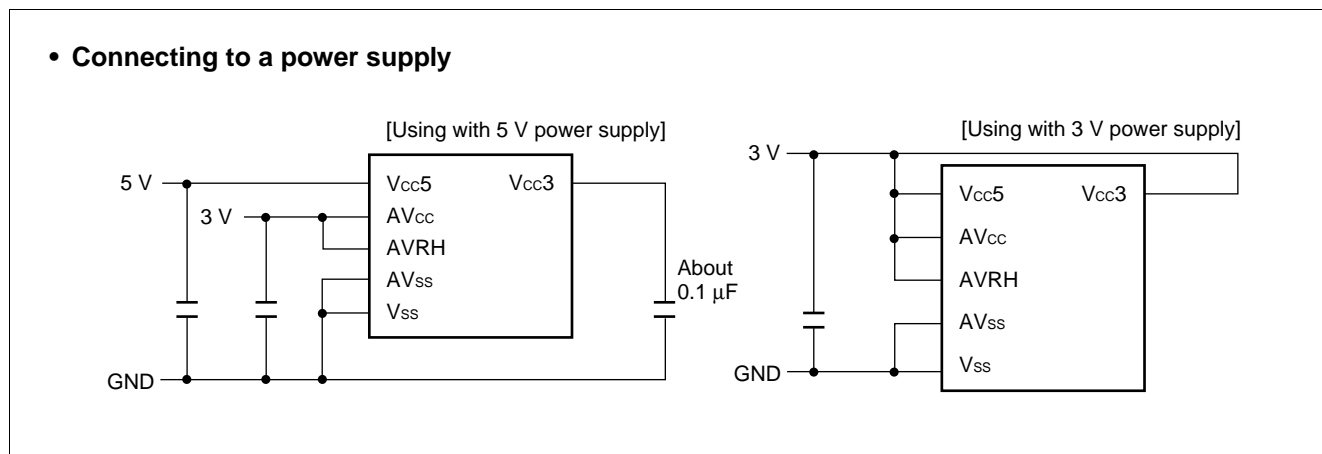
When there are several  $V_{CC}$  and  $V_{SS}$  pins, each of them is equipotentially connected to its counterpart inside of the device, minimizing the risk of malfunctions such as latch up. To further reduce the risk of malfunctions, to prevent EMI radiation, to prevent strobe signal malfunction resulting from creeping-up of ground level and to observe the total output current standard, connect all  $V_{CC}$  and  $V_{SS}$  pins to the power supply or GND.

It is preferred to connect  $V_{CC}$  and  $V_{SS}$  of the MB91101 and MB91101A to power supply with minimal impedance possible.

It is also recommended to connect a ceramic capacitor as a bypass capacitor of about 0.1  $\mu\text{F}$  between  $V_{CC}$  and  $V_{SS}$  at a position as close as possible to the MB91101 and MB91101A.

# MB91101/MB91101A

The MB91101 and MB91101A have an internal regulator. When using with 5 V power supply, supply 5 V to V<sub>cc5</sub> pin and make sure to connect about 0.1  $\mu$ F bypass capacitor to V<sub>cc3</sub> pin for regulator. And another 3 V power supply is needed for the A/D converter. When using with 3 V power supply, connect both V<sub>cc5</sub> pin and V<sub>cc3</sub> pin to the 3 V power supply.



## 6. Crystal Oscillator Circuit

Noises around X0 and X1 pins may cause malfunctions of the MB91101 and MB91101A. In designing the PC board, layout X0 and X1 pins, crystal oscillator (or ceramic oscillator) and bypass capacitor for grounding as close as possible.

It is strongly recommended to design PC board so that X1 and X0 pins are surrounded by grounding area for stable operation.

## 7. Turning-on Sequence of A/D Converter Power Supply and Analog Input

Make sure to turn on the digital power supply (V<sub>cc</sub>) before turning on the A/D converter (AV<sub>cc</sub>, AVRH) and applying voltage to analog input (AN0 to AN3).

Make sure to turn off digital power supply after power supply to A/D converters and analog inputs have been switched off. (There are no such limitations in turning on power supplies. Analog and digital power supplies may be turned on simultaneously.) Make sure that AVRH never exceeds AV<sub>cc</sub> when turning on/off power supplies.

## 8. Fluctuation of Power Supply Voltage

Warranty range for normal operation against fluctuation of power supply voltage V<sub>cc</sub> is as given in rating. However, sudden fluctuation of power supply voltage within the warranty range may cause malfunctions. It is recommended to make every effort to stabilize the power supply voltage to IC. It is also recommended that by controlling power supply as a reference of stabilizing, V<sub>cc</sub> ripple fluctuation (P-P value) at the commercial frequency (50 Hz to 60 Hz) should be less than 10% of the standard V<sub>cc</sub> value and the transient regulation should be less than 0.1 V/ms at instantaneous deviation like turning off the power supply.

## 9. Mode Setting Pins (MD0 to MD2)

Connect mode setting pins (MD0 to MD2) directly to V<sub>cc</sub> or V<sub>ss</sub>.

Arrange each mode setting pin and V<sub>cc</sub> or V<sub>ss</sub> patterns on the printed circuit board as close as possible and make the impedance between them minimal to prevent mistaken entrance to the test mode caused by noises.

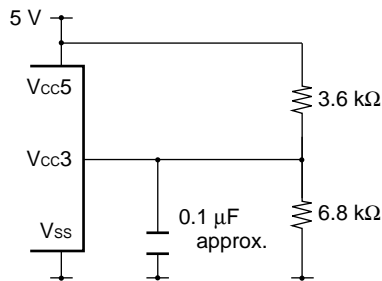
## 10. Internal DC Regulator

Internal DC regulator stops in stop mode. When the regulator stops owing to the increase of inner leakage current (I<sub>CCH</sub>) in stop mode, malfunction caused by noise or any troubles about power supply in normal operation, the internal 3 V power supply voltage may decrease less than the warranty range for normal operation. So when using the internal regulator and stop mode with 5 V power supply, never fail to support externally so that 3 V power supply voltage might not decrease. However, even in such a case, the internal regulator can be restarted



by inputting the reset procedure. (In this case, set the reset to "L" level within the oscillation stabilizing waiting time.)

- Using STOP mode with 5 V power supply



## 11. Pin Condition at Turning on the Power Supply

The pin condition at turning on the power supply is unstable. The circuit starts being initialized after turning on the power supply and then starting oscillation and then the operation of the internal regulator becomes stable. So it takes about 42 ms for the pin to be initialized from the oscillation starting at the source oscillation 12.5 MHz. Take care that the pin condition may be output condition at initial unstable condition.

(With the MB91101A, however, initialization can be achieved in less than about 42 ms after turning on the internal power supply by maintaining the  $\overline{\text{RST}}$  pin at "L" level.)

## 12. Source Oscillation Input at Turning on the Power Supply

At turning on the power supply, never fail to input the clock before cancellation of the oscillation stabilizing waiting.

## 13. Hardware Stand-by at Turning on the Power Supply

When turning on the power supply with the  $\overline{\text{HST}}$  pin being set to "L" level, the hardware doesn't stand by. However the  $\overline{\text{HST}}$  pin becomes available after the reset cancellation, the  $\overline{\text{HST}}$  pin must once be back to "H" level.

## 14. Power on Reset

Make sure to make power on reset at turning on the power supply or returning on the power supply when the power supply voltage is below the warranty range for normal operation.

## 15. Notes on during operation of PLL clock mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

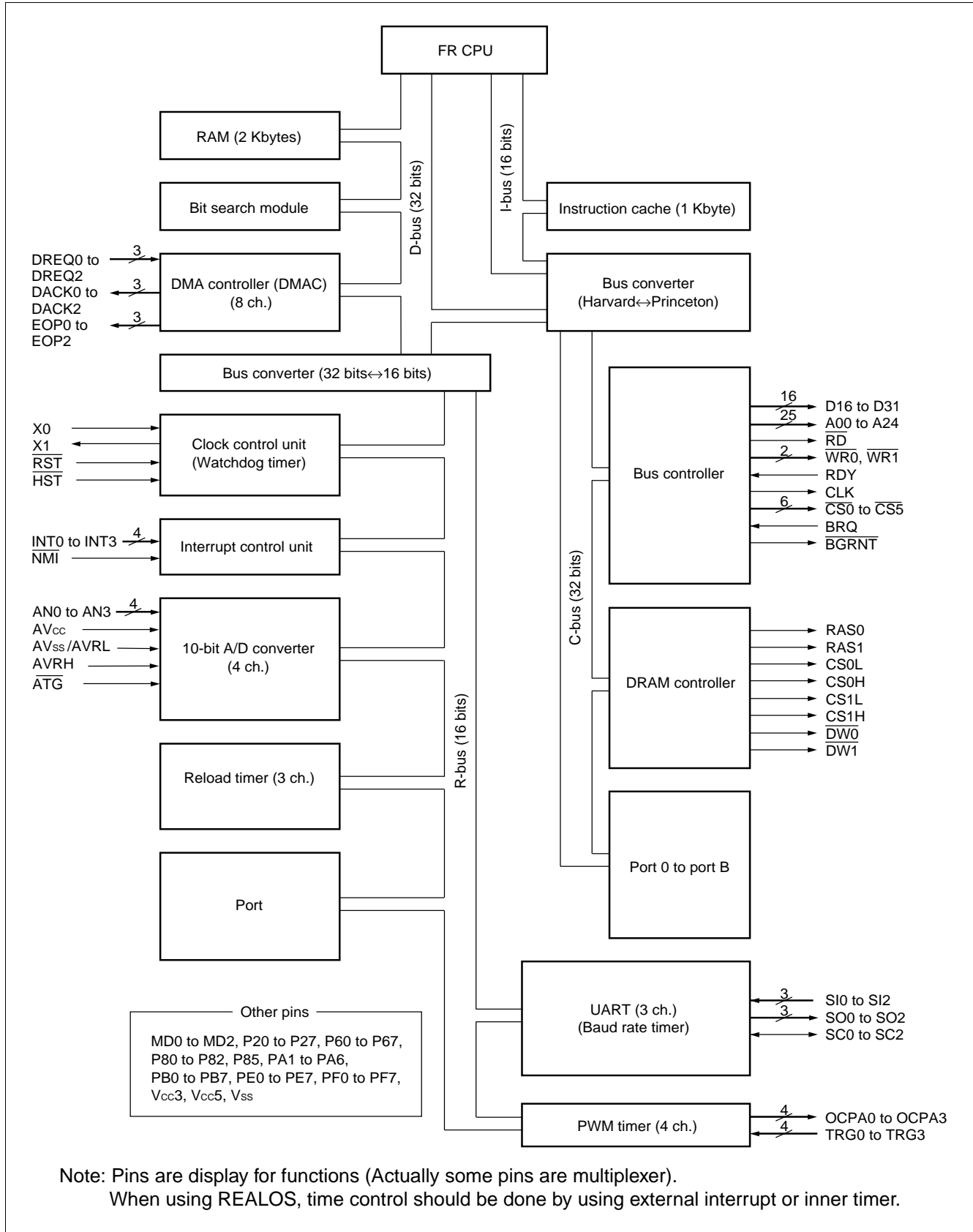
## 16. Watchdog timer function

The watchdog timer supported by the FR family monitors the program that performs the reset delay operation for a specified time. If the program hangs and the reset delay operation is not performed, the watchdog timer resets the CPU. Therefore, once the watchdog timer is enabled, operation continues until the CPU is reset.

As an exception, a reset delay automatically occurs if the CPU stops program execution.

# MB91101/MB91101A

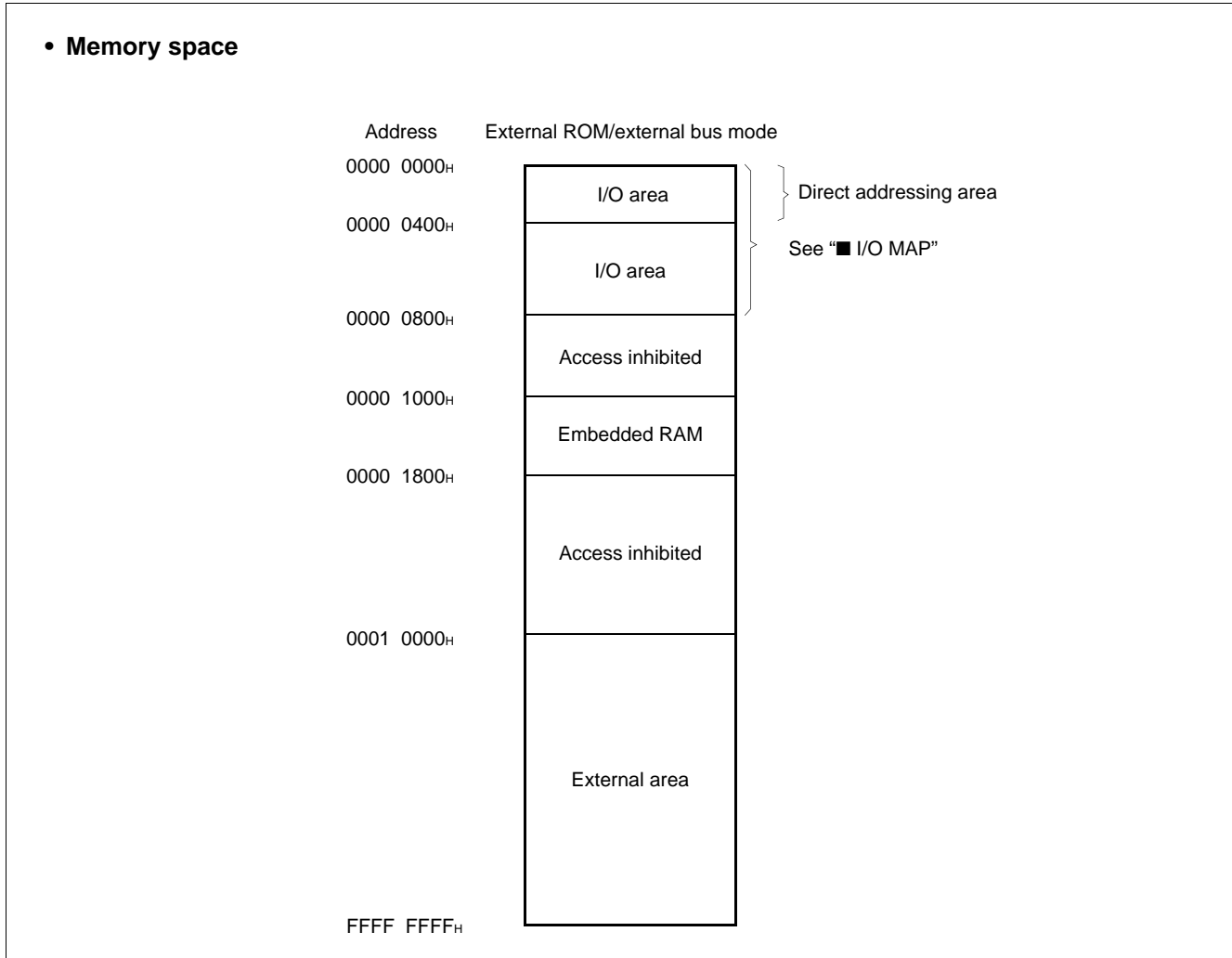
## ■ BLOCK DIAGRAM



## ■ CPU CORE

### 1. Memory Space

The FR family has a logical address space of 4 Gbytes ( $2^{32}$  bytes) and the CPU linearly accesses the memory space.



#### • Direct addressing area

The following areas on the memory space are assigned to direct addressing area for I/O. In these areas, an address can be specified in a direct operand of a code.

Direct areas consists of the following areas dependent on accessible data sizes.

Byte data access: 000<sub>H</sub> to 0FF<sub>H</sub>

Half word data access: 000<sub>H</sub> to 1FF<sub>H</sub>

Word data access: 000<sub>H</sub> to 3FF<sub>H</sub>

# MB91101/MB91101A

## 2. Registers

The FR family has two types of registers; dedicated registers embedded on the CPU and general-purpose registers on memory.

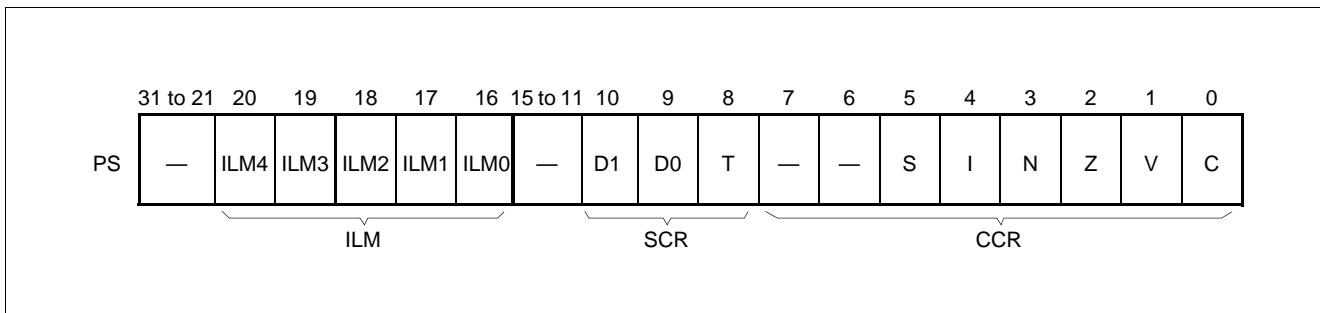
### • Dedicated registers

- Program counter (PC): 32-bit length, indicates the location of the instruction to be executed.
- Program status (PS): 32-bit length, register for storing register pointer or condition codes
- Table base register (TBR): Holds top address of vector table used in EIT (Exceptional/Interrupt/Trap) processing.
- Return pointer (RP): Holds address to resume operation after returning from a subroutine.
- System stack pointer (SSP): Indicates system stack space.
- User's stack pointer (USP): Indicates user's stack space.
- Multiplication/division result register (MDH/MDL): 32-bit length, register for multiplication/division

		Initial value	
← 32 bits →	PC	Program counter	XXXX XXXX <sub>H</sub> Indeterminate
	PS	Program status	
	TBR	Table base register	000F FC00 <sub>H</sub>
	RP	Return pointer	XXXX XXXX <sub>H</sub> Indeterminate
	SSP	System stack pointer	0000 0000 <sub>H</sub>
	USP	User's stack pointer	XXXX XXXX <sub>H</sub> Indeterminate
	MDH	Multiplication/division result register	XXXX XXXX <sub>H</sub> Indeterminate
	MDL		XXXX XXXX <sub>H</sub> Indeterminate

### • Program status (PS)

The PS register is for holding program status and consists of a condition code register (CCR), a system condition code register (SCR) and a interrupt level mask register (ILM).



- **Condition code register (CCR)**

S-flag: Specifies a stack pointer used as R15.

I-flag: Controls user interrupt request enable/disable.

N-flag: Indicates sign bit when division result is assumed to be in the 2's complement format.

Z-flag: Indicates whether or not the result of division was "0".

V-flag: Assumes the operand used in calculation in the 2's complement format and indicates whether or not overflow has occurred.

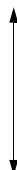
C-flag: Indicates if a carry or borrow from the MSB has occurred.

- **System condition code register (SCR)**

T-flag: Specifies whether or not to enable step trace trap.

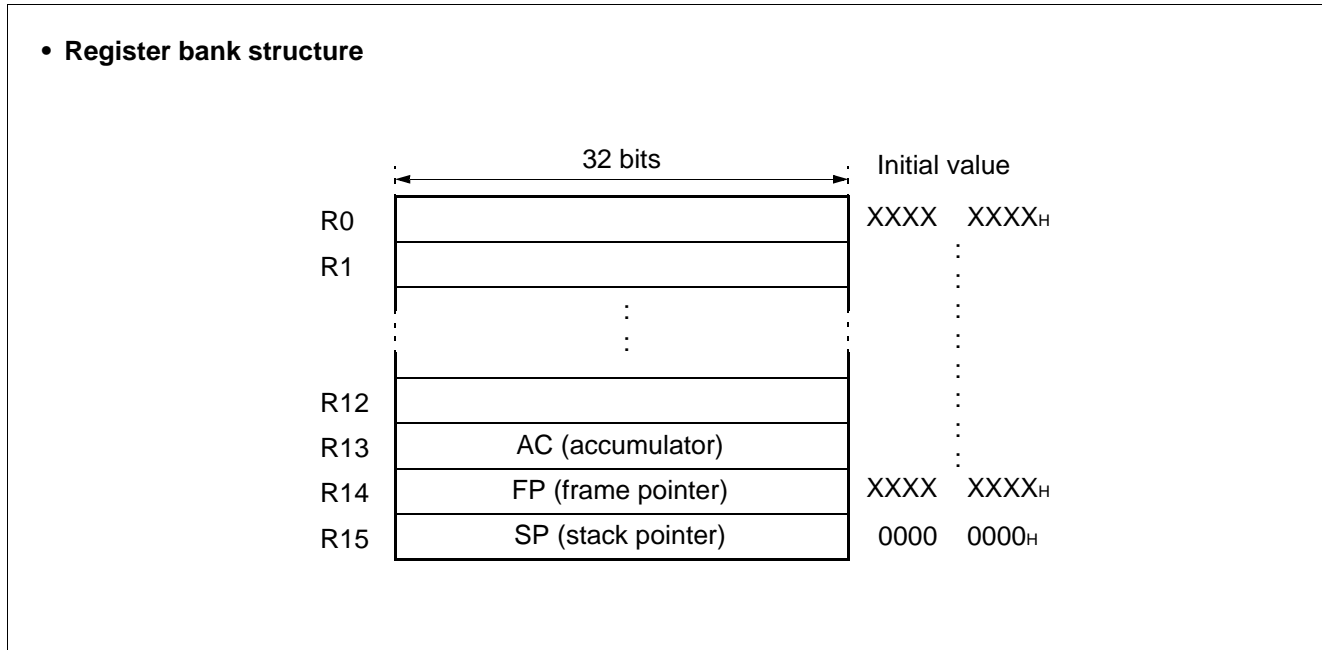
- **Interrupt level mask register (ILM)**

ILM4 to ILM0: Register for holding interrupt level mask value. The value held by this register is used as a level mask. When an interrupt request issued to the CPU is higher than the level held by ILM, the interrupt request is accepted.

ILM4	ILM3	ILM2	ILM1	ILM0	Interrupt level	High-low
0	0	0	0	0	0	High  Low
:					:	
0	1	0	0	0	15	
:					:	
1	1	1	1	1	31	

## ■ GENERAL-PURPOSE REGISTERS

R0 to R15 are general-purpose registers embedded on the CPU. These registers functions as an accumulator and a memory access pointer (field for indicating address).



Of the above 16 registers, following registers have special functions. To support the special functions, part of the instruction set has been sophisticated to have enhanced functions.

- R13: Virtual accumulator (AC)
- R14: Frame pointer (FP)
- R15: Stack pointer (SP)

Upon reset, values in R0 to R14 are not fixed. Value in R15 is initialized to be 0000 0000<sub>H</sub> (SSP value).

## SETTING MODE

### 1. Pin

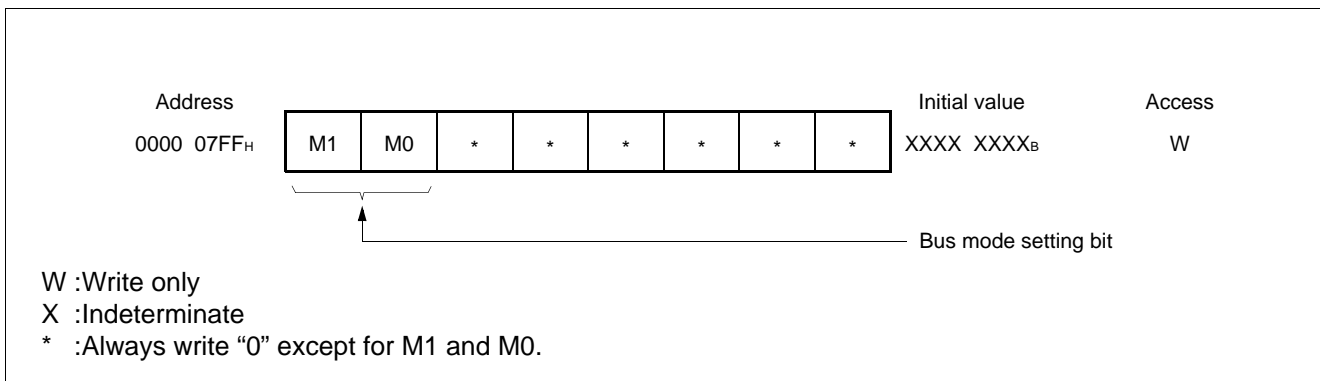
#### • Mode setting pins and modes

Mode setting pins			Mode name	Reset vector access area	External data bus width	Bus mode
MD2	MD1	MD0				
0	0	0	External vector mode 0	External	8 bits	External ROM/external bus mode
0	0	1	External vector mode 1	External	16 bits	
0	1	0	—	—	—	Inhibited
0	1	1	Internal vector mode	Internal	(Mode register)	Single-chip mode*
1	—	—	—	—	—	Inhibited

\*: The MB91101 and MB91101A do not support single-chip mode.

### 2. Registers

#### • Mode setting registers (MODR) and modes



#### • Bus mode setting bits and functions

M1	M0	Functions	Note
0	0	Single-chip mode	
0	1	Internal ROM/external bus mode	
1	0	External ROM/external bus mode	
1	1	—	Inhibited

Note: Because of without internal ROM, the MB91101 and MB91101A allow "10<sub>b</sub>" setting value only.

# MB91101/MB91101A

## ■ I/O MAP

Address	Abbreviation	Register name	Read/write	Initial value
0000H	(Reserved)			
0001H	PDR2	Port 2 data register	R/W	XXXXXXXX <sub>B</sub>
0002H to 0004H	(Reserved)			
0005H	PDR6	Port 6 data register	R/W	XXXXXXXX <sub>B</sub>
0006H 0007H	(Reserved)			
0008H	PDRB	Port B data register	R/W	XXXXXXXX <sub>B</sub>
0009H	PDRA	Port A data register	R/W	_XXXXXX_ <sub>B</sub>
000AH	(Reserved)			
000BH	PDR8	Port 8 data register	R/W	_ _ X _ _ XXX <sub>B</sub>
000CH to 0011H	(Reserved)			
0012H	PDRE	Port E data register	R/W	XXXXXXXX <sub>B</sub>
0013H	PDRF	Port F data register	R/W	XXXXXXXX <sub>B</sub>
0014H to 001BH	(Reserved)			
001CH	SSR0	Serial status register 0	R/W	0 0 0 0 1 _ 0 0 <sub>B</sub>
001DH	SIDR0/SODR0	Serial input register 0/serial output register 0	R/W	XXXXXXXX <sub>B</sub>
001EH	SCR0	Serial control register 0	R/W	0 0 0 0 0 1 0 0 <sub>B</sub>
001FH	SMR0	Serial mode register 0	R/W	0 0 _ _ 0 _ 0 0 <sub>B</sub>
0020H	SSR1	Serial status register 1	R/W	0 0 0 0 1 _ 0 0 <sub>B</sub>
0021H	SIDR1/SODR1	Serial input register 1/serial output register 1	R/W	XXXXXXXX <sub>B</sub>
0022H	SCR1	Serial control register 1	R/W	0 0 0 0 0 1 0 0 <sub>B</sub>
0023H	SMR2	Serial mode register 1	R/W	0 0 _ _ 0 _ 0 0 <sub>B</sub>
0024H	SSR2	Serial status register 2	R/W	0 0 0 0 1 _ 0 0 <sub>B</sub>
0025H	SIDR2/SODR2	Serial input register 2/serial output register 2	R/W	XXXXXXXX <sub>B</sub>
0026H	SCR2	Serial control register 2	R/W	0 0 0 0 0 1 0 0 <sub>B</sub>
0027H	SMR2	Serial mode register 2	R/W	0 0 _ _ 0 _ 0 0 <sub>B</sub>

(Continued)



# MB91101/MB91101A

Address	Abbreviation	Register name	Read/write	Initial value
0028 <sub>H</sub>	TMRLR0	16-bit reload register ch. 0	W	XXXXXXXX <sub>B</sub>
0029 <sub>H</sub>				XXXXXXXX <sub>B</sub>
002A <sub>H</sub>	TMR0	16-bit timer register ch. 0	R	XXXXXXXX <sub>B</sub>
002B <sub>H</sub>				XXXXXXXX <sub>B</sub>
002C <sub>H</sub>	(Reserved)			
002D <sub>H</sub>				
002E <sub>H</sub>	TMCSR0	16-bit reload timer control status register ch. 0	R/W	----0000 <sub>B</sub>
002F <sub>H</sub>				00000000 <sub>B</sub>
0030 <sub>H</sub>	TMRLR1	16-bit reload register ch. 1	W	XXXXXXXX <sub>B</sub>
0031 <sub>H</sub>				XXXXXXXX <sub>B</sub>
0032 <sub>H</sub>	TMR1	16-bit timer register ch. 1	R	XXXXXXXX <sub>B</sub>
0033 <sub>H</sub>				XXXXXXXX <sub>B</sub>
0034 <sub>H</sub>	(Reserved)			
0035 <sub>H</sub>				
0036 <sub>H</sub>	TMCSR1	16-bit reload timer control status register ch. 1	R/W	----0000 <sub>B</sub>
0037 <sub>H</sub>				00000000 <sub>B</sub>
0038 <sub>H</sub>	ADCR	A/D converter data register	R	-----XX <sub>B</sub>
0039 <sub>H</sub>				XXXXXXXX <sub>B</sub>
003A <sub>H</sub>	ADCS	A/D converter control status register	R/W	00000000 <sub>B</sub>
003B <sub>H</sub>				00000000 <sub>B</sub>
003C <sub>H</sub>	TMRLR2	16-bit reload register ch. 2	W	XXXXXXXX <sub>B</sub>
003D <sub>H</sub>				XXXXXXXX <sub>B</sub>
003E <sub>H</sub>	TMR2	16-bit timer register ch. 2	R	XXXXXXXX <sub>B</sub>
003F <sub>H</sub>				XXXXXXXX <sub>B</sub>
0040 <sub>H</sub>	(Reserved)			
0041 <sub>H</sub>				
0042 <sub>H</sub>	TMCSR2	16-bit reload timer control status register ch. 2	R/W	----0000 <sub>B</sub>
0043 <sub>H</sub>				00000000 <sub>B</sub>
0044 <sub>H</sub> to 0077 <sub>H</sub>	(Reserved)			

(Continued)

# MB91101/MB91101A

Address	Abbreviation	Register name	Read/write	Initial value
0078 <sub>H</sub>	UTIM0/UTIMR0	U-TIMER register ch. 0/reload register ch. 0	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
0079 <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
007A <sub>H</sub>	(Reserved)			
007B <sub>H</sub>	UTIMC0	U-TIMER control register ch. 0	R/W	0 _ _ 0 0 0 0 1 <sub>B</sub>
007C <sub>H</sub>	UTIM1/UTIMR1	U-TIMER register ch. 1/reload register ch. 1	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
007D <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
007E <sub>H</sub>	(Reserved)			
007F <sub>H</sub>	UTIMC1	U-TIMER control register ch. 1	R/W	0 _ _ 0 0 0 0 1 <sub>B</sub>
0080 <sub>H</sub>	UTIM2/UTIMR2	U-TIMER register ch. 2/reload register ch. 2	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
0081 <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
0082 <sub>H</sub>	(Reserved)			
0083 <sub>H</sub>	UTIMC2	U-TIMER control register ch. 2	R/W	0 _ _ 0 0 0 0 1 <sub>B</sub>
0084 <sub>H</sub> to 0093 <sub>H</sub>	(Reserved)			
0094 <sub>H</sub>	EIRR	External interrupt cause register	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
0095 <sub>H</sub>	ENIR	Interrupt enable register	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
0096 <sub>H</sub> to 0098 <sub>H</sub>	(Reserved)			
0099 <sub>H</sub>	ELVR	External interrupt request level setting register	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
009A <sub>H</sub> to 00D1 <sub>H</sub>	(Reserved)			
00D2 <sub>H</sub>	DDRE	Port E data direction register	W	0 0 0 0 0 0 0 0 <sub>B</sub>
00D3 <sub>H</sub>	DDRF	Port F data direction register	W	0 0 0 0 0 0 0 0 <sub>B</sub>
00D4 <sub>H</sub> to 00DB <sub>H</sub>	(Reserved)			
00DC <sub>H</sub>	GCN1	General control register 1	R/W	0 0 1 1 0 0 1 0 <sub>B</sub>
00DD <sub>H</sub>				0 0 0 1 0 0 0 0 <sub>B</sub>
00DE <sub>H</sub>	(Reserved)			
00DF <sub>H</sub>	GCN2	General control register 2	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>

(Continued)

# MB91101/MB91101A

Address	Abbreviation	Register name	Read/write	Initial value
00E0 <sub>H</sub>	PTMR0	Ch. 0 timer register	R	1 1 1 1 1 1 1 1 <sub>B</sub>
00E1 <sub>H</sub>				1 1 1 1 1 1 1 1 <sub>B</sub>
00E2 <sub>H</sub>	PCSR0	Ch. 0 cycle setting register	W	XXXXXXXX <sub>B</sub>
00E3 <sub>H</sub>				XXXXXXXX <sub>B</sub>
00E4 <sub>H</sub>	PDUT0	Ch. 0 duty setting register	W	XXXXXXXX <sub>B</sub>
00E5 <sub>H</sub>				XXXXXXXX <sub>B</sub>
00E6 <sub>H</sub>	PCNH0	Ch. 0 control status register H	R/W	0 0 0 0 0 0 0 _ <sub>B</sub>
00E7 <sub>H</sub>	PCNL0	Ch. 0 control status register L	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
00E8 <sub>H</sub>	PTMR1	Ch. 1 timer register	R	1 1 1 1 1 1 1 1 <sub>B</sub>
00E9 <sub>H</sub>				1 1 1 1 1 1 1 1 <sub>B</sub>
00EA <sub>H</sub>	PCSR1	Ch. 1 cycle setting register	W	XXXXXXXX <sub>B</sub>
00EB <sub>H</sub>				XXXXXXXX <sub>B</sub>
00EC <sub>H</sub>	PDUT1	Ch. 1 duty setting register	W	XXXXXXXX <sub>B</sub>
00ED <sub>H</sub>				XXXXXXXX <sub>B</sub>
00EE <sub>H</sub>	PCNH1	Ch. 1 control status register H	R/W	0 0 0 0 0 0 0 _ <sub>B</sub>
00EF <sub>H</sub>	PCNL1	Ch. 1 control status register L	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
00F0 <sub>H</sub>	PTMR2	Ch. 2 timer register	R	1 1 1 1 1 1 1 1 <sub>B</sub>
00F1 <sub>H</sub>				1 1 1 1 1 1 1 1 <sub>B</sub>
00F2 <sub>H</sub>	PCSR2	Ch. 2 cycle setting register	W	XXXXXXXX <sub>B</sub>
00F3 <sub>H</sub>				XXXXXXXX <sub>B</sub>
00F4 <sub>H</sub>	PDUT2	Ch. 2 duty setting register	W	XXXXXXXX <sub>B</sub>
00F5 <sub>H</sub>				XXXXXXXX <sub>B</sub>
00F6 <sub>H</sub>	PCNH2	Ch. 2 control status register H	R/W	0 0 0 0 0 0 0 _ <sub>B</sub>
00F7 <sub>H</sub>	PCNL2	Ch. 2 control status register L	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
00F8 <sub>H</sub>	PTMR3	Ch. 3 timer register	R	1 1 1 1 1 1 1 1 <sub>B</sub>
00F9 <sub>H</sub>				1 1 1 1 1 1 1 1 <sub>B</sub>
00FA <sub>H</sub>	PCSR3	Ch. 3 cycle setting register	W	XXXXXXXX <sub>B</sub>
00FB <sub>H</sub>				XXXXXXXX <sub>B</sub>
00FC <sub>H</sub>	PDUT3	Ch. 3 duty setting register	W	XXXXXXXX <sub>B</sub>
00FD <sub>H</sub>				XXXXXXXX <sub>B</sub>
00FE <sub>H</sub>	PCNH3	Ch. 3 control status register H	R/W	0 0 0 0 0 0 0 _ <sub>B</sub>
00FF <sub>H</sub>	PCNL3	Ch. 3 control status register L	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>

(Continued)

# MB91101/MB91101A

Address	Abbreviation	Register name	Read/write	Initial value
0100 <sub>H</sub> to 01FF <sub>H</sub>	(Reserved)			
0200 <sub>H</sub>	DPDP	DMAC parameter descriptor pointer	R/W	XXXXXXXX <sub>B</sub>
0201 <sub>H</sub>				XXXXXXXX <sub>B</sub>
0202 <sub>H</sub>				XXXXXXXX <sub>B</sub>
0203 <sub>H</sub>				X 0 0 0 0 0 0 0 <sub>B</sub>
0204 <sub>H</sub>	DACSR	DMAC control status register	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
0205 <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
0206 <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
0207 <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
0208 <sub>H</sub>	DATCR	DMAC pin control register	R/W	XXXXXXXX <sub>B</sub>
0209 <sub>H</sub>				XXXX 0 0 0 0 <sub>B</sub>
020A <sub>H</sub>				XXXX 0 0 0 0 <sub>B</sub>
020B <sub>H</sub>				XXXX 0 0 0 0 <sub>B</sub>
020C <sub>H</sub> to 03E3 <sub>H</sub>	(Reserved)			
03E4 <sub>H</sub>	ICHCR	Instruction cache control register	R/W	_____B
03E5 <sub>H</sub>				_____B
03E6 <sub>H</sub>				_____B
03E7 <sub>H</sub>				__ 0 0 0 0 0 <sub>B</sub>
03E8 <sub>H</sub> to 03EF <sub>H</sub>	(Reserved)			
03F0 <sub>H</sub>	BSD0	Bit search module 0-detection data register	W	XXXXXXXX <sub>B</sub>
03F1 <sub>H</sub>				XXXXXXXX <sub>B</sub>
03F2 <sub>H</sub>				XXXXXXXX <sub>B</sub>
03F3 <sub>H</sub>				XXXXXXXX <sub>B</sub>
03F4 <sub>H</sub>	BSD1	Bit search module 1-detection data register	R/W	XXXXXXXX <sub>B</sub>
03F5 <sub>H</sub>				XXXXXXXX <sub>B</sub>
03F6 <sub>H</sub>				XXXXXXXX <sub>B</sub>
03F7 <sub>H</sub>				XXXXXXXX <sub>B</sub>

(Continued)

# MB91101/MB91101A

Address	Abbreviation	Register name	Read/write	Initial value
03F8 <sub>H</sub>	BSDC	Bit search module transition-detection data register	W	XXXXXXXX <sub>B</sub>
03F9 <sub>H</sub>				XXXXXXXX <sub>B</sub>
03FA <sub>H</sub>				XXXXXXXX <sub>B</sub>
03FB <sub>H</sub>				XXXXXXXX <sub>B</sub>
03FC <sub>H</sub>	BSRR	Bit search module detection result register	R	XXXXXXXX <sub>B</sub>
03FD <sub>H</sub>				XXXXXXXX <sub>B</sub>
03FE <sub>H</sub>				XXXXXXXX <sub>B</sub>
03FF <sub>H</sub>				XXXXXXXX <sub>B</sub>
0400 <sub>H</sub>	ICR00	Interrupt control register 0	R/W	___ 1 1 1 1 1 <sub>B</sub>
0401 <sub>H</sub>	ICR01	Interrupt control register 1	R/W	___ 1 1 1 1 1 <sub>B</sub>
0402 <sub>H</sub>	ICR02	Interrupt control register 2	R/W	___ 1 1 1 1 1 <sub>B</sub>
0403 <sub>H</sub>	ICR03	Interrupt control register 3	R/W	___ 1 1 1 1 1 <sub>B</sub>
0404 <sub>H</sub>	ICR04	Interrupt control register 4	R/W	___ 1 1 1 1 1 <sub>B</sub>
0405 <sub>H</sub>	ICR05	Interrupt control register 5	R/W	___ 1 1 1 1 1 <sub>B</sub>
0406 <sub>H</sub>	ICR06	Interrupt control register 6	R/W	___ 1 1 1 1 1 <sub>B</sub>
0407 <sub>H</sub>	ICR07	Interrupt control register 7	R/W	___ 1 1 1 1 1 <sub>B</sub>
0408 <sub>H</sub>	ICR08	Interrupt control register 8	R/W	___ 1 1 1 1 1 <sub>B</sub>
0409 <sub>H</sub>	ICR09	Interrupt control register 9	R/W	___ 1 1 1 1 1 <sub>B</sub>
040A <sub>H</sub>	ICR10	Interrupt control register 10	R/W	___ 1 1 1 1 1 <sub>B</sub>
040B <sub>H</sub>	ICR11	Interrupt control register 11	R/W	___ 1 1 1 1 1 <sub>B</sub>
040C <sub>H</sub>	ICR12	Interrupt control register 12	R/W	___ 1 1 1 1 1 <sub>B</sub>
040D <sub>H</sub>	ICR13	Interrupt control register 13	R/W	___ 1 1 1 1 1 <sub>B</sub>
040E <sub>H</sub>	ICR14	Interrupt control register 14	R/W	___ 1 1 1 1 1 <sub>B</sub>
040F <sub>H</sub>	ICR15	Interrupt control register 15	R/W	___ 1 1 1 1 1 <sub>B</sub>
0410 <sub>H</sub>	ICR16	Interrupt control register 16	R/W	___ 1 1 1 1 1 <sub>B</sub>
0411 <sub>H</sub>	ICR17	Interrupt control register 17	R/W	___ 1 1 1 1 1 <sub>B</sub>
0412 <sub>H</sub>	ICR18	Interrupt control register 18	R/W	___ 1 1 1 1 1 <sub>B</sub>
0413 <sub>H</sub>	ICR19	Interrupt control register 19	R/W	___ 1 1 1 1 1 <sub>B</sub>
0414 <sub>H</sub>	ICR20	Interrupt control register 20	R/W	___ 1 1 1 1 1 <sub>B</sub>
0415 <sub>H</sub>	ICR21	Interrupt control register 21	R/W	___ 1 1 1 1 1 <sub>B</sub>
0416 <sub>H</sub>	ICR22	Interrupt control register 22	R/W	___ 1 1 1 1 1 <sub>B</sub>

(Continued)

# MB91101/MB91101A

Address	Abbreviation	Register name	Read/write	Initial value
0417 <sub>H</sub>	ICR23	Interrupt control register 23	R/W	___ 1 1 1 1 1 <sub>B</sub>
0418 <sub>H</sub>	ICR24	Interrupt control register 24	R/W	___ 1 1 1 1 1 <sub>B</sub>
0419 <sub>H</sub>	ICR25	Interrupt control register 25	R/W	___ 1 1 1 1 1 <sub>B</sub>
041A <sub>H</sub>	ICR26	Interrupt control register 26	R/W	___ 1 1 1 1 1 <sub>B</sub>
041B <sub>H</sub>	ICR27	Interrupt control register 27	R/W	___ 1 1 1 1 1 <sub>B</sub>
041C <sub>H</sub>	ICR28	Interrupt control register 28	R/W	___ 1 1 1 1 1 <sub>B</sub>
041D <sub>H</sub>	ICR29	Interrupt control register 29	R/W	___ 1 1 1 1 1 <sub>B</sub>
041E <sub>H</sub>	ICR30	Interrupt control register 30	R/W	___ 1 1 1 1 1 <sub>B</sub>
041F <sub>H</sub>	ICR31	Interrupt control register 31	R/W	___ 1 1 1 1 1 <sub>B</sub>
042F <sub>H</sub>	ICR47	Interrupt control register 47	R/W	___ 1 1 1 1 1 <sub>B</sub>
0430 <sub>H</sub>	DICR	Delayed interrupt control register	R/W	_____ 0 <sub>B</sub>
0431 <sub>H</sub>	HRCL	Hold request cancel request level setting register	R/W	___ 1 1 1 1 1 <sub>B</sub>
0432 <sub>H</sub> to 047F <sub>H</sub>	(Reserved)			
0480 <sub>H</sub>	RSRR/WTCR	Reset cause register/ watchdog peripheral control register	R/W	1 XXXX _ 0 0 <sub>B</sub>
0481 <sub>H</sub>	STCR	Standby control register	R/W	0 0 0 1 1 1 __ <sub>B</sub>
0482 <sub>H</sub>	PDRR	DMA controller request squelch register	R/W	_____ 0 0 0 0 <sub>B</sub>
0483 <sub>H</sub>	CTBR	Timebase timer clear register	W	XXXXXXXX <sub>B</sub>
0484 <sub>H</sub>	GCR	Gear control register	R/W	1 1 0 0 1 1 _ 1 <sub>B</sub>
0485 <sub>H</sub>	WPR	Watchdog reset occurrence postpone register	W	XXXXXXXX <sub>B</sub>
0486 <sub>H</sub> 0487 <sub>H</sub>	(Reserved)			
0488 <sub>H</sub>	PCTR	PLL control register	R/W	0 0 __ 0 __ __ <sub>B</sub>
0489 <sub>H</sub> to 0600 <sub>H</sub>	(Reserved)			
0601 <sub>H</sub>	DDR2	Port 2 data direction register	W	0 0 0 0 0 0 0 0 <sub>B</sub>
0602 <sub>H</sub> to 0604 <sub>H</sub>	(Reserved)			
0605 <sub>H</sub>	DDR6	Port 6 data direction register	W	0 0 0 0 0 0 0 0 <sub>B</sub>
0606 <sub>H</sub> 0607 <sub>H</sub>	(Reserved)			

(Continued)

# MB91101/MB91101A

Address	Abbreviation	Register name	Read/write	Initial value
0608 <sub>H</sub>	DDRB	Port B data direction register	W	0 0 0 0 0 0 0 0 <sub>B</sub>
0609 <sub>H</sub>	DDRA	Port A data direction register	W	_ 0 0 0 0 0 0 _ <sub>B</sub>
060A <sub>H</sub>	(Reserved)			
060B <sub>H</sub>	DDR8	Port 8 data direction register	W	_ _ 0 _ _ 0 0 0 <sub>B</sub>
060C <sub>H</sub>	ASR1	Area select register 1	W	0 0 0 0 0 0 0 0 <sub>B</sub>
060D <sub>H</sub>				0 0 0 0 0 0 0 1 <sub>B</sub>
060E <sub>H</sub>	AMR1	Area mask register 1	W	0 0 0 0 0 0 0 0 <sub>B</sub>
060F <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
0610 <sub>H</sub>	ASR2	Area select register 2	W	0 0 0 0 0 0 0 0 <sub>B</sub>
0611 <sub>H</sub>				0 0 0 0 0 0 1 0 <sub>B</sub>
0612 <sub>H</sub>	AMR2	Area mask register 2	W	0 0 0 0 0 0 0 0 <sub>B</sub>
0613 <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
0614 <sub>H</sub>	ASR3	Area select register 3	W	0 0 0 0 0 0 0 0 <sub>B</sub>
0615 <sub>H</sub>				0 0 0 0 0 0 1 1 <sub>B</sub>
0616 <sub>H</sub>	AMR3	Area mask register 3	W	0 0 0 0 0 0 0 0 <sub>B</sub>
0617 <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
0618 <sub>H</sub>	ASR4	Area select register 4	W	0 0 0 0 0 0 0 0 <sub>B</sub>
0619 <sub>H</sub>				0 0 0 0 0 1 0 0 <sub>B</sub>
061A <sub>H</sub>	AMR4	Area mask register 4	W	0 0 0 0 0 0 0 0 <sub>B</sub>
061B <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
061C <sub>H</sub>	ASR5	Area select register 5	W	0 0 0 0 0 0 0 0 <sub>B</sub>
061D <sub>H</sub>				0 0 0 0 0 1 0 1 <sub>B</sub>
061E <sub>H</sub>	AMR5	Area mask register 5	W	0 0 0 0 0 0 0 0 <sub>B</sub>
061F <sub>H</sub>				0 0 0 0 0 0 0 0 <sub>B</sub>
0620 <sub>H</sub>	AMD0	Area mode register 0	R/W	_ _ _ 0 0 1 1 1 <sub>B</sub>
0621 <sub>H</sub>	AMD1	Area mode register 1	R/W	0 _ _ 0 0 0 0 0 <sub>B</sub>
0622 <sub>H</sub>	AMD32	Area mode register 32	R/W	0 0 0 0 0 0 0 0 <sub>B</sub>
0623 <sub>H</sub>	AMD4	Area mode register 4	R/W	0 _ _ 0 0 0 0 0 <sub>B</sub>
0624 <sub>H</sub>	AMD5	Area mode register 5	R/W	0 _ _ 0 0 0 0 0 <sub>B</sub>
0625 <sub>H</sub>	DSCR	DRAM signal control register	W	0 0 0 0 0 0 0 0 <sub>B</sub>
0626 <sub>H</sub>	RFCR	Refresh control register	R/W	_ _ XXXXXX <sub>B</sub>
0627 <sub>H</sub>				0 0 _ _ _ 0 0 0 <sub>B</sub>

(Continued)

# MB91101/MB91101A

(Continued)

Address	Abbreviation	Register name	Read/write	Initial value
0628 <sub>H</sub>	EPCR0	External pin control register 0	W	____1100 <sub>B</sub>
0629 <sub>H</sub>				_1111111 <sub>B</sub>
062A <sub>H</sub>	(Reserved)			
062B <sub>H</sub>	EPCR1	External pin control register 1	W	11111111 <sub>B</sub>
062C <sub>H</sub>	DMCR4	DRAM control register 4	R/W	00000000 <sub>B</sub>
062D <sub>H</sub>				0000000_ <sub>B</sub>
062E <sub>H</sub>	DMCR5	DRAM control register 5	R/W	00000000 <sub>B</sub>
062F <sub>H</sub>				0000000_ <sub>B</sub>
0630 <sub>H</sub> to 07FD <sub>H</sub>	(Reserved)			
07FE <sub>H</sub>	LER	Little endian register	W	______000 <sub>B</sub>
07FF <sub>H</sub>	MODR	Mode register	W	XXXXXXXX <sub>B</sub>

Note : Do not use (reserved).



## ■ INTERRUPT CAUSES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTER ALLOCATIONS

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reset	0	00	—	3FC <sub>H</sub>	000FFFFC <sub>H</sub>
Reserved for system	1	01	—	3F8 <sub>H</sub>	000FFF8 <sub>H</sub>
Reserved for system	2	02	—	3F4 <sub>H</sub>	000FFF4 <sub>H</sub>
Reserved for system	3	03	—	3F0 <sub>H</sub>	000FFF0 <sub>H</sub>
Reserved for system	4	04	—	3EC <sub>H</sub>	000FFFE <sub>C</sub>
Reserved for system	5	05	—	3E8 <sub>H</sub>	000FFFE <sub>8</sub>
Reserved for system	6	06	—	3E4 <sub>H</sub>	000FFFE <sub>4</sub>
Reserved for system	7	07	—	3E0 <sub>H</sub>	000FFFE <sub>0</sub>
Reserved for system	8	08	—	3DC <sub>H</sub>	000FFFD <sub>C</sub>
Reserved for system	9	09	—	3D8 <sub>H</sub>	000FFFD <sub>8</sub>
Reserved for system	10	0A	—	3D4 <sub>H</sub>	000FFFD <sub>4</sub>
Reserved for system	11	0B	—	3D0 <sub>H</sub>	000FFFD <sub>0</sub>
Reserved for system	12	0C	—	3CC <sub>H</sub>	000FFF <sub>CC</sub>
Reserved for system	13	0D	—	3C8 <sub>H</sub>	000FFF <sub>C8</sub>
Exception for undefined instruction	14	0E	—	3C4 <sub>H</sub>	000FFF <sub>C4</sub>
NMI request	15	0F	F <sub>H</sub> fixed	3C0 <sub>H</sub>	000FFF <sub>C0</sub>
External interrupt 0	16	10	ICR00	3BC <sub>H</sub>	000FFF <sub>BC</sub>
External interrupt 1	17	11	ICR01	3B8 <sub>H</sub>	000FFF <sub>B8</sub>
External interrupt 2	18	12	ICR02	3B4 <sub>H</sub>	000FFF <sub>B4</sub>
External interrupt 3	19	13	ICR03	3B0 <sub>H</sub>	000FFF <sub>B0</sub>
UART0 receive complete	20	14	ICR04	3AC <sub>H</sub>	000FFF <sub>AC</sub>
UART1 receive complete	21	15	ICR05	3A8 <sub>H</sub>	000FFF <sub>A8</sub>
UART2 receive complete	22	16	ICR06	3A4 <sub>H</sub>	000FFF <sub>A4</sub>
UART0 transmit complete	23	17	ICR07	3A0 <sub>H</sub>	000FFF <sub>A0</sub>
UART1 transmit complete	24	18	ICR08	39C <sub>H</sub>	000FFF <sub>9C</sub>
UART2 transmit complete	25	19	ICR09	398 <sub>H</sub>	000FFF <sub>98</sub>
DMAC0 (complete, error)	26	1A	ICR10	394 <sub>H</sub>	000FFF <sub>94</sub>
DMAC1 (complete, error)	27	1B	ICR11	390 <sub>H</sub>	000FFF <sub>90</sub>
DMAC2 (complete, error)	28	1C	ICR12	38C <sub>H</sub>	000FFF <sub>8C</sub>
DMAC3 (complete, error)	29	1D	ICR13	388 <sub>H</sub>	000FFF <sub>88</sub>
DMAC4 (complete, error)	30	1E	ICR14	384 <sub>H</sub>	000FFF <sub>84</sub>
DMAC5 (complete, error)	31	1F	ICR15	380 <sub>H</sub>	000FFF <sub>80</sub>

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# MB91101/MB91101A

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
DMAC6 (complete, error)	32	20	ICR16	37C <sub>H</sub>	000FFF7C <sub>H</sub>
DMAC7 (complete, error)	33	21	ICR17	378 <sub>H</sub>	000FFF78 <sub>H</sub>
A/D converter (successive approximation conversion type)	34	22	ICR18	374 <sub>H</sub>	000FFF74 <sub>H</sub>
16-bit reload timer 0	35	23	ICR19	370 <sub>H</sub>	000FFF70 <sub>H</sub>
16-bit reload timer 1	36	24	ICR20	36C <sub>H</sub>	000FFF6C <sub>H</sub>
16-bit reload timer 2	37	25	ICR21	368 <sub>H</sub>	000FFF68 <sub>H</sub>
PWM 0	38	26	ICR22	364 <sub>H</sub>	000FFF64 <sub>H</sub>
PWM 1	39	27	ICR23	360 <sub>H</sub>	000FFF60 <sub>H</sub>
PWM 2	40	28	ICR24	35C <sub>H</sub>	000FFF5C <sub>H</sub>
PWM 3	41	29	ICR25	358 <sub>H</sub>	000FFF58 <sub>H</sub>
U-TIMER 0	42	2A	ICR26	354 <sub>H</sub>	000FFF54 <sub>H</sub>
U-TIMER 1	43	2B	ICR27	350 <sub>H</sub>	000FFF50 <sub>H</sub>
U-TIMER 2	44	2C	ICR28	34C <sub>H</sub>	000FFF4C <sub>H</sub>
Reserved for system	45	2D	ICR29	348 <sub>H</sub>	000FFF48 <sub>H</sub>
Reserved for system	46	2E	ICR30	344 <sub>H</sub>	000FFF44 <sub>H</sub>
Reserved for system	47	2F	ICR31	340 <sub>H</sub>	000FFF40 <sub>H</sub>
Reserved for system	48	30	ICR32	33C <sub>H</sub>	000FFF3C <sub>H</sub>
Reserved for system	49	31	ICR33	338 <sub>H</sub>	000FFF38 <sub>H</sub>
Reserved for system	50	32	ICR34	334 <sub>H</sub>	000FFF34 <sub>H</sub>
Reserved for system	51	33	ICR35	330 <sub>H</sub>	000FFF30 <sub>H</sub>
Reserved for system	52	34	ICR36	32C <sub>H</sub>	000FFF2C <sub>H</sub>
Reserved for system	53	35	ICR37	328 <sub>H</sub>	000FFF28 <sub>H</sub>
Reserved for system	54	36	ICR38	324 <sub>H</sub>	000FFF24 <sub>H</sub>
Reserved for system	55	37	ICR39	320 <sub>H</sub>	000FFF20 <sub>H</sub>
Reserved for system	56	38	ICR40	31C <sub>H</sub>	000FFF1C <sub>H</sub>
Reserved for system	57	39	ICR41	318 <sub>H</sub>	000FFF18 <sub>H</sub>
Reserved for system	58	3A	ICR42	314 <sub>H</sub>	000FFF14 <sub>H</sub>
Reserved for system	59	3B	ICR43	310 <sub>H</sub>	000FFF10 <sub>H</sub>
Reserved for system	60	3C	ICR44	30C <sub>H</sub>	000FFF0C <sub>H</sub>
Reserved for system	61	3D	ICR45	308 <sub>H</sub>	000FFF08 <sub>H</sub>
Reserved for system	62	3E	ICR46	304 <sub>H</sub>	000FFF04 <sub>H</sub>
Delayed interrupt cause bit	63	3F	ICR47	300 <sub>H</sub>	000FFF00 <sub>H</sub>

(Continued)

(Continued)

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reserved for system (used in REALOS*)	64	40	—	2FC <sub>H</sub>	000FFEFC <sub>H</sub>
Reserved for system (used in REALOS*)	65	41	—	2F8 <sub>H</sub>	000FEF8 <sub>H</sub>
Used in INT instructions	66 to 255	42 to FF	—	2F4 <sub>H</sub> to 000 <sub>H</sub>	000FEF4 <sub>H</sub> to 000FFC00 <sub>H</sub>

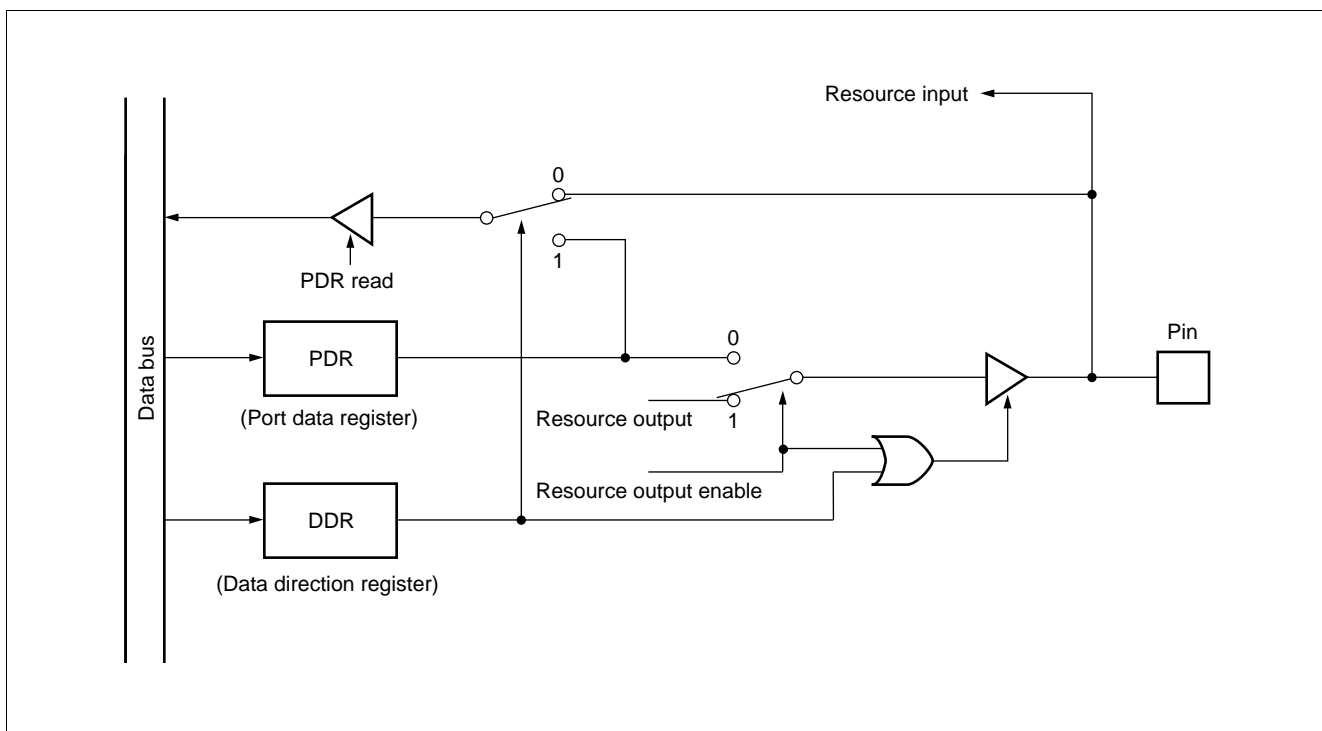
\*: REALOS/FR uses interrupt number 0x40 and 0x41 for system code.

## ■ PERIPHERAL RESOURCES

### 1. I/O Ports

There are 2 types of I/O port register structure; port data register (PDR0 to PDRF) and data direction register (DDR0 to DDRF), where bits PDR0 to PDRF and bits DDR0 to DDRF corresponds respectively. Each bit on the register corresponds to an external pin. In port registers input/output register of the port configures input/output function of the port, while corresponding bit (pin) configures input/output function in data direction registers. Bit "0" specifies input and "1" specifies output.

- For input (DDR = "0") setting;
  - PDR reading operation: reads level of corresponding external pin.
  - PDR writing operation: writes set value to PDR.
- For output (DDR = "1") setting;
  - PDR reading operation: reads PDR value.
  - PDR writing operation: outputs PDR value to corresponding external pin.
- **Block diagram**



## • Port data register

Address	bit 7	bit 0	Initial value	
000001H	PDR2		XXXXXXXX <sub>B</sub>	(R/W)
000005H	PDR6		XXXXXXXX <sub>B</sub>	(R/W)
00000BH	PDR8		-- X -- XXX <sub>B</sub>	(R/W)
000009H	PDRA		- XXXXXX - <sub>B</sub>	(R/W)
000008H	PDRB		XXXXXXXX <sub>B</sub>	(R/W)
000012H	PDRE		XXXXXXXX <sub>B</sub>	(R/W)
000013H	PDRF		XXXXXXXX <sub>B</sub>	(R/W)

( ) :Access  
 R/W :Readable and writable  
 X :Indeterminate

## • Data direction register

Address	bit 7	bit 0	Initial value	
000601H	DDR2		00000000 <sub>B</sub>	(W)
000605H	DDR6		00000000 <sub>B</sub>	(W)
00060BH	DDR8		-- 0 -- 000 <sub>B</sub>	(W)
000609H	DDRA		- 000000 - <sub>B</sub>	(W)
000608H	DDRB		00000000 <sub>B</sub>	(W)
0000D2H	DDRE		00000000 <sub>B</sub>	(W)
0000D3H	DDRF		00000000 <sub>B</sub>	(W)

( ) :Access  
 W :Write only  
 - :Unused

# MB91101/MB91101A

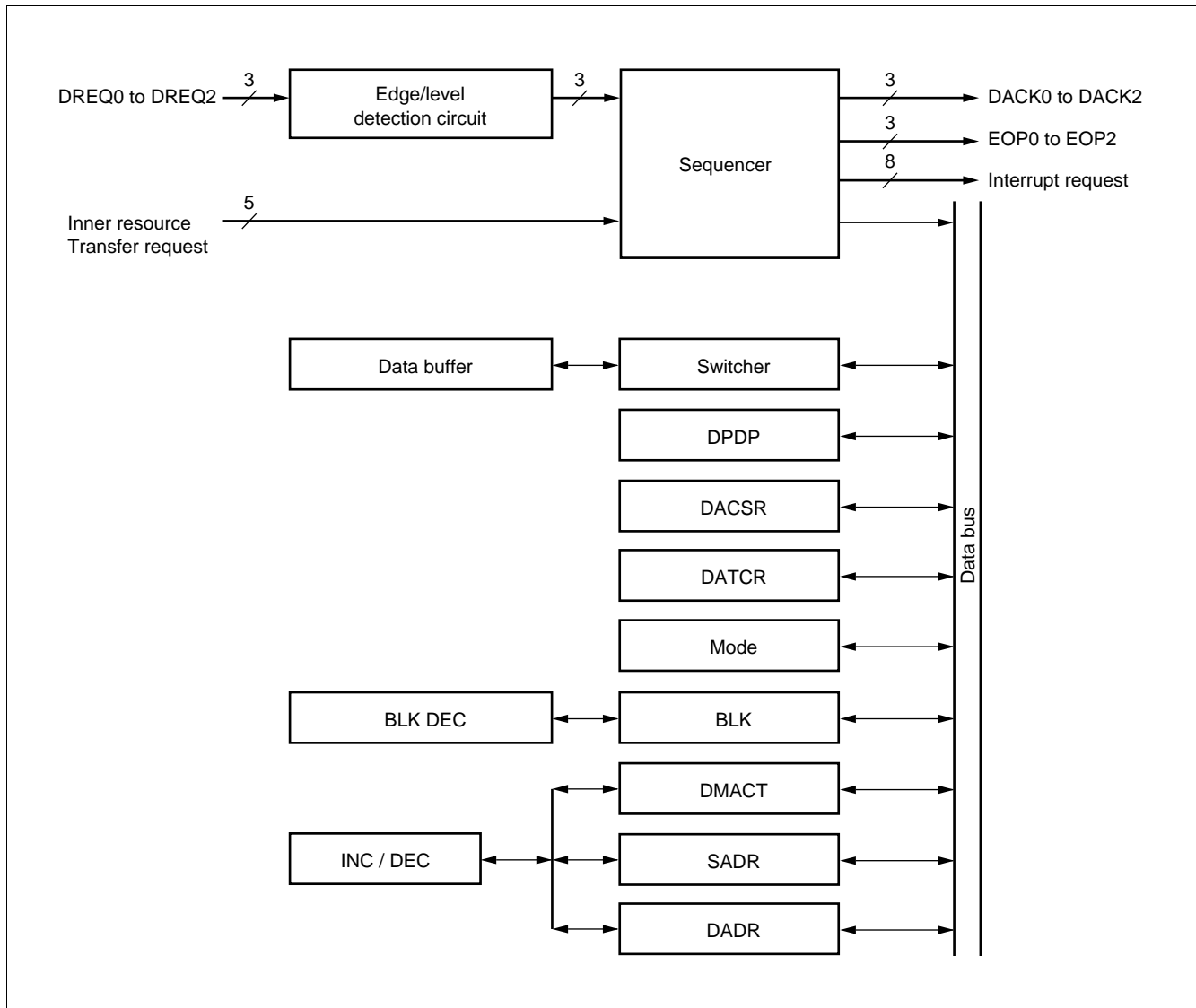
## 2. DMA Controller (DMAC)

The DMA controller is a module embedded in FR family devices, and performs DMA (direct memory access) transfer.

DMA transfer performed by the DMA controller transfers data without intervention of CPU, contributing to enhanced performance of the system.

- 8 channels
- Mode: single/block transfer, burst transfer and continuous transfer: 3 kinds of transfer
- Transfer all through the area
- Max 65536 of transfer cycles
- Interrupt function right after the transfer
- Selectable for address transfer increase/decrease by the software
- External transfer request input pin, external transfer request accept output pin, external transfer complete output pin three pins for each

### • Block diagram



## • Registers (DMAC internal registers)

Address	bit 31	bit 16	bit 0	Initial value	
00000200H 00000201H 00000202H 00000203H	DPDP			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> X0000000 <sub>B</sub>	(R/W)
00000204H 00000205H 00000206H 00000207H	DACSR			00000000 <sub>B</sub> 00000000 <sub>B</sub> 00000000 <sub>B</sub> 00000000 <sub>B</sub>	(R/W)
00000208H 00000209H 0000020AH 0000020BH	DATCR			XXXXXXXX <sub>B</sub> XXXX0000 <sub>B</sub> XXXX0000 <sub>B</sub> XXXX0000 <sub>B</sub>	(R/W)

( ) :Access  
R/W:Readable and writable  
X :Indeterminate

## • Registers (DMA descriptor)

Address	bit 31	bit 0	
DPDP + 0H	----- ----- -----		DMA ch.0 Descriptor
DPDP + 0CH			DMA ch.1 Descriptor
DPDP + 54H	----- -----		DMA ch.7 Descriptor

## 3. UART

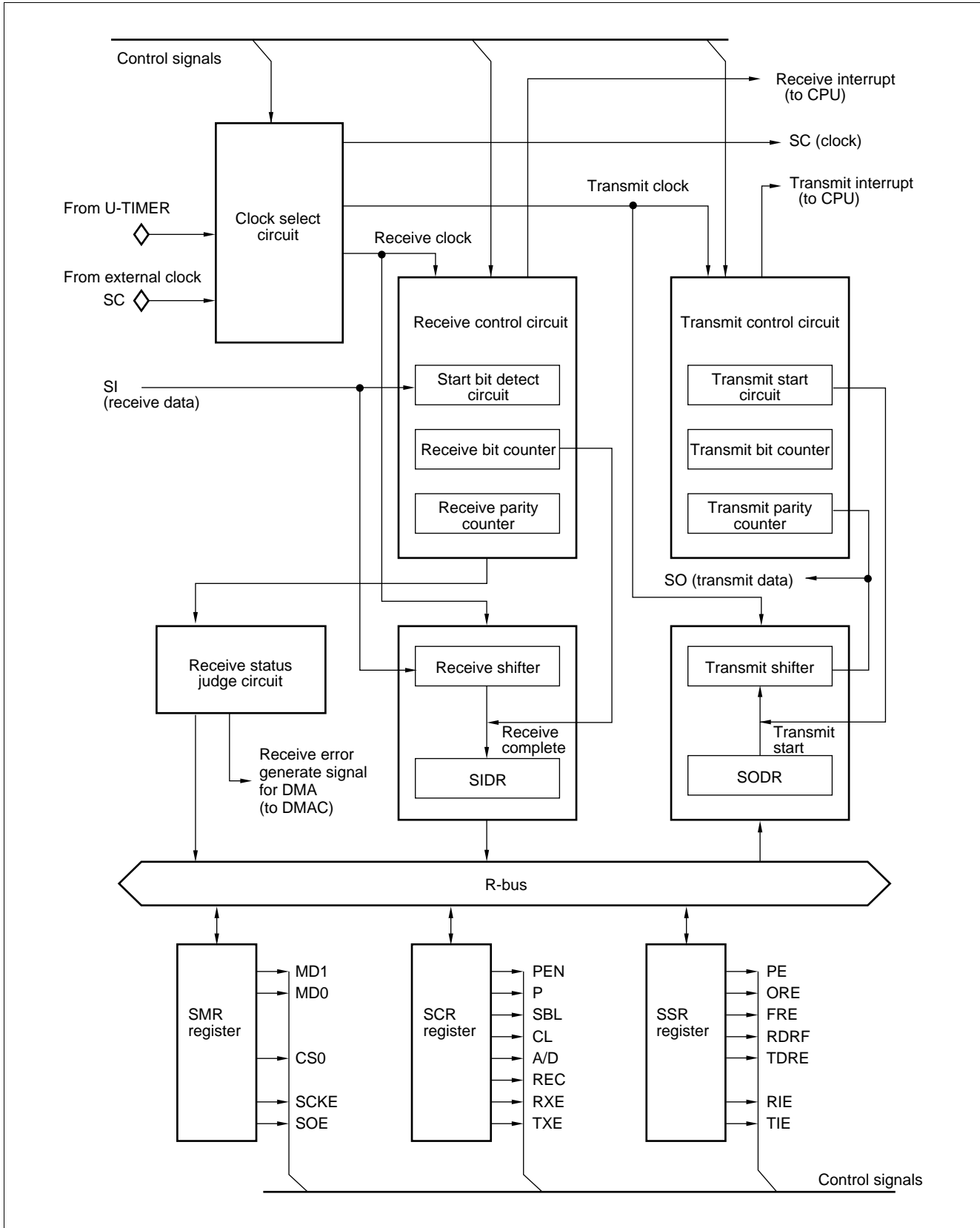
The UART is a serial I/O port for supporting asynchronous (start-stop system) communication or CLK synchronous communication, and it has the following features.

The MB91101 and MB91101A consist of 3 channels of UART.

- Full double double buffer
- Both a synchronous (start-stop system) communication and CLK synchronous communication are available.
- Supporting multi-processor mode
- Perfect programmable baud rate
  - Any baud rate can be set by internal timer (refer to section “4. U-TIMER”).
- Any baud rate can be set by external clock.
- Error checking function (parity, framing and overrun)
- Transfer signal: NRZ code
- Enable DMA transfer/start by interrupt.



• Block diagram



# MB91101/MB91101A

## • Register configuration

Address	bit 15	bit 8	bit 0	Initial value	
0000001EH	SCR0			00000100 <sub>B</sub>	(R/W)
00000022H	SCR1			00000100 <sub>B</sub>	(R/W)
00000026H	SCR2			00000100 <sub>B</sub>	(R/W)
0000001FH		SMR0		00 - - 0 - 00 <sub>B</sub>	(R/W)
00000023H		SMR1		00 - - 0 - 00 <sub>B</sub>	(R/W)
00000027H		SMR2		00 - - 0 - 00 <sub>B</sub>	(R/W)
0000001CH	SSR0			00001 - 00 <sub>B</sub>	(R/W)
00000020H	SSR1			00001 - 00 <sub>B</sub>	(R/W)
00000024H	SSR2			00001 - 00 <sub>B</sub>	(R/W)
0000001DH		SIDR0/SODR0		XXXXXXXX <sub>B</sub>	(R/W)
00000021H		SIDR1/SIDR1		XXXXXXXX <sub>B</sub>	(R/W)
00000002H		SIDR2/SIDR2		XXXXXXXX <sub>B</sub>	(R/W)

( ) :Access  
 R/W :Readable and writable  
 - :Unused  
 X :Indeterminate

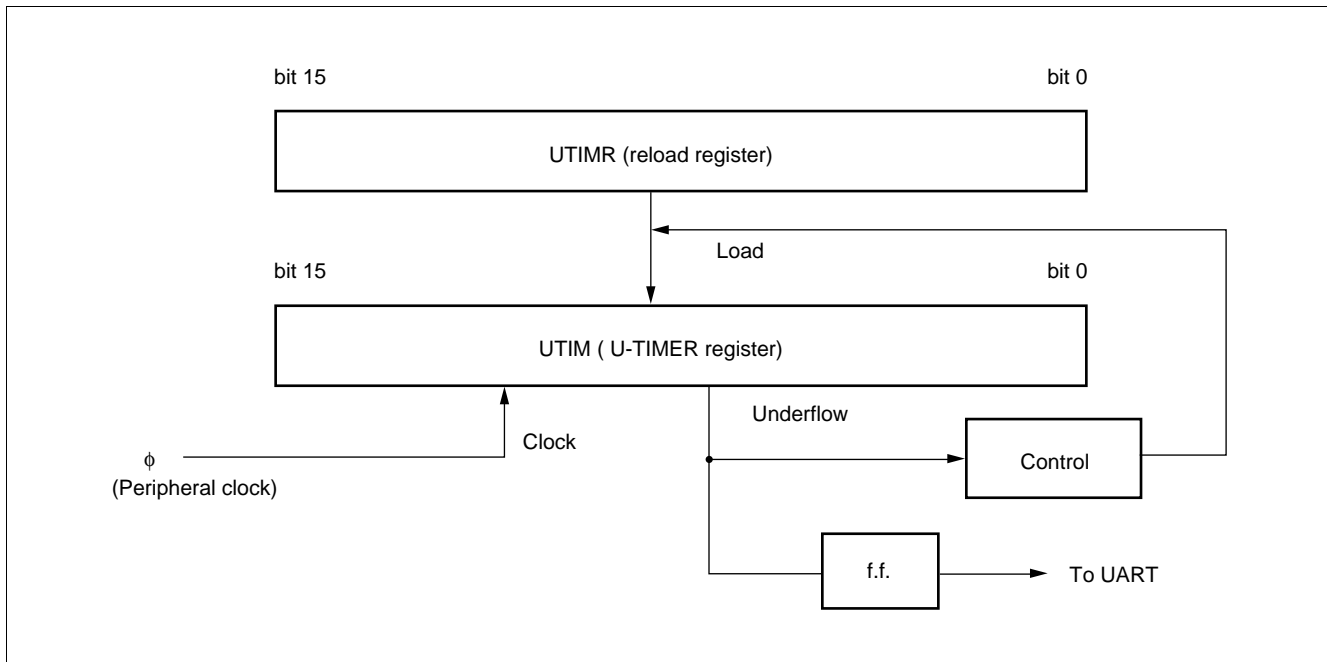
## 4. U-TIMER (16-bit Timer for UART Baud Rate Generation)

The U-TIMER is a 16-bit timer for generating UART baud rate. Combination of chip operating frequency and reload value of U-TIMER allows flexible setting of baud rate.

The U-TIMER operates as an interval timer by using interrupt issued on counter underflow.

The MB91101 and MB91101A have 3 channel U-TIMER embedded on the chip. An interval of up to  $2^{16} \times \phi$  can be counted.

### • Block diagram



### • Register configuration

Address	bit 15	bit 0	Initial value	
00000078 <sub>H</sub> 00000079 <sub>H</sub>	UTIM0/UTIMR0		00000000 <sub>B</sub> 00000000 <sub>B</sub>	(R/W)
0000007C <sub>H</sub> 0000007D <sub>H</sub>	UTIM1/UTIMR1		00000000 <sub>B</sub> 00000000 <sub>B</sub>	(R/W)
00000080 <sub>H</sub> 00000081 <sub>H</sub>	UTIM2/UTIMR2		00000000 <sub>B</sub> 00000000 <sub>B</sub>	(R/W)
0000007B <sub>H</sub>		UTIMC0	0 - - 00001 <sub>B</sub>	(R/W)
0000007F <sub>H</sub>		UTIMC1	0 - - 00001 <sub>B</sub>	(R/W)
00000083 <sub>H</sub>		UTIMC2	0 - - 00001 <sub>B</sub>	(R/W)

( ) :Access  
R/W :Readable and writable  
- :Unused

# MB91101/MB91101A

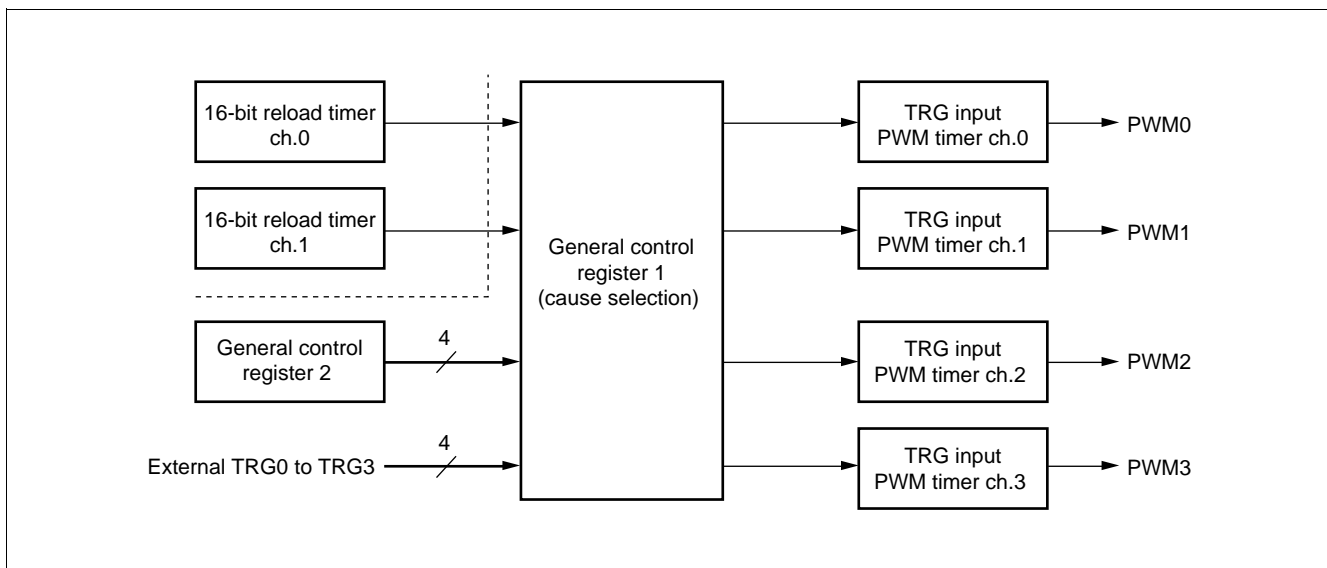
## 5. PWM Timer

The PWM timer can output high accurate PWM waves efficiently.

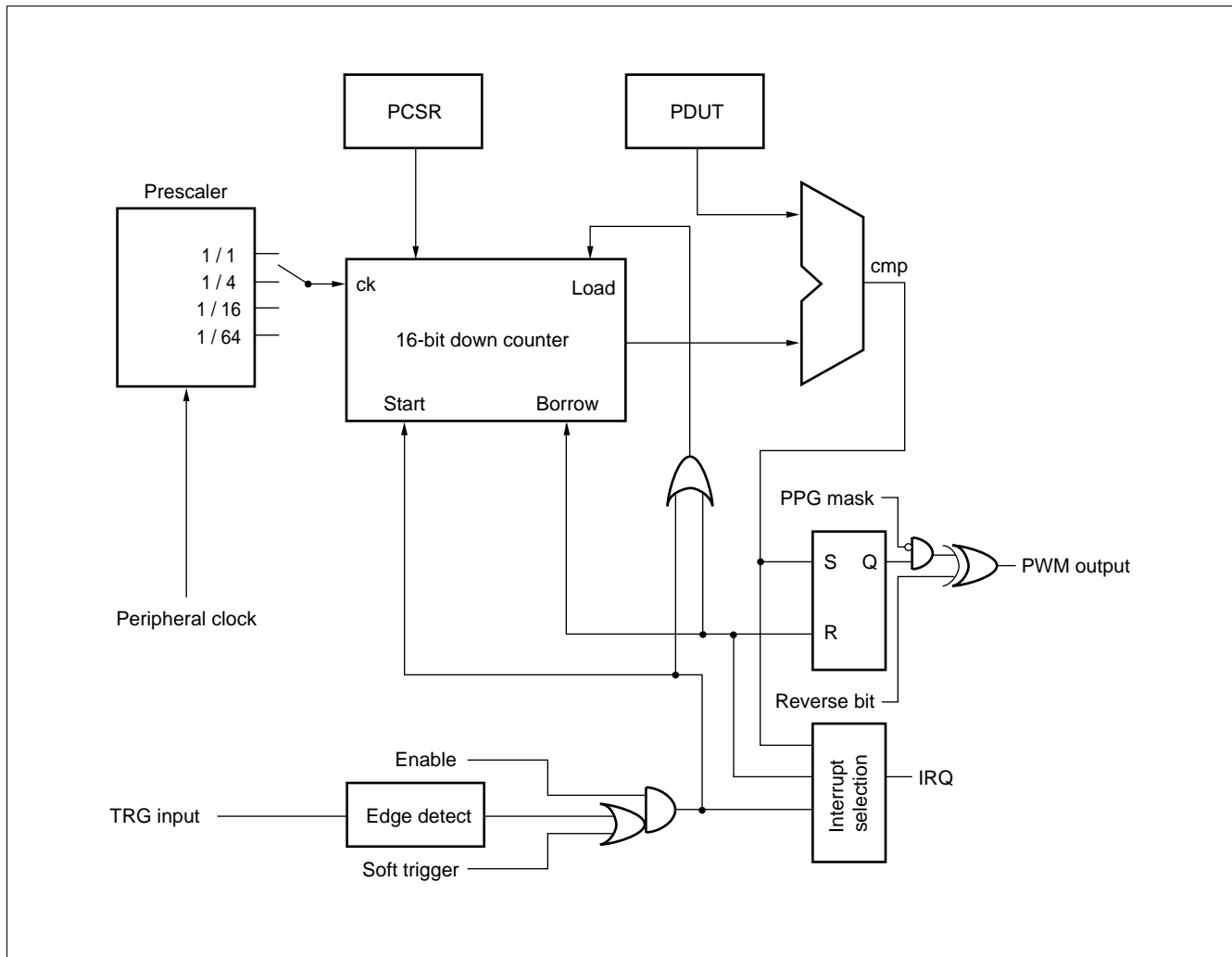
The MB91101 and MB91101A have inner 4-channel PWM timers, and has the following features.

- Each channel consists of a 16-bit down counter, a 16-bit data register with a buffer for scyde setting, a 16-bit compare register with a buffer for duty setting, and a pin controller.
- The count clock of a 16-bit down counter can be selected from the following four inner clocks.  
Inner clock  $\phi$ ,  $\phi/4$ ,  $\phi/16$ ,  $\phi/64$
- The counter value can be initialized “FFFF<sub>H</sub>” by the resetting or the counter borrow.
- PWM output (each channel)
- Resister description

- **Block diagram (general construction)**



• Block diagram (for one channel)



# MB91101/MB91101A

## • Register configuration

Address	bit 15	bit 8	bit 0	Initial value	
000000DC <sub>H</sub> 000000DD <sub>H</sub>	GCN1			00110010 <sub>B</sub> 00010000 <sub>B</sub>	(R/W)
000000DF <sub>H</sub>		GCN2		00000000 <sub>B</sub>	(R/W)
000000E0 <sub>H</sub> 000000E1 <sub>H</sub>	PTMR0			11111111 <sub>B</sub> 11111111 <sub>B</sub>	(R)
000000E2 <sub>H</sub> 000000E3 <sub>H</sub>	PCSR0			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
000000E4 <sub>H</sub> 000000E5 <sub>H</sub>	PDUT0			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
000000E6 <sub>H</sub>	PCNH0			0000000 - <sub>B</sub>	(R/W)
000000E7 <sub>H</sub>		PCNL0		00000000 <sub>B</sub>	(R/W)
000000E8 <sub>H</sub> 000000E9 <sub>H</sub>	PTMR1			11111111 <sub>B</sub> 11111111 <sub>B</sub>	(R)
000000EA <sub>H</sub> 000000EB <sub>H</sub>	PCSR1			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
000000EC <sub>H</sub> 000000ED <sub>H</sub>	PDUT1			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
000000EE <sub>H</sub>	PCNH1			0000000 - <sub>B</sub>	(R/W)
000000EF <sub>H</sub>		PCNL1		00000000 <sub>B</sub>	(R/W)
000000F0 <sub>H</sub> 000000F1 <sub>H</sub>	PTMR2			11111111 <sub>B</sub> 11111111 <sub>B</sub>	(R)
000000F2 <sub>H</sub> 000000F3 <sub>H</sub>	PCSR2			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
000000F4 <sub>H</sub> 000000F5 <sub>H</sub>	PDUT2			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
000000F6 <sub>H</sub>	PCNH2			0000000 - <sub>B</sub>	(R/W)
000000F7 <sub>H</sub>		PCNL2		00000000 <sub>B</sub>	(R/W)
000000F8 <sub>H</sub> 000000F9 <sub>H</sub>	PTMR3			11111111 <sub>B</sub> 11111111 <sub>B</sub>	(R)
000000FA <sub>H</sub> 000000FB <sub>H</sub>	PCSR3			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
000000FC <sub>H</sub> 000000FD <sub>H</sub>	PDUT3			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
000000FE <sub>H</sub>	PCNH3			0000000 - <sub>B</sub>	(R/W)
000000FF <sub>H</sub>		PCNL3		00000000 <sub>B</sub>	(R/W)

( ) :Access  
R/W :Readable and writable  
R :Read only  
W :Write only  
- :Unused  
X :Indeterminate

## 6. 16-bit Reload Timer

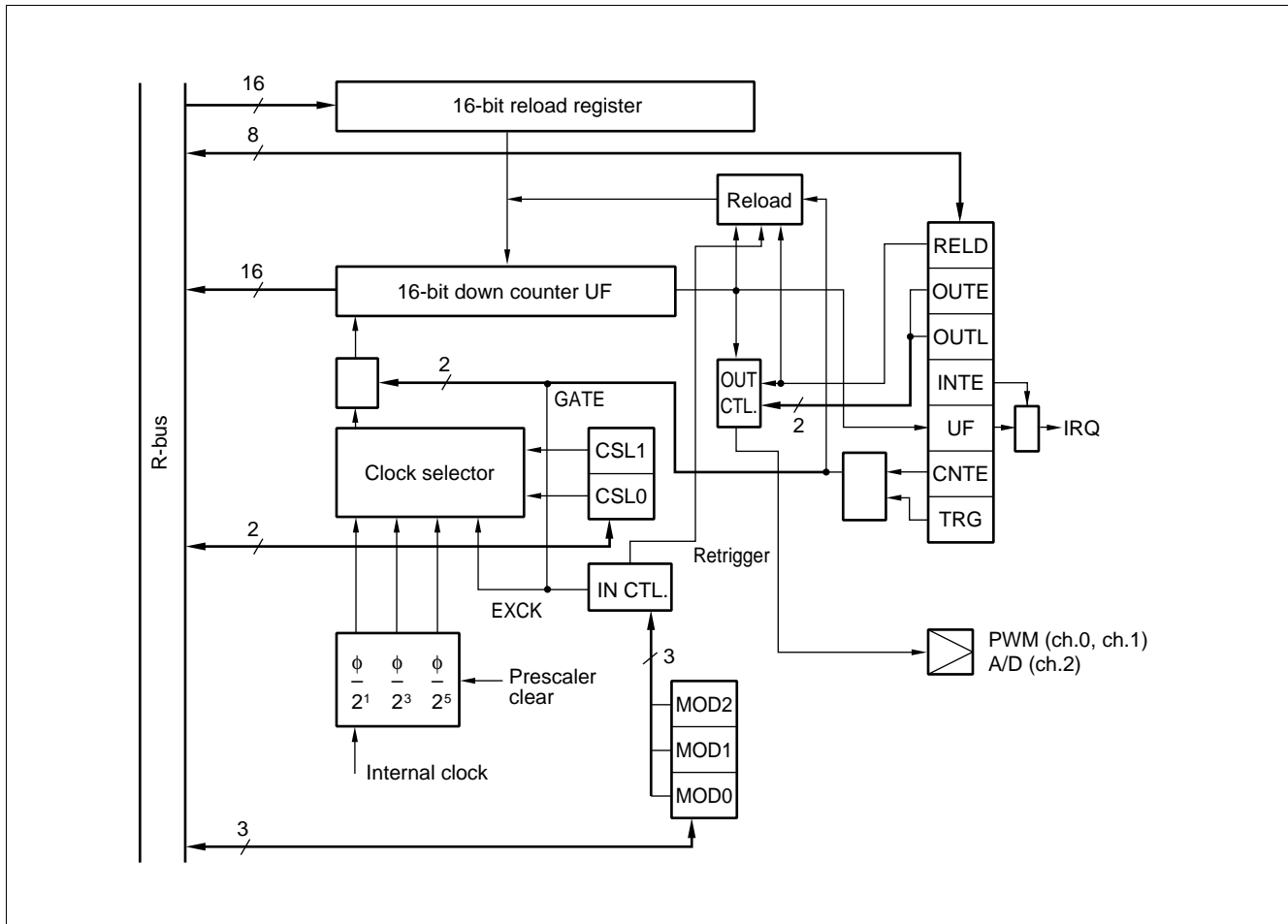
The 16-bit reload timer consists of a 16-bit down counter, a 16-bit reload timer, a prescaler for generating internal count clock and control registers.

Internal clock can be selected from 3 types of internal clocks (divided by 2/8/32 of machine clock).

The DMA transfer can be started by the interruption.

The MB91101 and MB91101A consist of 3 channels of the 16-bit reload timer.

### • Block diagram



# MB91101/MB91101A

## • Register configuration

Address	bit 15	bit 0	Initial value	
0000002E <sub>H</sub> 0000002F <sub>H</sub>	TMCSR0		----0000 <sub>B</sub> 00000000 <sub>B</sub>	(R/W)
00000036 <sub>H</sub> 00000037 <sub>H</sub>	TMCSR1		----0000 <sub>B</sub> 00000000 <sub>B</sub>	(R/W)
00000042 <sub>H</sub> 00000043 <sub>H</sub>	TMCSR2		----0000 <sub>B</sub> 00000000 <sub>B</sub>	(R/W)
0000002A <sub>H</sub> 0000002B <sub>H</sub>	TMR0		XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(R)
00000032 <sub>H</sub> 00000033 <sub>H</sub>	TMR1		XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(R)
0000003E <sub>H</sub> 0000003F <sub>H</sub>	TMR2		XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(R)
00000028 <sub>H</sub> 00000029 <sub>H</sub>	TMRLR0		XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
00000030 <sub>H</sub> 00000031 <sub>H</sub>	TMRLR1		XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
0000003C <sub>H</sub> 0000003D <sub>H</sub>	TMRLR2		XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)

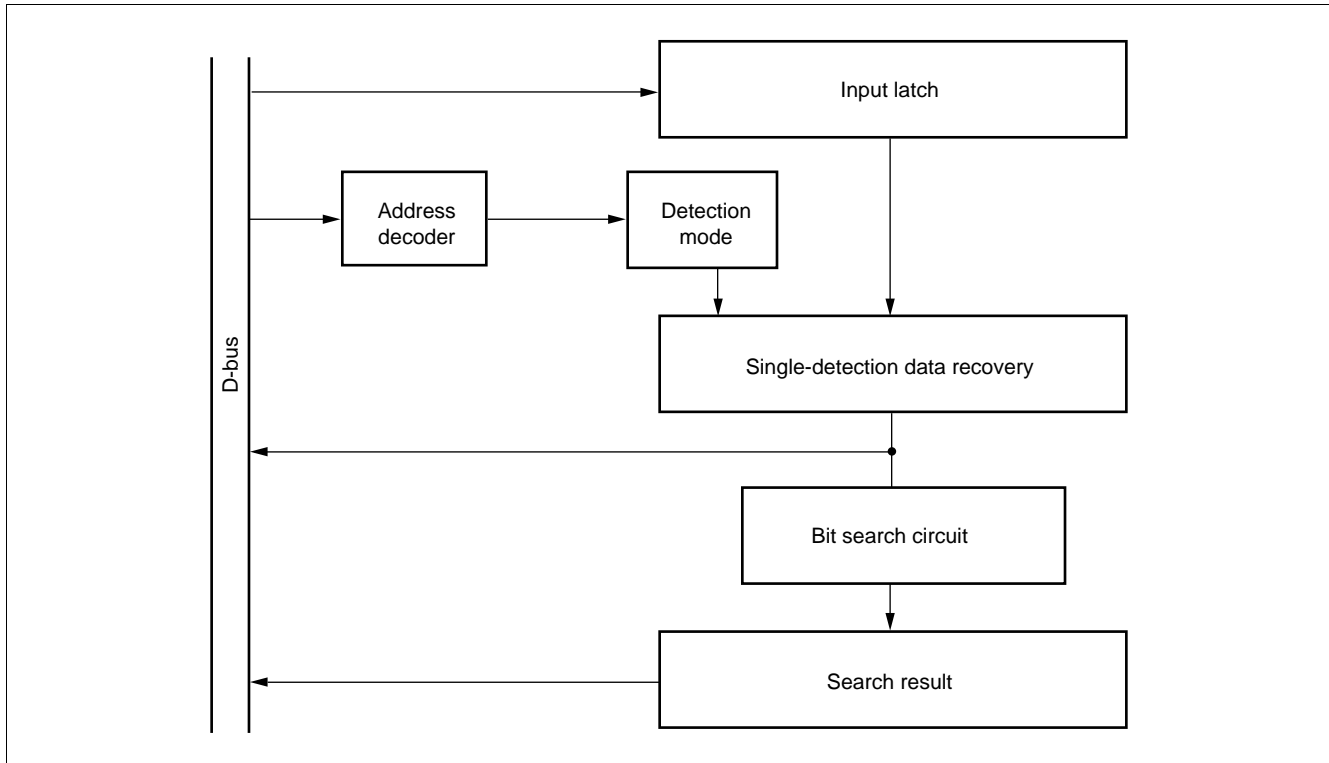
( ) :Access  
 R/W :Readable and writable  
 R :Read only  
 W :Write only  
 - :Unused  
 X :Indeterminate



## 7. Bit Search Module

The bit search module detects transitions of data (0 to 1/1 to 0) on the data written on the input registers and returns locations of the transitions.

### • Block diagram



### • Register configuration

Address	bit 31	bit 16	bit 0	Initial value	
000003F0 <sub>H</sub> 000003F1 <sub>H</sub> 000003F2 <sub>H</sub> 000003F3 <sub>H</sub>	BSD0			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
000003F4 <sub>H</sub> 000003F5 <sub>H</sub> 000003F6 <sub>H</sub> 000003F7 <sub>H</sub>	BSD1			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(R/W)
000003F8 <sub>H</sub> 000003F9 <sub>H</sub> 000003FA <sub>H</sub> 000003FB <sub>H</sub>	BSDC			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(W)
000003FC <sub>H</sub> 000003FE <sub>H</sub> 000003FD <sub>H</sub> 000003FF <sub>H</sub>	BSRR			XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>	(R)

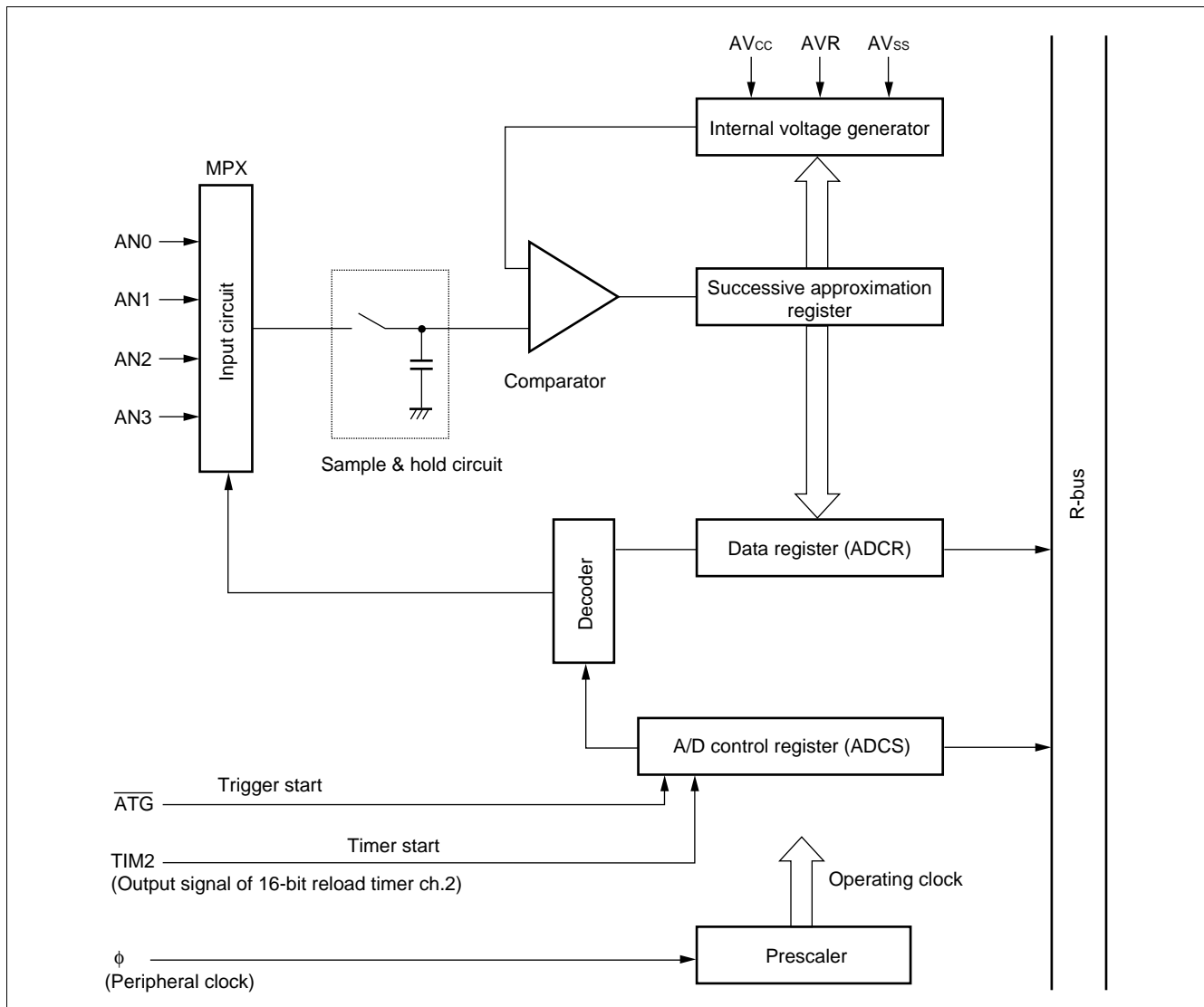
( ) :Access  
 R/W :Readable and writable  
 R :Read only  
 W :Write only  
 X :Indeterminate

# MB91101/MB91101A

## 8. 10-bit A/D Converter (Successive Approximation Conversion Type)

The A/D converter is the module which converts an analog input voltage to a digital value, and it has following features.

- Minimum converting time: 5.6  $\mu$ s/ch. (system clock: 25 MHz)
- Inner sample and hold circuit
- Resolution: 10 bits
- Analog input can be selected from 4 channels by program.
  - Single convert mode: 1 channel is selected and converted.
  - Scan convert mode: Converting continuous channels. Maximum 4 channels are programmable.
  - Continuous convert mode: Converting the specified channel repeatedly.
  - Stop convert mode: After converting one channel then stop and wait till next activation synchronizing at the beginning of conversion can be performed.
- DMA transfer operation is available by interruption.
- Operating factor can be selected from the software, the external trigger (falling edge), and 16-bit reload timer (rising edge).
- **Block diagram**



• Register configuration

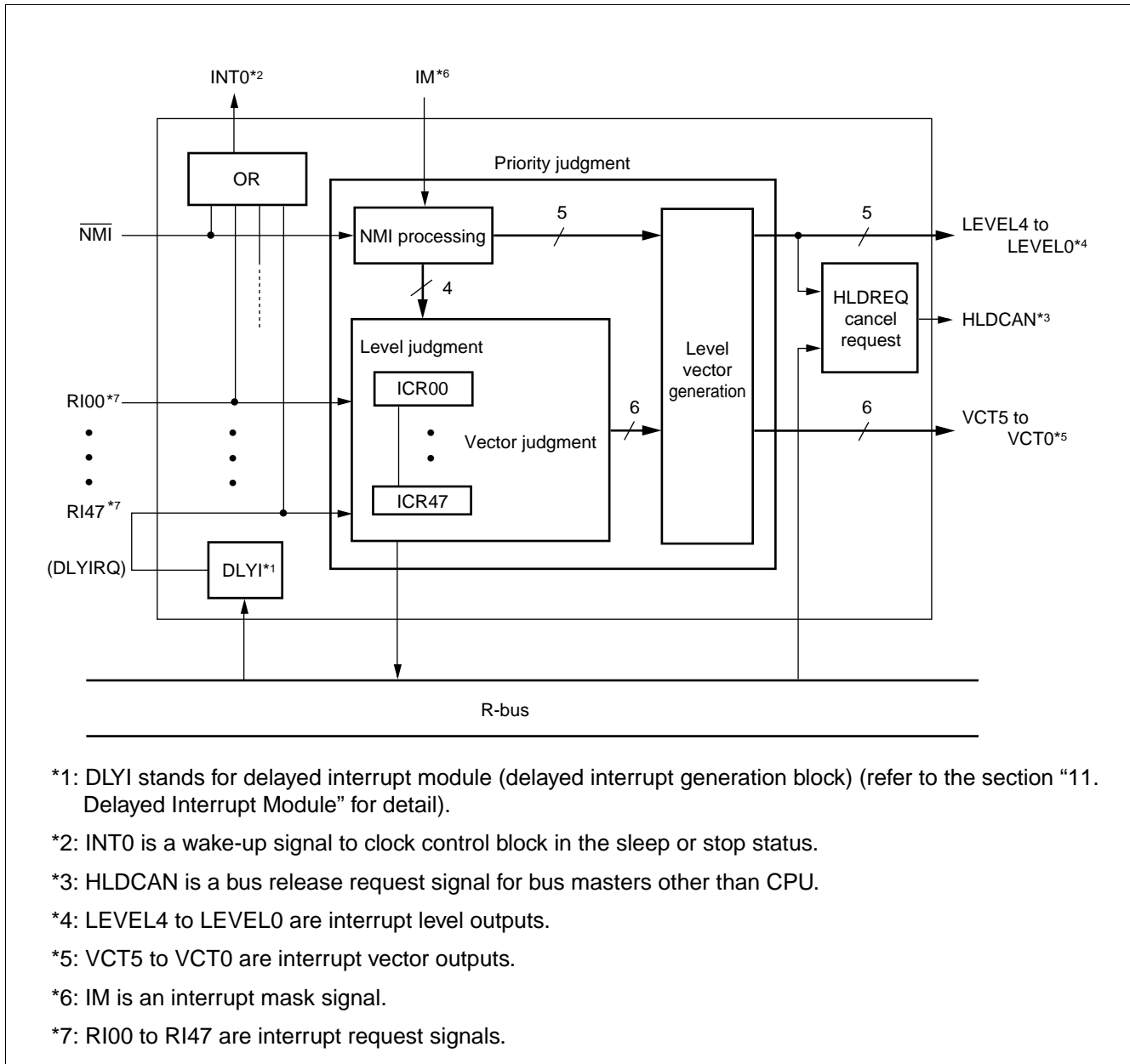
Address	bit 15	bit 0	Initial value	
0000003AH 0000003BH	ADCS		0000000B 0000000B	(R/W)
00000038H 00000039H	ADCR		-----XXB XXXXXXXXXB	(R)

( ) :Access  
 R/W :Readable and writable  
 R :Read only  
 - :Unused  
 X :Indeterminate

## 9. Interrupt Controller

The interrupt controller processes interrupt acknowledgments and arbitration between interrupts.

### • Block diagram



• Register configuration

Address	bit 7	bit 0	Initial value	Address	bit 7	bit 0	Initial value
00000400 <sub>H</sub>	ICR00	---	11111 <sub>B</sub> (R/W)	00000411 <sub>H</sub>	ICR17	---	11111 <sub>B</sub> (R/W)
00000401 <sub>H</sub>	ICR01	---	11111 <sub>B</sub> (R/W)	00000412 <sub>H</sub>	ICR18	---	11111 <sub>B</sub> (R/W)
00000402 <sub>H</sub>	ICR02	---	11111 <sub>B</sub> (R/W)	00000413 <sub>H</sub>	ICR19	---	11111 <sub>B</sub> (R/W)
00000403 <sub>H</sub>	ICR03	---	11111 <sub>B</sub> (R/W)	00000414 <sub>H</sub>	ICR20	---	11111 <sub>B</sub> (R/W)
00000404 <sub>H</sub>	ICR04	---	11111 <sub>B</sub> (R/W)	00000415 <sub>H</sub>	ICR21	---	11111 <sub>B</sub> (R/W)
00000405 <sub>H</sub>	ICR05	---	11111 <sub>B</sub> (R/W)	00000416 <sub>H</sub>	ICR22	---	11111 <sub>B</sub> (R/W)
00000406 <sub>H</sub>	ICR06	---	11111 <sub>B</sub> (R/W)	00000417 <sub>H</sub>	ICR23	---	11111 <sub>B</sub> (R/W)
00000407 <sub>H</sub>	ICR07	---	11111 <sub>B</sub> (R/W)	00000418 <sub>H</sub>	ICR24	---	11111 <sub>B</sub> (R/W)
00000408 <sub>H</sub>	ICR08	---	11111 <sub>B</sub> (R/W)	00000419 <sub>H</sub>	ICR25	---	11111 <sub>B</sub> (R/W)
00000409 <sub>H</sub>	ICR09	---	11111 <sub>B</sub> (R/W)	0000041A <sub>H</sub>	ICR26	---	11111 <sub>B</sub> (R/W)
0000040A <sub>H</sub>	ICR10	---	11111 <sub>B</sub> (R/W)	0000041B <sub>H</sub>	ICR27	---	11111 <sub>B</sub> (R/W)
0000040B <sub>H</sub>	ICR11	---	11111 <sub>B</sub> (R/W)	0000041C <sub>H</sub>	ICR28	---	11111 <sub>B</sub> (R/W)
0000040C <sub>H</sub>	ICR12	---	11111 <sub>B</sub> (R/W)	0000041D <sub>H</sub>	ICR29	---	11111 <sub>B</sub> (R/W)
0000040D <sub>H</sub>	ICR13	---	11111 <sub>B</sub> (R/W)	0000041E <sub>H</sub>	ICR30	---	11111 <sub>B</sub> (R/W)
0000040E <sub>H</sub>	ICR14	---	11111 <sub>B</sub> (R/W)	0000041F <sub>H</sub>	ICR31	---	11111 <sub>B</sub> (R/W)
0000040F <sub>H</sub>	ICR15	---	11111 <sub>B</sub> (R/W)	0000042F <sub>H</sub>	ICR47	---	11111 <sub>B</sub> (R/W)
00000410 <sub>H</sub>	ICR16	---	11111 <sub>B</sub> (R/W)	00000431 <sub>H</sub>	HRCL	---	11111 <sub>B</sub> (R/W)
				00000430 <sub>H</sub>	DICR	-----	0 <sub>B</sub> (R/W)

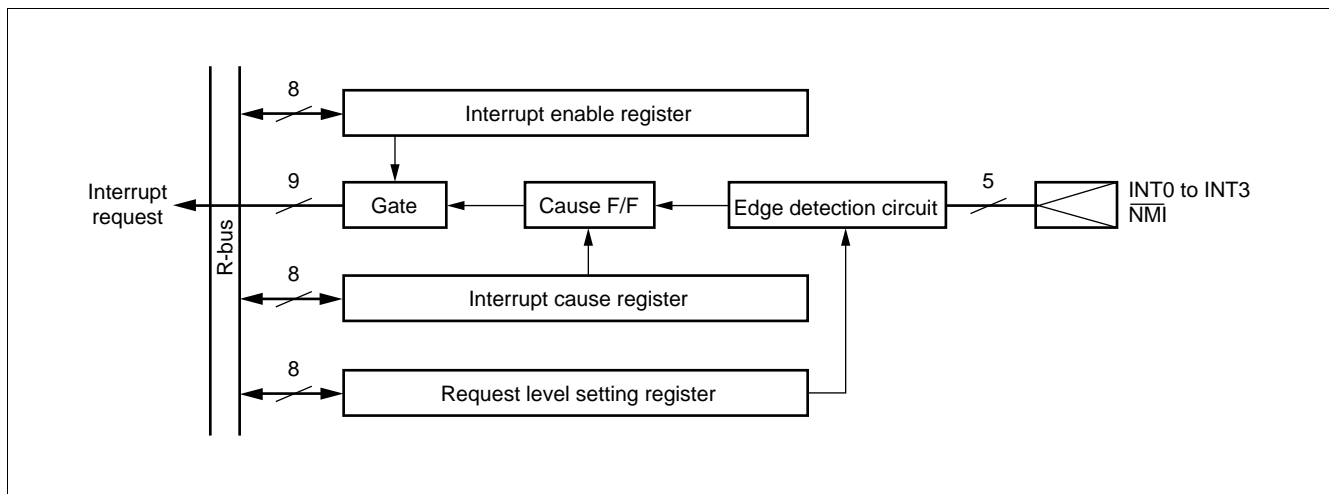
( ) :Access  
R/W :Readable and writable  
- :Unused

## 10. External Interrupt/NMI Control Block

The external interrupt/NMI control block controls external interrupt request signals input to  $\overline{\text{NMI}}$  pin and INT0 to INT3 pins.

Detecting levels can be selected from "H", "L", rising edge and falling edge (not for  $\overline{\text{NMI}}$  pin).

### • Block diagram



### • Register configuration

Address	bit 15	bit 8	bit 0	Initial value
00000095H		ENIR		00000000 <sub>B</sub> (R/W)
00000094H	EIRR			00000000 <sub>B</sub> (R/W)
00000099H		ELVR		00000000 <sub>B</sub> (R/W)

( ) :Access

R/W :Readable and writable

## 11. Delayed Interrupt Module

Delayed interrupt module is a module which generates a interrupt for changing a task. By using this delayed interrupt module, an interrupt request to CPU can be generated/cancelled by the software.

Refer to the section "9. Interrupt Controller" for delayed interrupt module block diagram.

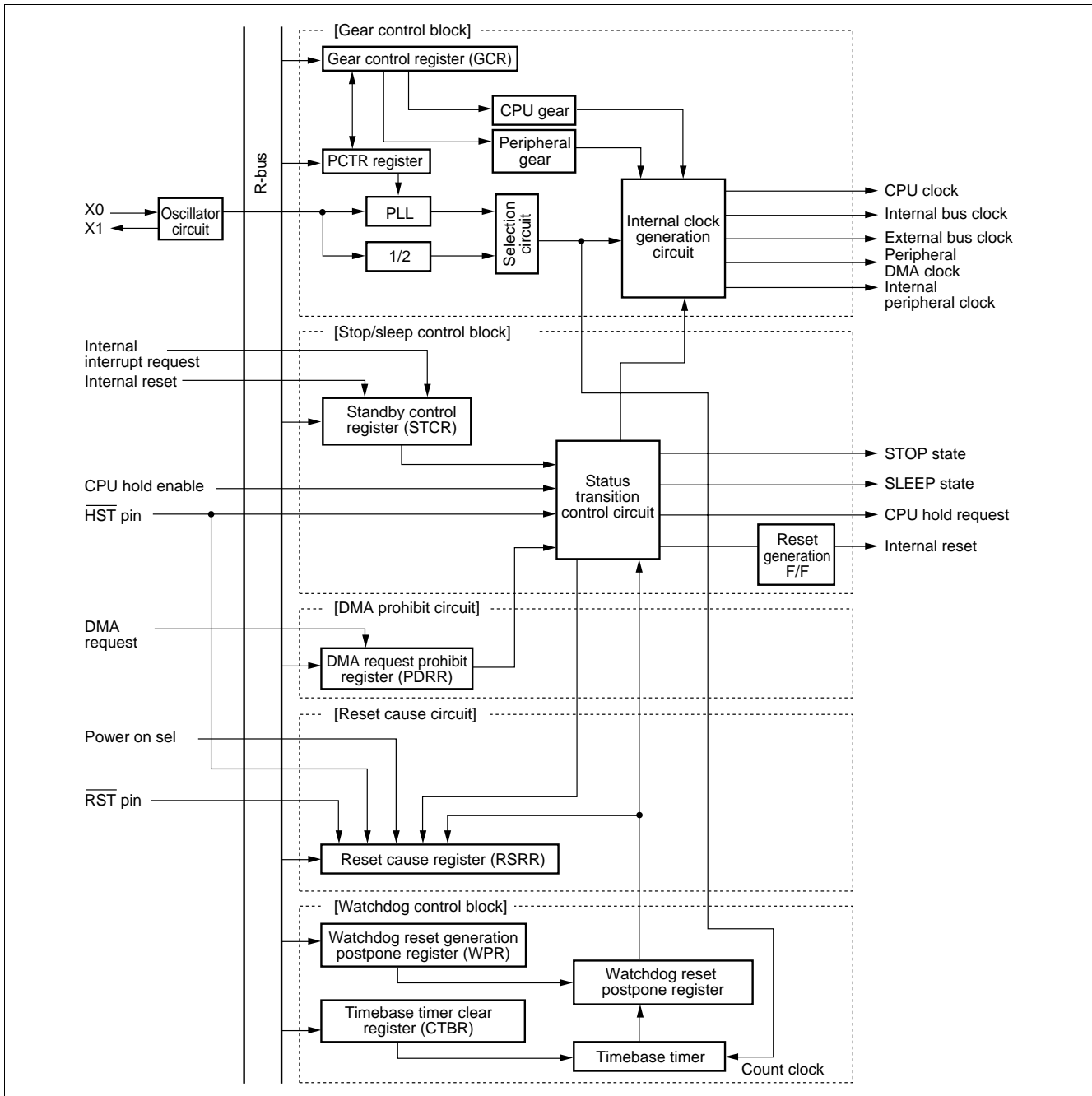
- Register configuration

Address	bit 7	bit 0	Initial value	
00000430 <sub>H</sub>	DICR		----- 0 <sub>B</sub>	(R/W)
( )	:Access			
R/W	:Readable and writable			
-	:Unused			

## 12. Clock Generation (Low-power consumption mechanism)

The clock control block is a module which undertakes the following functions.

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and cause hold
- Standby function (including hardware standby)
- DMA request prohibit
- PLL (multiplier circuit) embedded
- **Block diagram**





• Register configuration

Address	bit 15	bit 8	bit 0	Initial value	
00000480H	RSRR/WTCR			1XXXX - 00 <sub>B</sub>	(R/W)
00000481H			STCR	000111 - - <sub>B</sub>	(R/W)
00000482H	PDRR			- - - - 0000 <sub>B</sub>	(R/W)
00000483H			CTBR	XXXXXXXX <sub>B</sub>	(W)
00000484H	GCR			110011 - 1 <sub>B</sub>	(R/W)
00000485H			WPR	XXXXXXXX <sub>B</sub>	(W)
00000488H	PCTR			00 - - 0 - - - <sub>B</sub>	(R/W)

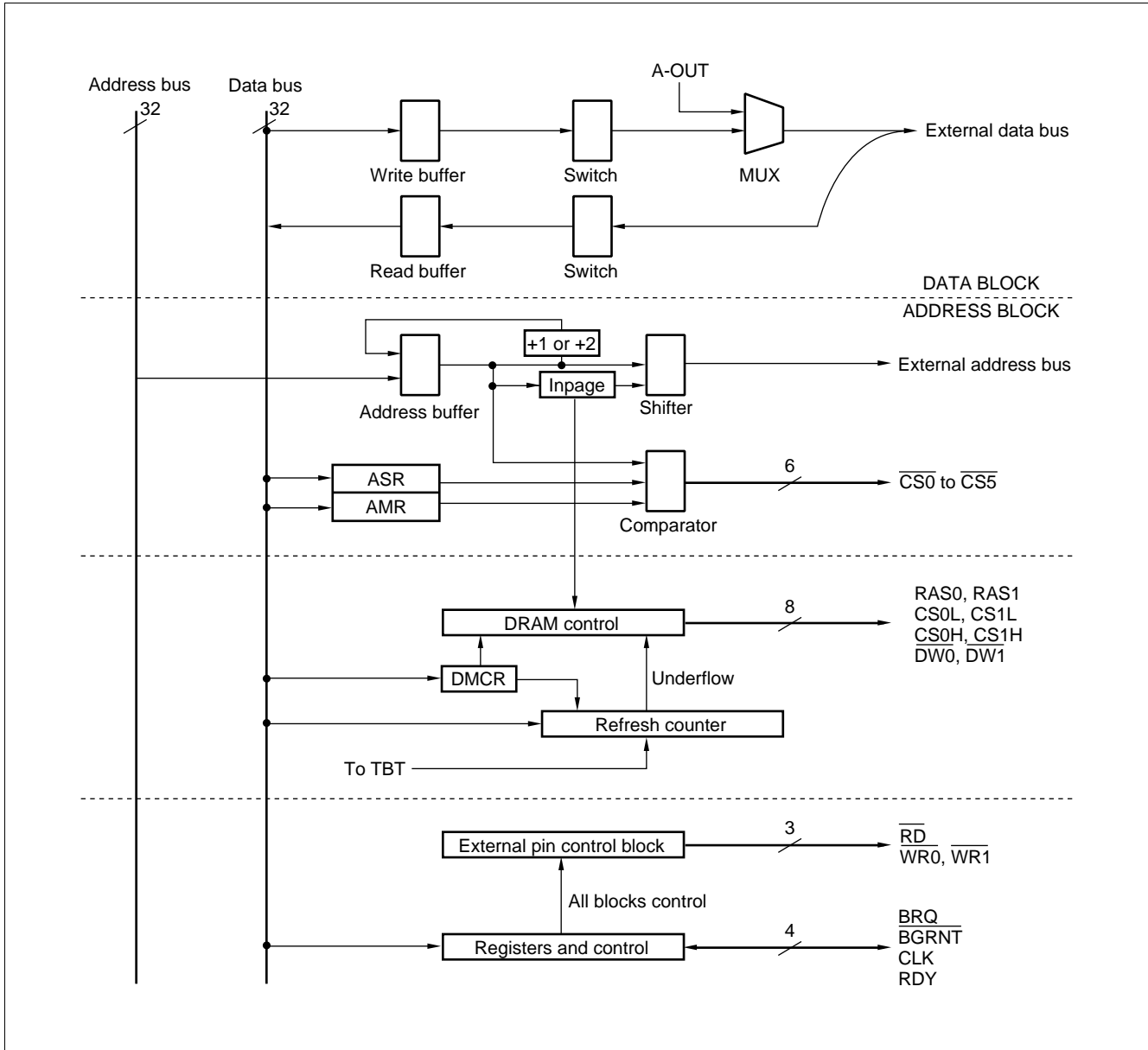
( ) :Access  
R/W :Readable and writable  
W :Write only  
- :Unused  
X :Indeterminate

## 13. External Bus Interface

The external bus interface controls the interface between the device and the external memory and also the external I/O, and has the following features.

- 25-bit (32 Mbytes) address output
- 6 independent banks owing to the chip select function.  
Can be set to anywhere on the logical address space for minimum unit 64 Kbytes.  
Total 32 Mbytes × 6 area setting is available by the address pin and the chip select pin.
- 8/16-bit bus width setting are available for every chip select area.
- Programmable automatic memory wait (Max for 7 cycles) can be inserted.
- DRAM interface support  
Three kinds of DRAM interface: Double CAS DRAM (normally DRAM I/F)  
Single CAS DRAM  
Hyper DRAM  
2 banks independent control (RAS, CAS, etc. control signals)  
DRAM select is available from 2CAS/1WE and 1CAS/2WE.  
Hi-speed page mode supported  
CBR/self refresh supported  
Programmable wave form
- Unused address/data pin can be used for I/O port.
- Little endian mode supported
- Clock doubler: Internal bus 50 MHz, external bus 25 MHz

• Block diagram



# MB91101/MB91101A

## • Register configuration

Address	bit 31	bit 16	bit 0	Initial value	
0000060C <sub>H</sub> 0000060D <sub>H</sub>	ASR1			00000000 <sub>B</sub> 00000001 <sub>B</sub>	(W)
0000060E <sub>H</sub> 0000060F <sub>H</sub>		AMR1		00000000 <sub>B</sub> 00000000 <sub>B</sub>	(W)
00000610 <sub>H</sub> 00000611 <sub>H</sub>	ASR2			00000000 <sub>B</sub> 00000010 <sub>B</sub>	(W)
00000612 <sub>H</sub> 00000613 <sub>H</sub>		AMR2		00000000 <sub>B</sub> 00000000 <sub>B</sub>	(W)
00000614 <sub>H</sub> 00000615 <sub>H</sub>	ASR3			00000000 <sub>B</sub> 00000011 <sub>B</sub>	(W)
00000616 <sub>H</sub> 00000617 <sub>H</sub>		AMR3		00000000 <sub>B</sub> 00000000 <sub>B</sub>	(W)
00000618 <sub>H</sub> 00000619 <sub>H</sub>	ASR4			00000000 <sub>B</sub> 00000100 <sub>B</sub>	(W)
0000061A <sub>H</sub> 0000061B <sub>H</sub>		AMR4		00000000 <sub>B</sub> 00000000 <sub>B</sub>	(W)
0000061C <sub>H</sub> 0000061D <sub>H</sub>	ASR5			00000000 <sub>B</sub> 00000101 <sub>B</sub>	(W)
0000061E <sub>H</sub> 0000061F <sub>H</sub>		AMR5		00000000 <sub>B</sub> 00000000 <sub>B</sub>	(W)
00000620 <sub>H</sub>	AMD0			---00111 <sub>B</sub>	(R/W)
00000621 <sub>H</sub>		AMD1		0--00000 <sub>B</sub>	(R/W)
00000622 <sub>H</sub>			AMD32	00000000 <sub>B</sub>	(R/W)
00000623 <sub>H</sub>			AMD4	0--00000 <sub>B</sub>	(R/W)
00000624 <sub>H</sub>	AMD5			0--00000 <sub>B</sub>	(R/W)
00000625 <sub>H</sub>		DSCR		00000000 <sub>B</sub>	(W)
00000626 <sub>H</sub> 00000627 <sub>H</sub>			RFCR	--XXXXXX <sub>B</sub> 00---000 <sub>B</sub>	(R/W)
00000628 <sub>H</sub> 00000629 <sub>H</sub>	EPCR0			----1100 <sub>B</sub> -11111111 <sub>B</sub>	(W)
0000062B <sub>H</sub>			EPCR1	11111111 <sub>B</sub>	(W)
0000062C <sub>H</sub> 0000062D <sub>H</sub>	DMCR4			00000000 <sub>B</sub> 0000000- <sub>B</sub>	(R/W)
0000062E <sub>H</sub> 0000062F <sub>H</sub>			DMCR5	00000000 <sub>B</sub> 0000000- <sub>B</sub>	(R/W)
000007FE <sub>H</sub>		LER		-----000 <sub>B</sub>	(W)
000007FF <sub>H</sub>			MODR	XXXXXXXX <sub>B</sub>	(W)

( ) :Access  
R/W :Readable and writable  
W :Write only  
- :Unused  
X :Indeterminate

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

Parameter		Symbol	Rating		Unit	Remarks
			Min	Max		
Power supply voltage	At 5 V power supply	$V_{CC5}$	$V_{SS} - 0.3$	$V_{SS} + 6.5$	V	
		$V_{CC3}$	—	—	V	
	At 3 V power supply	$V_{CC5}$	$V_{CC3} - 0.3$	$V_{SS} + 6.5$	V	*1
		$V_{CC3}$	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	*1
Analog supply voltage		$AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	*2
Analog reference voltage		$AVRH$	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	*2
Analog pin input voltage		$V_{IA}$	$V_{SS} - 0.3$	$AV_{CC} + 0.3$	V	
Input voltage		$V_I$	$V_{SS} - 0.3$	$V_{CC5} + 0.3$	V	
Output voltage		$V_O$	$V_{SS} - 0.3$	$V_{CC5} + 0.3$	V	
“L” level maximum output current		$I_{OL}$	—	10	mA	*3
“L” level average output current		$I_{OLAV}$	—	4	mA	*4
“L” level maximum total output current		$\Sigma I_{OL}$	—	100	mA	
“L” level average total output current		$\Sigma I_{OLAV}$	—	50	mA	*5
“H” level maximum output current		$I_{OH}$	—	-10	mA	*3
“H” level average output current		$I_{OHAV}$	—	-4	mA	*4
“H” level maximum total output current		$\Sigma I_{OH}$	—	-50	mA	
“H” level average total output current		$\Sigma I_{OHAV}$	—	-20	mA	*5
Power consumption		$P_D$	—	500	mW	
Operating temperature		$T_A$	-40	+70	°C	
Storage temperature		$T_{stg}$	-55	+150	°C	

\*1:  $V_{CC5}$  must not be less than  $V_{SS} - 0.3\text{ V}$ .

\*2: Care must be taken that  $AV_{CC}$  and  $AVRH$  do not exceed  $V_{CC5} + 0.3\text{ V}$  and  $V_{SS} + 3.6\text{ V}$ .  
Also care must be taken that  $AVRH$  does not exceed  $AV_{CC}$ .

\*3: Maximum output current is a peak current value measured at a corresponding pin.

\*4: Average output current is an average current for a 100 ms period at a corresponding pin.

\*5: Average total output current is an average current for a 100 ms period for all corresponding pins.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB91101/MB91101A

## 2. Recommended Operating Conditions

### (1) At 5 V operation (4.5 V to 5.5 V)

(V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V <sub>CC5</sub>	4.5	5.5	V	Normal operation
	V <sub>CC5</sub>	*1	*1	V	Retaining the RAM state in stop mode
	V <sub>CC3</sub>	—	—	V	*2
Analog supply voltage	AV <sub>CC</sub>	V <sub>SS</sub> + 2.7	V <sub>SS</sub> + 3.6	V	
Analog reference voltage	AV <sub>RH</sub>	V <sub>SS</sub> - 0.3	AV <sub>CC</sub>	V	
Operating temperature	T <sub>A</sub>	-40	+70	°C	
Smoothing capacitor	C <sub>S</sub>	0.1	1.0	μF	V <sub>CC3</sub> pin, *3

\*1: At V<sub>CC5</sub>, the RAM state holding is not warranted in stop mode.

\*2: V<sub>CC3</sub> is used for the bypass capacitor pin.

\*3: Use the ceramic capacitor or the capacitor whose frequency characteristic is equivalent to that of the ceramic capacitor.

And select the larger capacity bypass capacitor to connect to the power supply (V<sub>CC5</sub>) than C<sub>S</sub>.

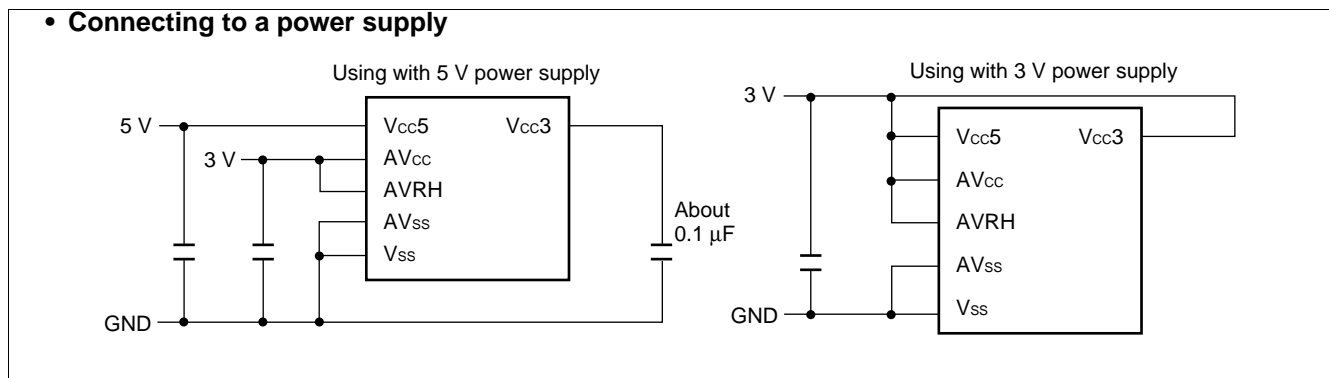
### (2) At 3 V operation (2.7 V to 3.6 V)

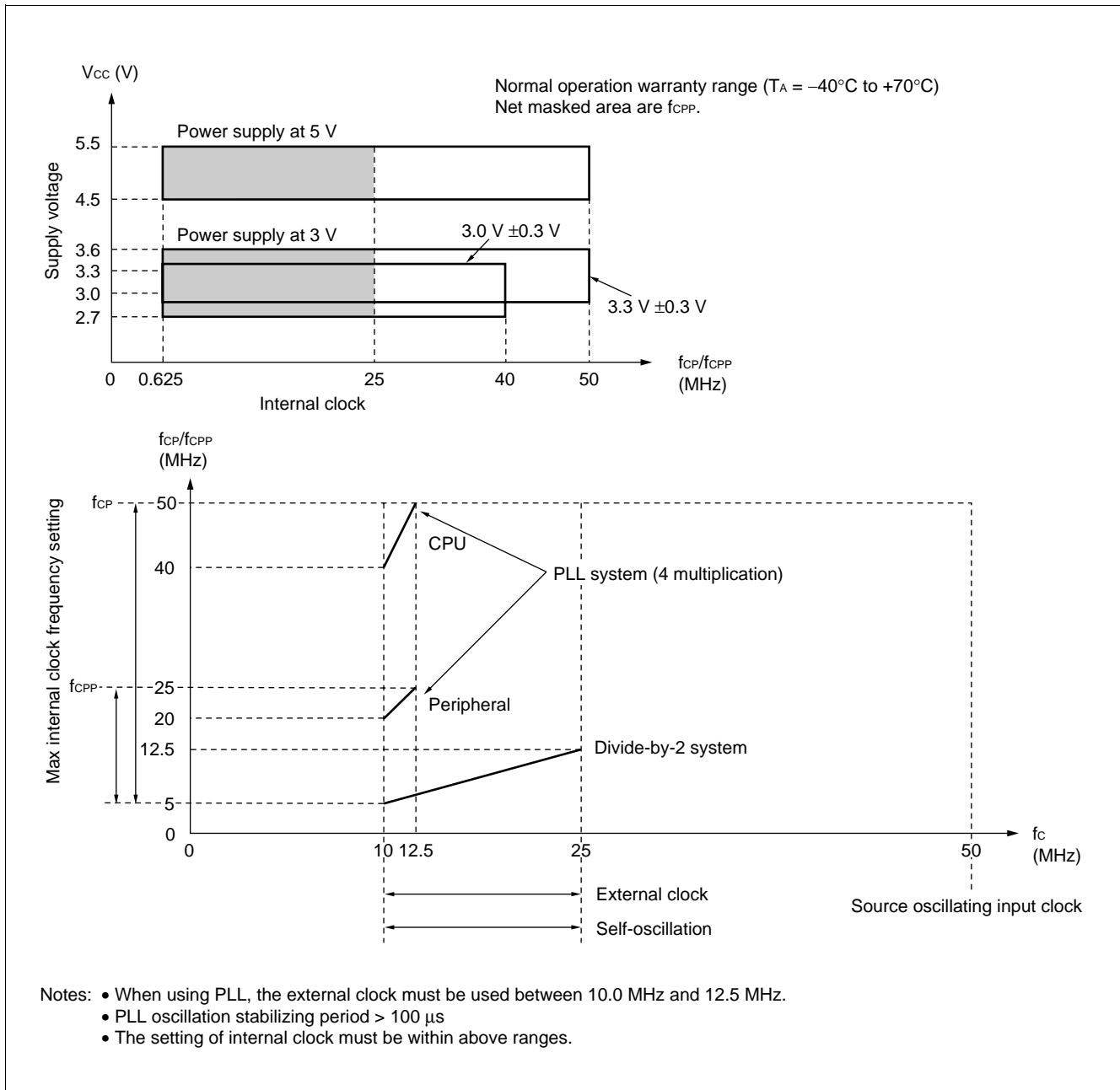
(V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V <sub>CC5</sub>	2.7	3.6	V	Normal operation
	V <sub>CC5</sub>	2.7	3.6	V	Retaining the RAM state in stop mode
	V <sub>CC3</sub>	2.7	3.6	V	*
Analog power supply voltage	AV <sub>CC</sub>	V <sub>SS</sub> + 2.7	V <sub>SS</sub> + 3.6	V	
Analog reference voltage	AV <sub>RH</sub>	AV <sub>SS</sub>	AV <sub>CC</sub>	V	
Operating temperature	T <sub>A</sub>	-40	+70	°C	

\*: Connect to V<sub>CC5</sub> for the power supply pin.

#### • Connecting to a power supply





**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB91101/MB91101A

## 3. DC Characteristics

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	$V_{IH}$	Input pin except for hysteresis input	—	$0.65 \times V_{CC3}$	—	$V_{CC5} + 0.3$	V	*
	$V_{IHS}$	$\overline{HST}$ , $\overline{NMI}$ , $\overline{RST}$ , PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	—	$0.8 \times V_{CC3}$	—	$V_{CC5} + 0.3$	V	Hysteresis input *
"L" level input voltage	$V_{IL}$	Input other than following symbols	—	$V_{SS} - 0.3$	—	$0.25 \times V_{CC3}$	V	*
	$V_{ILS}$	$\overline{HST}$ , $\overline{NMI}$ , $\overline{RST}$ , PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	—	$V_{SS} - 0.3$	—	$0.2 \times V_{CC3}$	V	Hysteresis input *
"H" level output voltage	$V_{OH}$	D16 to D31, A00 to A24, P60 to P67, P80 to P82, P85, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7 CS0, WR0	$V_{CC5} = 4.5\text{ V}$ $I_{OH} = -4.0\text{ mA}$	$V_{CC5} - 0.5$	—	—	V	
			$V_{CC5} = V_{CC3} = 2.7\text{ V}$ $I_{OH} = -4.0\text{ mA}$	$V_{CC5} - 0.8$	—	—		
"L" level output voltage	$V_{OL}$	D16 to D31, A00 to A24, P60 to P67, P80 to P82, P85, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7 CS0, WR0	$V_{CC5} = 4.5\text{ V}$ $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
			$V_{CC5} = V_{CC3} = 2.7\text{ V}$ $I_{OL} = 4.0\text{ mA}$	—	—	0.6		
Input leakage current (High-Z output leakage current)	$I_{LI}$	D16 to D31, A00 to A23, P80 to P82, P85, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	$V_{CC5} = 5.5\text{ V}$ $0.45\text{ V} < V_i < V_{CC}$	-5	—	+5	$\mu\text{A}$	
			$V_{CC5} = V_{CC3} = 3.6\text{ V}$ $0.45\text{ V} < V_i < V_{CC}$	-5	—	+5		

(Continued)



(Continued)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistance	R <sub>PULL</sub>	RST	V <sub>CC5</sub> = 5.5 V V <sub>I</sub> = 0.45 V	25	50	100	kΩ	
			V <sub>CC5</sub> = V <sub>CC3</sub> = 3.6 V V <sub>I</sub> = 0.45 V	60	125	250		
Power supply current	I <sub>CC</sub>	V <sub>CC5</sub> , V <sub>CC3</sub>	F <sub>C</sub> = 12.5 MHz V <sub>CC5</sub> = 5.5 V	—	75	100	mA	(4 multiplication) Operation at 50 MHz
			F <sub>C</sub> = 12.5 MHz V <sub>CC5</sub> = V <sub>CC3</sub> = 3.6 V	—	75	100		
	I <sub>CCS</sub>	V <sub>CC5</sub> , V <sub>CC3</sub>	F <sub>C</sub> = 12.5 MHz V <sub>CC5</sub> = 5.5 V	—	40	60	mA	Sleep mode
			F <sub>C</sub> = 12.5 MHz V <sub>CC5</sub> = V <sub>CC3</sub> = 3.6 V	—	40	60		
	I <sub>CCH</sub>	V <sub>CC5</sub> , V <sub>CC3</sub>	T <sub>A</sub> = +25°C V <sub>CC5</sub> = 5.5 V	—	10	100	μA	Stop mode
			T <sub>A</sub> = +25°C V <sub>CC5</sub> = V <sub>CC3</sub> = 3.6 V	—	10	100		
Input capacitance	C <sub>IN</sub>	Except for V <sub>CC5</sub> , V <sub>CC3</sub> , AV <sub>CC</sub> , AV <sub>SS</sub> , V <sub>SS</sub>	—	—	10	—	pF	

\*: V<sub>CC3</sub> = 3.3 ± 0.2 V (internal regulator output voltage) when using 5 V power supply, V<sub>CC3</sub> = power supply voltage when using 3 V power supply (internal regulator unused).

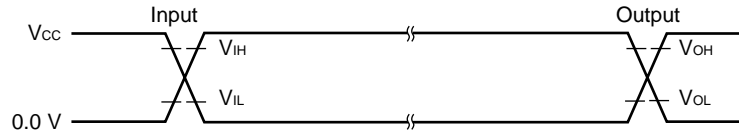
# MB91101/MB91101A

## 4. AC Characteristics

### Measurement Conditions

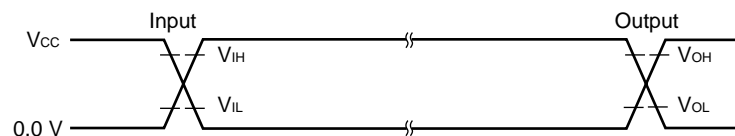
- $V_{cc5} = 5.0\text{ V} \pm 10\%$

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
"H" level input voltage	$V_{IH}$	—	2.4	—	V	
"L" level input voltage	$V_{IL}$	—	0.8	—	V	
"H" level output voltage	$V_{OH}$	—	2.4	—	V	
"L" level output voltage	$V_{OL}$	—	0.8	—	V	

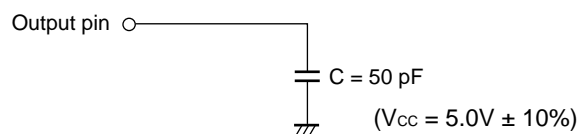


- $V_{cc5} = V_{cc3} = 2.7\text{ V to }3.6\text{ V}$

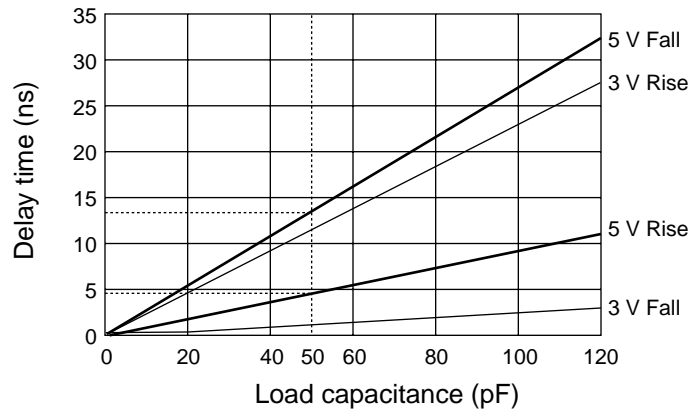
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
"H" level input voltage	$V_{IH}$	—	$1/2 \times V_{cc3}$	—	V	
"L" level input voltage	$V_{IL}$	—	$1/2 \times V_{cc3}$	—	V	
"H" level output voltage	$V_{OH}$	—	$1/2 \times V_{cc3}$	—	V	
"L" level output voltage	$V_{OL}$	—	$1/2 \times V_{cc3}$	—	V	



- Load conditions



- Load capacitance - Delay characteristics (Output delay with reference to the internal)



# MB91101/MB91101A

## (1) Clock Timing Rating

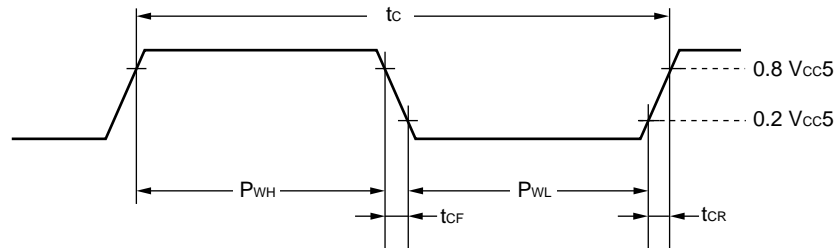
( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Clock frequency	$f_c$	X0, X1	When using PLL	10	12.5	MHz	
	$f_c$	X0, X1	Self-oscillation (divide-by-2 input)	10	25	MHz	
	$f_c$	X0, X1	External clock (divide-by-2 input)	10	25	MHz	
Clock cycle time	$t_c$	X0, X1	When using PLL	80	100	ns	
	$t_c$	X0, X1	—	40	100	ns	
Input clock pulse width	$P_{WH}, P_{WL}$	X0, X1	—	25	—	ns	Input to X0 only, when using 5 V power supply
	$P_{WH}, P_{WL}$	X0, X1		10	—	ns	Input to X0, X1
Input clock rising/falling time	$t_{CR}, t_{CF}$	X0, X1		—	8	ns	( $t_{CR} + t_{CF}$ )
Internal operating clock frequency	$f_{CP}$	—	CPU system	$0.625^{*1}$	50	MHz	
	$f_{CPB}$	—	Bus system	$0.625^{*1}$	$25^{*2}$	MHz	
	$f_{CPP}$	—	Peripheral system	$0.625^{*1}$	25	MHz	
Internal operating clock cycle time	$t_{CP}$	—	CPU system	20	$1600^{*1}$	ns	
	$t_{CPB}$	—	Bus system	$40^{*2}$	$1600^{*1}$	ns	
	$t_{CPP}$	—	Peripheral system	40	$1600^{*1}$	ns	

\*1: These values are for a minimum clock of 10 MHz input to X0, a divide-by-2 system of the source oscillation and a 1/8 gear.

\*2: Values when using the doubler and CPU operation at 50 MHz.

- Clock timing rating measurement conditions



# MB91101/MB91101A

## (2) Clock Output Timing

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	$t_{CYC}$	CLK	—	$t_{CP}$	—	ns	*1
	$t_{CYC}$	CLK	Using the doubler	$t_{CPB}$	—	ns	
CLK $\uparrow \rightarrow$ CLK $\downarrow$	$t_{CHCL}$	CLK	—	$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*2
CLK $\downarrow \rightarrow$ CLK $\uparrow$	$t_{CLCH}$	CLK		$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*3

$t_{CP}$ ,  $t_{CPB}$  (internal operating clock cycle time): Refer to “(1) Clock Timing Rating.”

\*1:  $t_{CYC}$  is a frequency for 1 clock cycle including a gear cycle.  
 Use the doubler when CPU frequency is above 25 MHz.

\*2: Rating at a gear cycle of  $\times 1$ .  
 When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equations with 1/2, 1/4, 1/8, respectively.

$$\text{Min} : (1 - n/2) \times t_{CYC} - 10$$

$$\text{Max} : (1 - n/2) \times t_{CYC} + 10$$

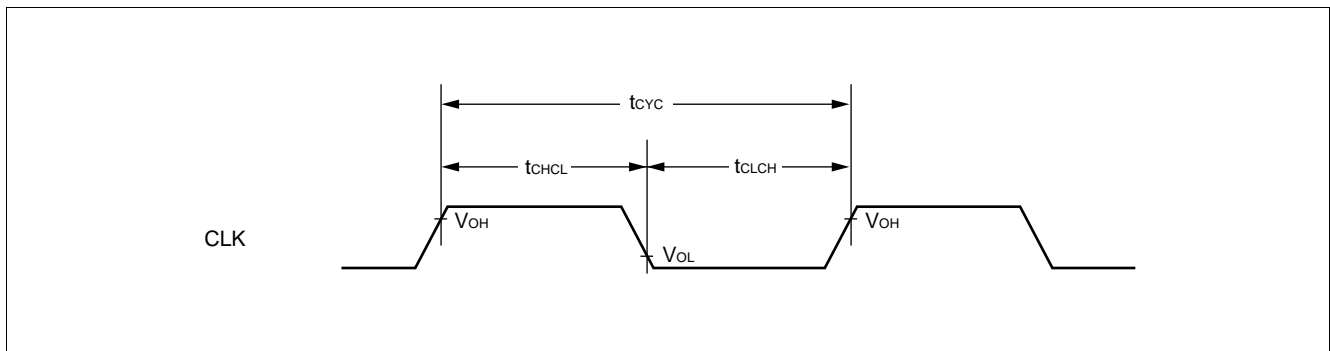
Select a gear cycle of  $\times 1$  when using the doubler.

\*3: Rating at a gear cycle of  $\times 1$ .  
 When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equations with 1/2, 1/4, 1/8, respectively.

$$\text{Min} : n/2 \times t_{CYC} - 10$$

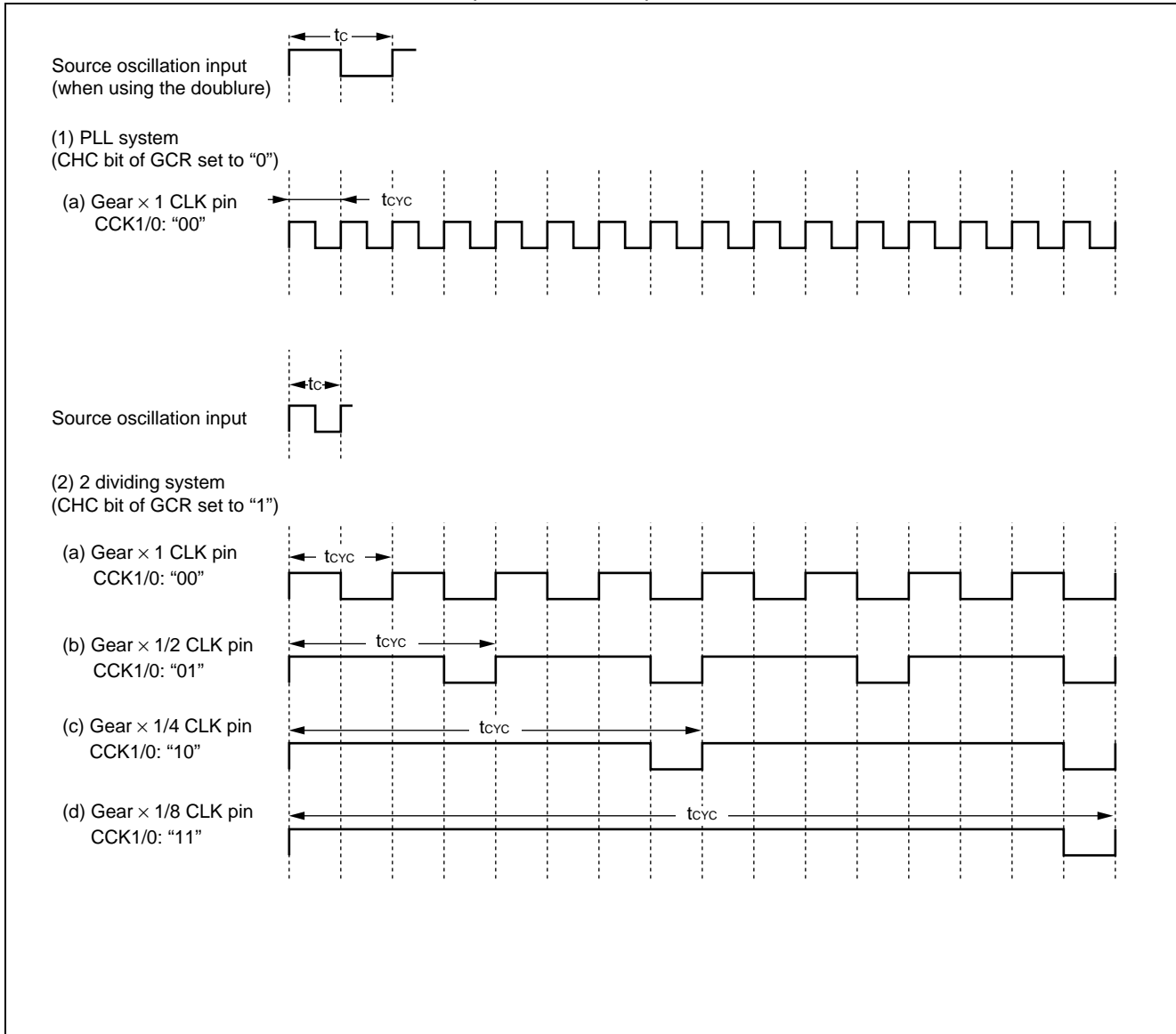
$$\text{Max} : n/2 \times t_{CYC} + 10$$

Select a gear cycle of  $\times 1$  when using the doubler.



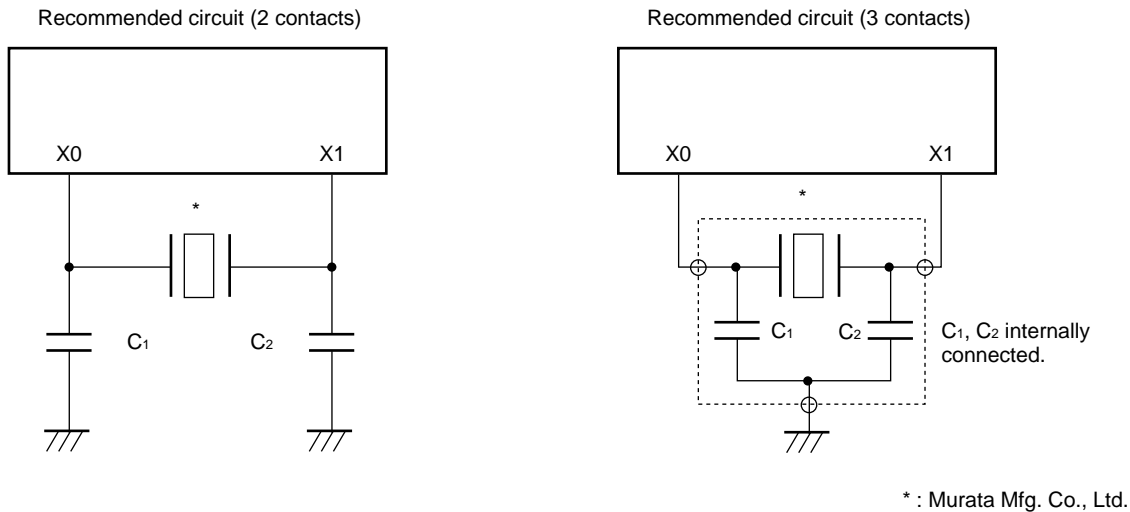
The relation between the input waveform of source oscillation and the output waveform of CLK pin for configured by CHC/CCK1/CCK0 settings of GCR (gear control register) is as follows:

However, in this chart source oscillation input means X0 input clock.



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## • Ceramic oscillator applications



## • Discreet type

Oscillation frequency [MHz]	Model	Load capacitance $C_1 = C_2$ [pF]	Power supply voltage $V_{CC5}$ [V]
5.00 to 6.30	CSA□□□MG	30	2.9 to 5.5
	CST□□□MGW	(30)	
	CSA□□□MG093	30	2.7 to 5.5
	CST□□□MGW093	(30)	
6.31 to 10.0	CSA□□□MTZ	30	2.9 to 5.5
	CST□□□MTW	(30)	
	CSA□□□MTZ093	30	2.7 to 5.5
	CST□□□MTW093	(30)	
10.1 to 13.0	CSA□□□MTZ	30	3.0 to 5.5
	CST□□□MTW	(30)	
	CSA□□□MTZ093	30	2.9 to 5.5
	CST□□□MTW093	(30)	
13.01 to 15.00	CSA□□□□MXZ040	15	3.2 to 5.5
	CST□□□□MXW0C3	(15)	

( ):  $C_1$  and  $C_2$  internally connected 3 contacts type.

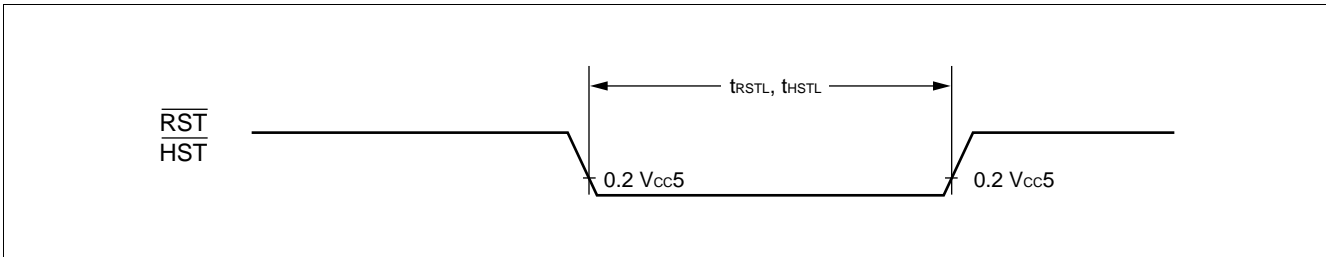


### (3) Reset/Hardware Standby Input Ratings

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	$t_{RSTL}$	$\overline{RST}$	—	$t_{CP} \times 5$	—	ns	
Hardware standby input time	$t_{HSTL}$	$\overline{HST}$		$t_{CP} \times 5$	—	ns	

$t_{CP}$  (internal operating clock cycle time): Refer to “(1) Clock Timing Rating.”



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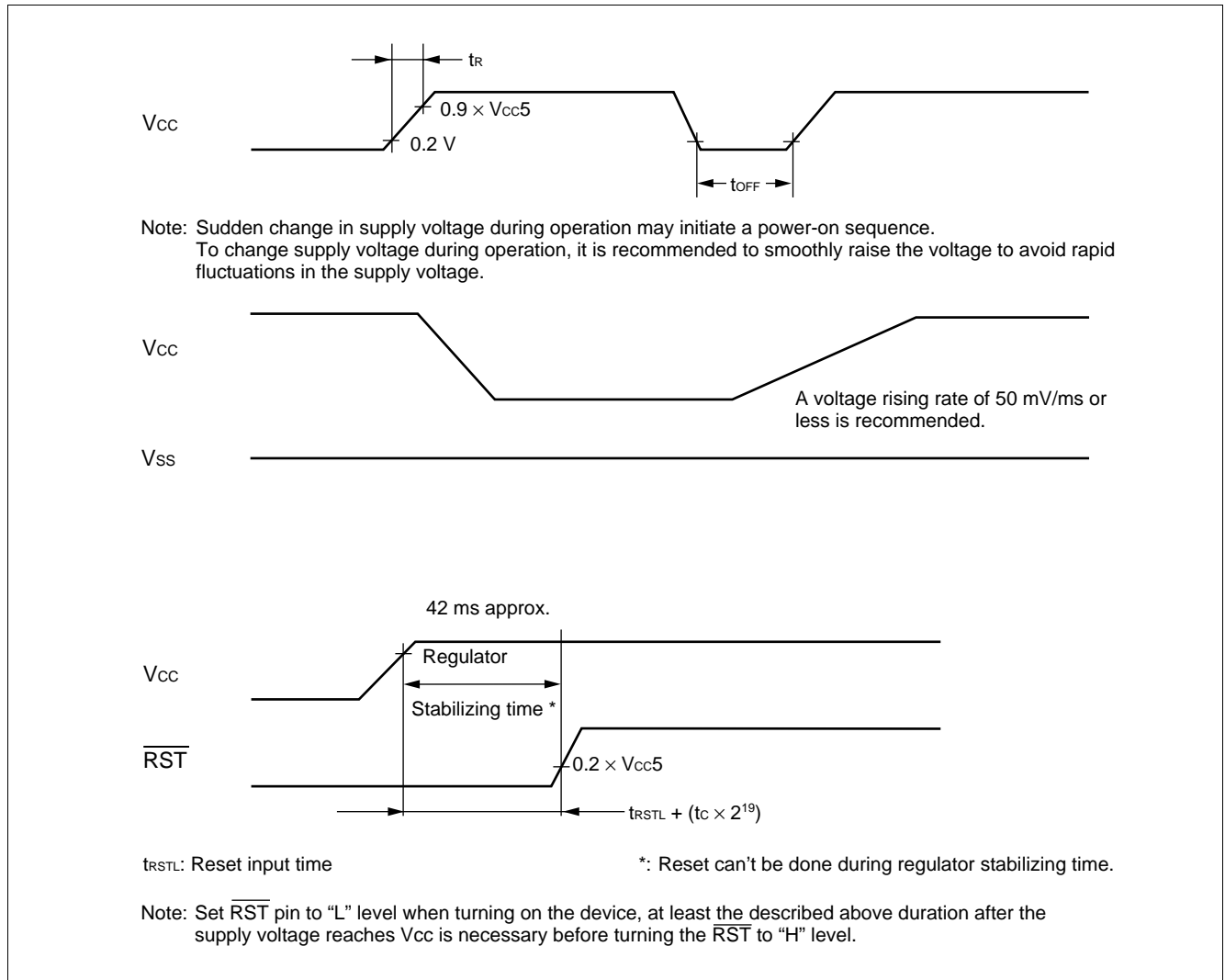
## (4) Power on Supply Specifications (Power-on Reset)

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	$t_R$	$V_{CC}$	$V_{CC} = 5.0\text{ V}$	50	—	$\mu\text{s}$	*
	$t_R$	$V_{CC}$		—	30	ms	*
	$t_R$	$V_{CC}$	$V_{CC} = 3.0/3.3\text{ V}$	50	—	$\mu\text{s}$	*
	$t_R$	$V_{CC}$		—	18	ms	*
Power supply shut off time	$t_{OFF}$	$V_{CC}$	—	1	—	ms	Repeated operations

$t_c$  (clock cycle time): Refer to "(1) Clock Timing Rating."

\*:  $V_{CC} < 0.2\text{ V}$  before the power supply rising



## (5) Normal Bus Access Read/Write Operation

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS5}$ delay time	$t_{CHCSL}$	CLK, $\overline{CS0}$ to $\overline{CS5}$	—	—	15	ns	
	$t_{CHCSH}$	CLK, $\overline{CS0}$ to $\overline{CS5}$		—	15	ns	
Address delay time	$t_{CHAV}$	CLK, A24 to A00		—	15	ns	
Data delay time	$t_{CHDV}$	CLK, D31 to D16		—	15	ns	
$\overline{RD}$ delay time	$t_{CLR L}$	CLK, $\overline{RD}$		—	6	ns	
	$t_{CLR H}$	CLK, $\overline{RD}$		—	6	ns	
$\overline{WR0}$ , $\overline{WR1}$ delay time	$t_{CLWL}$	CLK, $\overline{WR0}$ , $\overline{WR1}$		—	6	ns	
	$t_{CLWH}$	CLK, $\overline{WR0}$ , $\overline{WR1}$		—	6	ns	
Valid address → valid data input time	$t_{AVDV}$	A24 to A00, D31 to D16		—	$\frac{3}{2} \times t_{CYC}$ – 25	ns	*1 *2
$\overline{RD} \downarrow \rightarrow$ valid data input time	$t_{RLDV}$	$\overline{RD}$ , D31 to D16		—	$t_{CYC} - 10$	ns	*1
Data set up → $\overline{RD} \uparrow$ time	$t_{DSRH}$	$\overline{RD}$ , D31 to D16	10	—	ns		
$\overline{RD} \uparrow \rightarrow$ data hold time	$t_{RHDX}$	$\overline{RD}$ , D31 to D16	0	—	ns		

$t_{CYC}$  (a cycle time of peripheral system clock): Refer to “(2) Clock Output Timing.”

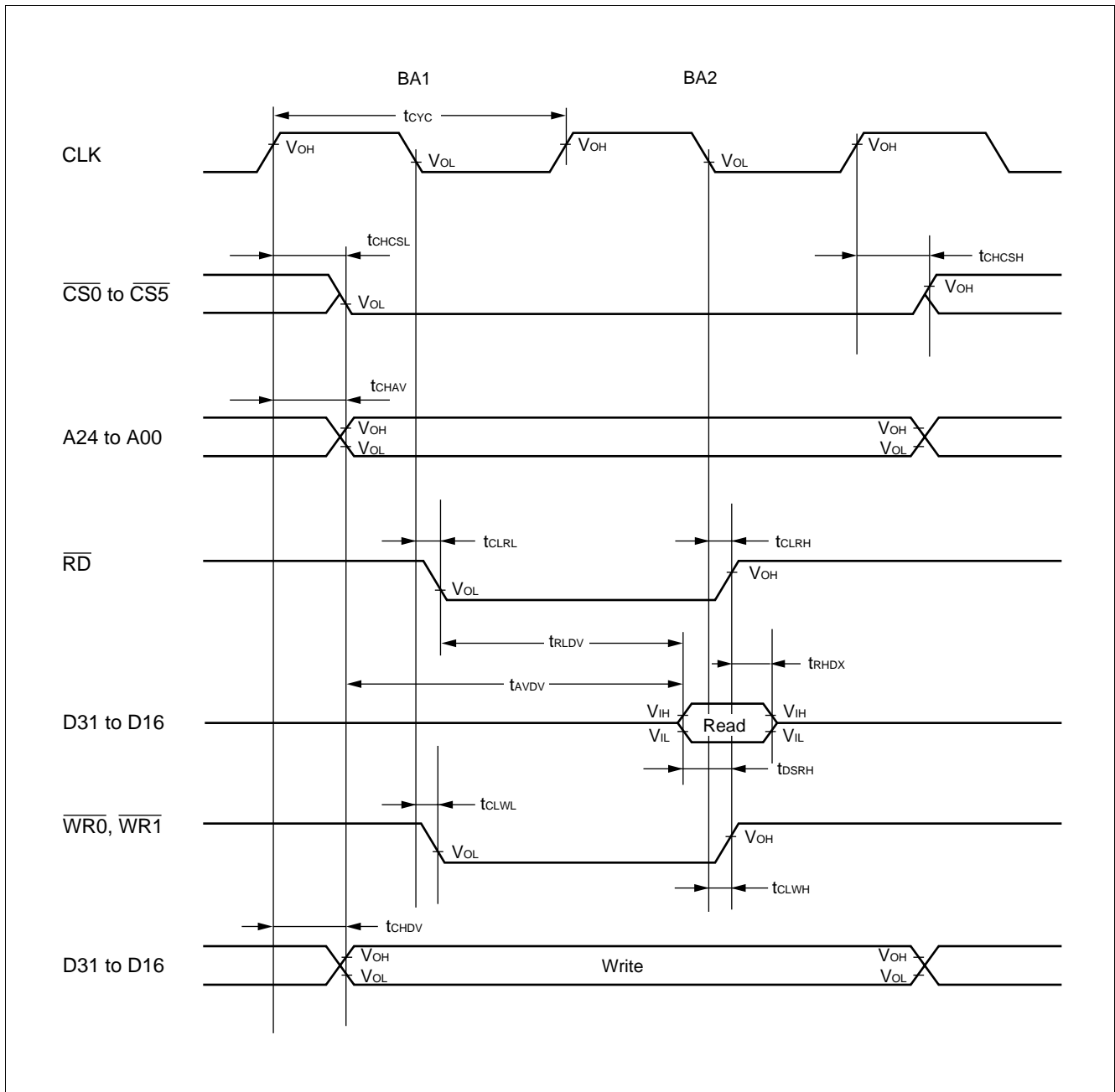
\*1: When bus timing is delayed by automatic wait insertion or RDY input, add ( $t_{CYC} \times$  extended cycle number for delay) to this rating.

\*2: Rating at a gear cycle of  $\times 1$ .

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.

Equation:  $(2 - n/2) \times t_{CYC} - 25$

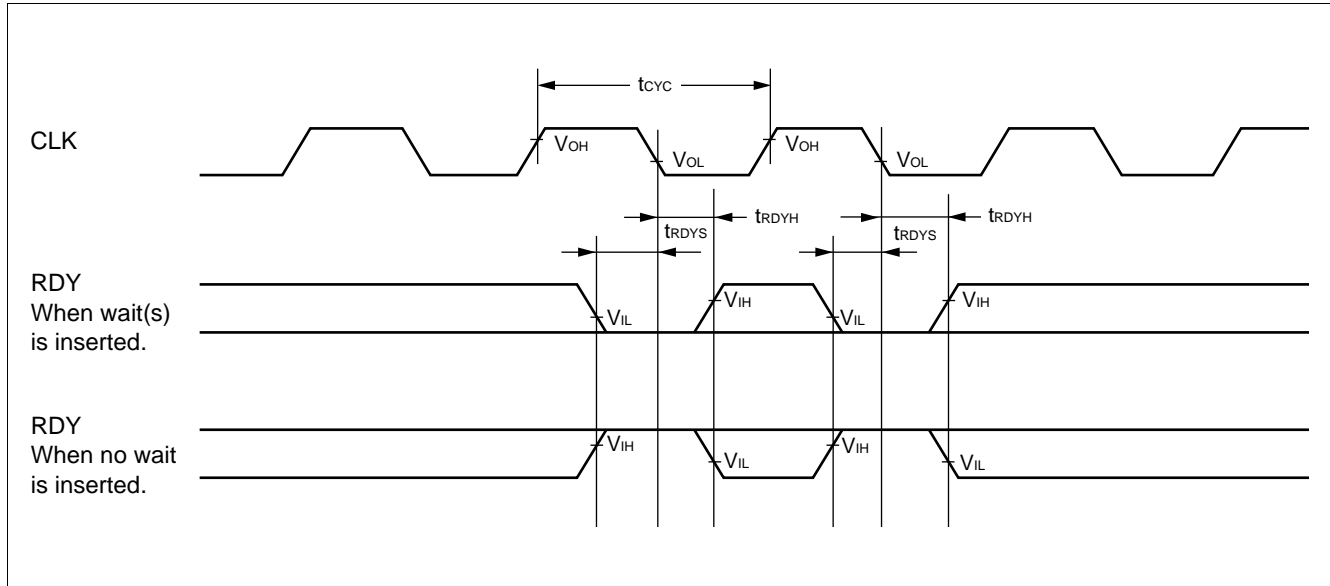
# MB91101/MB91101A



## (6) Ready Input Timing

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RDY set up time → CLK ↓	$t_{RDYS}$	RDY, CLK	—	15	—	ns	
CLK ↓ → RDY hold time	$t_{RDYH}$	RDY, CLK		0	—	ns	



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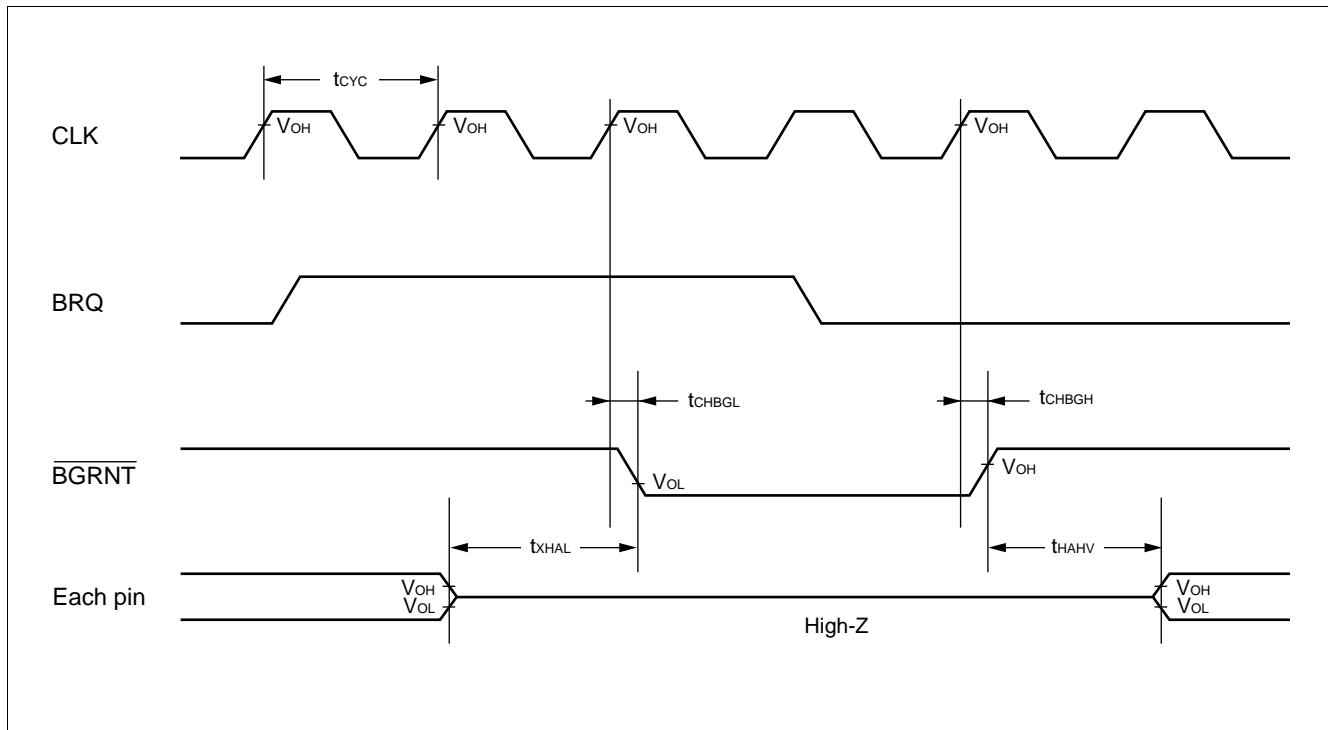
## (7) Hold Timing

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{\text{BGRNT}}$ delay time	$t_{\text{CHBGL}}$	CLK, $\overline{\text{BGRNT}}$	—	—	6	ns	
	$t_{\text{CHBGH}}$	CLK, $\overline{\text{BGRNT}}$		—	6	ns	
Pin floating $\rightarrow$ $\overline{\text{BGRNT}}$ $\downarrow$ time	$t_{\text{XHAL}}$	$\overline{\text{BGRNT}}$		$t_{\text{CYC}} - 10$	$t_{\text{CYC}} + 10$	ns	
$\overline{\text{BGRNT}}$ $\uparrow$ $\rightarrow$ pin valid time	$t_{\text{HAHV}}$	$\overline{\text{BGRNT}}$		$t_{\text{CYC}} - 10$	$t_{\text{CYC}} + 10$	ns	

$t_{\text{CYC}}$  (a cycle time of peripheral system clock): Refer to “(2) Clock Output Timing.”

Note : There is a delay time of more than 1 cycle from BRQ input to  $\overline{\text{BGRNT}}$  change.



## (8) Normal DRAM Mode Read/Write Cycle

(V<sub>CC5</sub> = 5.0 V ±10%, V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +70°C)  
(V<sub>CC5</sub> = V<sub>CC3</sub> = 2.7 V to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t <sub>CLRAH</sub>	CLK, RAS0, RAS1	—	—	6	ns	
	t <sub>CHRAL</sub>	CLK, RAS0, RAS1		—	6	ns	
CAS delay time	t <sub>CLCASL</sub>	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
	t <sub>CLCASH</sub>	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
ROW address delay time	t <sub>CHRAV</sub>	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t <sub>CHCAV</sub>	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t <sub>CHDWL</sub>	CLK, $\overline{DW0}$ , $\overline{DW1}$		—	15	ns	
	t <sub>CHDWH</sub>	CLK, $\overline{DW0}$ , $\overline{DW1}$		—	15	ns	
Output data delay time	t <sub>CHDV1</sub>	CLK, D31 to D16		—	15	ns	
RAS ↓→ valid data input time	t <sub>RLDV</sub>	RAS0, RAS1, D31 to D16		—	$5/2 \times t_{CYC} - 16$	ns	*1 *2
CAS ↓→ valid data input time	t <sub>CLDV</sub>	CS0H, CS0L, CS1H, CS1L, D31 to D16		—	$t_{CYC} - 17$	ns	*1
CAS ↑→ data hold time	t <sub>CADH</sub>	CS0H, CS0L, CS1H, CS1L, D31 to D16		0	—	ns	

t<sub>CYC</sub> (a cycle time of peripheral system clock): Refer to “(2) Clock Output Timing.”

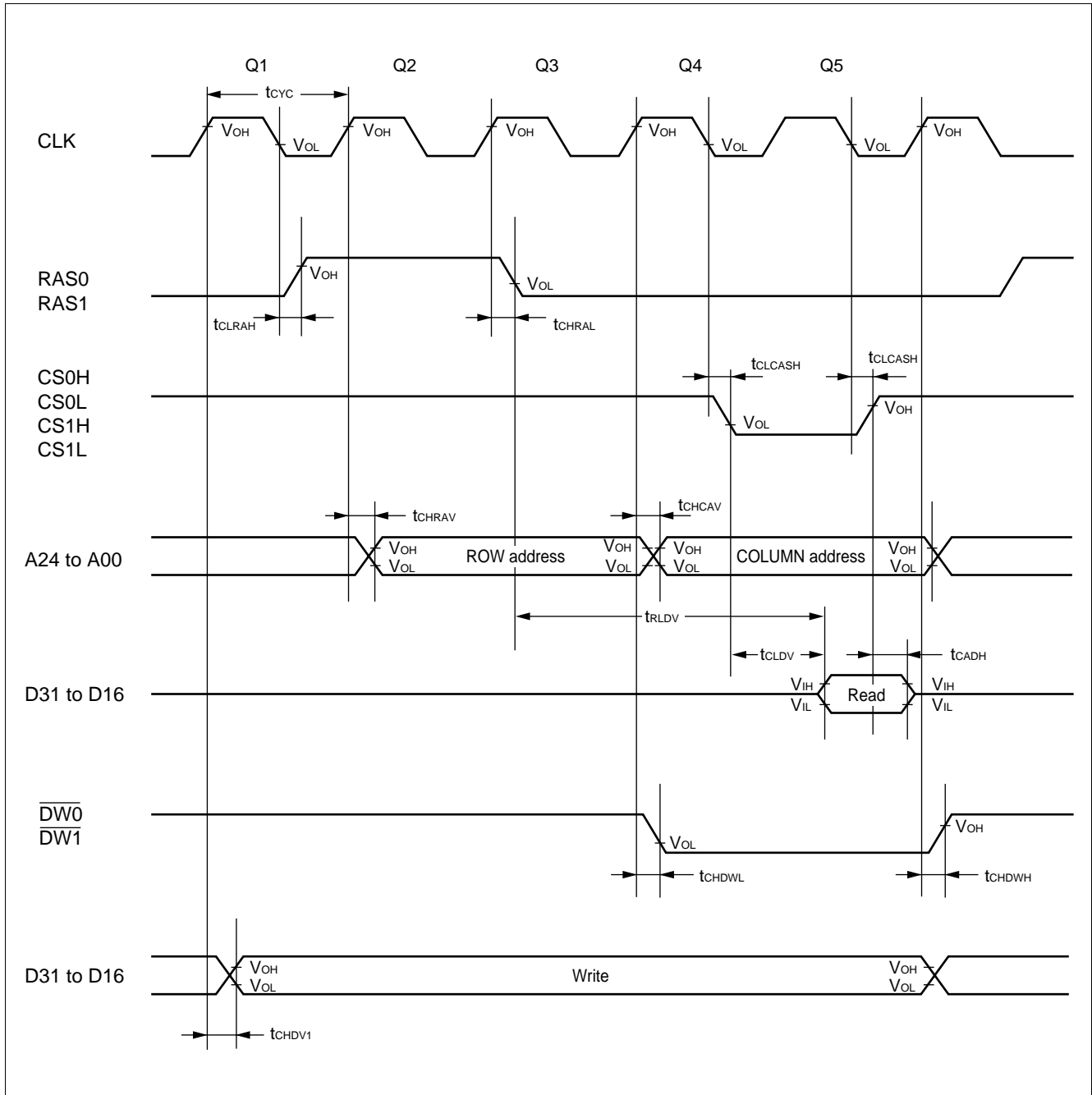
\*1: When Q1 cycle or Q4 cycle is extended for 1 cycle, add t<sub>CYC</sub> time to this rating.

\*2: Rating at a gear cycle of × 1.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.

$$\text{Equation: } (3 - n/2) \times t_{CYC} - 16$$

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## (9) Normal DRAM Mode Fast Page Read/Write Cycle

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

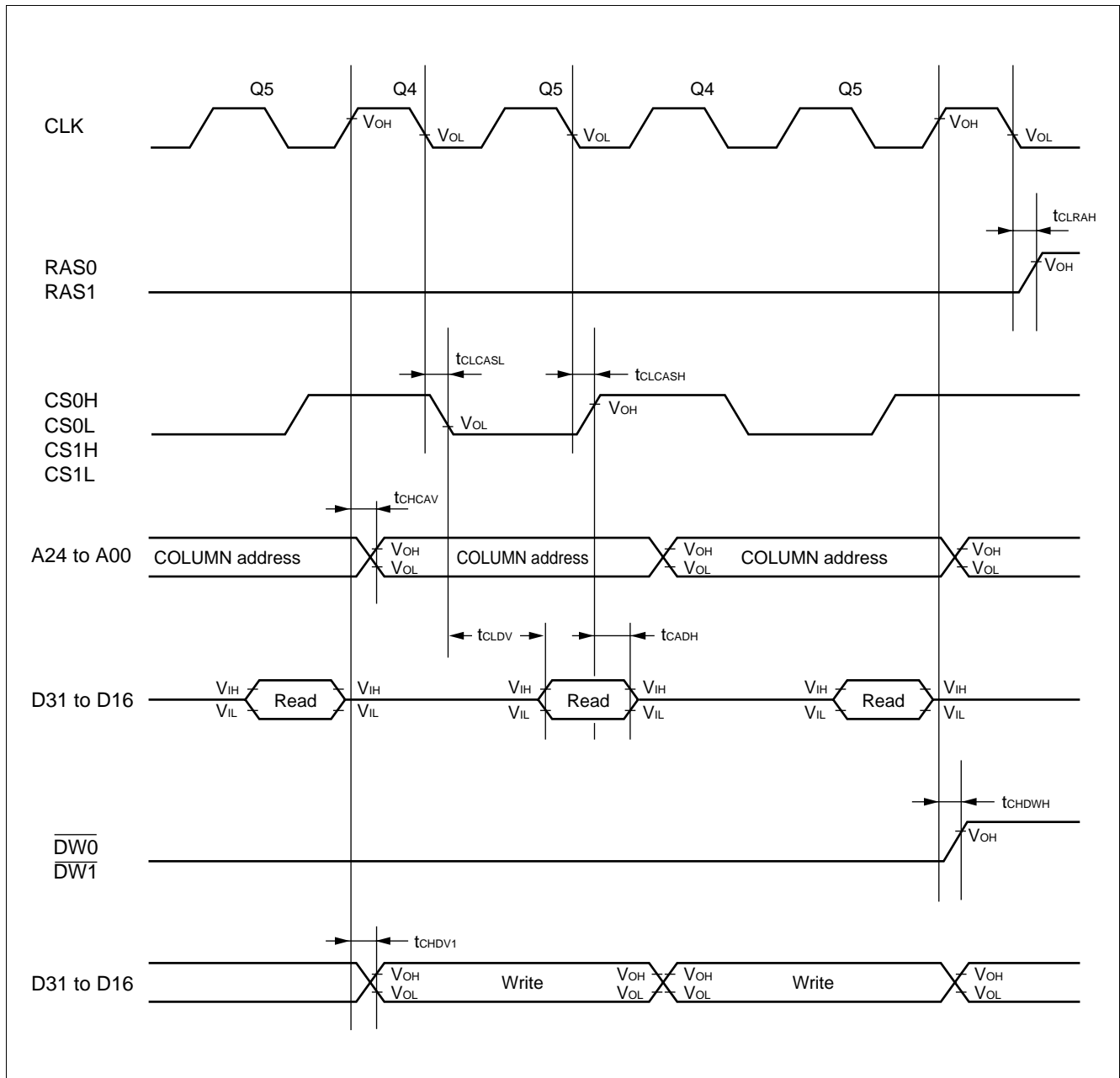
( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	$t_{CLRAH}$	CLK, RAS0, RAS1	—	—	6	ns	
CAS delay time	$t_{CLCASL}$	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
	$t_{CLCASH}$	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
COLUMN address delay time	$t_{CHCAV}$	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	$t_{CHDWH}$	CLK, $\overline{DW0}$ , $\overline{DW1}$		—	15	ns	
Output data delay time	$t_{CHDV1}$	CLK, D31 to D16		—	15	ns	
CAS $\downarrow \rightarrow$ valid data input time	$t_{CLDV}$	CS0H, CS0L, CS1H, CS1L, D31 to D16		—	$t_{CYC} - 17$	ns	*
CAS $\uparrow \rightarrow$ data hold time	$t_{CADH}$	CS0H, CS0L, CS1H, CS1L, D31 to D16		0	—	ns	

$t_{CYC}$  (a cycle time of peripheral system clock): Refer to "(2) Clock Output Timing."

\*: When Q4 cycle is extended for 1 cycle, add  $t_{CYC}$  time to this rating.

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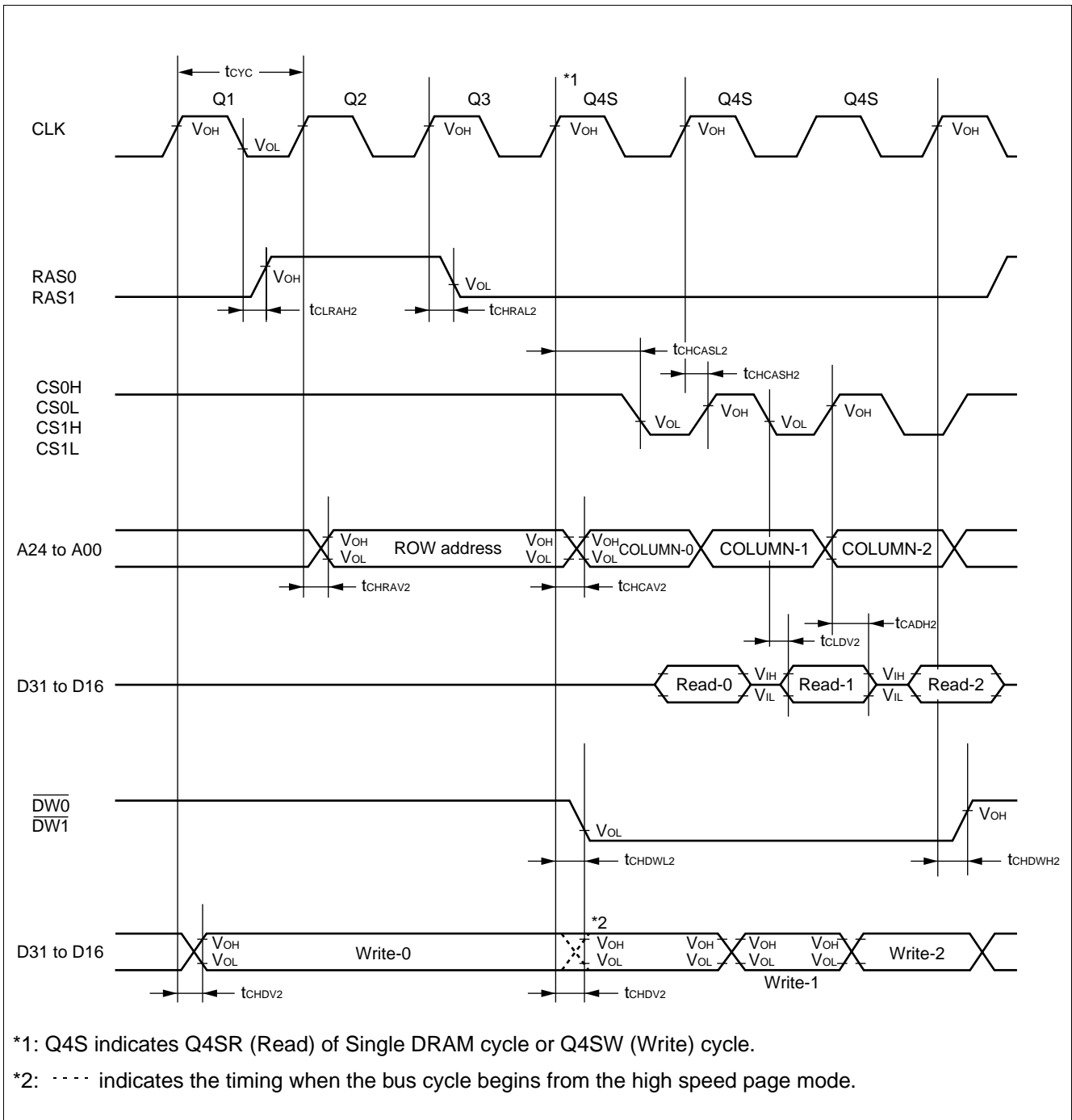
## (10) Single DRAM Timing

(V<sub>CC5</sub> = 5.0 V ±10%, V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +70°C)  
(V<sub>CC5</sub> = V<sub>CC3</sub> = 2.7 V to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t <sub>CLRAH2</sub>	CLK, RAS0, RAS1	—	—	6	ns	
	t <sub>CHRAL2</sub>	CLK, RAS0, RAS1			6	ns	
CAS delay time	t <sub>CHCASL2</sub>	CLK, CS0H, CS0L, CS1H, CS1L		—	n/2 × t <sub>cyC</sub>	ns	
	t <sub>CHCASH2</sub>	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
ROW address delay time	t <sub>CHRAV2</sub>	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t <sub>CHCAV2</sub>	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t <sub>CHDWL2</sub>	CLK, $\overline{DW0}$ , $\overline{DW1}$		—	15	ns	
	t <sub>CHDWH2</sub>	CLK, $\overline{DW0}$ , $\overline{DW1}$		—	15	ns	
Output data delay time	t <sub>CHDV2</sub>	CLK, D31 to D16		—	15	ns	
CAS ↓→ Valid data input time	t <sub>CLDV2</sub>	CS0H, CS0L, CS1H, CS1L, D31 to D16		—	(1 - n/2) × t <sub>cyC</sub> - 17	ns	
CAS ↑→ data hold time	t <sub>CADH2</sub>	CS0H, CS0L, CS1H, CS1L, D31 to D16		0	—	ns	

t<sub>cyC</sub> (a cycle time of peripheral system clock): Refer to “(2) Clock Output Timing.”

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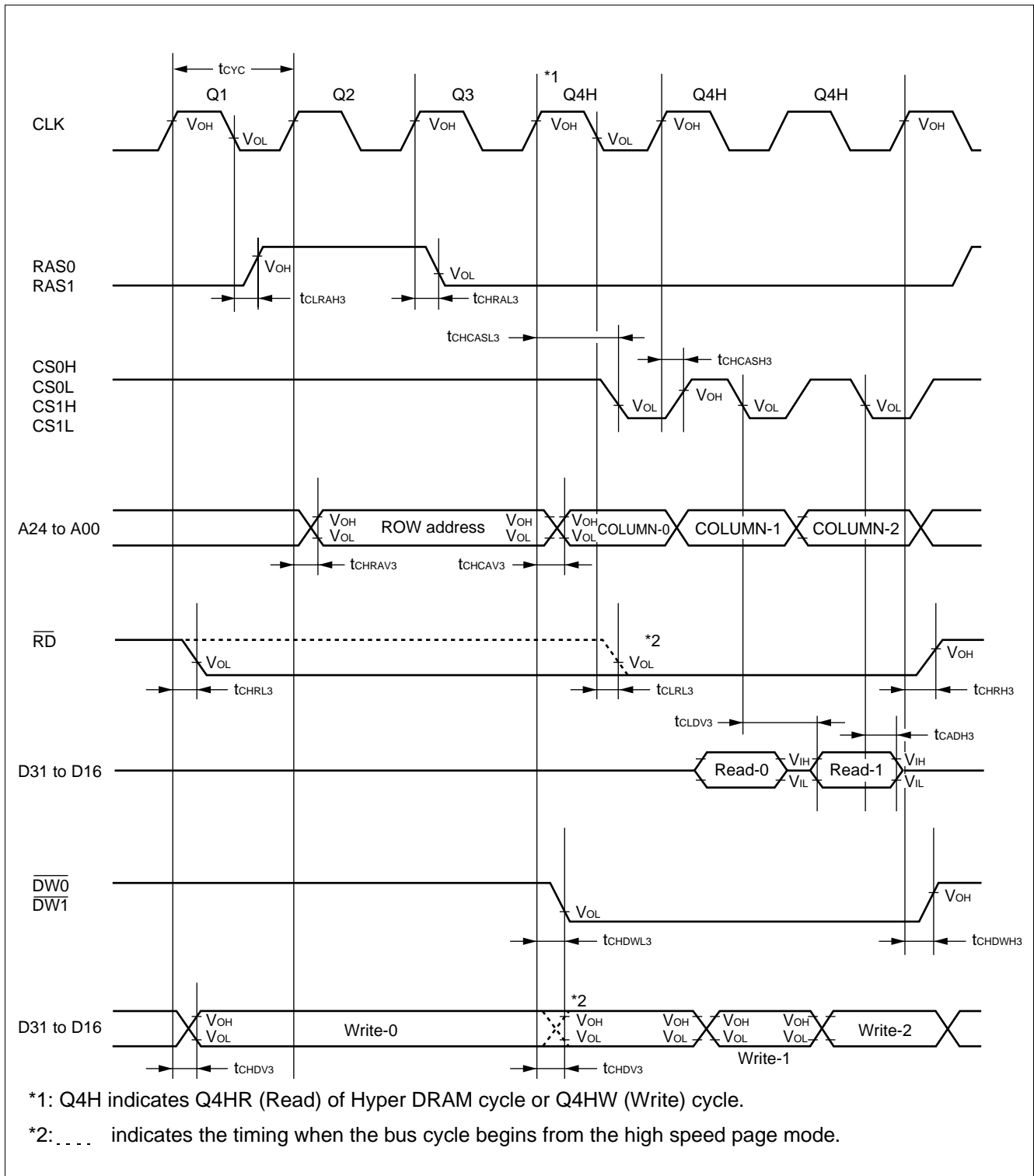
## (11) Hyper DRAM Timing

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t <sub>CLRAH3</sub>	CLK, RAS0, RAS1	—	—	6	ns	
	t <sub>CHRAL3</sub>	CLK, RAS0, RAS1		—	6	ns	
CAS delay time	t <sub>CHCASL3</sub>	CLK, CS0H, CS0L, CS1H, CS1L		—	n/2 × t <sub>cyc</sub>	ns	
	t <sub>CHCASH3</sub>	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
ROW address delay time	t <sub>CHRAV3</sub>	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t <sub>CHCAV3</sub>	CLK, A24 to A00		—	15	ns	
$\overline{\text{RD}}$ delay time	t <sub>CHRL3</sub>	CLK, $\overline{\text{RD}}$		—	15	ns	
	t <sub>CHRH3</sub>	CLK, $\overline{\text{RD}}$		—	15	ns	
	t <sub>CLRL3</sub>	CLK, $\overline{\text{RD}}$		—	15	ns	
$\overline{\text{DW}}$ delay time	t <sub>CHDWL3</sub>	CLK, $\overline{\text{DW0}}$ , $\overline{\text{DW1}}$		—	15	ns	
	t <sub>CHDWH3</sub>	CLK, $\overline{\text{DW0}}$ , $\overline{\text{DW1}}$		—	15	ns	
Output data delay time	t <sub>CHDV3</sub>	CLK, D31 to D16		—	15	ns	
CAS ↓ → valid data input time	t <sub>CLDV3</sub>	CS0H, CS0L, CS1H, CS1L, D31 to D16		—	t <sub>cyc</sub> - 17	ns	
CAS ↓ → data hold time	t <sub>CADH3</sub>	CS0H, CS0L, CS1H, CS1L, D31 to D16	0	—	ns		

t<sub>cyc</sub> (a cycle time of peripheral system clock): Refer to “(2) Clock Output Timing.”

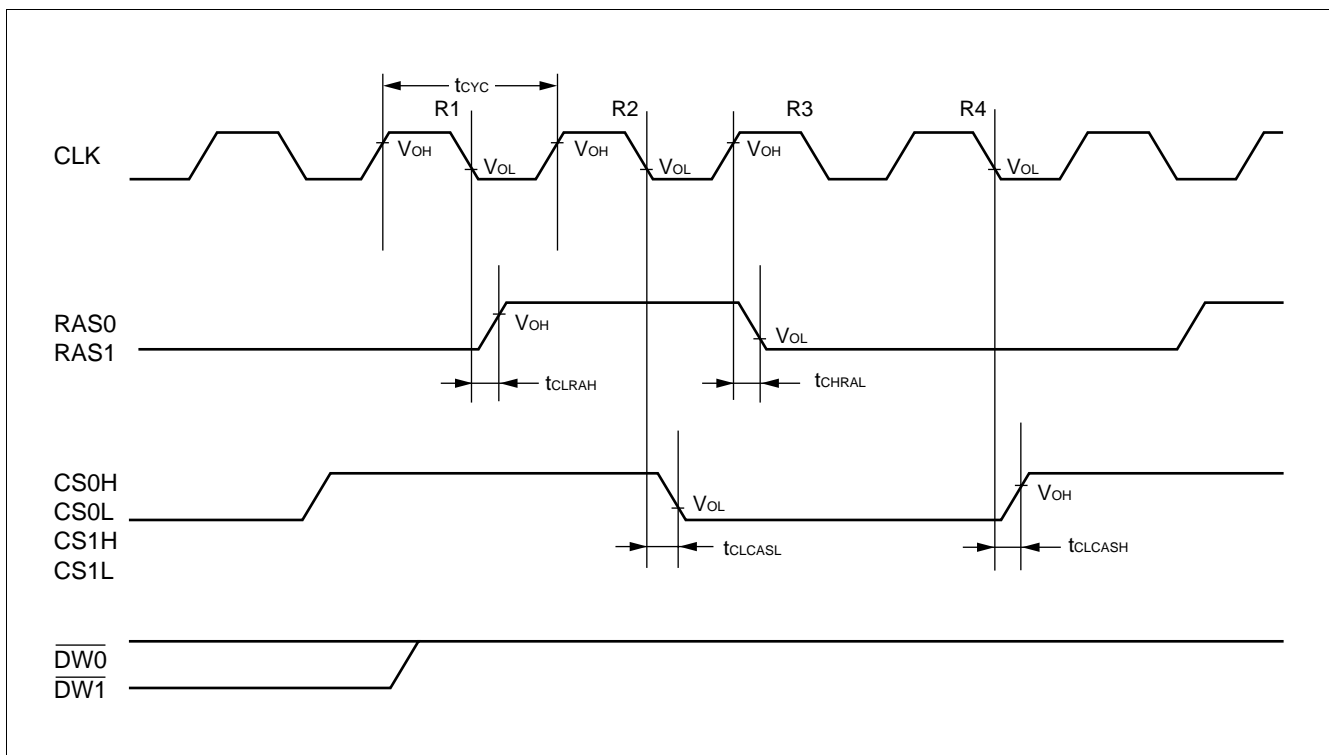
# MB91101/MB91101A



## (12) CBR Refresh

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	$t_{CLRAH}$	CLK, RAS0, RAS1	—	—	6	ns	
	$t_{CHRAL}$	CLK, RAS0, RAS1		—	6	ns	
CAS delay time	$t_{CLCASL}$	CLK, CS0H, CS0L, CS1H, CS1L	—	—	6	ns	
	$t_{CLCASH}$	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	

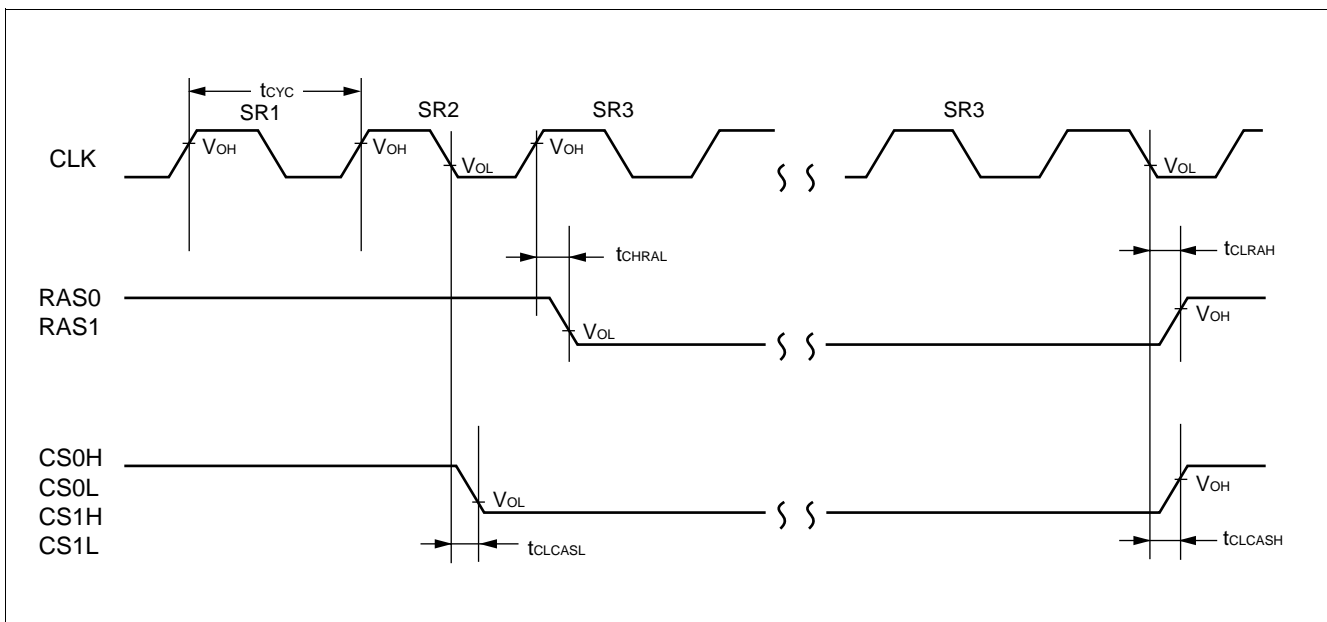


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## (13) Self Refresh

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	$t_{CLRAH}$	CLK, RAS0, RAS1	—	—	6	ns	
	$t_{CHRAL}$	CLK, RAS0, RAS1		—	6	ns	
CAS delay time	$t_{CLCASL}$	CLK, CS0H, CS0L, CS1H, CS1L	—	—	6	ns	
	$t_{CLCASH}$	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	





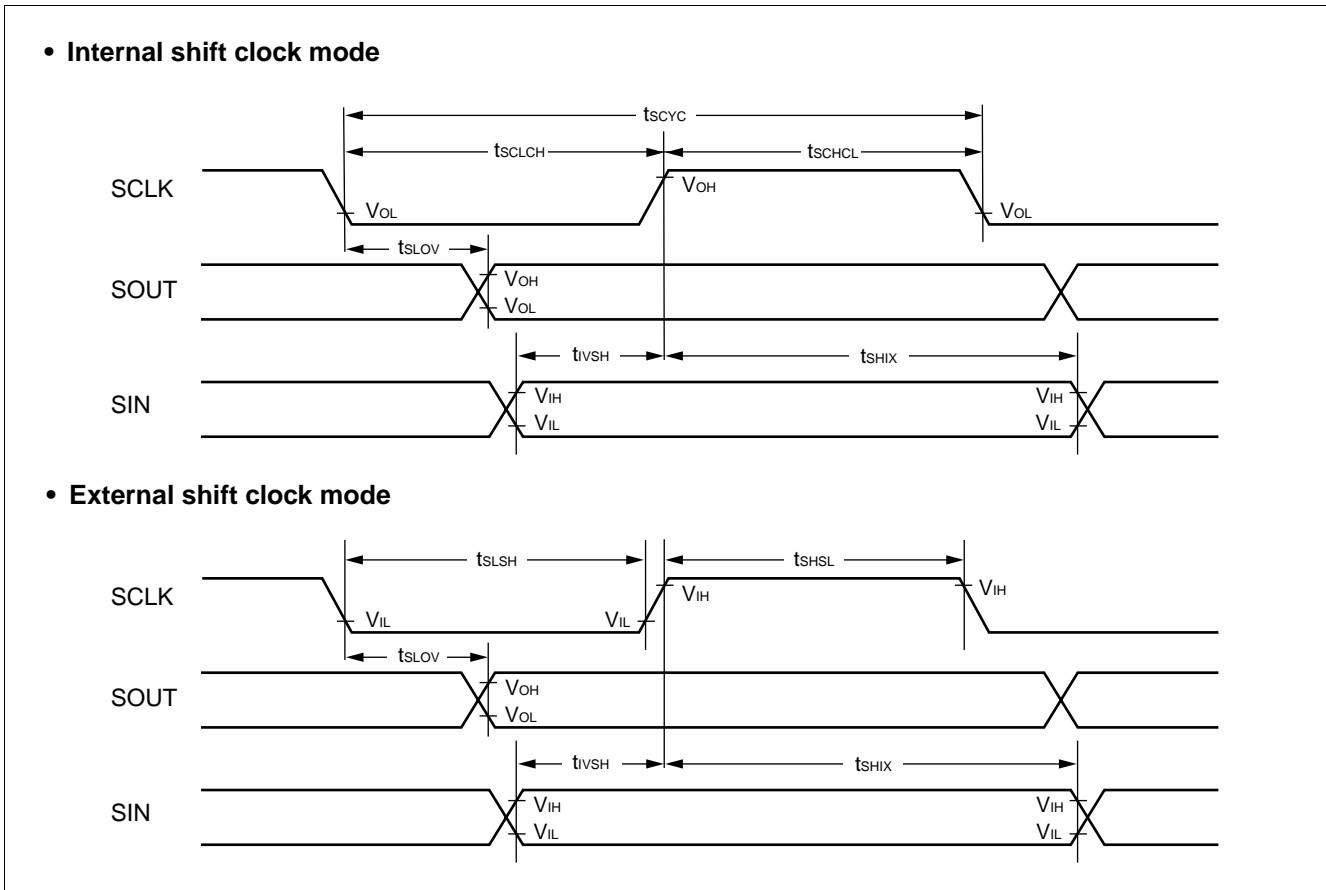
## (14) UART Timing

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t <sub>SCYC</sub>	—	Internal shift clock mode	$8 \times t_{CYCP}$	—	ns	
SCLK ↓ → SCLK ↑	t <sub>SCLCH</sub>	—		$4 \times t_{CYCP} - 10$	$4 \times t_{CYCP} + 10$	ns	
SCLK ↑ → SCLK ↓	t <sub>SCHCL</sub>	—		$4 \times t_{CYCP} - 10$	$4 \times t_{CYCP} + 10$	ns	
SCLK ↓ → SOUT delay time	t <sub>SLOV</sub>	—		-80	+80	ns	
Valid SIN → SCLK ↑	t <sub>IVSH</sub>	—		100	—	ns	
SCLK ↑ → valid SIN hold time	t <sub>SHIX</sub>	—		60	—	ns	
Serial clock "H" pulse width	t <sub>SHSL</sub>	—	External shift clock mode	$4 \times t_{CYCP}$	—	ns	
Serial clock "L" pulse width	t <sub>SLSH</sub>	—		$4 \times t_{CYCP}$	—	ns	
SCLK ↓ → SOUT delay time	t <sub>SLOV</sub>	—		—	150	ns	
Valid SIN → SCLK ↑	t <sub>IVSH</sub>	—		60	—	ns	
SCLK ↑ → valid SIN hold time	t <sub>SHIX</sub>	—		60	—	ns	

t<sub>CYCP</sub>: A cycle time of peripheral system clock

Note : This rating is for AC characteristics in CLK synchronous mode.



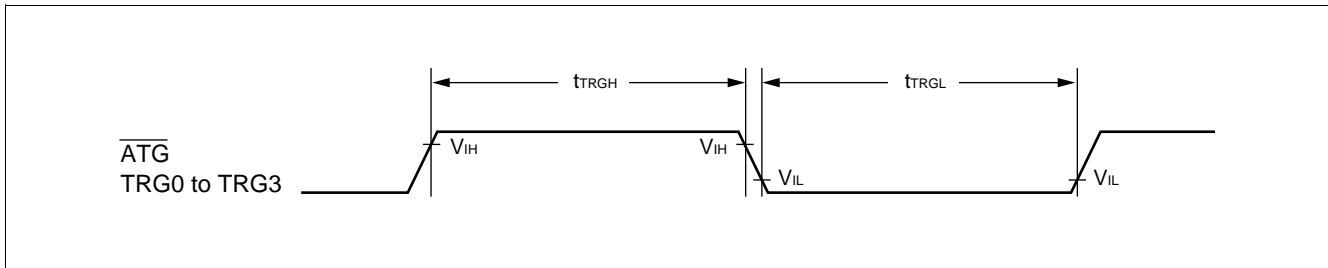
# MB91101/MB91101A

## (15) Trigger System Input Timing

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
A/D start trigger input time	$t_{TRGH}$ , $t_{TRGL}$	$\overline{ATG}$	—	$5 \times t_{CYCP}$	—	ns	
PWM external trigger input time	$t_{TRGH}$ , $t_{TRGL}$	TRG0 to TRG3		$5 \times t_{CYCP}$	—	ns	

$t_{CYCP}$ : A cycle time of peripheral system clock

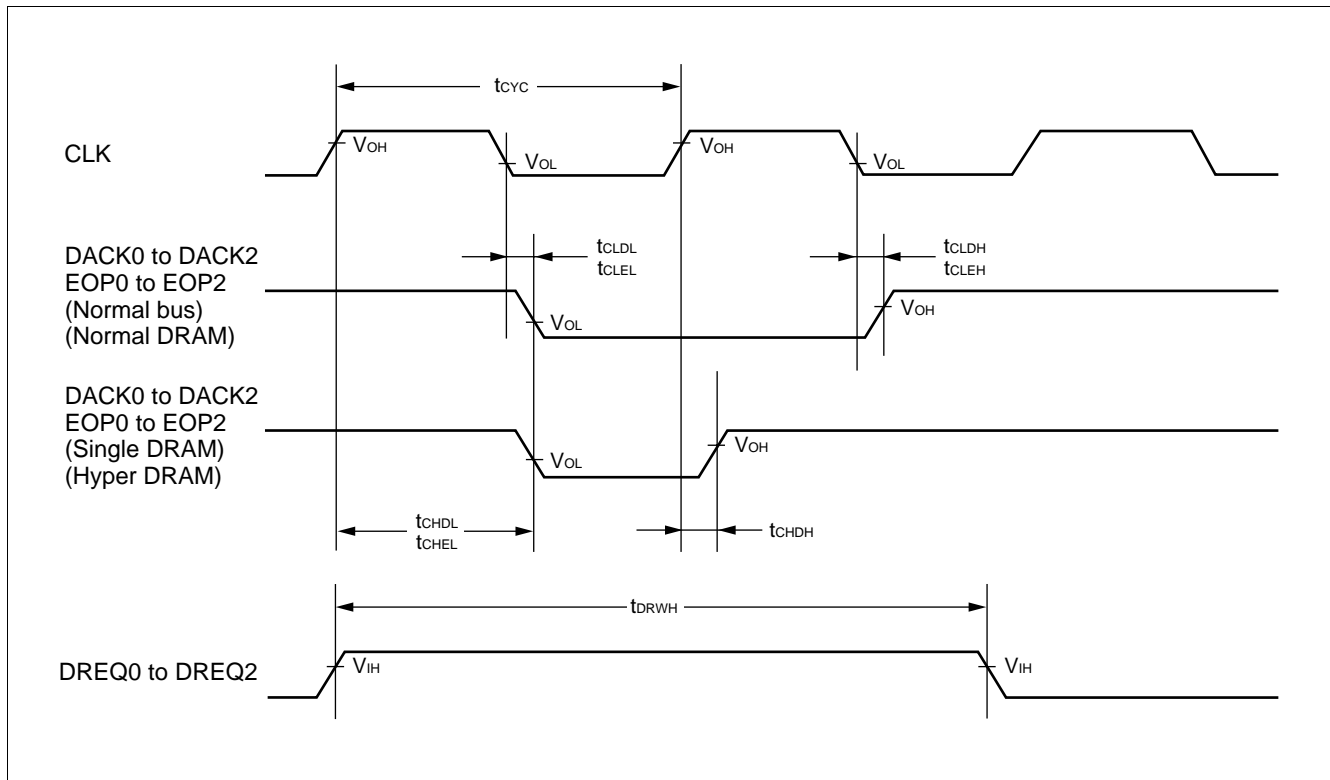


## (16) DMA Controller Timing

( $V_{CC5} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
 ( $V_{CC5} = V_{CC3} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
DREQ input pulse width	$t_{DRWH}$	DREQ0 to DREQ2	—	$2 \times t_{CYC}$	—	ns	
DACK delay time (Normal bus) (Normal DRAM)	$t_{CLDL}$	CLK, DACK0 to DACK2		—	6	ns	
	$t_{CLDH}$	CLK, DACK0 to DACK2		—	6	ns	
EOP delay time (Normal bus) (Normal DRAM)	$t_{CLEL}$	CLK, EOP0 to EOP2		—	6	ns	
	$t_{CLEH}$	CLK, EOP0 to EOP2		—	6	ns	
DACK delay time (Single DRAM) (Hyper DRAM)	$t_{CHDL}$	CLK, DACK0 to DACK2		—	$n/2 \times t_{CYC}$	ns	
	$t_{CHDH}$	CLK, DACK0 to DACK2		—	6	ns	
EOP delay time (Single DRAM) (Hyper DRAM)	$t_{CHEL}$	CLK, EOP0 to EOP2		—	$n/2 \times t_{CYC}$	ns	
	$t_{CHEH}$	CLK, EOP0 to EOP2		—	6	ns	

$t_{CYC}$  (a cycle time of peripheral system clock): Refer to “(2) Clock Output Timing.”



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## 5. A/D Converter Block Electrical Characteristics

( $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,  $AV_{SS} = 0.0\text{ V}$ ,  $AVRH = 2.7\text{ V}$ ,  $T_A = -40^\circ\text{C to }+70^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Resolution	—	—	—	10	10	bit
Total error	—	—	—	—	$\pm 4.0$	LSB
Linearity error	—	—	—	—	$\pm 3.5$	LSB
Differentiation linearity error	—	—	—	—	$\pm 2.0$	LSB
Zero transition voltage	$V_{OT}$	AN0 to AN3	-1.5	+0.5	+2.5	LSB
Full-scale transition voltage	$V_{FST}$	AN0 to AN3	$AVRH - 4.5$	$AVRH - 1.5$	$AVRH + 0.5$	LSB
Conversion time	—	—	5.6 *1	—	—	$\mu\text{s}$
Analog port input current	$I_{AIN}$	AN0 to AN3	—	0.1	10	$\mu\text{A}$
Analog input voltage	$V_{AIN}$	AN0 to AN3	$AV_{SS}$	—	$AVRH$	V
Reference voltage	—	$AVRH$	$AV_{SS}$	—	$AV_{CC}$	V
Power supply current	$I_A$	$AV_{CC}$	—	4	—	mA
	$I_{AH}$	$AV_{CC}$	—	—	5 *2	$\mu\text{A}$
Reference voltage supply current	$I_R$	$AVRH$	—	200	—	$\mu\text{A}$
	$I_{RH}$	$AVRH$	—	—	5 *2	$\mu\text{A}$
Conversion variance between channels	—	AN0 to AN3	—	—	4	LSB

\*1:  $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$

\*2 Current value for A/D converters not in operation, CPU stop mode ( $V_{CC} = AV_{CC} = AVRH = 3.6\text{ V}$ )

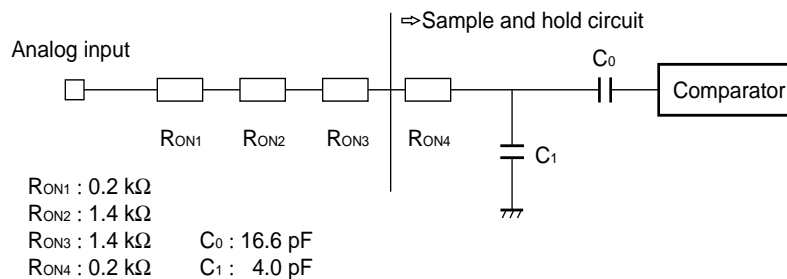
Notes: • As the absolute value of  $AVRH$  decreases, relative error increases.

• Output impedance of external circuit of analog input under following conditions;

Output impedance of external circuit < 10 k $\Omega$ .

If output impedance of external circuit is too high, analog voltage sampling time may be too short for accurate sampling (sampling time is 5.6  $\mu\text{s}$  for a machine clock of 25 MHz).

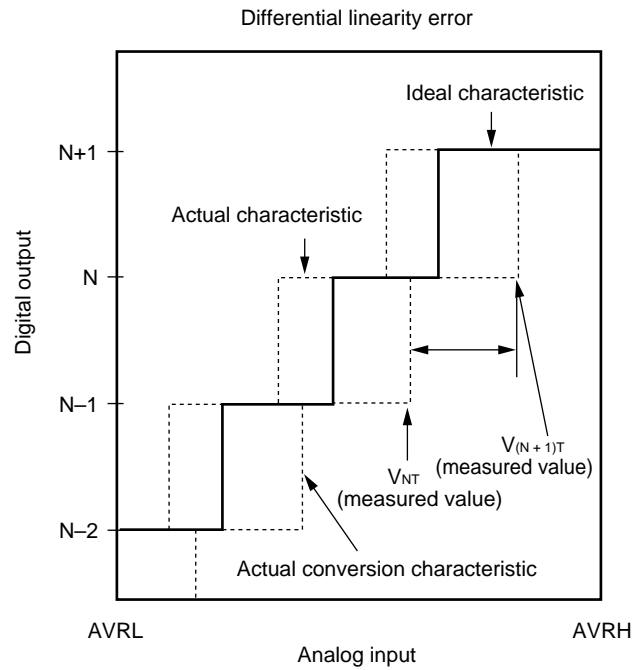
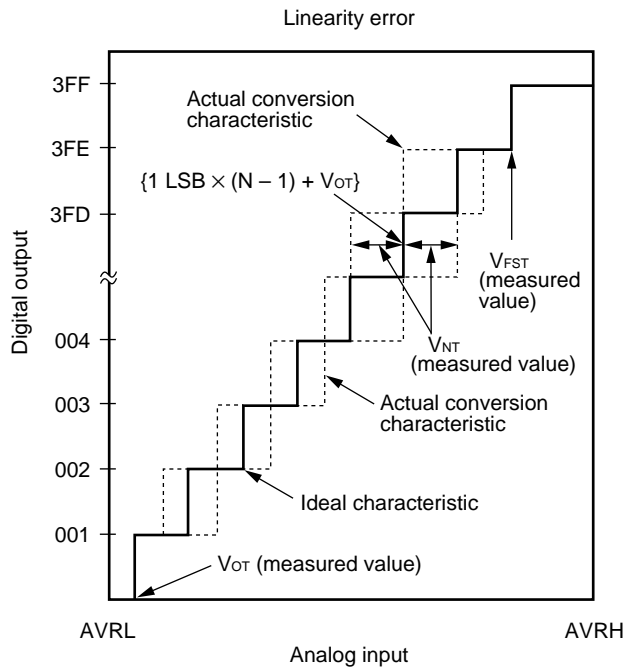
### • Analog input circuit



Note: Listed values are for reference purposes only.

## 6. A/D Converter Glossary

- Resolution  
The smallest change in analog voltage detected by A/D converter.
- Linearity error  
A deviation of actual conversion characteristic from a line connecting the zero-traction point (between “00 0000 0000” ↔ “00 0000 0001”) to the full-scale transition point (between “11 1111 1110” ↔ “11 1111 1111”).
- Differential linearity error  
A deviation of a step voltage for changing the LSB of output code from ideal input voltage.



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

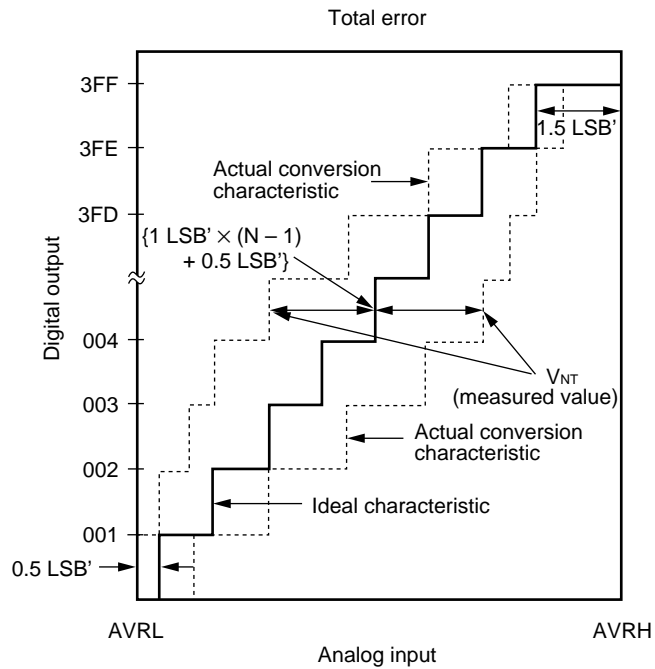
$V_{OT}$ : A voltage for causing transition of digital output from (000)<sub>H</sub> to (001)<sub>H</sub>

$V_{FST}$ : A voltage for causing transition of digital output from (3FE)<sub>H</sub> to (3FF)<sub>H</sub>

$V_{NT}$ : A voltage for causing transition of digital output from (N - 1) to N

- Total error

A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.



$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'} \quad [\text{LSB}]$$

$$1 \text{ LSB}' \text{ (ideal value)} = \frac{AVRH - AVRL}{1024} \quad [\text{V}]$$

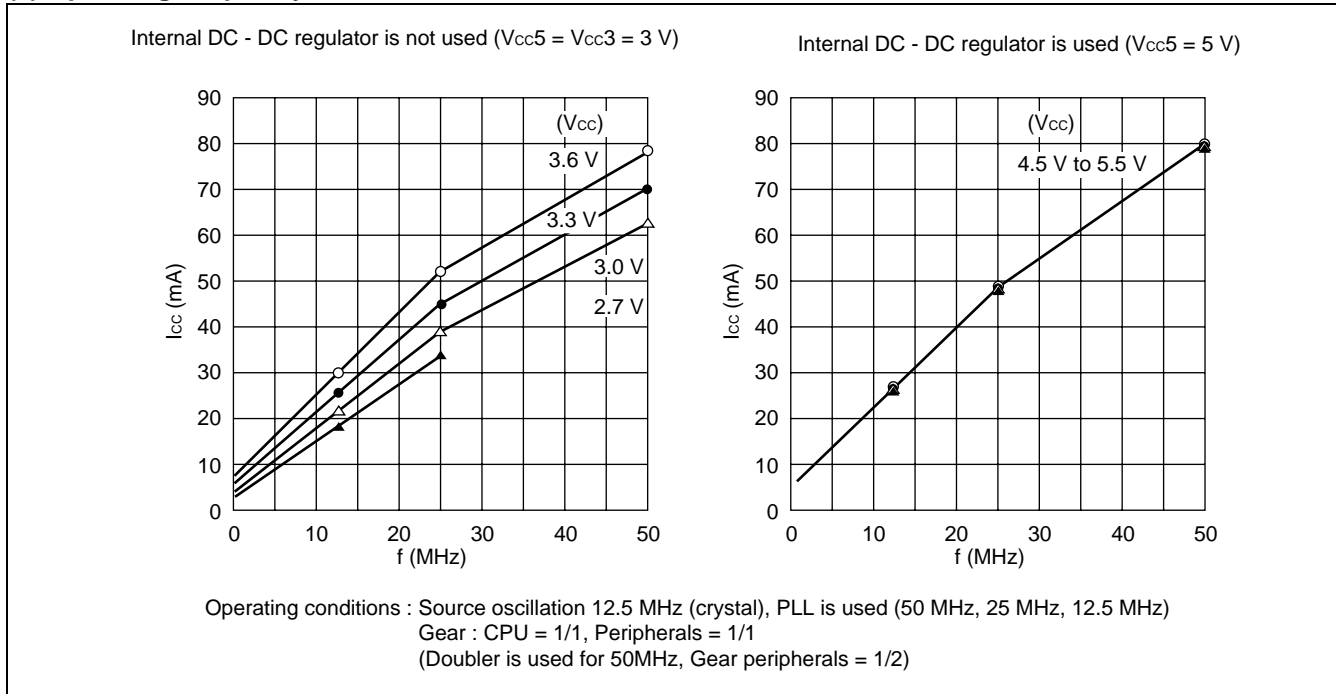
$$V_{OT}' \text{ (ideal value)} = AVRL + 0.5 \text{ LSB}' \quad [\text{V}]$$

$$V_{FST}' \text{ (ideal value)} = AVRH - 1.5 \text{ LSB}' \quad [\text{V}]$$

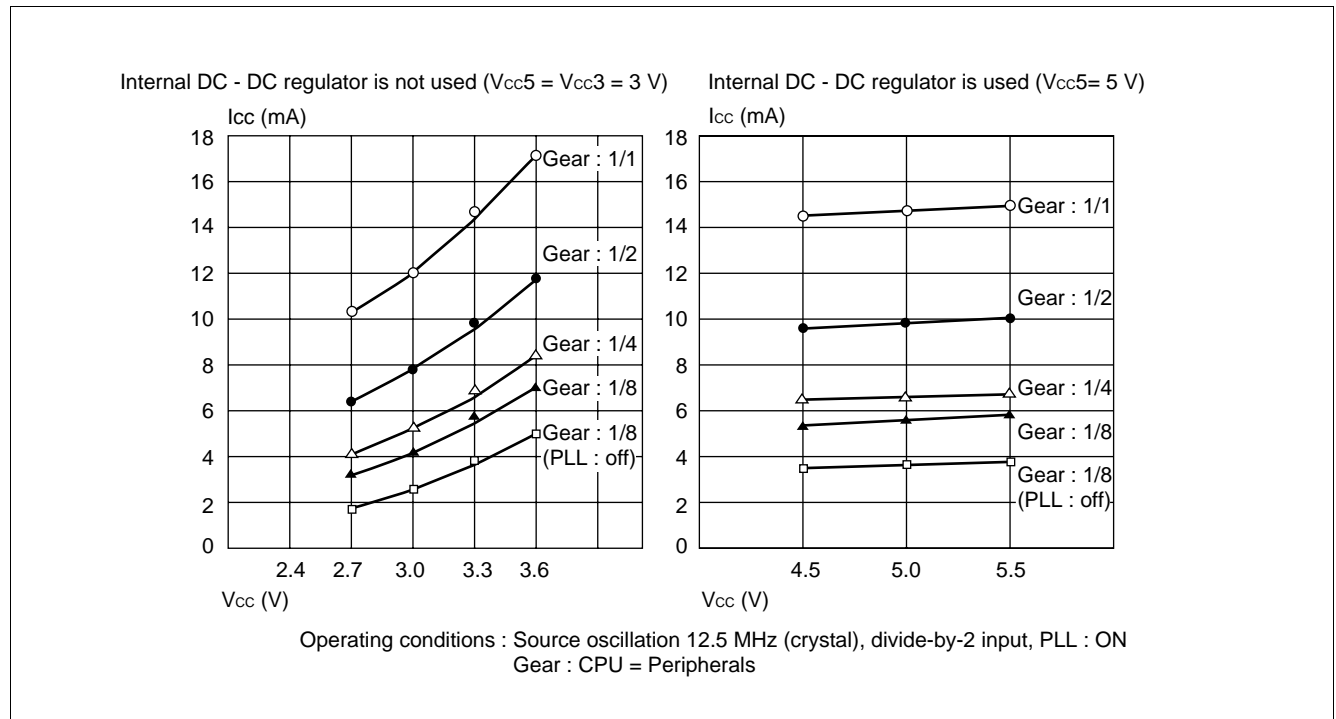
$V_{NT}$ : A voltage for causing transition of digital output from  $(N - 1)$  to  $N$

## REFERENCE DATA

### (1) Operating frequency vs. I<sub>cc</sub> characteristics



### (2) V<sub>cc</sub> vs. I<sub>cc</sub> characteristics



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## ■ ORDERING INFORMATION

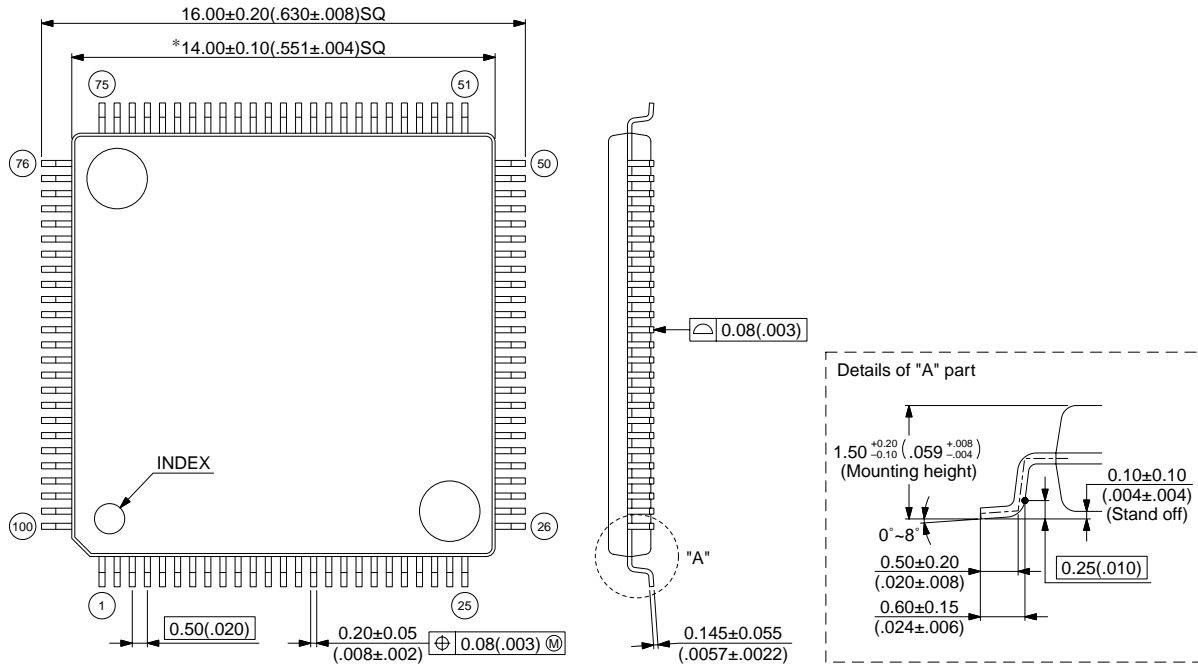
Part number	Package	Remarks
MB91101APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB91101APF	100-pin Plastic QFP (FPT-100P-M06)	



## PACKAGE DIMENSIONS

100-pin Plastic LQFP  
(FPT-100P-M05)

Note 1) \* : These dimensions do not include resin protrusion.  
 Note 2) Pins width and pins thickness include plating thickness.  
 Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches)

Note : The values in parentheses are reference values.

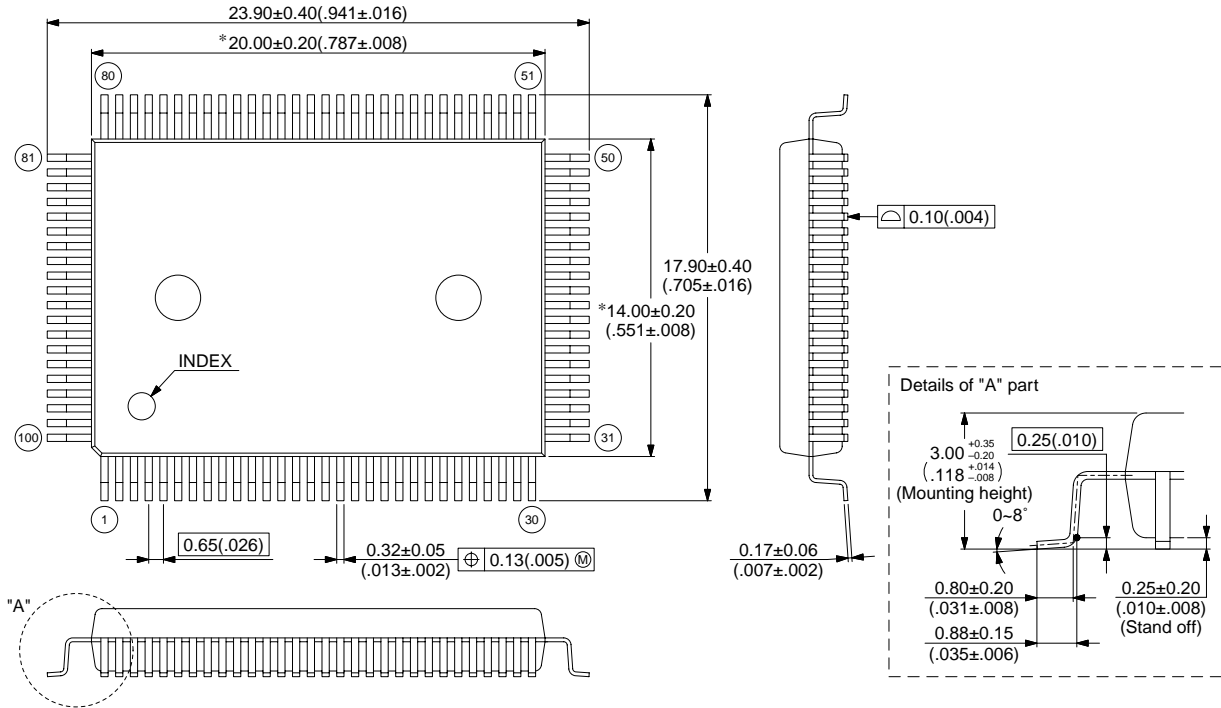
(Continued)

# MB91101/MB91101A

(Continued)

100-pin Plastic QFP  
(FPT-100P-M06)

Note 1) \* : These dimensions do not include resin protrusion.  
 Note 2) Pins width and pins thickness include plating thickness.  
 Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches)

Note : The values in parentheses are reference values.

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