MX29LV640T/B

64M-BIT [8M x 8/4M x 16] SINGLE VOLTAGE 3V ONLY FLASH MEMORY

FEATURES

GENERAL FEATURES

- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- 8,388,608 x 8 / 4,194,304 x 16 switchable
- Sector structure
  - 8KB (4KW) x 8 and 64KB(32KW) x 127
- Sector Protection/Chip Unprotect
  - Provides sector group protect function to prevent program or erase operation in the protected sector group
  - Provides chip unprotect function to allow code changes
  - Provides temporary sector group unprotect function for code changes in previously protected sector groups
- Secured Silicon Sector
  - Provides a 128-word area for code or data that can be permanently protected.
  - Once this sector is protected, it is prohibited to program or erase within the sector again.
- Latch-up protected to 250mA from -1V to Vcc + 1V
- Low Vcc write inhibit is equal to or less than 1.5V
- Compatible with JEDEC standard
  - Pin-out and software compatible to single power supply Flash

PERFORMANCE

- High Performance
  - Fast access time: 90/120ns
  - Fast program time: 11us/word, 45s/chip (typical)
  - Fast erase time: 0.9s/sector, 45s/chip (typical)
- Low Power Consumption
  - Low active read current: 10mA (typical) at 5MHz
  - Low standby current: 0.2uA (typ.)
- Minimum 100,000 erase/program cycle
- 20-year data retention

SOFTWARE FEATURES

- Support Common Flash Interface (CFI)
  - Flash device parameters stored on the device and provide the host system to access.
- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data polling & Toggle bits provide detection of program and erase operation completion

HARDWARE FEATURES

- Ready/Busy (RY/$\overline{BY}$) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset ($\overline{RESET}$) Input
  - Provides a hardware method to reset the internal state machine to read mode
- $\overline{WP}$ Pin
  - Write protect ($\overline{WP}$) function allows protection of two outermost boot sectors, regardless of sector protect status

PACKAGE

- 48-pin TSOP
- 63-ball CSP
- 64-ball Easy BGA

GENERAL DESCRIPTION

The MX29LV640T/B is a 64-mega bit Flash memory organized as 8M bytes of 8 bits or 4M bytes of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV640T/B is packaged in 48-pin TSOP, 63-ball CSP and 64-ball Easy BGA. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29LV640T/B offers access time as fast as 90ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV640T/B has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The

MX29LV640T/B uses a command register to manage this functionality.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29LV640T/B uses a 2.7V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamperes on address and data pin from -1V to VCC + 1V.

AUTOMATIC PROGRAMMING

The MX29LV640T/B is byte/word programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX29LV640T/B is less than 50 seconds.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm require the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to $\overline{\text{DATA}}$ polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 50 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 115 seconds. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX29LV640T/B is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

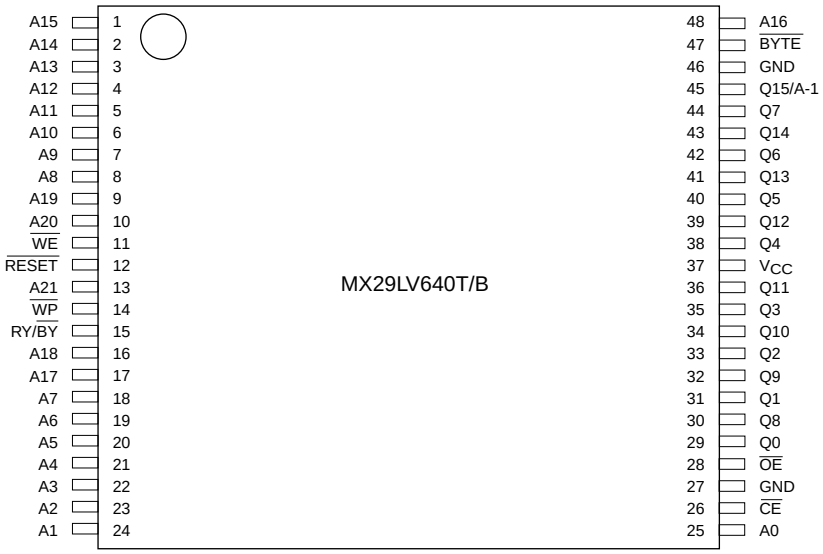
Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of $\overline{\text{WE}}$.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29LV640T/B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

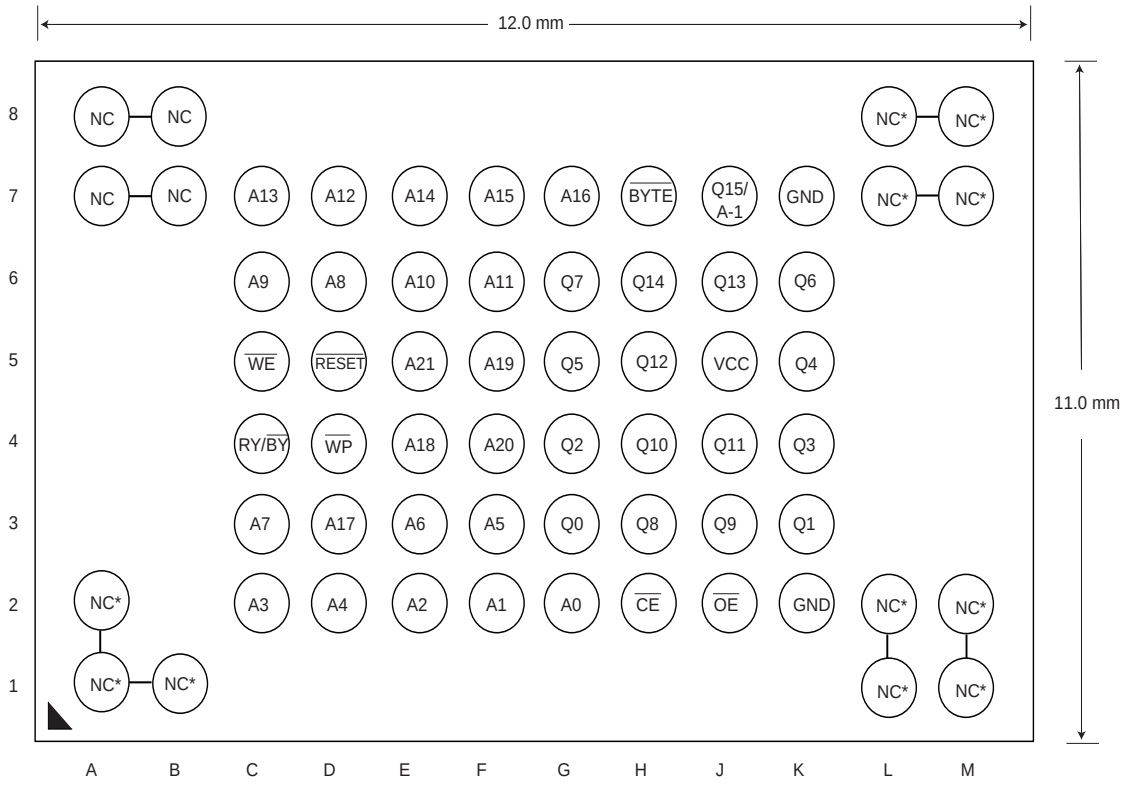
During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

PIN CONFIGURATION

48 TSOP

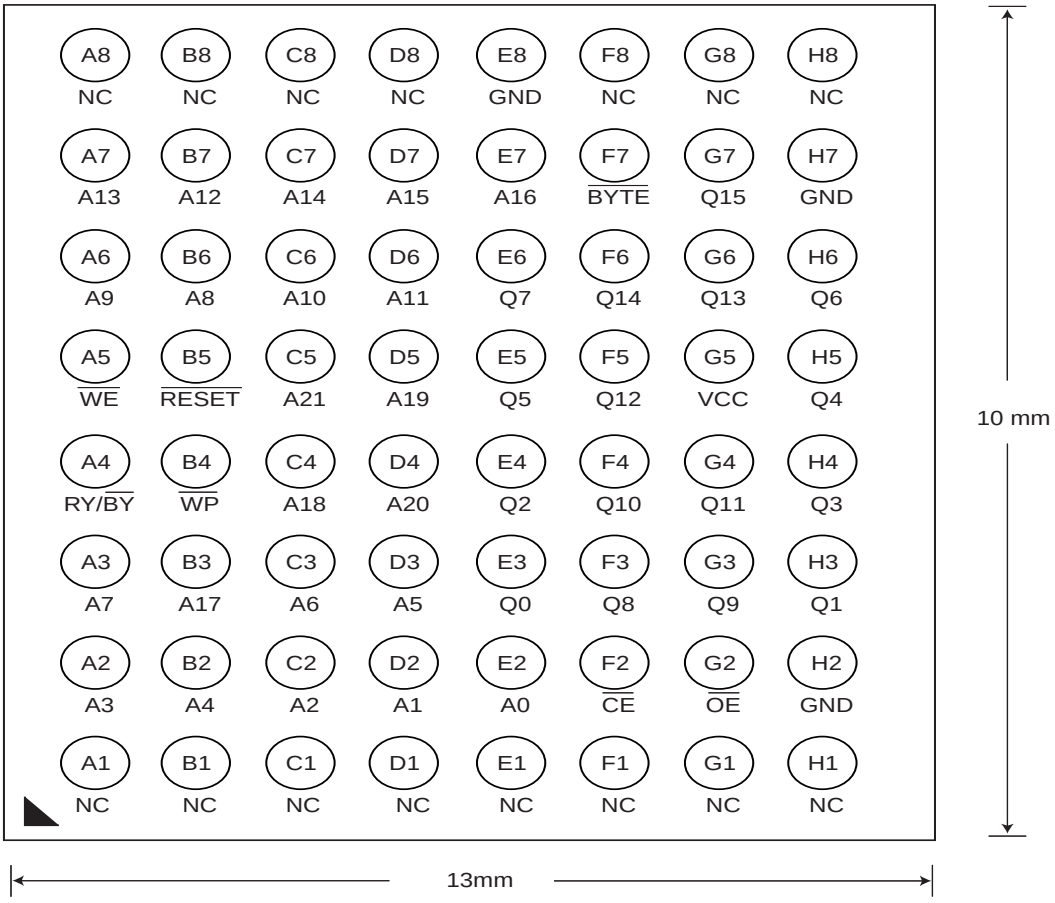


63 Ball CSP (Top View, Ball Down)



* Ball are shorted together via the substrate but not connected to the die.

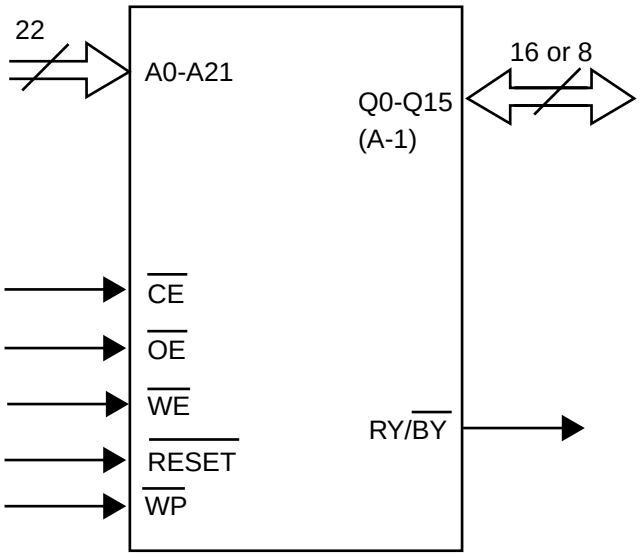
64 Ball Easy BGA (Top View, Ball Down)



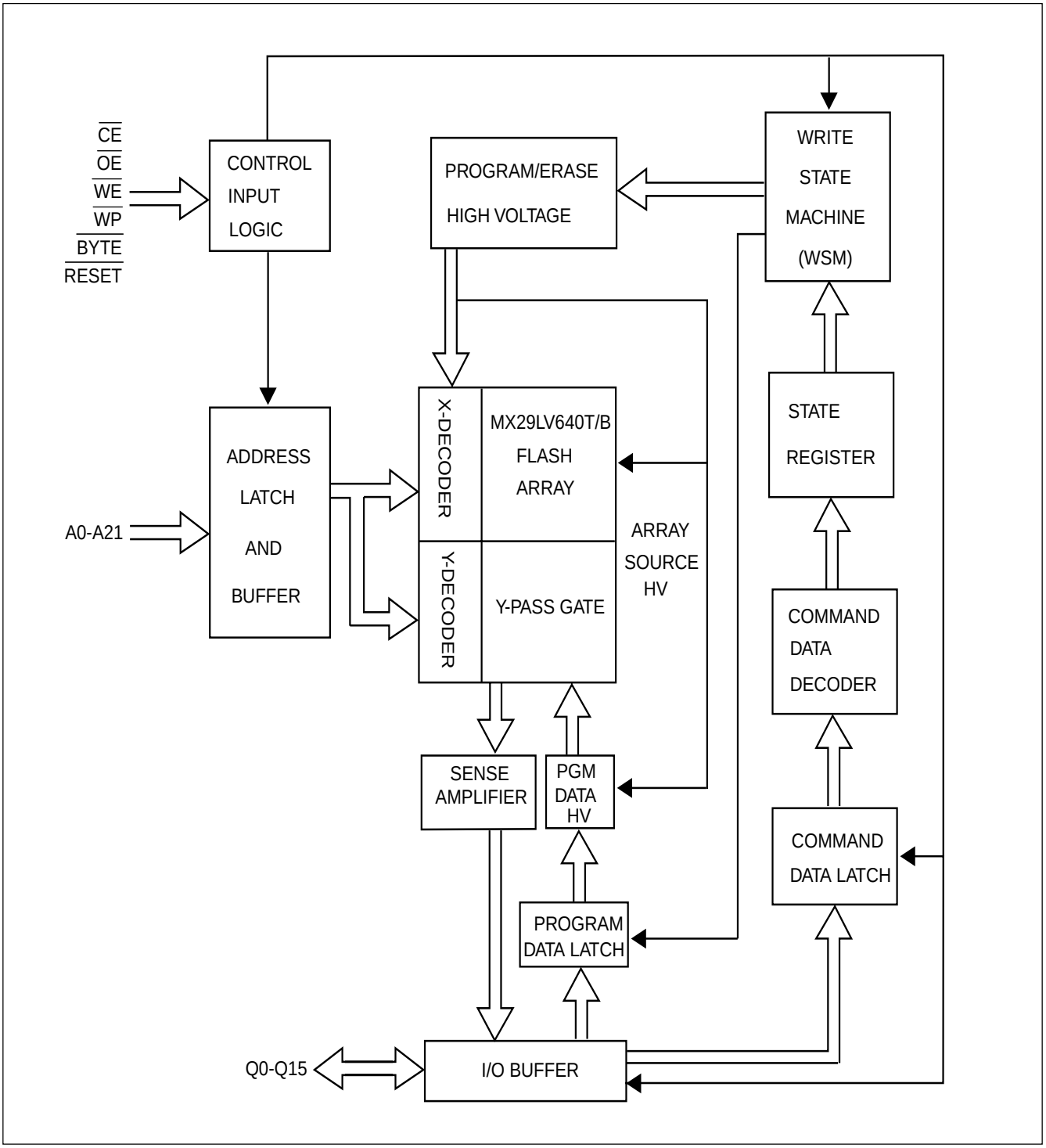
PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A21	Address Input
Q0~Q14	Data Inputs/Outputs
Q15/A-1	Q15(Word Mode)/LSB addr(Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{RESET}$	Hardware Reset Pin, Active Low
$\overline{WP}$	Hardware Write Protect
RY/$\overline{BY}$	Read/Busy Output
VCC	+3.0V single power supply
GND	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



BLOCK DIAGRAM



MX29LV640T SECTOR GROUP ARCHITECTURE

Sector Group	Sector	Sector Address A21-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
1	SA0	0000000xxx	64/32	000000h-00FFFFh	000000h-07FFFh
1	SA1	0000001xxx	64/32	010000h-01FFFFh	008000h-0FFFFh
1	SA2	0000010xxx	64/32	020000h-02FFFFh	010000h-17FFFh
1	SA3	0000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
2	SA4	0000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
2	SA5	0000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
2	SA6	0000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
2	SA7	0000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
3	SA8	0001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
3	SA9	0001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
3	SA10	0001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
3	SA11	0001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
4	SA12	0001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
4	SA13	0001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
4	SA14	0001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
4	SA15	0001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
5	SA16	0010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
5	SA17	0010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
5	SA18	0010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
5	SA19	0010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
6	SA20	0010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
6	SA21	0010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
6	SA22	0010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
6	SA23	0010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
7	SA24	0011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
7	SA25	0011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
7	SA26	0011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
7	SA27	0011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
8	SA28	0011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
8	SA29	0011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
8	SA30	0011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
8	SA31	0011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh
9	SA32	0100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
9	SA33	0100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
9	SA34	0100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
9	SA35	0100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
10	SA36	0100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
10	SA37	0100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
10	SA38	0100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
10	SA39	0100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh

Sector Group	Sector	Sector Address A21-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
11	SA40	0101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
11	SA41	0101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
11	SA42	0101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
11	SA43	0101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
12	SA44	0101100xxx	64/32	2C0000h-2CFFFFh	160000h-147FFFh
12	SA45	0101101xxx	64/32	2D0000h-2DFFFFh	168000h-14FFFFh
12	SA46	0101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
12	SA47	0101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
13	SA48	0110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
13	SA49	0110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
13	SA50	0110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
13	SA51	0110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
14	SA52	0110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
14	SA53	0110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
14	SA54	0110110xxx	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
14	SA55	0110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
15	SA56	0111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
15	SA57	0111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
15	SA58	0111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
15	SA59	0111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
16	SA60	0111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
16	SA61	0111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
16	SA62	0111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
16	SA63	0111111xxx	64/32	3F0000h-3FFFFFh	1F8000h-1FFFFFh
17	SA64	1000000xxx	64/32	400000h-40FFFFh	200000h-207FFFh
17	SA65	1000001xxx	64/32	410000h-41FFFFh	208000h-20FFFFh
17	SA66	1000010xxx	64/32	420000h-42FFFFh	210000h-217FFFh
17	SA67	1000011xxx	64/32	430000h-43FFFFh	218000h-21FFFFh
18	SA68	1000100xxx	64/32	440000h-44FFFFh	220000h-227FFFh
18	SA69	1000101xxx	64/32	450000h-45FFFFh	228000h-22FFFFh
18	SA70	1000110xxx	64/32	460000h-46FFFFh	230000h-237FFFh
18	SA71	1000111xxx	64/32	470000h-47FFFFh	238000h-23FFFFh
19	SA72	1001000xxx	64/32	480000h-48FFFFh	240000h-247FFFh
19	SA73	1001001xxx	64/32	490000h-49FFFFh	248000h-24FFFFh
19	SA74	1001010xxx	64/32	4A0000h-4AFFFFh	250000h-257FFFh
19	SA75	1001011xxx	64/32	4B0000h-4BFFFFh	258000h-25FFFFh
20	SA76	1001100xxx	64/32	4C0000h-4CFFFFh	260000h-247FFFh
20	SA77	1001101xxx	64/32	4D0000h-4DFFFFh	268000h-24FFFFh
20	SA78	1001110xxx	64/32	4E0000h-4EFFFFh	270000h-277FFFh
20	SA79	1001111xxx	64/32	4F0000h-4FFFFFh	278000h-27FFFFh

Sector Group	Sector	Sector Address A21-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
21	SA80	1010000xxx	64/32	500000h-50FFFFh	280000h-287FFFh
21	SA81	1010001xxx	64/32	510000h-51FFFFh	288000h-28FFFFh
21	SA82	1010010xxx	64/32	520000h-52FFFFh	290000h-297FFFh
21	SA83	1010011xxx	64/32	530000h-53FFFFh	298000h-29FFFFh
22	SA84	1010100xxx	64/32	540000h-54FFFFh	2A0000h-2A7FFFh
22	SA85	1010101xxx	64/32	550000h-55FFFFh	2A8000h-2AFFFFh
22	SA86	1010110xxx	64/32	560000h-56FFFFh	2B0000h-2B7FFFh
22	SA87	1010111xxx	64/32	570000h-57FFFFh	2B8000h-2BFFFFh
23	SA88	1011000xxx	64/32	580000h-58FFFFh	2C0000h-2C7FFFh
23	SA89	1011001xxx	64/32	590000h-59FFFFh	2C8000h-2CFFFFh
23	SA90	1011010xxx	64/32	5A0000h-5AFFFFh	2D0000h-2D7FFFh
23	SA91	1011011xxx	64/32	5B0000h-5BFFFFh	2D8000h-2DFFFFh
24	SA92	1011100xxx	64/32	5C0000h-5CFFFFh	2E0000h-2E7FFFh
24	SA93	1011101xxx	64/32	5D0000h-5DFFFFh	2E8000h-2EFFFFh
24	SA94	1011110xxx	64/32	5E0000h-5EFFFFh	2F0000h-2F7FFFh
24	SA95	1011111xxx	64/32	5F0000h-5FFFFFh	2F8000h-2FFFFFh
25	SA96	1100000xxx	64/32	600000h-60FFFFh	300000h-307FFFh
25	SA97	1100001xxx	64/32	610000h-61FFFFh	308000h-30FFFFh
25	SA98	1100010xxx	64/32	620000h-62FFFFh	310000h-317FFFh
25	SA99	1100011xxx	64/32	630000h-63FFFFh	318000h-31FFFFh
26	SA100	1100100xxx	64/32	640000h-64FFFFh	320000h-327FFFh
26	SA101	1100101xxx	64/32	650000h-65FFFFh	328000h-32FFFFh
26	SA102	1100110xxx	64/32	660000h-66FFFFh	330000h-337FFFh
26	SA103	1100111xxx	64/32	670000h-67FFFFh	338000h-33FFFFh
27	SA104	1101000xxx	64/32	680000h-68FFFFh	340000h-347FFFh
27	SA105	1101001xxx	64/32	690000h-69FFFFh	348000h-34FFFFh
27	SA106	1101010xxx	64/32	6A0000h-6AFFFFh	350000h-357FFFh
27	SA107	1101011xxx	64/32	6B0000h-6BFFFFh	358000h-35FFFFh
28	SA108	1101100xxx	64/32	6C0000h-6CFFFFh	360000h-347FFFh
28	SA109	1101101xxx	64/32	6D0000h-6DFFFFh	368000h-34FFFFh
28	SA110	1101110xxx	64/32	6E0000h-6EFFFFh	370000h-377FFFh
28	SA111	1101111xxx	64/32	6F0000h-6FFFFFh	378000h-37FFFFh
29	SA112	1110000xxx	64/32	700000h-70FFFFh	380000h-387FFFh
29	SA113	1110001xxx	64/32	710000h-71FFFFh	388000h-38FFFFh
29	SA114	1110010xxx	64/32	720000h-72FFFFh	390000h-397FFFh
29	SA115	1110011xxx	64/32	730000h-73FFFFh	398000h-39FFFFh
30	SA116	1110100xxx	64/32	740000h-74FFFFh	3A0000h-3A7FFFh
30	SA117	1110101xxx	64/32	750000h-75FFFFh	3A8000h-3AFFFFh
30	SA118	1110110xxx	64/32	760000h-76FFFFh	3B0000h-3B7FFFh
30	SA119	1110111xxx	64/32	770000h-77FFFFh	3B8000h-3BFFFFh

Sector Group	Sector	Sector Address A21-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
31	SA120	1111000xxx	64/32	780000h-78FFFFh	3C0000h-3C7FFFh
31	SA121	1111001xxx	64/32	790000h-79FFFFh	3C8000h-3CFFFFh
31	SA122	1111010xxx	64/32	7A0000h-7AFFFFh	3D0000h-3D7FFFh
31	SA123	1111011xxx	64/32	7B0000h-7BFFFFh	3D8000h-3DFFFFh
32	SA124	1111100xxx	64/32	7C0000h-7CFFFFh	3E0000h-3E7FFFh
32	SA125	1111101xxx	64/32	7D0000h-7DFFFFh	3E8000h-3EFFFFh
32	SA126	1111110xxx	64/32	7E0000h-7EFFFFh	3F0000h-3F7FFFh
33	SA127	1111111000	8/4	7F0000h-7F1FFFh	3F8000h-3FFFFFh
34	SA128	1111111001	8/4	7F2000h-7F3FFFh	3F9000h-3F9FFFh
35	SA129	1111111010	8/4	7F4000h-7F5FFFh	3FA000h-3FAFFFh
36	SA130	1111111011	8/4	7F6000h-7F7FFFh	3FB000h-3FBFFFh
37	SA131	1111111100	8/4	7F8000h-7F9FFFh	3FC000h-3FCFFFh
38	SA132	1111111101	8/4	7FA000h-7FBFFFh	3FD000h-3FDFFFh
39	SA133	1111111110	8/4	7FC000h-7FDFFFh	3FE000h-3FEFFFh
40	SA134	1111111111	8/4	7FE000h-7FFFFFh	3FF000h-3FFFFFh

Note:The address range is A21:A-1 in byte mode ($\overline{BYTE}$=VIL) or A20:A0 in word mode ($\overline{BYTE}$=VIH)

Top Boot Security Sector Addresses

Sector Address A21~A12	Sector Size (bytes/words)	(x8) Address Range	(x16) Address Range
1111111111	256/128	7FFF00h-7FFFFFh	3FFF70h-3FFFFFh

MX29LV640B SECTOR GROUP ARCHITECTURE

Sector Group	Sector	Sector Address A21-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
1	SA0	0000000000	8/4	000000h-001FFFh	000000h-000FFFh
2	SA1	0000000001	8/4	002000h-003FFFh	001000h-001FFFh
3	SA2	0000000010	8/4	004000h-005FFFh	002000h-002FFFh
4	SA3	0000000011	8/4	006000h-007FFFh	003000h-003FFFh
5	SA4	0000000100	8/4	008000h-009FFFh	004000h-004FFFh
6	SA5	0000000101	8/4	00A000h-00BFFFh	005000h-005FFFh
7	SA6	0000000110	8/4	00C000h-00DFFFh	006000h-006FFFh
8	SA7	0000000111	8/4	00E000h-00FFFFh	007000h-007FFFh
9	SA8	0000001xxx	64/32	010000h-01FFFFh	008000h-00FFFFh
9	SA9	0000010xxx	64/32	020000h-02FFFFh	010000h-017FFFh
9	SA10	0000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
10	SA11	0000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
10	SA12	0000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
10	SA13	0000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
10	SA14	0000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
11	SA15	0001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
11	SA16	0001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
11	SA17	0001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
11	SA18	0001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
12	SA19	0001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
12	SA20	0001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
12	SA21	0001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
12	SA22	0001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
13	SA23	0010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
13	SA24	0010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
13	SA25	0010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
13	SA26	0010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
14	SA27	0010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
14	SA28	0010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
14	SA29	0010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
14	SA30	0010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
15	SA31	0011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
15	SA32	0011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
15	SA33	0011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
15	SA34	0011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
16	SA35	0011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
16	SA36	0011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
16	SA37	0011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
16	SA38	0011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh

Sector Group	Sector	Sector Address A21-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
17	SA39	0100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
17	SA40	0100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
17	SA41	0100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
17	SA42	0100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
18	SA43	0100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
18	SA44	0100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
18	SA45	0100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
18	SA46	0100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh
19	SA47	0101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
19	SA48	0101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
19	SA49	0101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
19	SA50	0101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
20	SA51	0101100xxx	64/32	2C0000h-2CFFFFh	160000h-167FFFh
20	SA52	0101101xxx	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
20	SA53	0101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
20	SA54	0101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
21	SA55	0110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
21	SA56	0110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
21	SA57	0110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
21	SA58	0110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
22	SA59	0110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
22	SA60	0110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
22	SA61	0110110xxx	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
22	SA62	0110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
23	SA63	0111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
23	SA64	0111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
23	SA65	0111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
23	SA66	0111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
24	SA67	0111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
24	SA68	0111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
24	SA69	0111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
24	SA70	0111111xxx	64/32	3F0000h-3FFFFFh	1F8000h-1FFFFFh
25	SA71	1000000xxx	64/32	400000h-40FFFFh	200000h-207FFFh
25	SA72	1000001xxx	64/32	410000h-41FFFFh	208000h-20FFFFh
25	SA73	1000010xxx	64/32	420000h-42FFFFh	210000h-217FFFh
25	SA74	1000011xxx	64/32	430000h-43FFFFh	218000h-21FFFFh
26	SA75	1000100xxx	64/32	440000h-44FFFFh	220000h-227FFFh
26	SA76	1000101xxx	64/32	450000h-45FFFFh	228000h-22FFFFh
26	SA77	1000110xxx	64/32	460000h-46FFFFh	230000h-237FFFh
26	SA78	1000111xxx	64/32	470000h-47FFFFh	238000h-23FFFFh

Sector Group	Sector	Sector Address A21-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
27	SA79	1001000xxx	64/32	480000h-48FFFFh	240000h-247FFFh
27	SA80	1001001xxx	64/32	490000h-49FFFFh	248000h-24FFFFh
27	SA81	1001010xxx	64/32	4A0000h-4AFFFFh	250000h-257FFFh
27	SA82	1001011xxx	64/32	4B0000h-4BFFFFh	258000h-25FFFFh
28	SA83	1001100xxx	64/32	4C0000h-4CFFFFh	260000h-267FFFh
28	SA84	1001101xxx	64/32	4D0000h-4DFFFFh	268000h-26FFFFh
28	SA85	1001110xxx	64/32	4E0000h-4EFFFFh	270000h-277FFFh
28	SA86	1001111xxx	64/32	4F0000h-4FFFFFh	278000h-27FFFFh
29	SA87	1010000xxx	64/32	500000h-50FFFFh	280000h-287FFFh
29	SA88	1010001xxx	64/32	510000h-51FFFFh	288000h-28FFFFh
29	SA89	1010010xxx	64/32	520000h-52FFFFh	290000h-297FFFh
29	SA90	1010011xxx	64/32	530000h-53FFFFh	298000h-29FFFFh
30	SA91	1010100xxx	64/32	540000h-54FFFFh	2A0000h-2A7FFFh
30	SA92	1010101xxx	64/32	550000h-55FFFFh	2A8000h-2AFFFFh
30	SA93	1010110xxx	64/32	560000h-56FFFFh	2B0000h-2B7FFFh
30	SA94	1010111xxx	64/32	570000h-57FFFFh	2B8000h-2BFFFFh
31	SA95	1011000xxx	64/32	580000h-58FFFFh	2C0000h-2C7FFFh
31	SA96	1011001xxx	64/32	590000h-59FFFFh	2C8000h-2CFFFFh
31	SA97	1011010xxx	64/32	5A0000h-5AFFFFh	2D0000h-2D7FFFh
31	SA98	1011011xxx	64/32	5B0000h-5BFFFFh	2D8000h-2DFFFFh
32	SA99	1011100xxx	64/32	5C0000h-5CFFFFh	2E0000h-2E7FFFh
32	SA100	1011101xxx	64/32	5D0000h-5DFFFFh	2E8000h-2EFFFFh
32	SA101	1011110xxx	64/32	5E0000h-5EFFFFh	2F0000h-2F7FFFh
32	SA102	1011111xxx	64/32	5F0000h-5FFFFFh	2F8000h-2FFFFFh
33	SA103	1100000xxx	64/32	600000h-60FFFFh	300000h-307FFFh
33	SA104	1100001xxx	64/32	610000h-61FFFFh	308000h-30FFFFh
33	SA105	1100010xxx	64/32	620000h-62FFFFh	310000h-317FFFh
33	SA106	1100011xxx	64/32	630000h-63FFFFh	318000h-31FFFFh
34	SA107	1100100xxx	64/32	640000h-64FFFFh	320000h-327FFFh
34	SA108	1100101xxx	64/32	650000h-65FFFFh	328000h-32FFFFh
34	SA109	1100110xxx	64/32	660000h-66FFFFh	330000h-337FFFh
34	SA110	1100111xxx	64/32	670000h-67FFFFh	338000h-33FFFFh
35	SA111	1101000xxx	64/32	680000h-68FFFFh	340000h-347FFFh
35	SA112	1101001xxx	64/32	690000h-69FFFFh	348000h-34FFFFh
35	SA113	1101010xxx	64/32	6A0000h-6AFFFFh	350000h-357FFFh
35	SA114	1101011xxx	64/32	6B0000h-6BFFFFh	358000h-35FFFFh
36	SA115	1101100xxx	64/32	6C0000h-6CFFFFh	360000h-367FFFh
36	SA116	1101101xxx	64/32	6D0000h-6DFFFFh	368000h-36FFFFh
36	SA117	1101110xxx	64/32	6E0000h-6EFFFFh	370000h-377FFFh
36	SA118	1101111xxx	64/32	6F0000h-6FFFFFh	378000h-37FFFFh

Sector Group	Sector	Sector Address A21-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
37	SA119	1110000xxx	64/32	700000h-70FFFFh	380000h-387FFFh
37	SA120	1110001xxx	64/32	710000h-71FFFFh	388000h-38FFFFh
37	SA121	1110010xxx	64/32	720000h-72FFFFh	390000h-397FFFh
37	SA122	1110011xxx	64/32	730000h-73FFFFh	398000h-39FFFFh
38	SA123	1110100xxx	64/32	740000h-74FFFFh	3A0000h-3A7FFFh
38	SA124	1110101xxx	64/32	750000h-75FFFFh	3A8000h-3AFFFFh
38	SA125	1110110xxx	64/32	760000h-76FFFFh	3B0000h-3B7FFFh
38	SA126	1110111xxx	64/32	770000h-77FFFFh	3B8000h-3BFFFFh
39	SA127	1111000xxx	64/32	780000h-78FFFFh	3C0000h-3C7FFFh
39	SA128	1111001xxx	64/32	790000h-79FFFFh	3C8000h-3CFFFFh
39	SA129	1111010xxx	64/32	7A0000h-7AFFFFh	3D0000h-3D7FFFh
39	SA130	1111011xxx	64/32	7B0000h-7BFFFFh	3D8000h-3DFFFFh
40	SA131	1111100xxx	64/32	7C0000h-7CFFFFh	3E0000h-3E7FFFh
40	SA132	1111101xxx	64/32	7D0000h-7DFFFFh	3E8000h-3EFFFFh
40	SA133	1111110xxx	64/32	7E0000h-7EFFFFh	3F0000h-3F7FFFh
40	SA134	1111111xxx	64/32	7F0000h-7FFFFFh	3F8000h-3FFFFFh

Note:The address range is A20:A-1 in byte mode ($\overline{BYTE}$=VIL) or A20:A0 in word mode ($\overline{BYTE}$=VIH)

Bottom Boot Security Sector Addresses

Sector Address A21~A12	Sector Size (bytes/words)	(x8) Address Range	(x16) Address Range
0000000000	256/128	000000h-0000FFh	000000-00007Fh

Table 1

BUS OPERATION (1)

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	$\overline{WP}$	Address	Q15~Q0
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}
Write (Program/Erase)	L	H	L	H	(Note 2)	A_{IN}	D_{IN}
Standby	VCC±0.3V	X	X	VCC±0.3V	H	X	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z
Reset	X	X	X	L	L/H	X	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	L/H	Sector Addresses, A6=L, A1=H, A0=L	D_{IN}, D_{OUT}
Chip unprotect (Note 2)	L	H	L	V_{ID}	(Note 2)	Sector Addresses, A6=H, A1=H, A0=L	D_{IN}, D_{OUT}
Temporary Sector Group Unprotect	X	X	X	V_{ID}	(Note 2)	A_{IN}	D_{IN}

Legend:
L=Logic LOW=V_{IL}, H=Logic High=V_{IH}, V_{ID}=12.0±0.5V, X=Don't Care, A_{IN}=Address IN, D_{IN}=Data IN, D_{OUT}=Data OUT

Notes:
1. The sector group protect and chip unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Chip Unprotect" section.
2. If $\overline{WP}$=VIL, the two outermost boot sectors remain protected. If $\overline{WP}$=VIH, the two outermost boot sector protection depends on whether they were last protected or unprotect using the method described in "Sector/ Sector Block Protection and Unprotect".
3. D_{IN} or D_{OUT} as required by command sequence, $\overline{Data}$ polling or sector protect algorithm (see Figure 2).

AUTOSELECT CODES (High Voltage Method)

Operation		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A5 to A2	A6	A8 to A7	A9	A14 to A10	A15 to A21	Q0~Q15
Read Silicon ID	Manufactures Code	L	L	H	L	L	X	X	X	V_{ID}	X	X	XXC2H
	Device Code (Top Boot Block)	L	L	H	H	L	X	X	X	V_{ID}	X	X	22C9H (word) XXC9H (byte)
	Device Code (Bottom Boot Block)	L	L	H	H	L	X	X	X	V_{ID}	X	X	22CBH (word) XXCBH (byte)
Sector Protect Verify		L	L	H	X	H	X	X	X	V_{ID}	X	SA	Code(1)
Secured Silicon Sector Indicator Bit (Q7)		L	L	H	H	H	X	L	X	V_{ID}	X	X	xx88h (factory locked) xx08h (non-factory locked)

Notes:
1.code=xx00h means unprotected, or code=xx01h means protected, SA=Sector Address, X=Don't care.

REQUIREMENTS FOR READING ARRAY DATA

To read array data from the outputs, the system must drive the $\overline{CE}$ and $\overline{OE}$ pins to VIL. $\overline{CE}$ is the power control and selects the device. $\overline{OE}$ is the output control and gates array data to the output pins. $\overline{WE}$ should remain at VIH.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid address on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory , the system must drive $\overline{WE}$ and $\overline{CE}$ to VIL, and $\overline{OE}$ to VIH.

An erase operation can erase one sector, multiple sectors , or the entire device. Table indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Writing specific address and data commands or sequences into the command register initiates device operations. Table 1 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the Automatic Select command sequence, the device enters the Automatic Select mode. The system can then read Automatic Select codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Automatic Select Mode and Automatic Select Command Sequence section for more information.

ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

STANDBY MODE

MX29LV640T/B can be set into Standby mode with two different approaches. One is using both $\overline{CE}$ and $\overline{RESET}$ pins and the other one is using $\overline{RESET}$ pin only.

When using both pins of $\overline{CE}$ and $\overline{RESET}$, a CMOS Standby mode is achieved with both pins held at Vcc ± 0.3V. Under this condition, the current consumed is less than 0.2uA (typ.). If both of the $\overline{CE}$ and $\overline{RESET}$ are held at VIH, but not within the range of VCC ± 0.3V, the device will still be in the standby mode, but the standby current will be larger. During Auto Algorithm operation, Vcc active current (Icc2) is required even $\overline{CE}$ = "H" until the operation is completed. The device can be read with standard access time (tCE) from either of these standby modes.

When using only $\overline{RESET}$, a CMOS standby mode is achieved with $\overline{RESET}$ input held at Vss ± 0.3V, Under this condition the current is consumed less than 1uA (typ.). Once the $\overline{RESET}$ pin is taken high, the device is back to active without recovery delay.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

MX29LV640T/B is capable to provide the Automatic Standby Mode to restrain power consumption during readout of data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To active this mode, MX29LV640T/B automatically switch themselves to low power mode when MX29LV640T/B addresses remain stable during access time of tACC+30ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on the mode. Under the mode, the current consumed is typically 0.2uA (CMOS level).

AUTOMATIC SLEEP MODE

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when address remain stable for tACC+30ns. The automatic sleep mode is independent of the $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. ICC4 in the DC Characteristics table represents the automatic sleep mode current specification.

OUTPUT DISABLE

With the $\overline{OE}$ input at a logic high level (VIH), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

$\overline{RESET}$ OPERATION

The $\overline{RESET}$ pin provides a hardware method of resetting the device to reading array data. When the $\overline{RESET}$ pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity

Current is reduced for the duration of the $\overline{RESET}$ pulse. When $\overline{RESET}$ is held at VSS±0.3V, the device draws CMOS standby current (ICC4). If $\overline{RESET}$ is held at VIL but not within VSS±0.3V, the standby current will be greater.

The $\overline{RESET}$ pin may be tied to system reset circuitry. A system reset would that also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If $\overline{RESET}$ is asserted during a program or erase operation, the RY/$\overline{BY}$ pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of tREADY (during Embedded Algorithms). The system can thus monitor RY/$\overline{BY}$ to determine whether the reset operation is complete. If $\overline{RESET}$ is asserted when a program or erase operation is completed within a time of tREADY (not during Embedded Algorithms). The system can read data tRH after the $\overline{RESET}$ pin returns to VIH.

Refer to the AC Characteristics tables for $\overline{RESET}$ parameters and to Figure 14 for the timing diagram.

SECTOR GROUP PROTECT OPERATION

The MX29LV640T/B features hardware sector group protection. This feature will disable both program and erase operations for these sector group protected. In this device, a sector group consists of four adjacent sectors which are protected or unprotected at the same time. To activate this mode, the programming equipment must force VID on address pin A9 and control pin $\overline{OE}$, (suggest VID = 12V) A6 = VIL and $\overline{CE}$ = VIL. (see Table 2) Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated on the rising edge. Please refer to sector group protect algorithm and waveform.

MX29LV640T/B also provides another method. Which requires VID on the $\overline{RESET}$ only. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with $\overline{CE}$ and $\overline{OE}$ at VIL and $\overline{WE}$ at VIH). When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses, except for A1, are don't care. Address locations with A1 = VIL are reserved to read manufacturer and device codes. (Read Silicon ID)

It is also possible to determine if the group is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

CHIP UNPROTECT OPERATION

The MX29LV640T/B also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin $\overline{OE}$ and address pin A9. The $\overline{CE}$ pins must be set at VIL. Pins A6 must be set to VIH. (see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotect mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated on the rising edge.

MX29LV640T/B also provides another method. Which requires VID on the $\overline{RESET}$ only. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing.

It is also possible to determine if the chip is unprotect in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs (Q0-Q7) for an unprotect sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

WRITE PROTECT ($\overline{WP}$)

The write protect function provides a hardware method to protect boot sectors without using V_{ID}.

If the system asserts VIL on the $\overline{WP}$ pin, the device disables program and erase functions in the two "outermost" 8 Kbyte boot sectors independently of whether those sectors were protected or unprotect using the method described in Sector/Sector Group Protection and Chip Unprotect". The two outermost 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts VIH on the $\overline{WP}$ pin, the device reverts to whether the two outermost 8K Byte boot sectors were last set to be protected or unprotect. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotect using the method described in "Sector/Sector Group Protection and Chip Unprotect".

Note that the $\overline{WP}$ pin must not be left floating or unconnected; inconsistent behavior of the device may result.

TEMPORARY SECTOR GROUP UNPROTECT OPERATION

This feature allows temporary unprotect of previously protected sector to change data in-system. The Temporary Sector Unprotect mode is activated by setting the $\overline{RESET}$ pin to VID(11.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased as unprotect sector. Once VID is remove from the $\overline{RESET}$ pin, all the previously protected sectors are protected again.

SILICON ID READ OPERATION

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

MX29LV640T/B provides hardware method to access the silicon ID read operation. Which method requires VID on A9 pin, VIL on $\overline{CE}$, $\overline{OE}$, A6, and A1 pins. Which apply VIL on A0 pin, the device will output MXIC's manufacture code of C2H. Which apply VIH on A0 pin, the device will output MX29LV640T/B device code of C9H/CBH.

VERIFY SECTOR GROUP PROTECT STATUS OPERATION

MX29LV640T/B provides hardware method for sector group protect status verify. Which method requires VID on A9 pin, VIH on $\overline{WE}$ and A1 pins, VIL on $\overline{CE}$, $\overline{OE}$, A6, and A0 pins, and sector address on A16 to A21 pins. Which the identified sector is protected, the device will output 01H. Which the identified sector is not protect, the device will output 00H.

DATA PROTECTION

The MX29LV640T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

SECURED SILICON SECTOR

The MX29LV640T/B features a OTP memory region where the system may access through a command sequence to create a permanent part identification as so called Electronic Serial Number (ESN) in the device. Once this region is programmed, any further modification on the region is impossible. The secured silicon sector is a 128 words in length, and uses a Secured Silicon Sector Indicator Bit (Q7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevent duplication of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The MX29LV640T/B offers the device with Secured Silicon Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory , and has the Secured Silicon Sector Indicator Bit permanently set to a "1". The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to utilize that sector in any form they prefer. The customer-lockable version has the secured sector Indicator Bit permanently set to a "0". Therefore, the Secured Silicon Sector Indicator Bit prevents customer, lockable device from being used to replace devices that are factory locked.

The system access the Secured Silicon Sector through a command sequence (refer to "Enter Secured Silicon/ Exit Secured Silicon Sector command Sequence). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the address normally occupied by the last sector SA134 (for MX29LV640T) or first sector SA0 (for MX29LV640B). Once entry the Secured Silicon Sector the operation of boot sectors is disabled but the operation of main sectors is as normally. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending command to sector SA0.

LOW VCC WRITE INHIBIT

When VCC is less than VLKO the device does not accept any write cycles. This protects data during VCC power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until VCC is greater than VLKO. The system must provide the proper signals to the control pins to prevent unintentional write when VCC is greater than VLKO.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns (typical) on $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

POWER-UP SEQUENCE

The MX29LV640T/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

POWER-UP WRITE INHIBIT

If $\overline{WE}$=$\overline{CE}$=VIL and $\overline{OE}$=VIH during power up, the device does not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

POWER SUPPLY DE COUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

FACTORY LOCKED:Secured Silicon Sector Programmed and Protected At the Factory

In device with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. A factory locked device has an 8-word random ESN at address 3FFF70h-3FFF77h (for MX29LV640T) or 000000h-000007h (for MX29LV640B).

CUSTOMER LOCKABLE:Secured Silicon Sector NOT Programmed or Protected At the Factory

As an alternative to the factory-locked version, the device may be ordered such that the customer may program and protect the 128-word Secured Silicon Sector. Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotected the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that RESET may be at either VIH or VID. This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that method is only applicable to the Secured Silicon Sector.

Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then alternate method of sector protection described in the :Sector Group Protection and Unprotect" section.

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

SOFTWARE COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 2 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device (when applicable).

All addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. All data are latched on rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first.

TABLE 2. MX29LV640T/B COMMAND DEFINITIONS

Command		Bus Cycles	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Automatic Select (Note 7)														
Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	C2H				
	Byte	4	AAA	AA	555	55	AAA	90	X00	C2H				
Device ID	Word	4	555	AA	2AA	55	555	90	X01	DDI				
	Byte	4	AAA	AA	555	55	AAA	90	X02					
Secured Sector Factory Protect (Note 9)	Word	4	555	AA	2AA	55	555	90	X03	see				
	Byte	4	AAA	AA	555	55	AAA	90	X06	note 9				
Sector Group Protect Verify (Note 8)	Word	4	555	AA	2AA	55	555	90	(SA)X02	xx00/				
	Byte	4	AAA	AA	555	55	AAA	90	(SA)X04	xx01				
Enter Secured Silicon Sector	Word	3	555	AA	2AA	55	555	88						
	Byte	3	AAA	AA	555	55	AAA	88						
Exit Secured Silicon Sector	Word	4	555	AA	2AA	55	555	90	XXX	00				
	Byte	4	AAA	AA	555	55	AAA	90	XXX	00				
Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte	4	AAA	AA	555	55	AAA	A0	PA	PD				
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
CFI Query (Note 12)	Word	1	55	98										
	Byte	1	AA	98										
Erase Suspend (Note 10)		1	BA	B0										
Erase Resume (Note 11)		1	BA	30										

Legend:
X=Don't care
RA=Address of the memory location to be read.
RD=Data read from location RA during read operation.
PA=Address of the memory location to be programmed.
Addresses are latched on the falling edge of the WE or CE pulse, whichever happen later.
DDI=Data of device identifier
C2H for manufacture code
C9/CBH (Top/Bottom) for device code

PD=Data to be programmed at location PA. Data is latched on the rising edge of WE or CE pulse.
SA=Address of the sector to be erase or verified (in autoselect mode).
Address bits A21-A12 uniquely select any sector.

Notes:
1. See Table 1 for descriptions of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or automatic select data, all bus cycles are write operation.
4. Address bits are don't care for unlock and command cycles, except when PA or SA is required.
5. No unlock or command cycles required when device is in read mode.
6. The Reset command is required to return to the read mode when the device is in the automatic select mode or if Q5 goes high.
7. The fourth cycle of the automatic select command sequence is a read cycle.
8. The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block. In the third cycle of the command sequence, address bit A21=0 to verify sectors 0~63, A21=1 to verify sectors 64~134 for Top Boot device.
9. The data is 88h for factory locked and 08h for not factory locked.
10. The system may read and program functions in non-erasing sectors, or enter the automatic select mode, when in the erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
11. The Erase Resume command is valid only during the Erase Suspend mode.
12. Command is valid when device is ready to read array data or when device is in automatic select mode.

READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands for more information on this mode. The system must issue the reset command to re-enable the device for reading array data if Q5 goes high, or while in the automatic select mode. See the "Reset Command" section, next.

RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data (also applies to SILICON ID READ during Erase Suspend).

If Q5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

SILICON ID READ COMMAND SEQUENCE

The SILICON ID READ command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 2 shows the address and data requirements.
This method is an alternative to that shown in Table 1, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The SILICON ID READ command sequence is initiated by writing two unlock cycles, followed by the SILICON ID READ command. The device then enters the SILICON ID READ mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table for valid sector addresses.

The system must write the reset command to exit the automatic select mode and return to reading array data.

Byte/Word PROGRAM COMMAND SEQUENCE

The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 1 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using Q7, Q6, or RY/$\overline{BY}$. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. The Byte/Word Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across

sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set Q5 to "1" ," or cause the Data Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

SETUP AUTOMATIC CHIP/SECTOR ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H, or the sector erase command 30H.

The MX29LV640T/B contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL,A0=VIL retrieves the manufacturer code of C2H. A read cycle with A1=VIL, A0=VIH returns the device code of 22C9H/22CBH for MX29LV640T/B.

TABLE 3. SILICON ID CODE

Pins	A0	A1	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
Manufacture code	VIL	VIL	1	1	0	0	0	0	1	0	C2H
Device code for MX29LV640T	VIH	VIL	1	1	0	0	1	0	0	1	22C9H (word) XXC9H (byte)
Device code for MX29LV640B	VIH	VIL	1	1	0	0	1	0	1	1	22CBH (word) XXCBH (byte)

AUTOMATIC CHIP/SECTOR ERASE COMMAND

The device does not require the system to preprogram prior to erase. The Automatic Erase algorithm automatically pre-program and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 2 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Automatic Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using Q7, Q6, Q2, or RY/BY. See "Write Operation Status" for information on these status bits. When the Automatic Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 3 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to Figure 16 for timing diagrams.

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later , while the command (data) is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Sector addresses selected are loaded into internal register on the sixth falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. Each successive sector load cycle started by the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later must begin within 50us from the rising edge of the preceding $\overline{WE}$ or $\overline{CE}$, whichever happens first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase(30H) or Erase Suspend(B0H) during the time-out period resets the device to read mode.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. When the Erase Suspend command is issued during the sector erase operation, the device requires a maximum 20us to suspend the sector erase operation. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Erase Resume, program data to, or read data from any sector not selected for erasure.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended blocks.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV640T/B is capable of operating in the CFI mode. This mode all the host system to determine the manufacturer of the device such as operating parameters and configuration. Two commands are required in CFI mode. Query command of CFI mode is placed first, then the Reset command exits CFI mode. These are described in Table 3.

The single cycle Query command is valid only when the device is in the Read mode, including Erase Suspend, Standby mode, and Read ID mode; however, it is ignored otherwise.

The Reset command exits from the CFI mode to the Read mode, or Erase Suspend mode, or read ID mode. The command is valid only when the device is in the CFI mode.

Table 4-1. CFI mode: Identification Data Values

(All values in these tables are in hexadecimal)

Description	Address h (x16)	Address h (x8)	Data h
Query-unique ASCII string "QRY"	10	20	0051
	11	22	0052
	12	24	0059
Primary vendor command set and control interface ID code	13	26	0002
	14	28	0000
Address for primary algorithm extended query table	15	2A	0040
	16	2C	0000
Alternate vendor command set and control interface ID code (none)	17	2E	0000
	18	30	0000
Address for secondary algorithm extended query table (none)	19	32	0000
	1A	34	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address h (x16)	Address h (x8)	Data h
VCC supply, minimum (2.7V)	1B	36	0027
VCC supply, maximum (3.6V)	1C	38	0036
VPP supply, minimum (none)	1D	3A	0000
VPP supply, maximum (none)	1E	3C	0000
Typical timeout for single word/byte write (2^N us)	1F	3E	0004
Typical timeout for maximum size buffer write (2^N us)	20	40	0000
Typical timeout for individual block erase (2^N ms)	21	42	000A
Typical timeout for full chip erase (2^N ms)	22	44	0000
Maximum timeout for single word/byte write times (2^N X Typ)	23	46	0005
Maximum timeout for maximum size buffer write times (2^N X Typ)	24	48	0000
Maximum timeout for individual block erase times (2^N X Typ)	25	4A	0004
Maximum timeout for full chip erase times (not supported)	26	4C	0000

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address h (x16)	Address h (x8)	Data h
Device size (2^n bytes)	27	4E	0017
Flash device interface code (02=asynchronous x8/x16)	28	50	0002
	29	52	0000
Maximum number of bytes in multi-byte write (not supported)	2A	54	0000
	2B	56	0000

Number of erase block regions	2C	58	0002
Erase block region 1 information	2D	5A	0007
[2E,2D] = # of blocks in region -1	2E	5C	0000
[30, 2F] = size in multiples of 256-bytes	2F	5E	0020
	30	60	0000
	31h	62	007Eh
Erase Block Region 2 Information (refer to CFI publication 100)	32h	64	0000h
	33h	66	0000h
	34h	68	0001h
	35h	6A	0000h
Erase Block Region 3 Information (refer to CFI publication 100)	36h	6C	0000h
	37h	6E	0000h
	38h	70	0000h
	39h	72	0000h
Erase Block Region 4 Information (refer to CFI publication 100)	3Ah	74	0000h
	3Bh	76	0000h
	3Ch	78	0000h

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address h (x16)	Address h (x8)	Data h
Query-unique ASCII string "PRI"	40	80	0050
	41	82	0052
	42	84	0049
Major version number, ASCII	43	86	0031
Minor version number, ASCII	44	88	0031
Address sensitive unlock (0=required, 1= not required)	45	8A	0000
Erase suspend (2= to read and write)	46	8C	0002
Sector protect (N= # of sectors/group)	47	8E	0004
Temporary sector unprotect (1=supported)	48	90	0001
Sector protect/unprotect scheme	49	92	0004
Simultaneous R/W operation (0=not supported)	4A	94	0000
Burst mode type (0=not supported)	4B	96	0000
Page mode type (0=not supported)	4C	98	0000
ACC (Acceleration) Supply Minimum 00h=Not Supported, D7-D4: Volt, D3-D0:100mV	4Dh	9A	00h
ACC (Acceleration) Supply Maximum 00h=Not Supported, D7-D4: Volt, D3-D0:100mV	4Eh	9C	00h
Top/Bottom Boot Sector Flag 02h=Bottom Boot Device, 03h=Top Boot Device	4Fh	9E	0002h/ 0003h

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6, Q7, and RY/BY. Table 10 and the following subsections describe the functions of these bits. Q7, RY/BY, and Q6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Table 5. Write Operation Status

	Status		Q7 Note1	Q6	Q5 Note2	Q3	Q2	RY/BY
In Progress	Byte/Word Program in Auto Program Algorithm		Q7	Toggle	0	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	0	1	Toggle	0
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle	1
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	1
		Erase Suspend Program	Q7	Toggle	0	N/A	N/A	0
Exceeded Time Limits	Byte/Word Program in Auto Program Algorithm		Q7	Toggle	1	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	1	1	Toggle	0
	Erase Suspend Program		Q7	Toggle	1	N/A	N/A	0

Notes:
1. Performing successive read operations from the erase-suspended sector will cause Q2 to toggle.
2. Performing successive read operations from any address will cause Q6 to toggle.
3. Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the Q2 bit.
   However, successive reads from the erase-suspended sector will cause Q2 to toggle.

Q7: Data Polling

The Data Polling bit, Q7, indicates to the host system whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data Polling is valid after the rising edge of the final WE pulse in the program or erase command sequence.

During the Automatic Program algorithm, the device outputs on Q7 the complement of the datum programmed to Q7. This Q7 status also applies to programming during Erase Suspend. When the Automatic Program algorithm is complete, the device outputs the datum programmed to Q7. The system must provide the program address to read valid status information on Q7. If a program address falls within a protected sector, Data Polling on Q7 is active for approximately 1 us, then the device returns to reading array data.

During the Automatic Erase algorithm, Data Polling produces a "0" on Q7. When the Automatic Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data Polling produces a "1" on Q7. This is analogous to the complement/true datum output described for the Automatic Program algorithm: the erase function changes all the bits in a sector to "1" prior to this, the device outputs the "complement," or "0"." The system must provide an address within any of the sectors selected for erasure to read valid status information on Q7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data Polling on Q7 is active for approximately 100 us, then the device returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects Q7 has changed from the complement to true data, it can read valid data at Q7-Q0 on the following read cycles. This is because Q7 may change asynchronously with Q0-Q6 while Output Enable (OE) is asserted low.

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE or CE, whichever happens first pulse in the command sequence (prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE or CE to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles for 100us and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 4 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE or CE, whichever happens first pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE or CE to control the read

cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 4 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5:Program/Erase Timing

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte/word programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

The Q5 failure condition may appear if the system tries to program a to a "1" location that is previously programmed to "0". Only an erase operation can change a "0" back to a "1"." Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, Q5 produces a "1".

Q3:Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is

still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

If the time between additional erase commands from the system can be less than 50us, the system need not to monitor Q3.

RY/BY:READY/BUSY OUTPUT

The RY/BY is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY status is valid after the rising edge of the final WE pulse in the command sequence. Since RY/BY is an open-drain output, several RY/BY pins can be tied together in parallel with a pull-up resistor to VCC .

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages . . . . -65°C to +150°C

Ambient Temperature

with Power Applied. . . . . -65°C to +125°C

Voltage with Respect to Ground

VCC (Note 1) . . . . . -0.5 V to +4.0 V

A9, $\overline{OE}$, and

$\overline{RESET}$ (Note 2) . . . .-0.5 V to +12.5 V

All other pins (Note 1) . . . . . -0.5 V to VCC +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot VSS to -2.0 V for periods of up to 20 ns. See Figure 6. Maximum DC voltage on input or I/O pins is VCC +0.5 V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods up to 20 ns. See Figure 7.
2. Minimum DC input voltage on pins A9, $\overline{OE}$, and $\overline{RESET}$ is -0.5 V. During voltage transitions, A9, $\overline{OE}$, and $\overline{RESET}$ may overshoot VSS to -2.0 V for periods of up to 20 ns. See Figure 6. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RATINGS

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . -40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for full voltage range. . . . . +2.7 V to 3.6 V

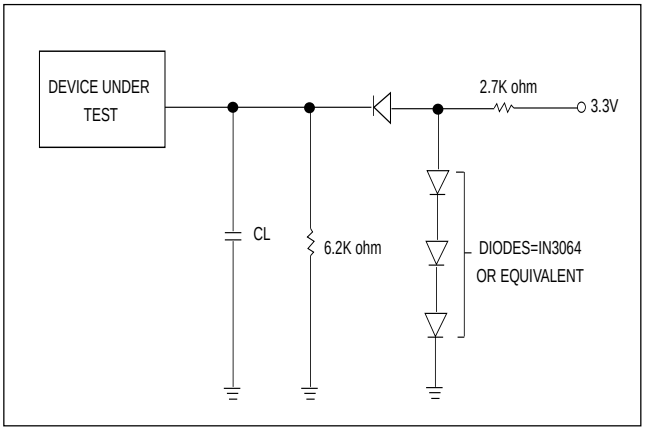
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS TA=-40℃ to 85℃, VCC=2.7V~3.6V

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I LI	Input Load Current (Note 1)	VIN = VSS to VCC , VCC = VCC max				±1.0	uA
I LIT	A9 Input Leakage Current	VCC=VCC max; A9 = 12.5V				35	uA
I LO	Output Leakage Current	VOUT = VSS to VCC , VCC= VCC max				±1.0	uA
ICC1	VCC Active Read Current (Notes 2,3)	$\overline{CE}$= VIL, $\overline{OE}$ = VIH	5 MHz		9	16	mA
			1 MHz		2	4	mA
ICC2	VCC Active Write Current (Notes 2,4,6)	$\overline{CE}$= V IL , $\overline{OE}$ = V IH			26	30	mA
ICC3	VCC Standby Current (Note 2)	$\overline{CE}$,$\overline{RESET}$=VCC±0.3V $\overline{WP}$=VIH			0.2	15	uA
ICC4	VCC Reset Current (Note 2)	$\overline{RESET}$=VSS±0.3V $\overline{WP}$=VIH			0.2	15	uA
ICC5	Automatic Sleep Mode (Note 2,5)	VIL = V SS ± 0.3 V, VIH = VCC ± 0.3 V, $\overline{WP}$=VIH			0.2	15	uA
VIL	Input Low Voltage			-0.5		0.8	V
VIH	Input High Voltage			0.7xVcc		Vcc+0.3	V
VID	Voltage for Autoselect and Temporary Sector Unprotect	VCC = 3.0 V ± 10%		11.5		12.5	V
VOL	Output Low Voltage	IOL= 4.0mA,VCC=VCC min				0.45	V
VOH1	Output High Voltage	IOH=-2.0mA,VCC=VCC min		0.85VCC			V
VOH2		IOH=-100uA,VCC=VCC min		VCC-0.4			V
VLKO	Low VCC Lock-Out Voltage (Note 4)			1.5			V

Notes:
1. On the $\overline{WP}$ pin only, the maximum input load current when $\overline{WP}$ = VIL is ±5.0uA
2. Maximum ICC specifications are tested with VCC = VCC max.
3. The ICC current listed is typically is less than 2 mA/MHz, with $\overline{OE}$ at VIH . Typical specifications are for VCC = 3.0V.
4. ICC active while Embedded Erase or Embedded Program is in progress.
5. Automatic sleep mode enables the low power mode when addresses remain stable for t ACC + 30 ns. Typical sleep mode current is 200 nA.
6. Not 100% tested.

SWITCHING TEST CIRCUITS



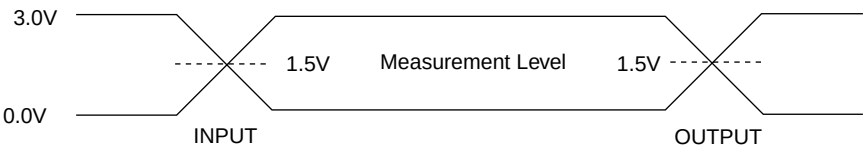
TEST SPECIFICATIONS

Test Condition	90	120	Unit
Output Load	1 TTL gate		
Output Load Capacitance, CL (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0-3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State(High Z)

SWITCHING TEST WAVEFORMS



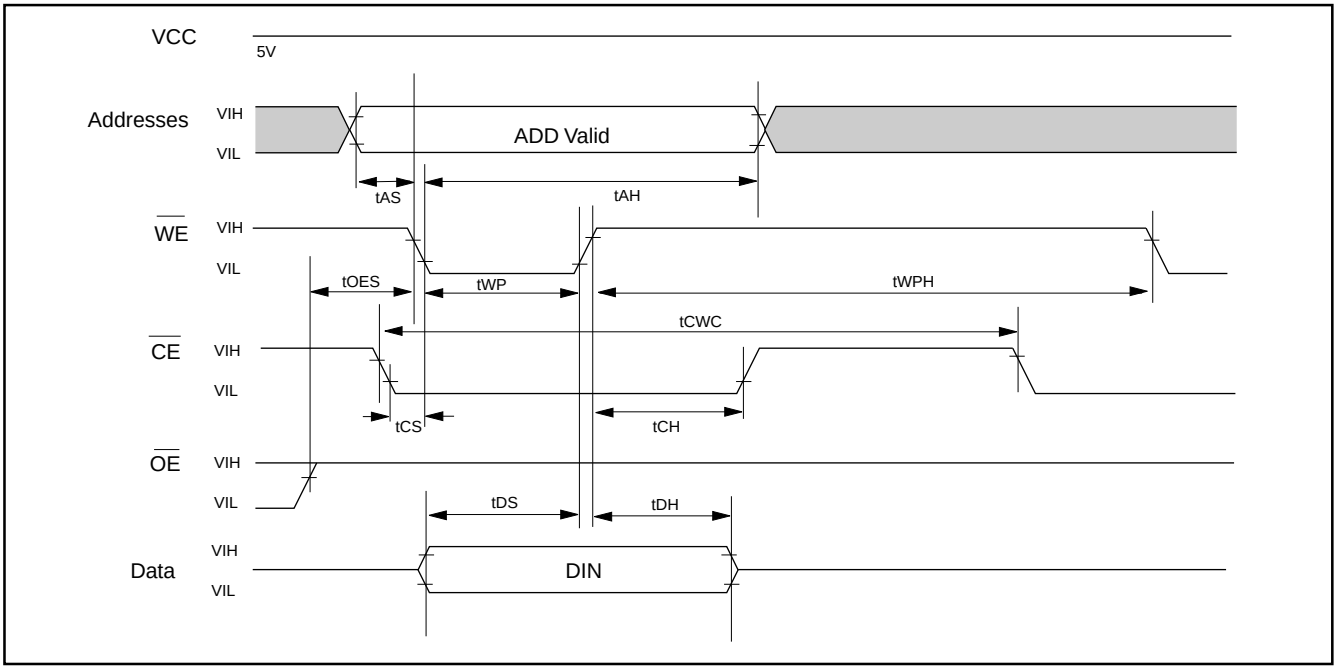
AC CHARACTERISTICS

Read-Only Operations TA=-40℃ to 85℃, VCC=2.7V~3.6V

Parameter Std.	Description		Test Setup		Speed Options 90	Speed Options 120	Unit
tRC	Read Cycle Time (Note 1)			Min	90	120	ns
tACC	Address to Output Delay		$\overline{CE}$, $\overline{OE}$=VIL	Max	90	120	ns
tCE	Chip Enable to Output Delay		$\overline{OE}$=VIL	Max	90	120	ns
tOE	Output Enable to Output Delay			Max	35	50	ns
tDF	Chip Enable to Output High Z (Note 1)			Max	30	30	ns
tDF	Output Enable to Output High Z (Note 1)			Max	30	30	ns
tOH	Output Hold Time From Address, $\overline{CE}$ or $\overline{OE}$, whichever Occurs First			Min	0		ns
tOEH	Output Enable Hold Time (Note 1)	Read		Min	0		ns
		Toggle and $\overline{Data}$ Polling		Min	10		ns

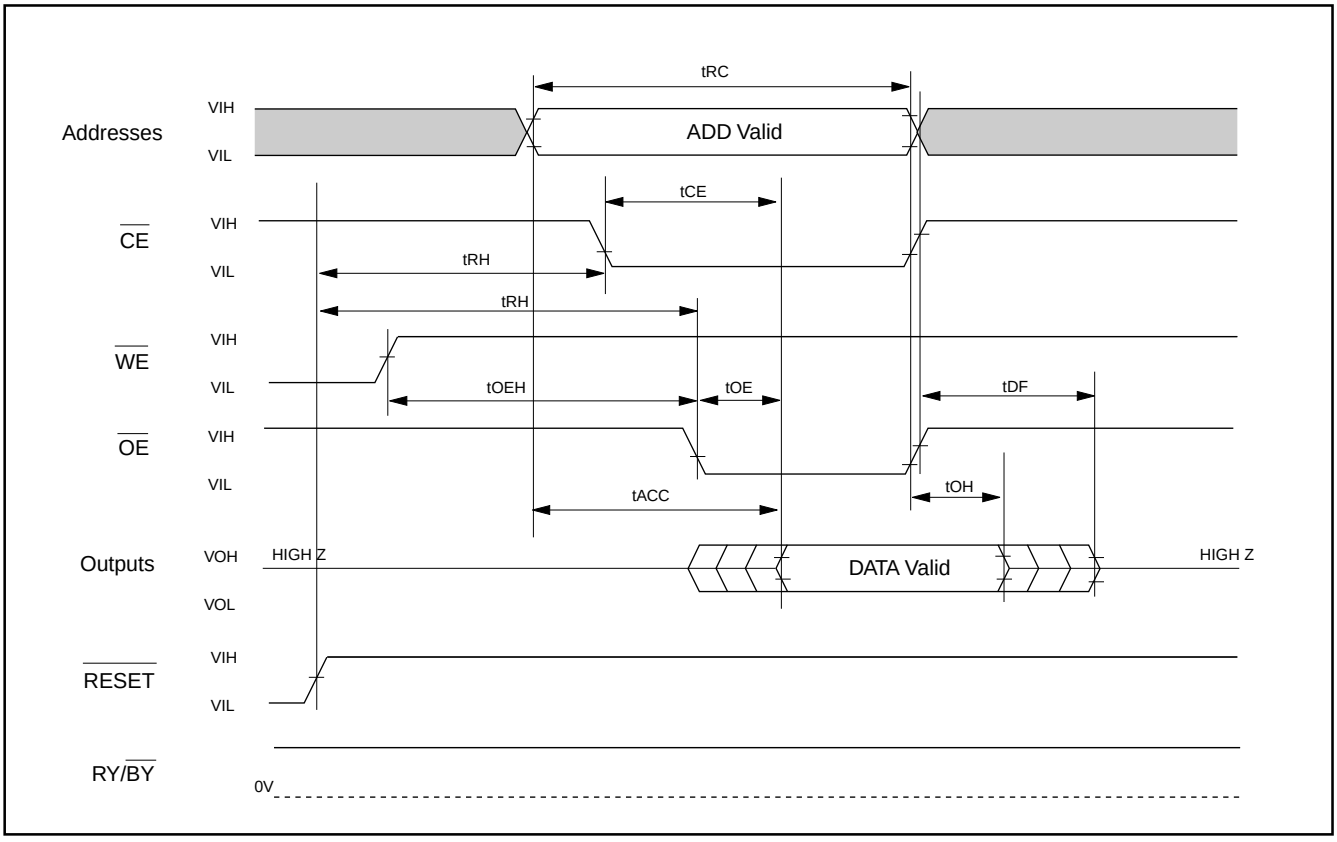
Notes:
1. Not 100% tested.
2. See SWITCHING TEST CIRCUITS and TEST SPECIFICATIONS TABLE for test specifications.

Fig 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

Fig 2. READ TIMING WAVEFORMS

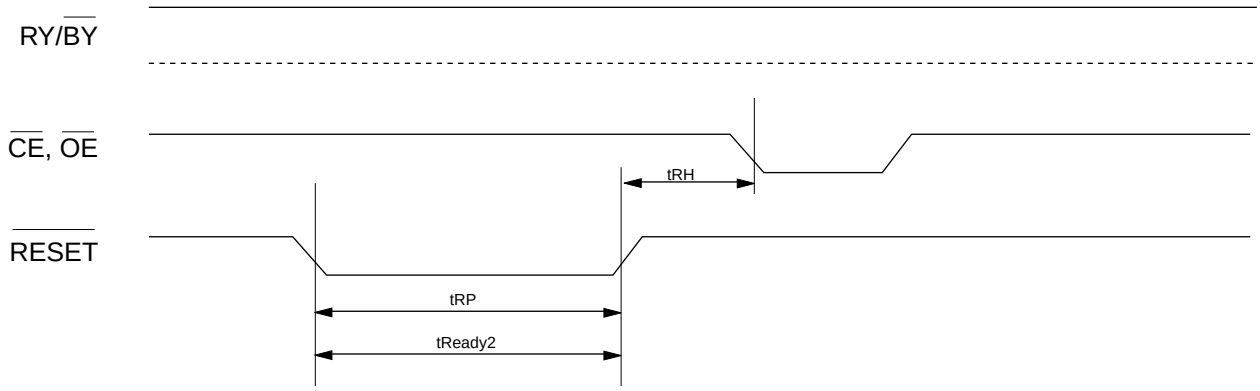


AC CHARACTERISTICS

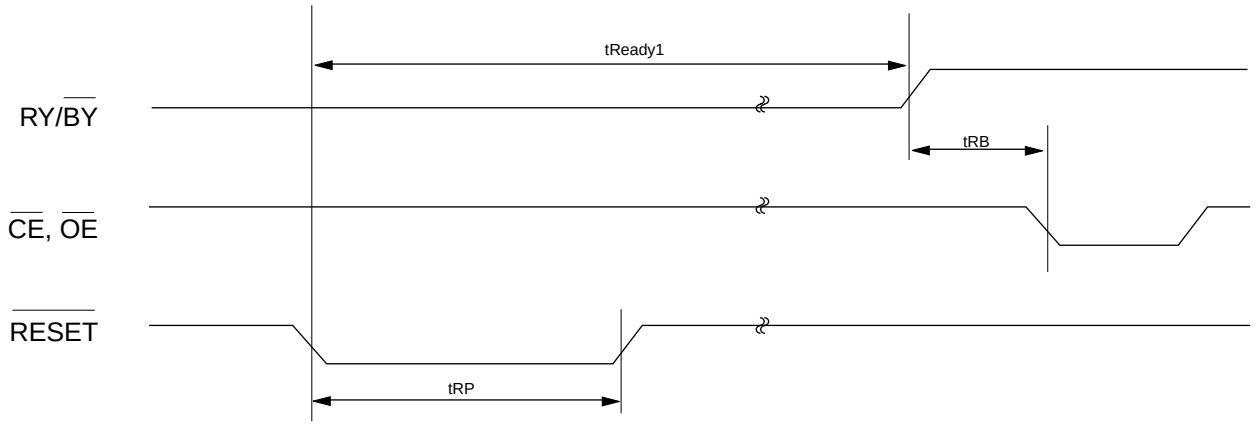
Parameter	Description	Test Setup	All Speed Options	Unit
tREADY1	$\overline{\text{RESET}}$ PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	$\overline{\text{RESET}}$ PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP	$\overline{\text{RESET}}$ Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	$\overline{\text{RESET}}$ High Time Before Read(See Note)	MIN	50	ns
tRB	RY/$\overline{\text{BY}}$ Recovery Time(to $\overline{\text{CE}}$, $\overline{\text{OE}}$ go low)	MIN	0	ns
tRPD	$\overline{\text{RESET}}$ Low to Standby Mode	MIN	20	us

Note:Not 100% tested

Fig 3. $\overline{\text{RESET}}$ TIMING WAVEFORM



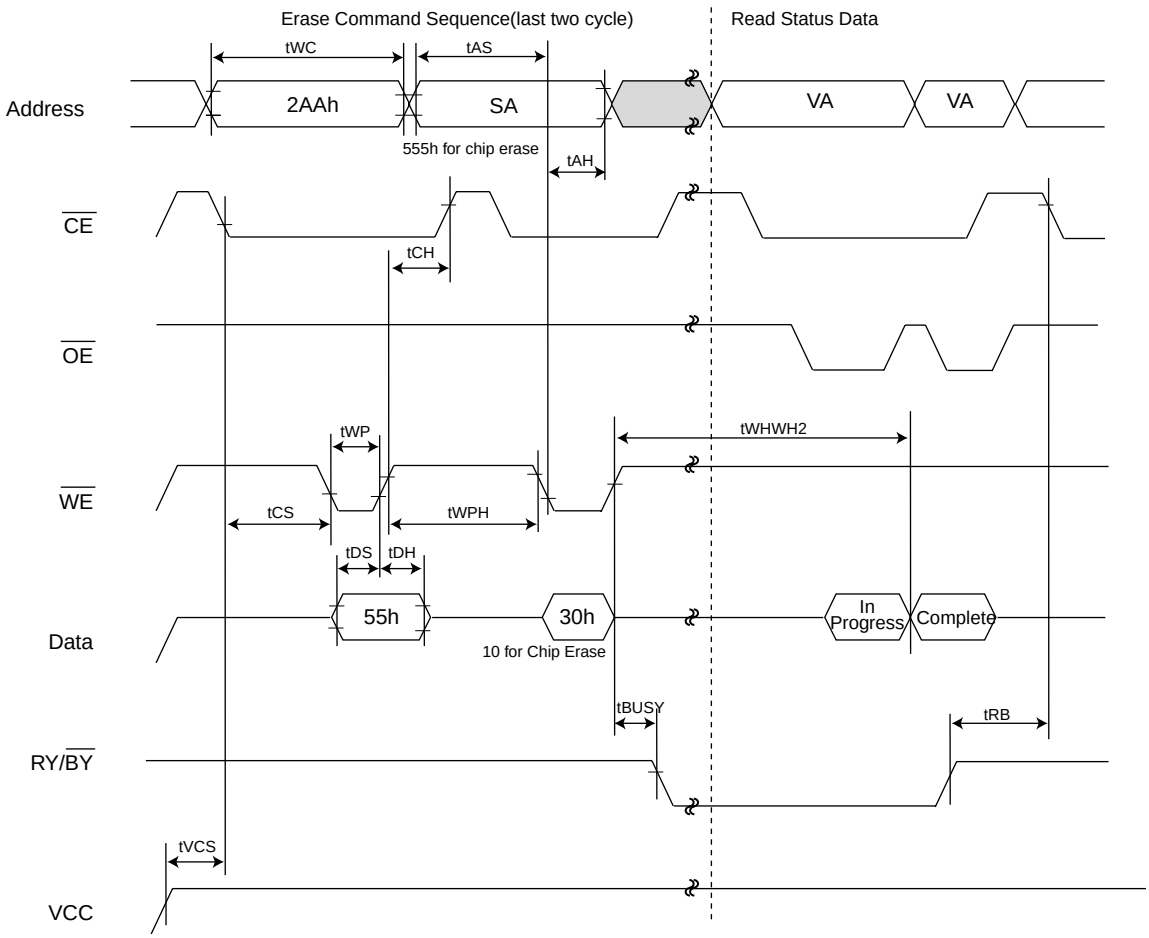
Reset Timing NOT during Automatic Algorithms



Reset Timing during Automatic Algorithms

ERASE/PROGRAM OPERATION

Fig 4. AUTOMATIC CHIP/SECTOR ERASE TIMING WAVEFORM



NOTES:
1.SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

Fig 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

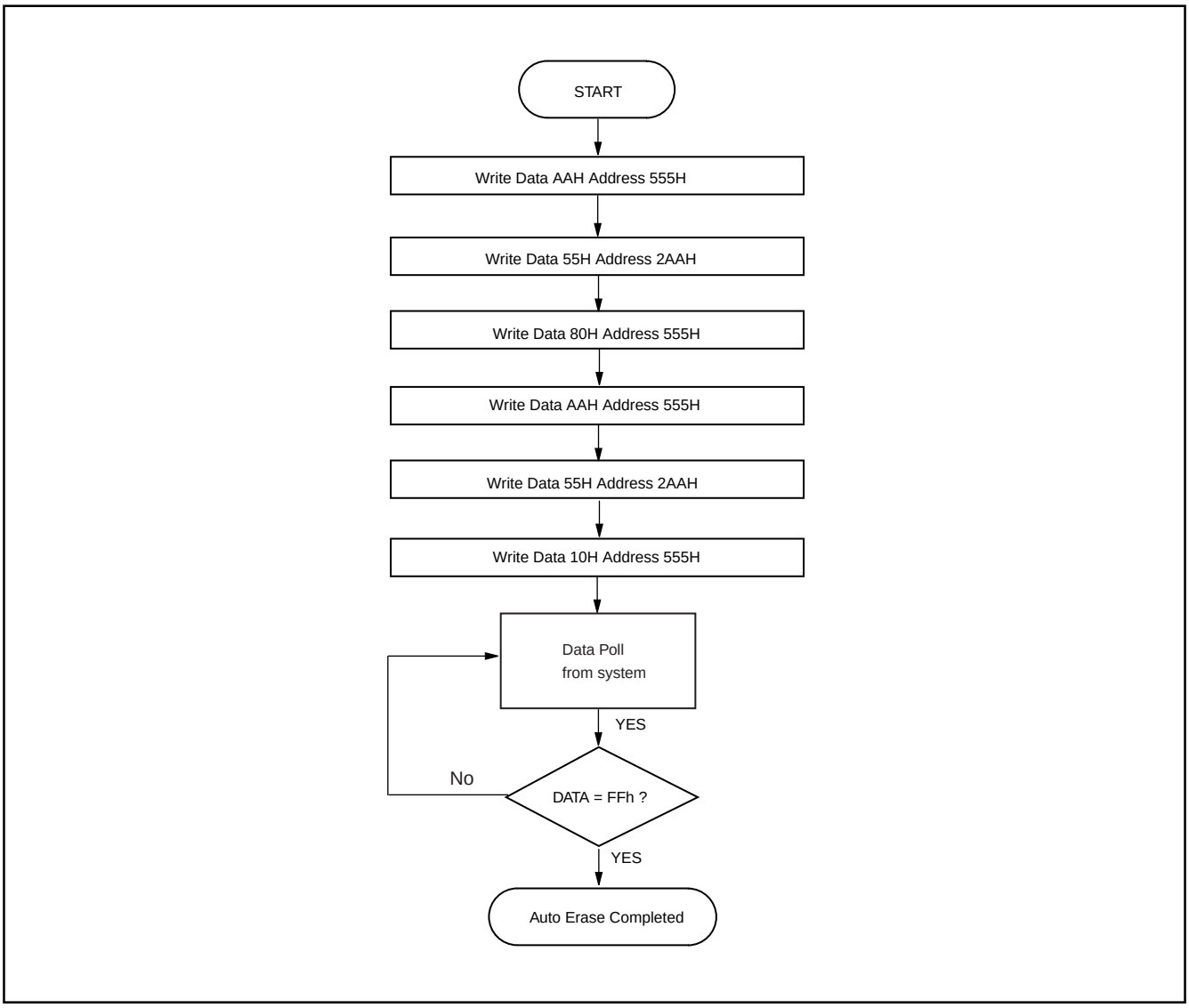


Fig 6. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

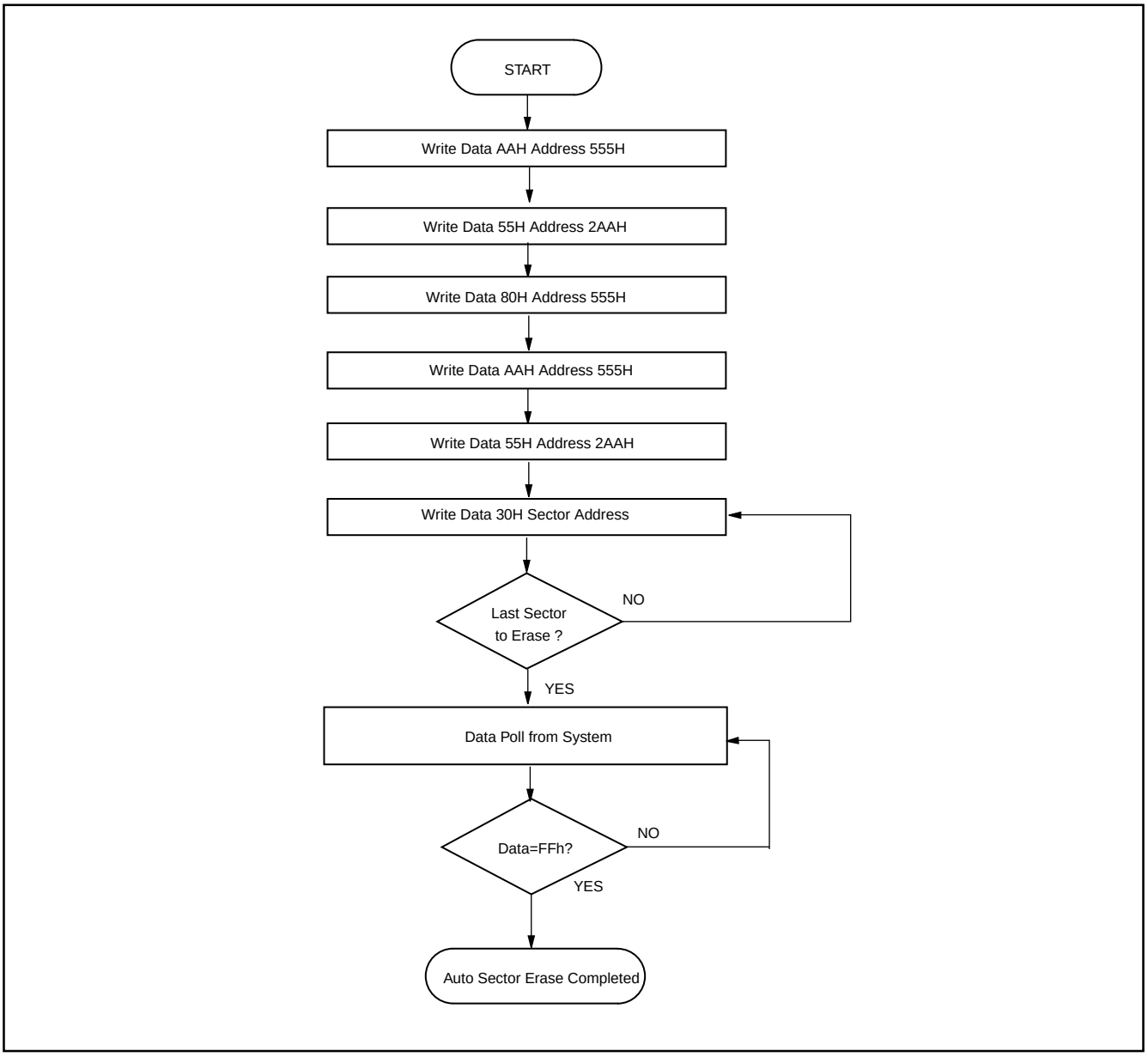


Fig 7. ERASE SUSPEND/RESUME FLOWCHART

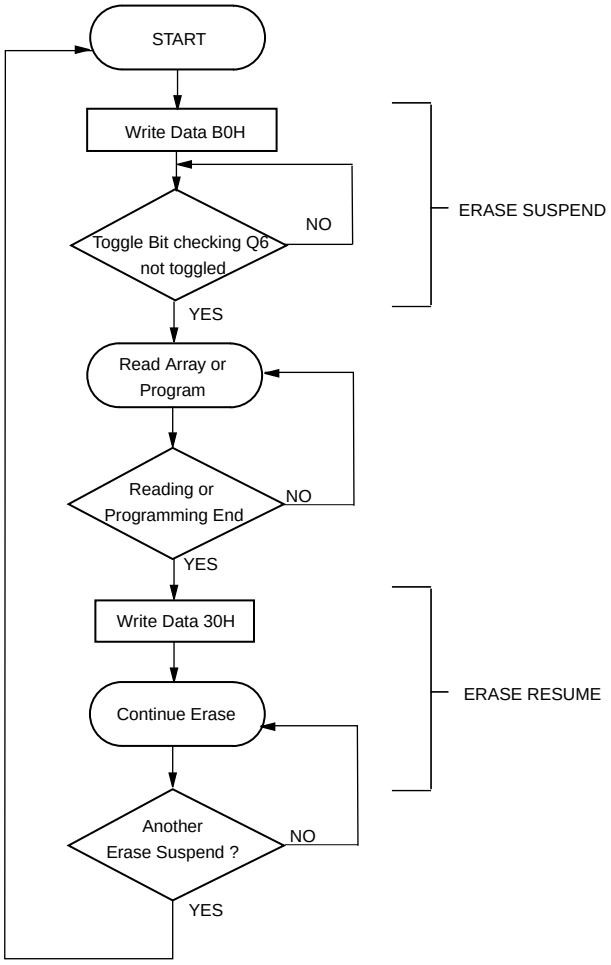
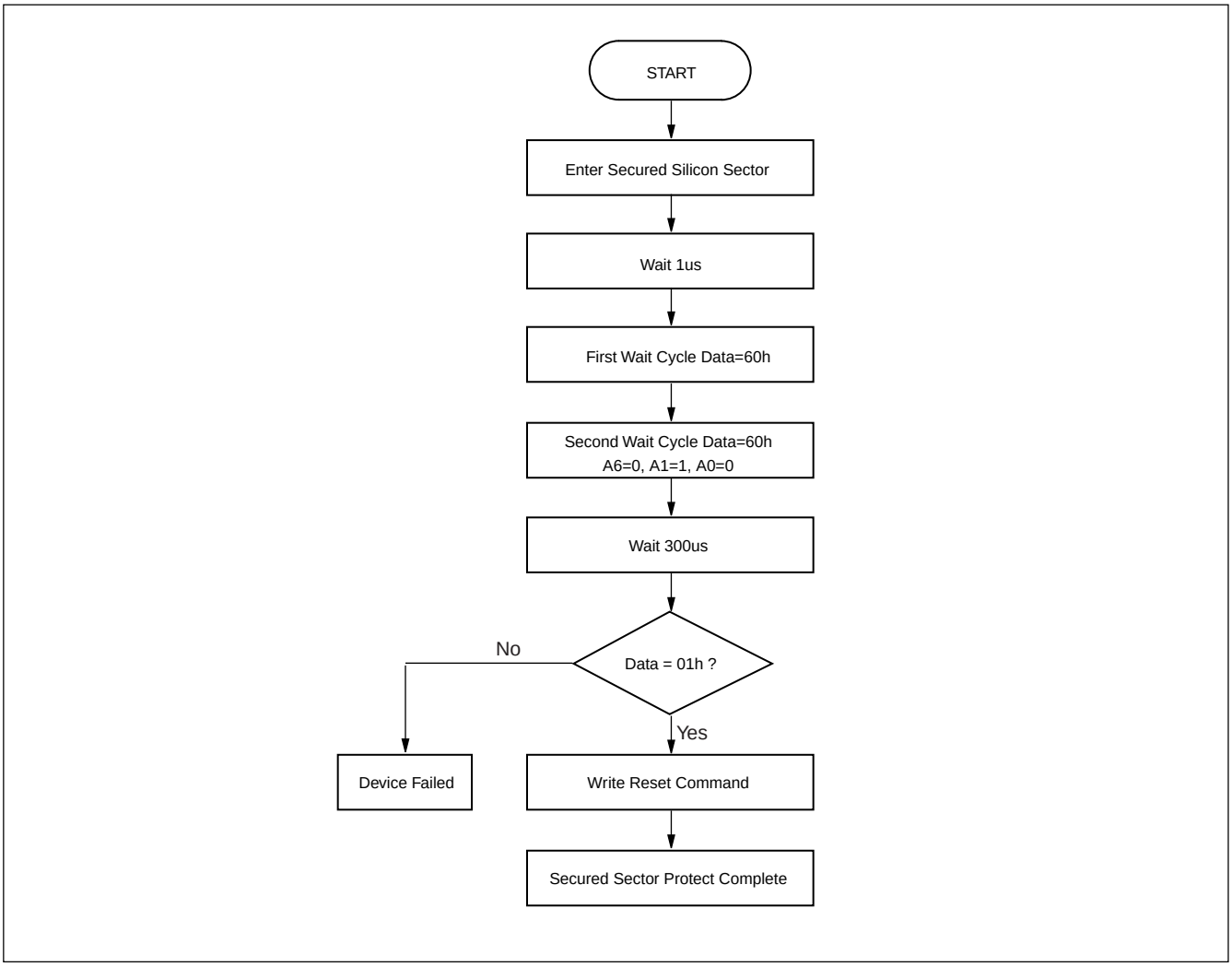


Fig 8. SECURED SILICON SECTOR PROTECTED ALGORITHMS FLOWCHART



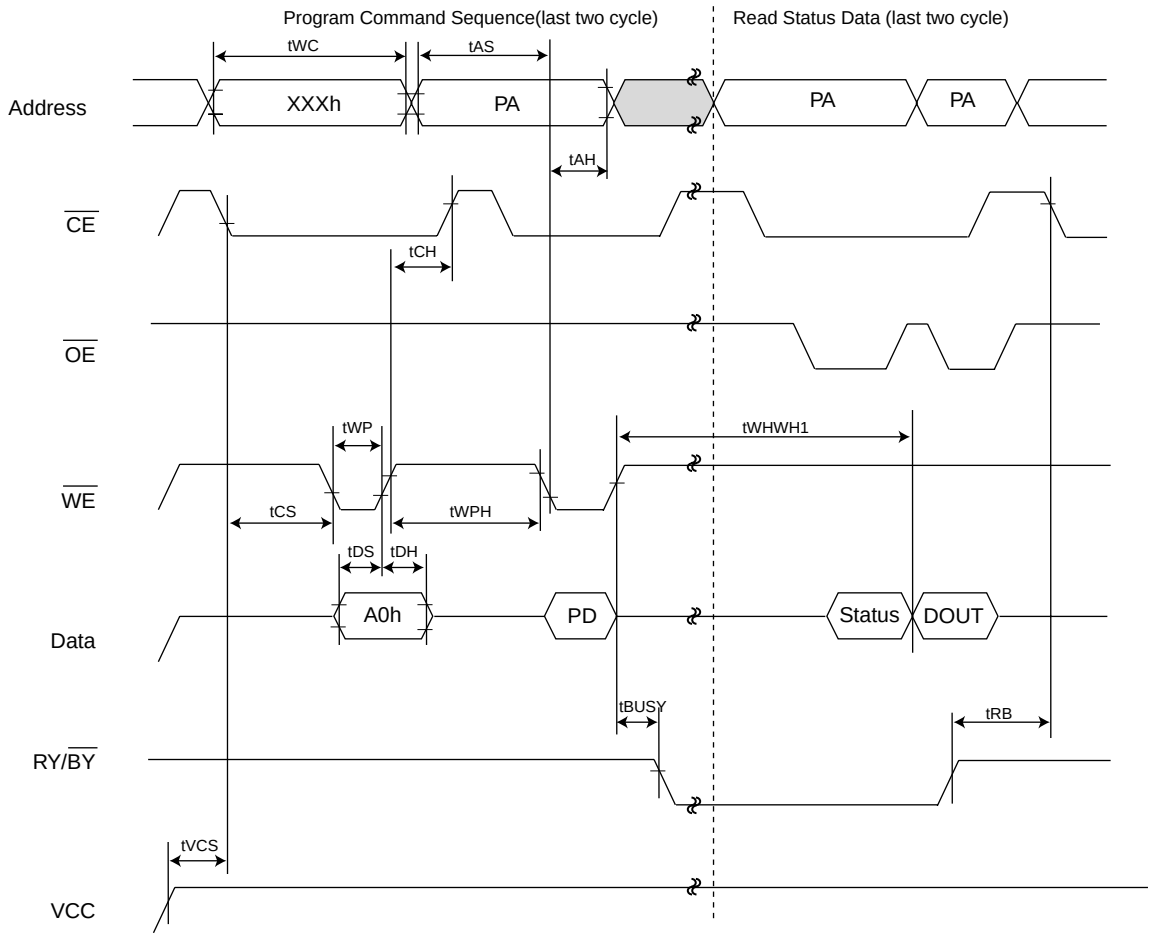
AC CHARACTERISTICS

Erase and Program Operations TA=-40℃ to 85℃, VCC=2.7V~3.6V

Parameter Std.	Description			Speed Options 90	Speed Options 120	Unit
tWC	Write Cycle Time (Note 1)		Min	90	120	ns
tAS	Address Setup Time		Min	0		ns
tASO	Address Setup Time to $\overline{OE}$ low during toggle bit polling		Min	15		ns
tAH	Address Hold Time		Min	45	50	ns
tAHT	Address Hold Time From $\overline{CE}$ or $\overline{OE}$ high during toggle bit polling		Min	0		ns
tDS	Data Setup Time		Min	45	50	ns
tDH	Data Hold Time		Min	0		ns
tOEPH	Output Enable High during toggle bit polling		Min	20		ns
tGHWL	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min	0		ns
tGHEL	Read Recovery Time Before Write		Min	0		ns
tCS	$\overline{CE}$ Setup Time		Min	0		ns
tCH	$\overline{CE}$ Hold Time		Min	0		ns
tWP	Write Pulse Width		Min	35	50	ns
tWPH	Write Pulse Width High		Min	30		ns
tWHWH1	Programming Operation	Byte	Typ	9		us
		Word	Typ	11		us
tWHWH2	Sector Erase Operation (Note 2)		Typ	1.6		sec
tVCS	VCC Setup Time (Note 1)		Min	50		us
tRB	Write Recovery Time from RY/$\overline{BY}$		Min	0		ns
tBUSY	Program/Erase Valid to RY/$\overline{BY}$ Delay		Min	90		ns

Notes:
1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.

Fig 9. AUTOMATIC PROGRAM TIMING WAVEFORMS



NOTES:

1.PA=Program Address, PD=Program Data, DOUT is the true data the program address

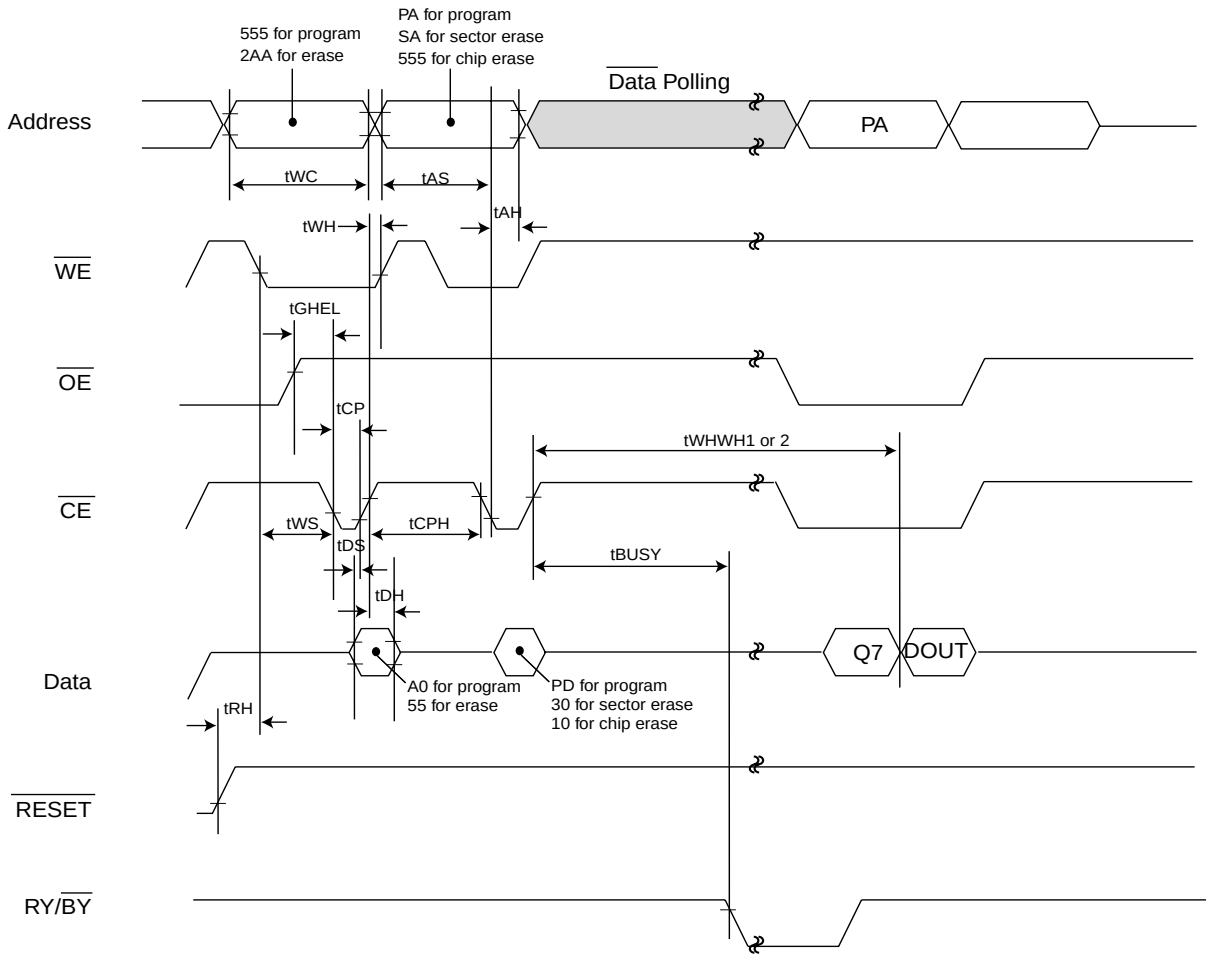
AC CHARACTERISTICS

Alternate $\overline{CE}$ Controlled Erase and Program Operations

Parameter Std.	Description			Speed Options 90	Speed Options 120	Unit
tWC	Write Cycle Time (Note 1)		Min	90	120	ns
tAS	Address Setup Time		Min	0		ns
tAH	Address Hold Time		Min	45	50	ns
tDS	Data Setup Time		Min	45	50	ns
tDH	Data Hold Time		Min	0		ns
tGHEL	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min	0		ns
tWS	$\overline{WE}$ Setup Time		Min	0		ns
tWH	$\overline{WE}$ Hold Time		Min	0		ns
tCP	$\overline{CE}$ Pulse Width		Min	45	50	ns
tCPH	$\overline{CE}$ Pulse Width High		Min	30		ns
tWHWH1	Programming Operation	Byte	Typ	9		us
		Word	Typ	11		us
tWHWH2	Sector Erase Operation (Note 2)		Typ	1.6		sec

Notes:
1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.

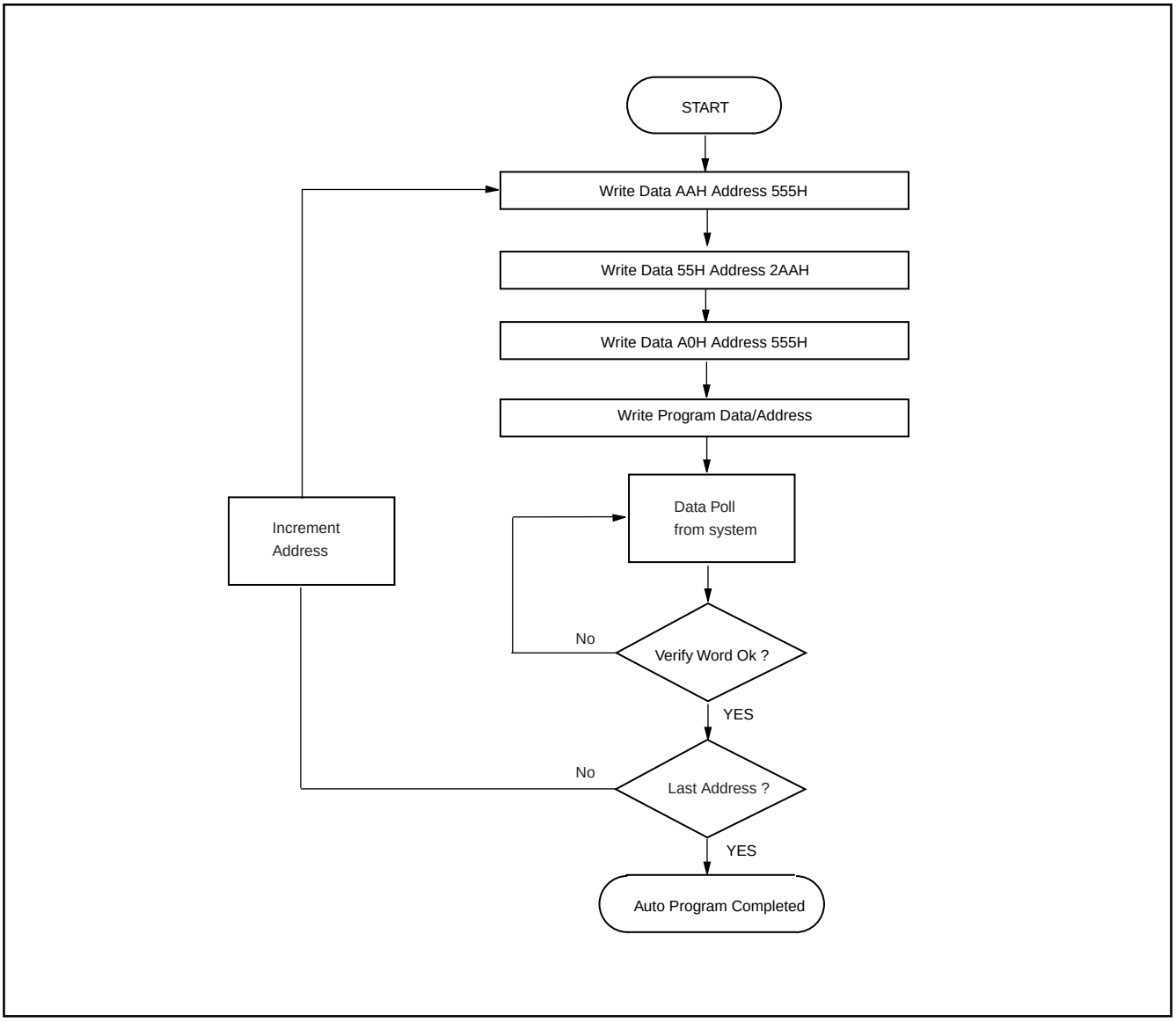
Fig 10. $\overline{CE}$ CONTROLLED PROGRAM TIMING WAVEFORM



NOTES:

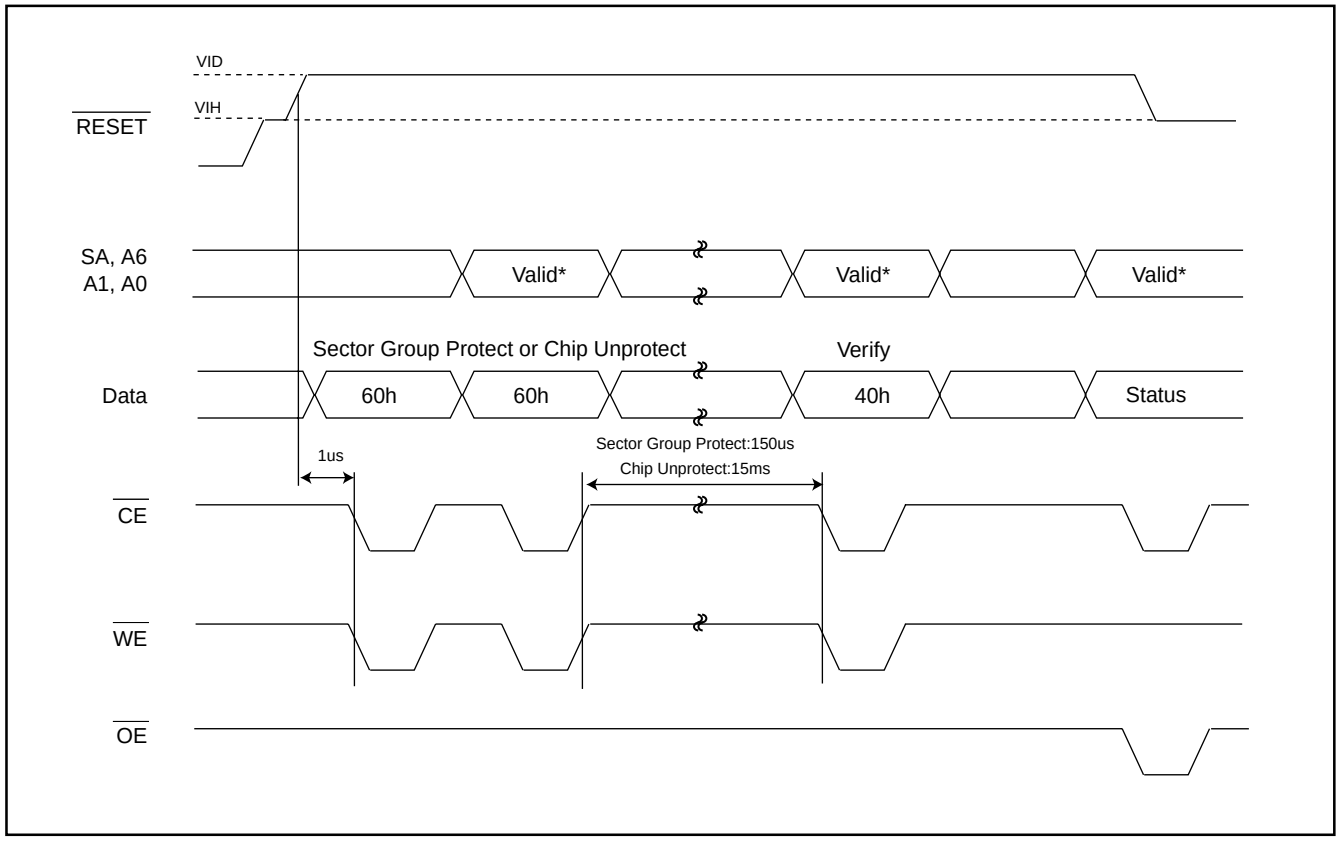
1.PA=Program Address, PD=Program Data, DOUT=Data Out, Q7=complement of data written to device.
2.Figure indicates the last two bus cycles of the command sequence.

Fig 11. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



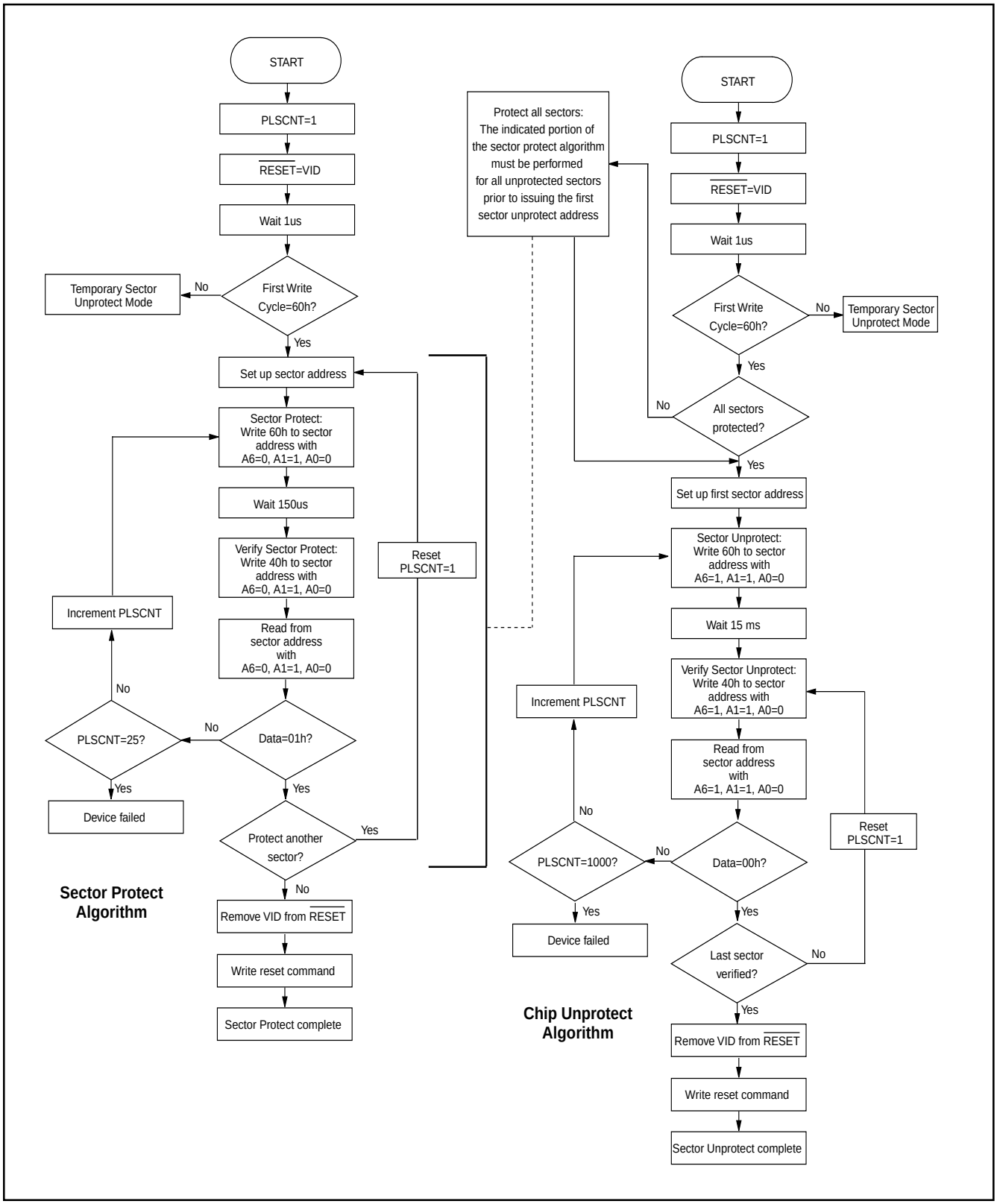
SECTOR GROUP PROTECT/CHIP UNPROTECT

Fig 12. Sector Group Protect / Chip Unprotect Waveform ($\overline{\text{RESET}}$ Control)



Note: For sector group protect A6=0, A1=1, A0=0. For chip unprotect A6=1, A1=1, A0=0

Fig 13. IN-SYSTEM SECTOR GROUP PROTECT/CHIP UNPROTECT ALGORITHMS WITH RESET=VID



AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tVLHT	Voltage transition time	Min.	4	us
tWPP1	Write pulse width for sector group protect	Min.	100	ns
tOESP	$\overline{OE}$ setup time to $\overline{WE}$ active	Min.	4	us

Fig 14. SECTOR GROUP PROTECT TIMING WAVEFORM (A9, $\overline{OE}$ Control)

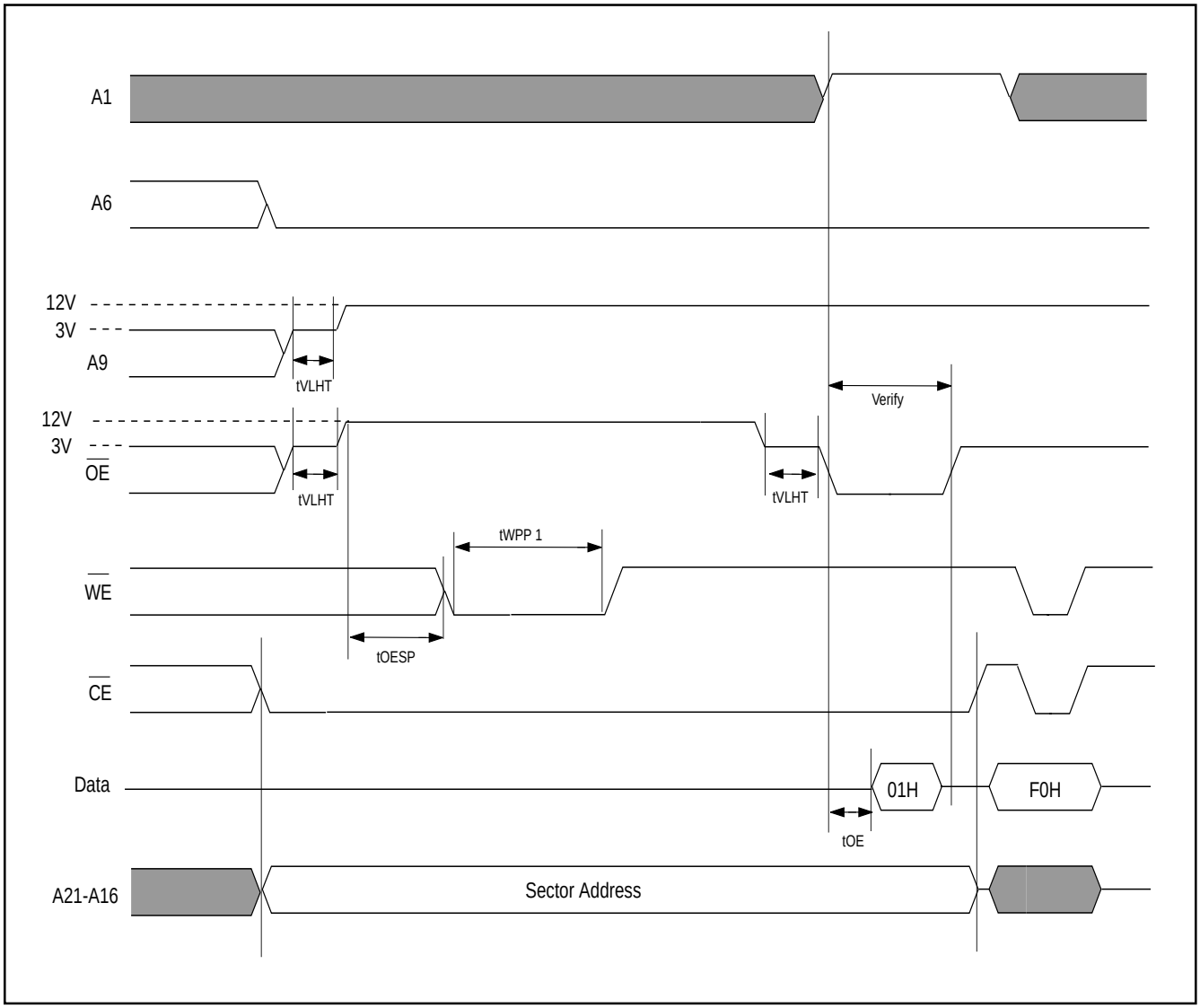


Fig 15. SECTOR GROUP PROTECTION ALGORITHM (A9, $\overline{OE}$ Control)

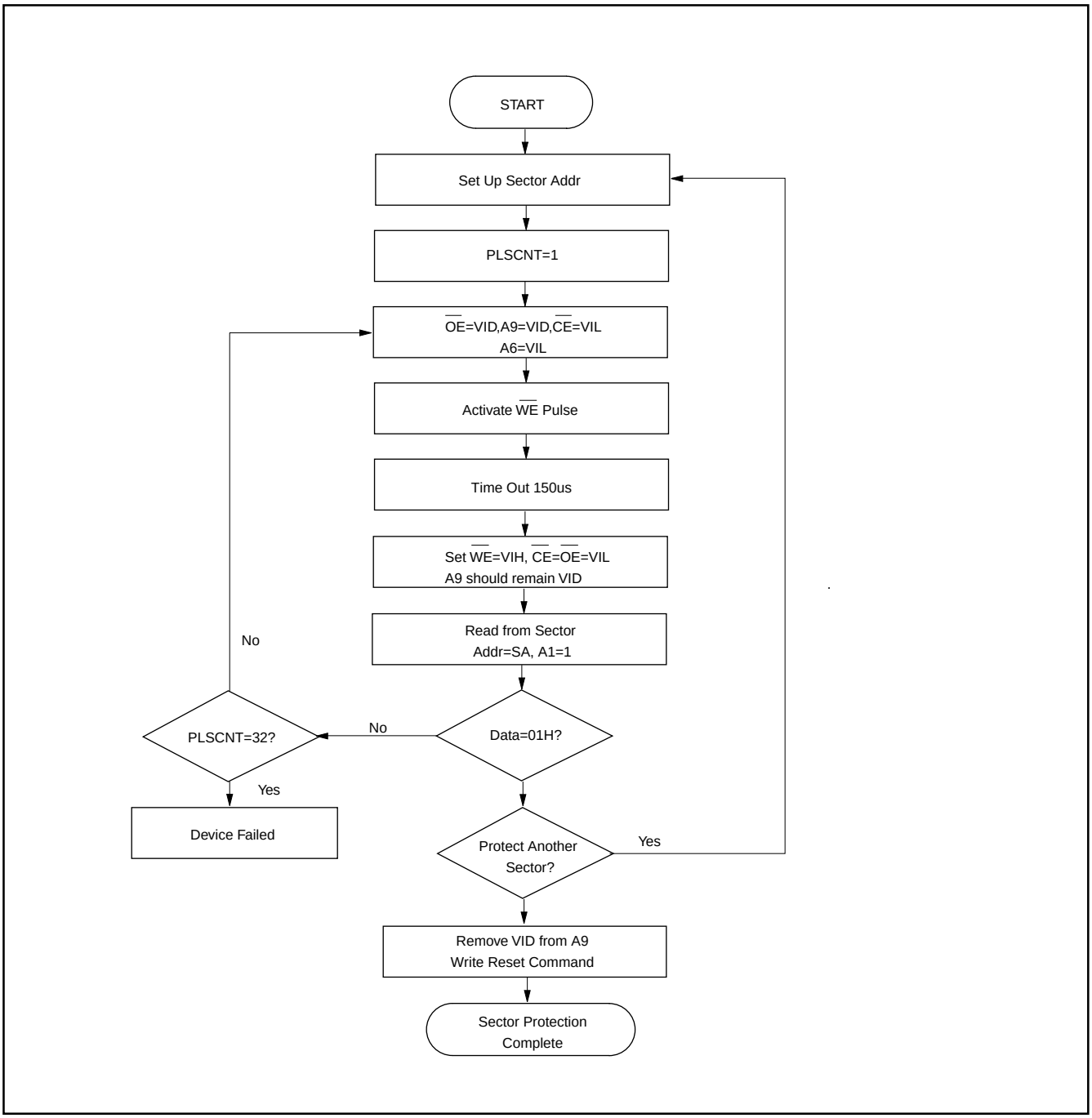


Fig 16. CHIP UNPROTECT TIMING WAVEFORM (A9, $\overline{OE}$ Control)

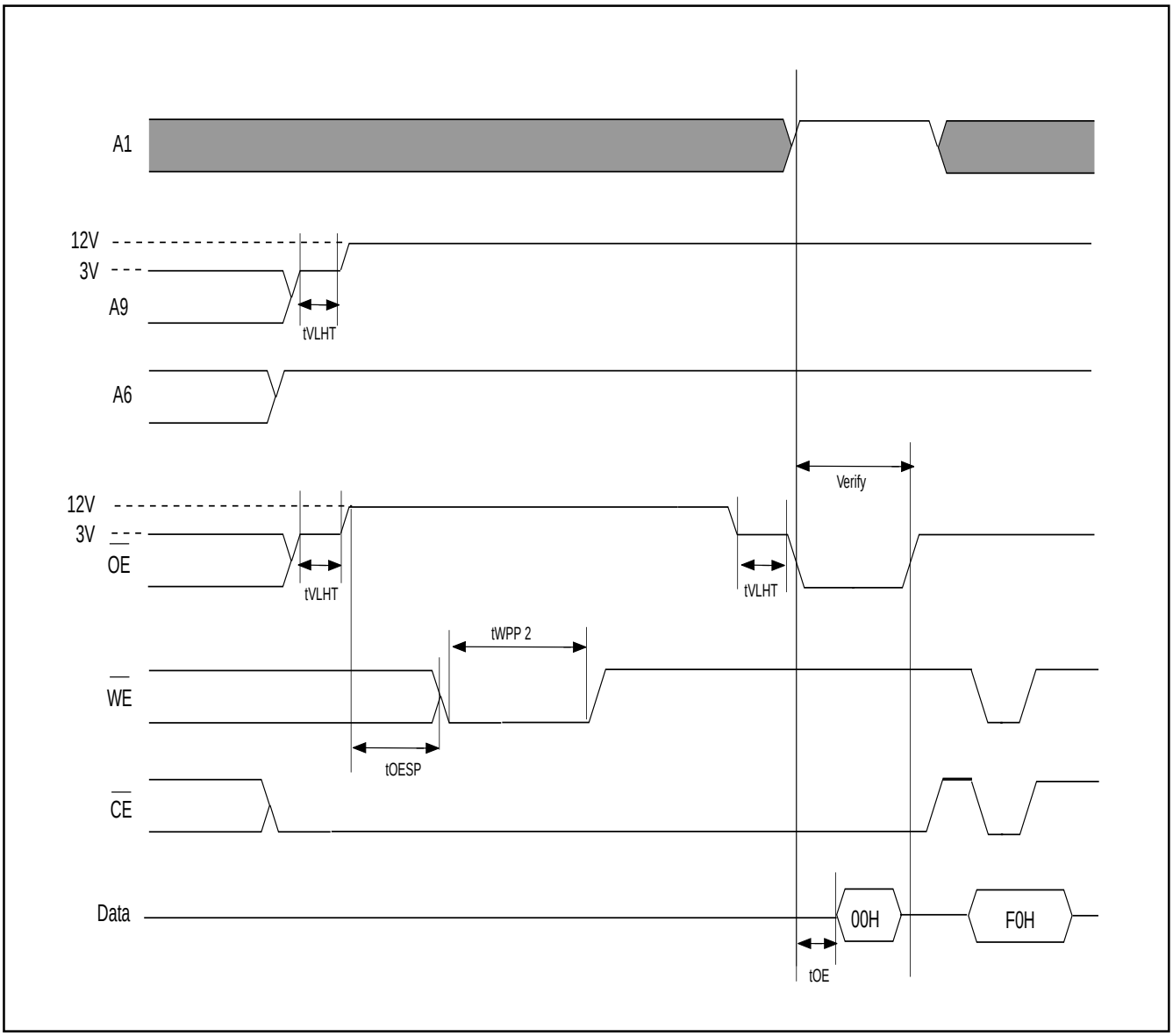
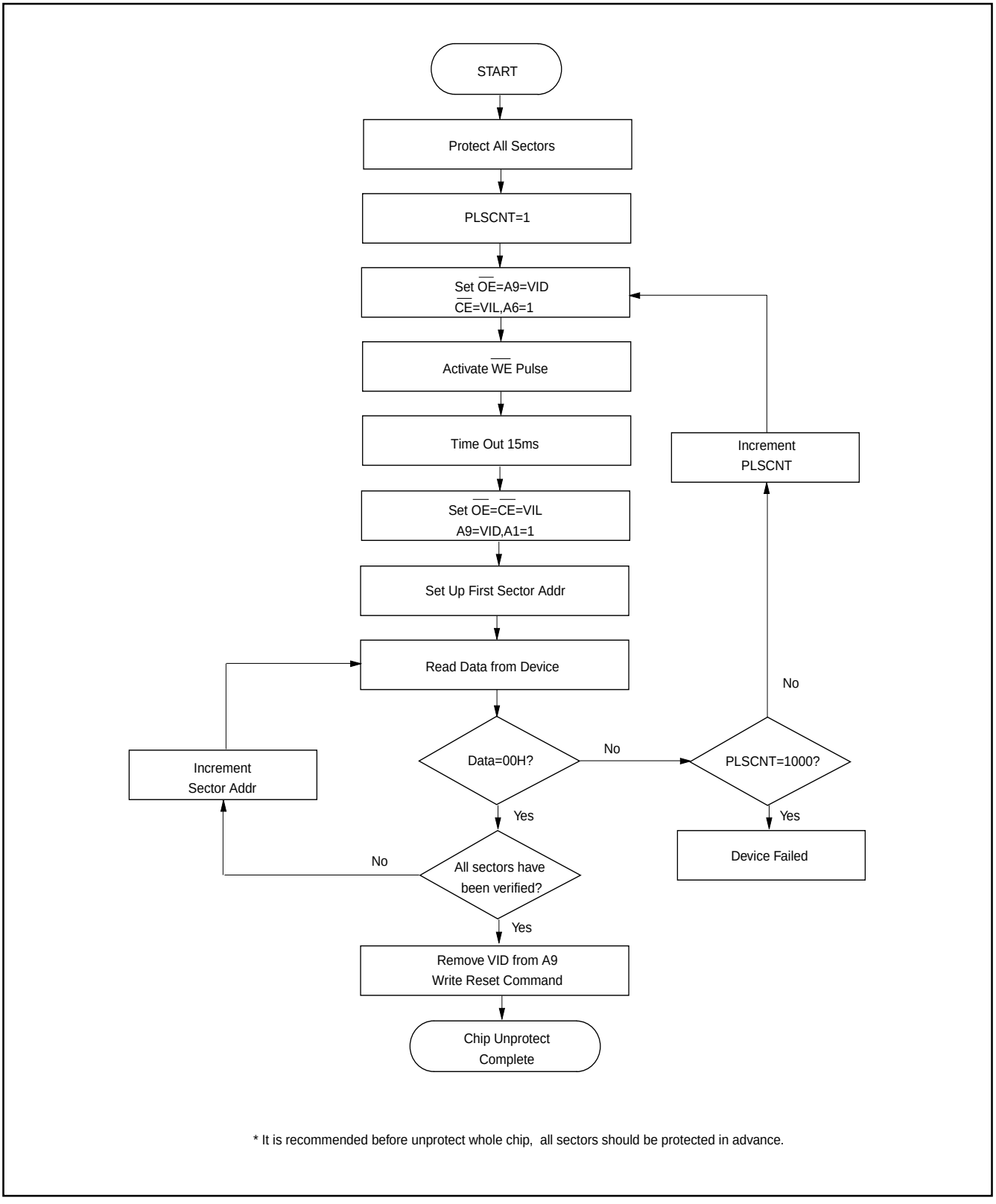


Fig 17. CHIP UNPROTECT FLOWCHART (A9, $\overline{OE}$ Control)



* It is recommended before unprotect whole chip, all sectors should be protected in advance.

AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tVIDR	VID Rise and Fall Time (see Note)	Min	500	ns
tRSP	$\overline{\text{RESET}}$ Setup Time for Temporary Sector Unprotect	Min	4	us
tRRB	$\overline{\text{RESET}}$ Hold Time from RY/$\overline{\text{BY}}$ High for Temporary Sector Group Unprotect	Min	4	us

Fig 18. TEMPORARY SECTOR GROUP UNPROTECT WAVEFORMS

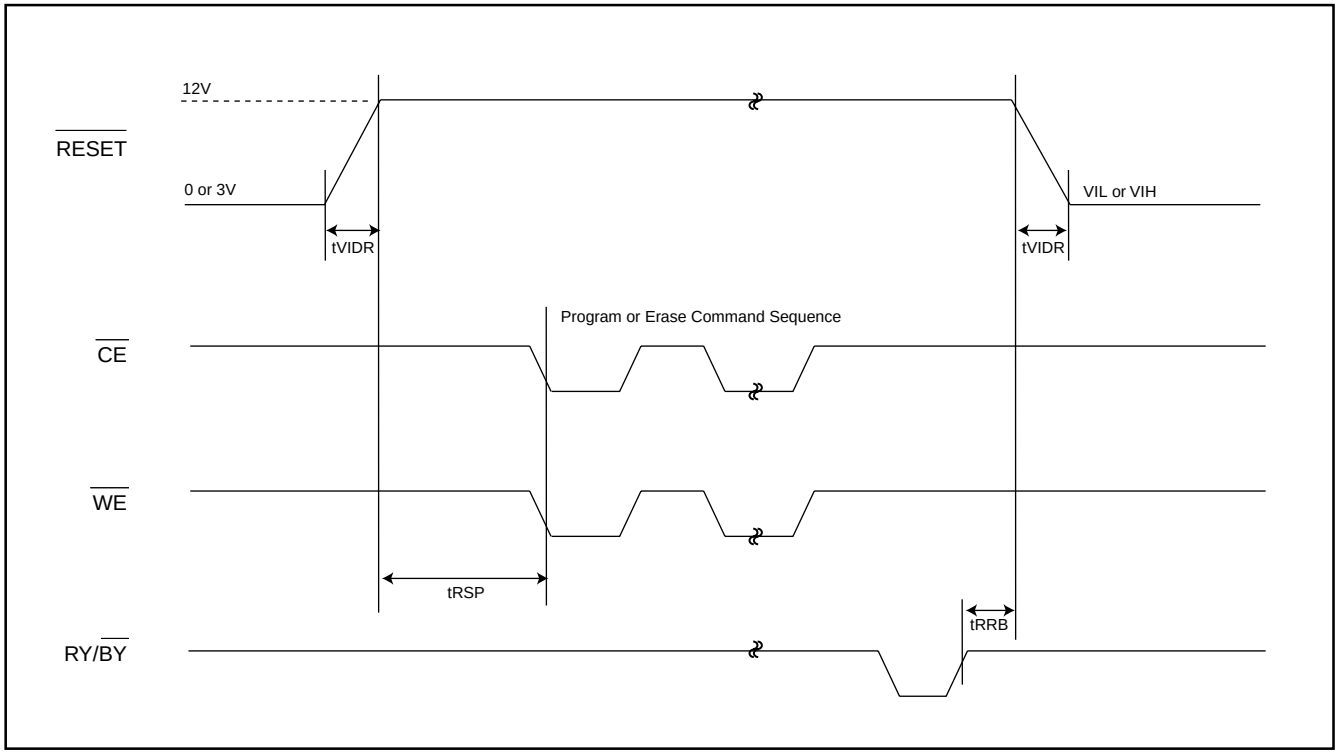
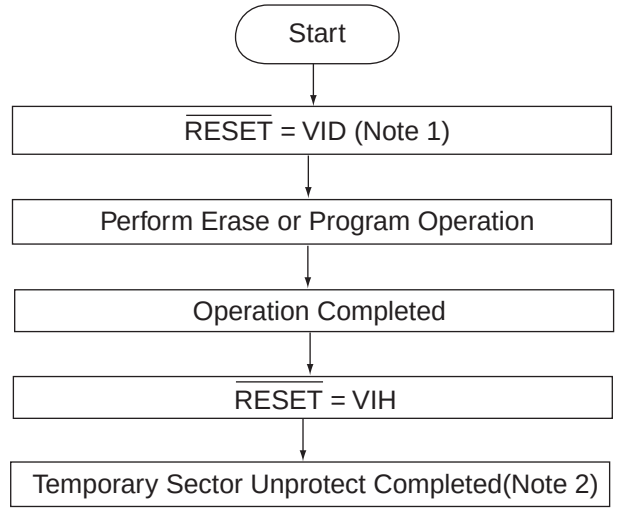


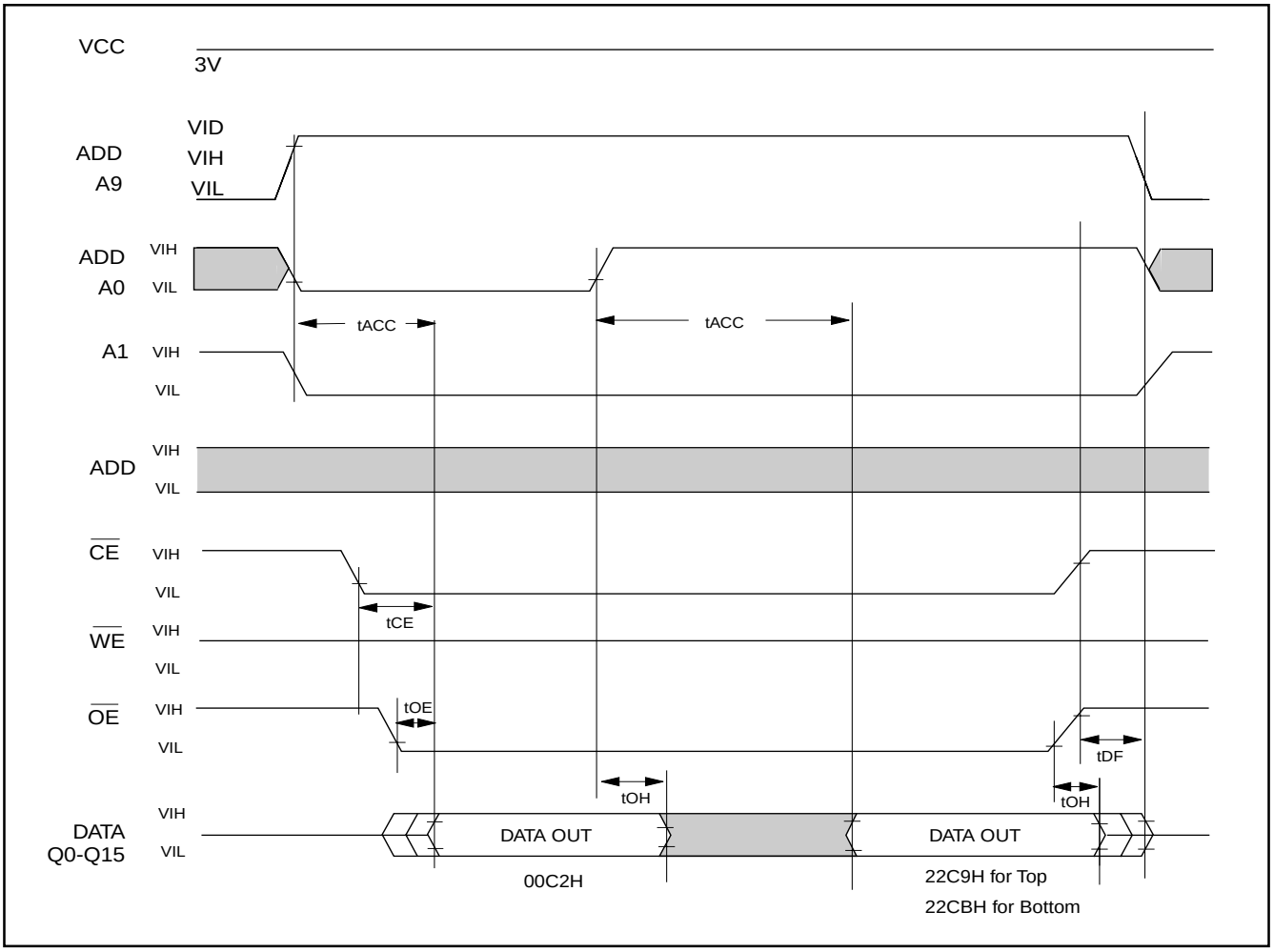
Fig 19. TEMPORARY SECTOR GROUP UNPROTECT FLOWCHART



Note : 1. All protected sectors are temporary unprotected.
VID=11.5V~12.5V

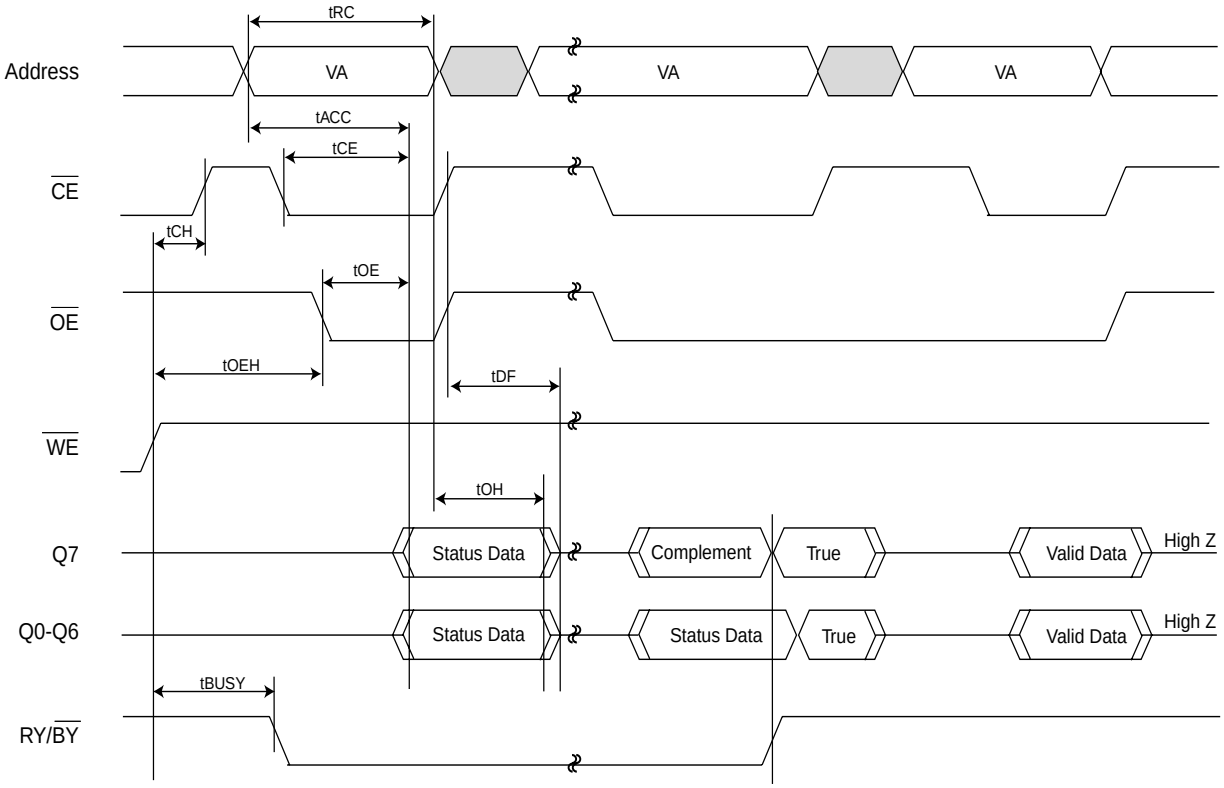
2. All previously protected sectors are protected again.

Fig 20. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

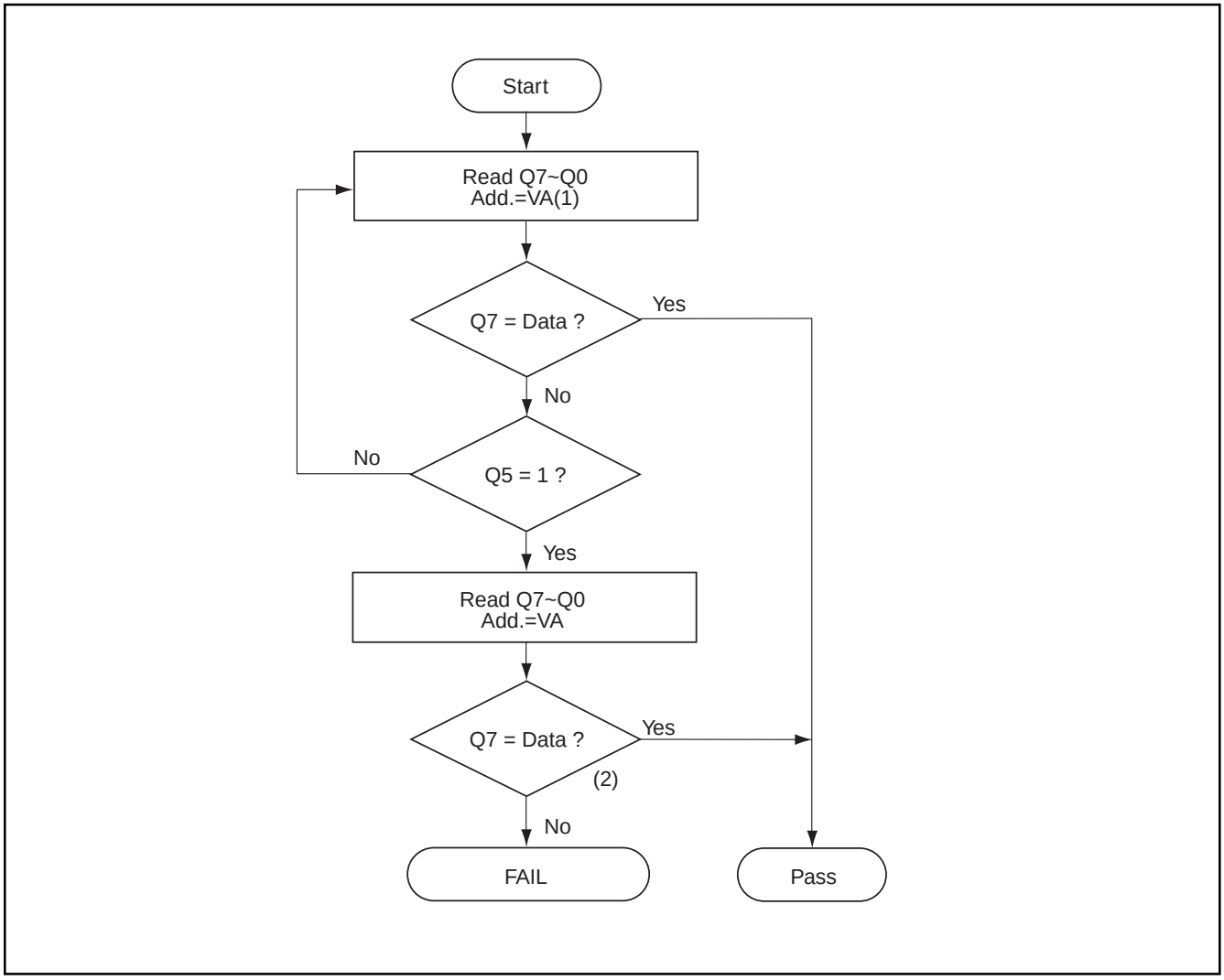
Fig 21. $\overline{\text{DATA}}$ POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



NOTES:

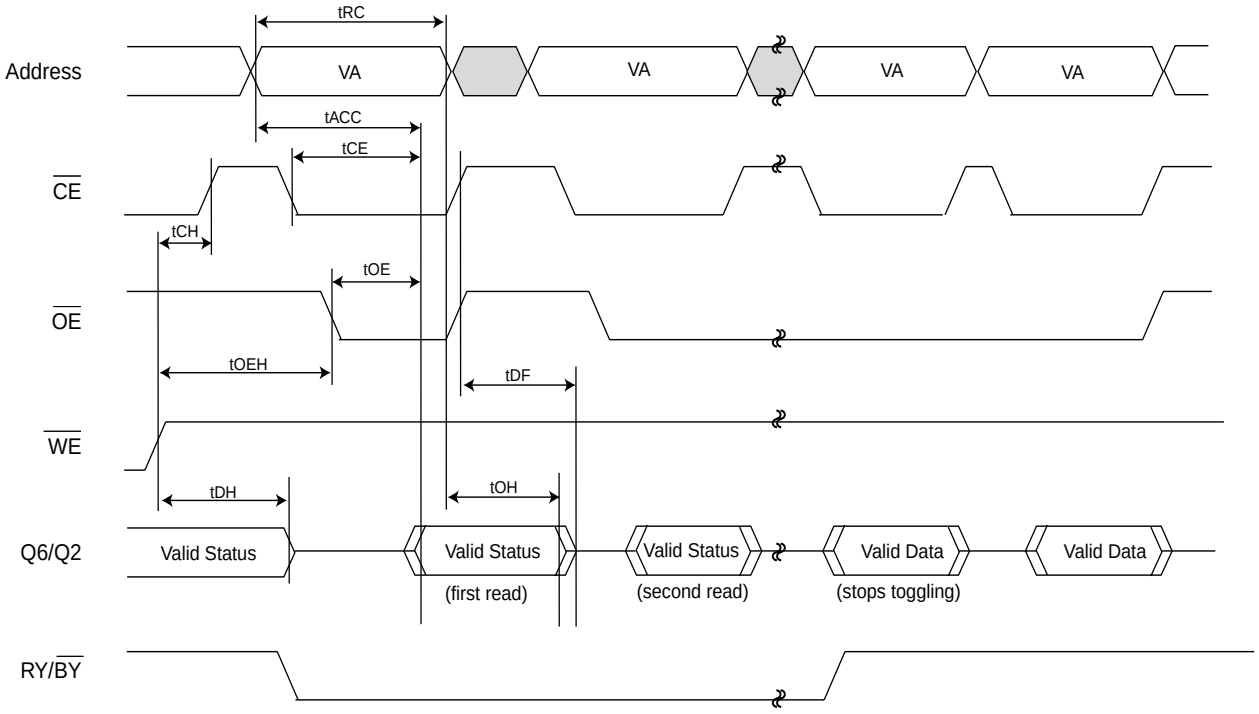
VA=Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data raed cycle.

Fig 22. $\overline{\text{DATA}}$ POLLING ALGORITHM



Notes:
1.VA=valid address for programming.
2.Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

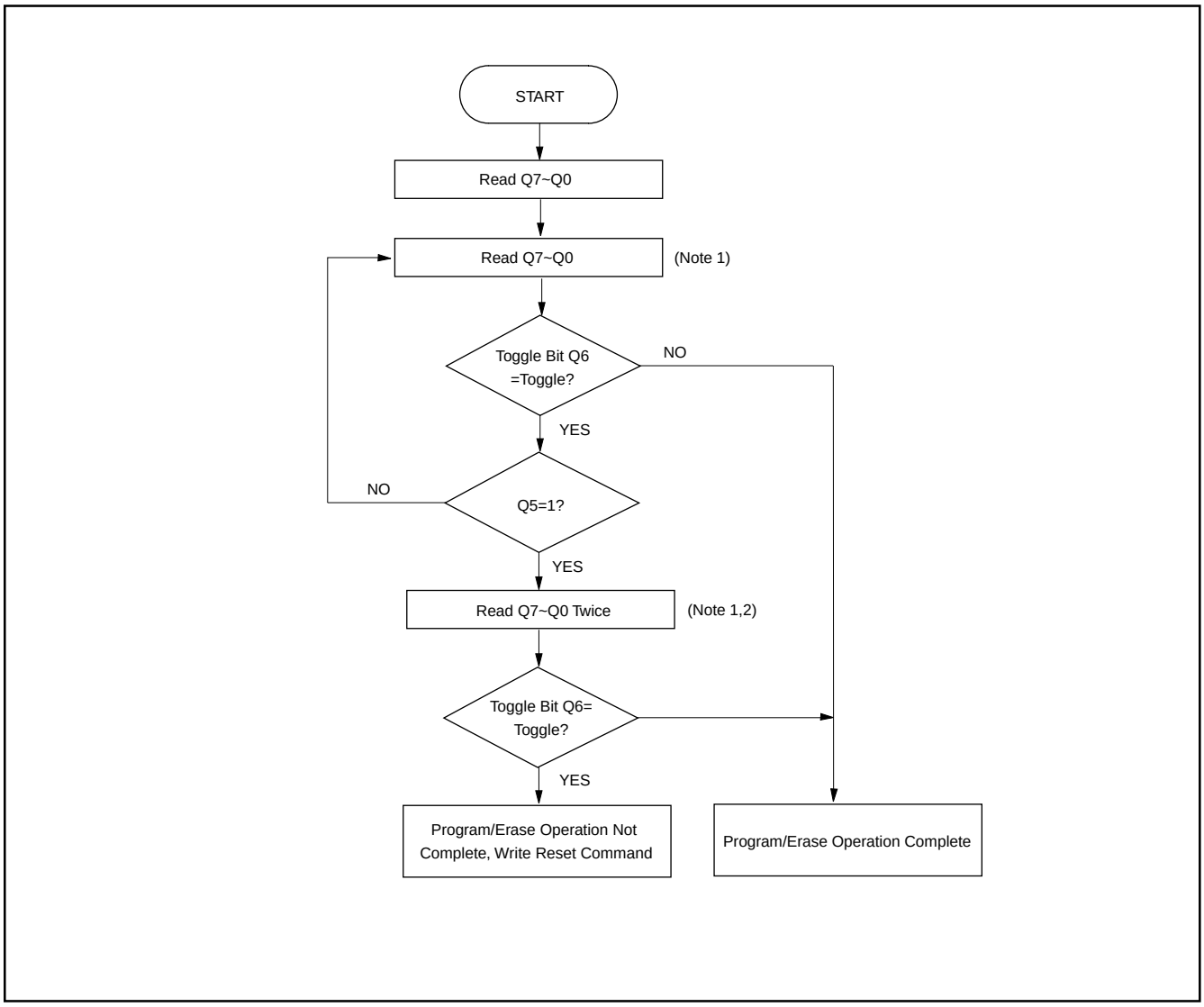
Fig 23. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



NOTES:

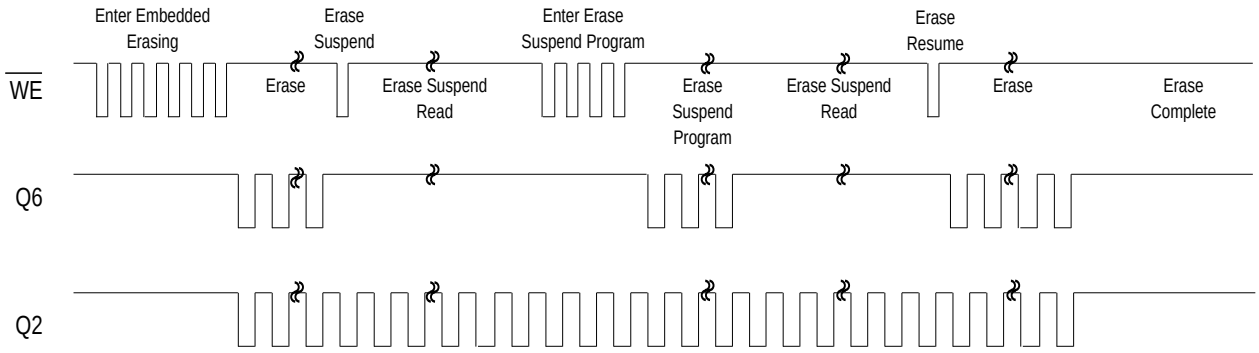
VA=Valid address; not required for Q6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Fig 24. TOGGLE BIT ALGORITHM



Note:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

Fig 25. Q6 versus Q2



NOTES:

The system can use OE or CE to toggle Q2/Q6, Q2 toggles only when read at an address within an erase-suspended

ERASE AND PROGRAMMING PERFORMANCE (1)

PARAMETER		LIMITS MIN.	TYP.(2)	MAX.	UNITS
Sector Erase Time			0.9	15	sec
Chip Erase Time			45	65	sec
Byte Programming Time			9	300	us
Word Programming Time			11	360	us
Chip Programming Time	Byte Mode		50	160	sec
	Word Mode		45	140	sec
Erase/Program Cycles		100,000			Cycles

Note: 1. Not 100% Tested, Excludes external system level over head.
2. Typical program and erase times assume the following condition= 25℃,3.0V VCC. Additionally, programming typicals assume checkerboard pattern.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 3.0V, one pin at a time.		

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN	Input Capacitance	VIN=0	6	7.5	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA=25℃, f=1.0MHz

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150	10	Years
	125	20	Years

ORDERING INFORMATION

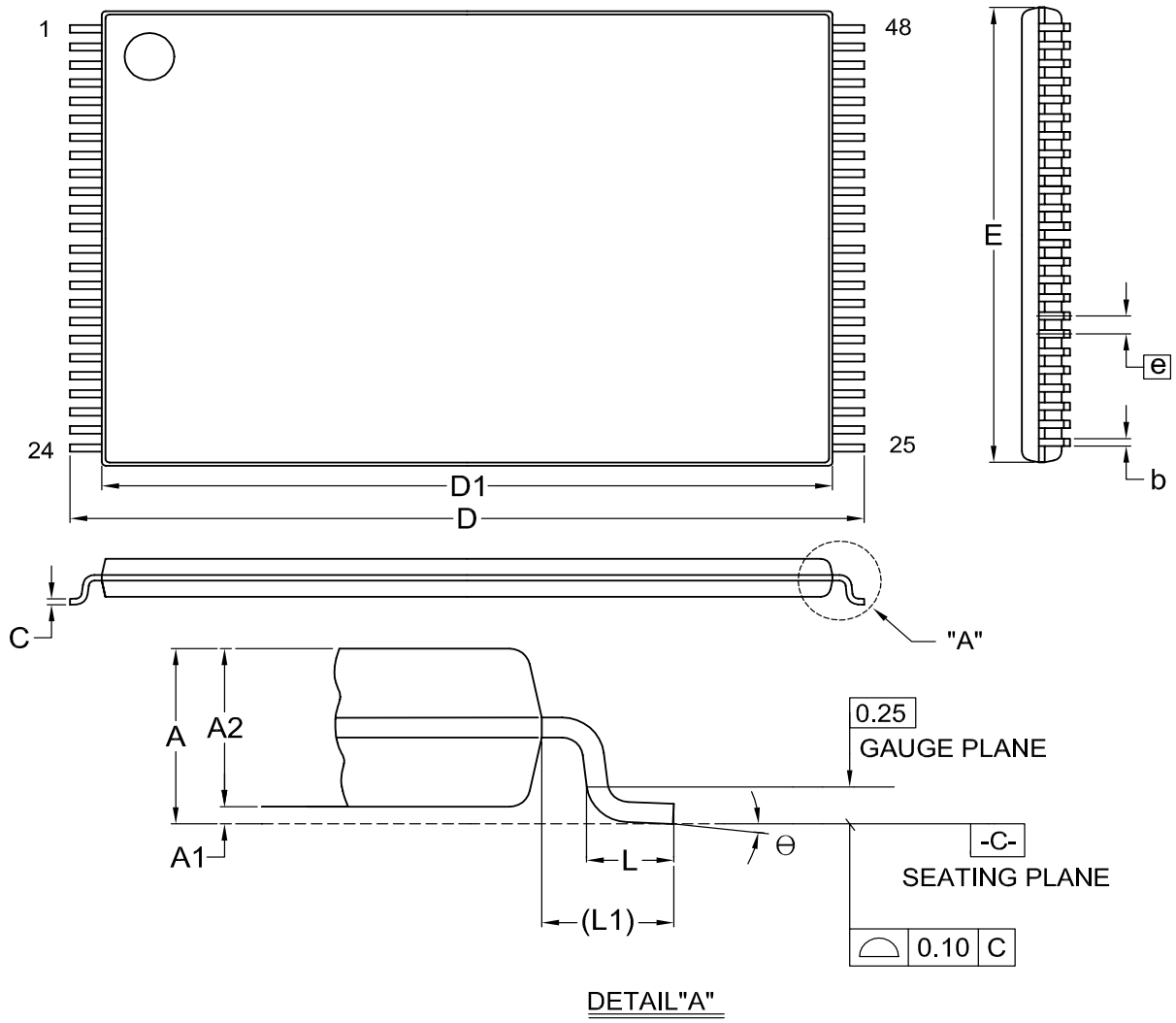
PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	Ball Pitch/ Ball size	PACKAGE	Remark
MX29LV640TTC-90	90		48 Pin TSOP (Normal Type)	
MX29LV640TTC-12	120		48 Pin TSOP (Normal Type)	
MX29LV640BTC-90	90		48 Pin TSOP (Normal Type)	
MX29LV640BTC-12	120		48 Pin TSOP (Normal Type)	
MX29LV640TTI-90	90		48 Pin TSOP (Normal Type)	
MX29LV640TTI-12	120		48 Pin TSOP (Normal Type)	
MX29LV640BTI-90	90		48 Pin TSOP (Normal Type)	
MX29LV640BTI-12	120		48 Pin TSOP (Normal Type)	
MX29LV640TXBC-90	90	0.8mm/0.3mm	63 Ball CSP	
MX29LV640TXBC-12	120	0.8mm/0.3mm	63 Ball CSP	
MX29LV640BXBC-90	90	0.8mm/0.3mm	63 Ball CSP	
MX29LV640BXBC-12	120	0.8mm/0.3mm	63 Ball CSP	
MX29LV640TXBI-90	90	0.8mm/0.3mm	63 Ball CSP	
MX29LV640TXBI-12	120	0.8mm/0.3mm	63 Ball CSP	
MX29LV640BXBI-90	90	0.8mm/0.3mm	63 Ball CSP	
MX29LV640BXBI-12	120	0.8mm/0.3mm	63 Ball CSP	
MX29LV640TXEC-90	90	0.8mm/0.4mm	63 Ball CSP	
MX29LV640TXEC-12	120	0.8mm/0.4mm	63 Ball CSP	
MX29LV640BXEC-90	90	0.8mm/0.4mm	63 Ball CSP	
MX29LV640BXEC-12	120	0.8mm/0.4mm	63 Ball CSP	
MX29LV640TXEI-90	90	0.8mm/0.4mm	63 Ball CSP	
MX29LV640TXEI-12	120	0.8mm/0.4mm	63 Ball CSP	
MX29LV640BXEI-90	90	0.8mm/0.4mm	63 Ball CSP	
MX29LV640BXEI-12	120	0.8mm/0.4mm	63 Ball CSP	
MX29LV640TXCC-90	90	1mm/0.4mm	64 Ball CSP	
MX29LV640TXCC-12	120	1mm/0.4mm	64 Ball CSP	
MX29LV640BXCC-90	90	1mm/0.4mm	64 Ball CSP	
MX29LV640BXCC-12	120	1mm/0.4mm	64 Ball CSP	
MX29LV640TXCI-90	90	1mm/0.4mm	64 Ball CSP	
MX29LV640TXCI-12	120	1mm/0.4mm	64 Ball CSP	
MX29LV640BXCI-90	90	1mm/0.4mm	64 Ball CSP	
MX29LV640BXCI-12	120	1mm/0.4mm	64 Ball CSP	

PART NO.	ACCESS TIME (ns)	Ball Pitch/ Ball size	PACKAGE	Remark
MX29LV640TTC-90G	90		48 Pin TSOP (Normal Type)	PB-free
MX29LV640TTC-12G	120		48 Pin TSOP (Normal Type)	PB-free
MX29LV640BTC-90G	90		48 Pin TSOP (Normal Type)	PB-free
MX29LV640BTC-12G	120		48 Pin TSOP (Normal Type)	PB-free
MX29LV640TTI-90G	90		48 Pin TSOP (Normal Type)	PB-free
MX29LV640TTI-12G	120		48 Pin TSOP (Normal Type)	PB-free
MX29LV640BTI-90G	90		48 Pin TSOP (Normal Type)	PB-free
MX29LV640BTI-12G	120		48 Pin TSOP (Normal Type)	PB-free

PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM



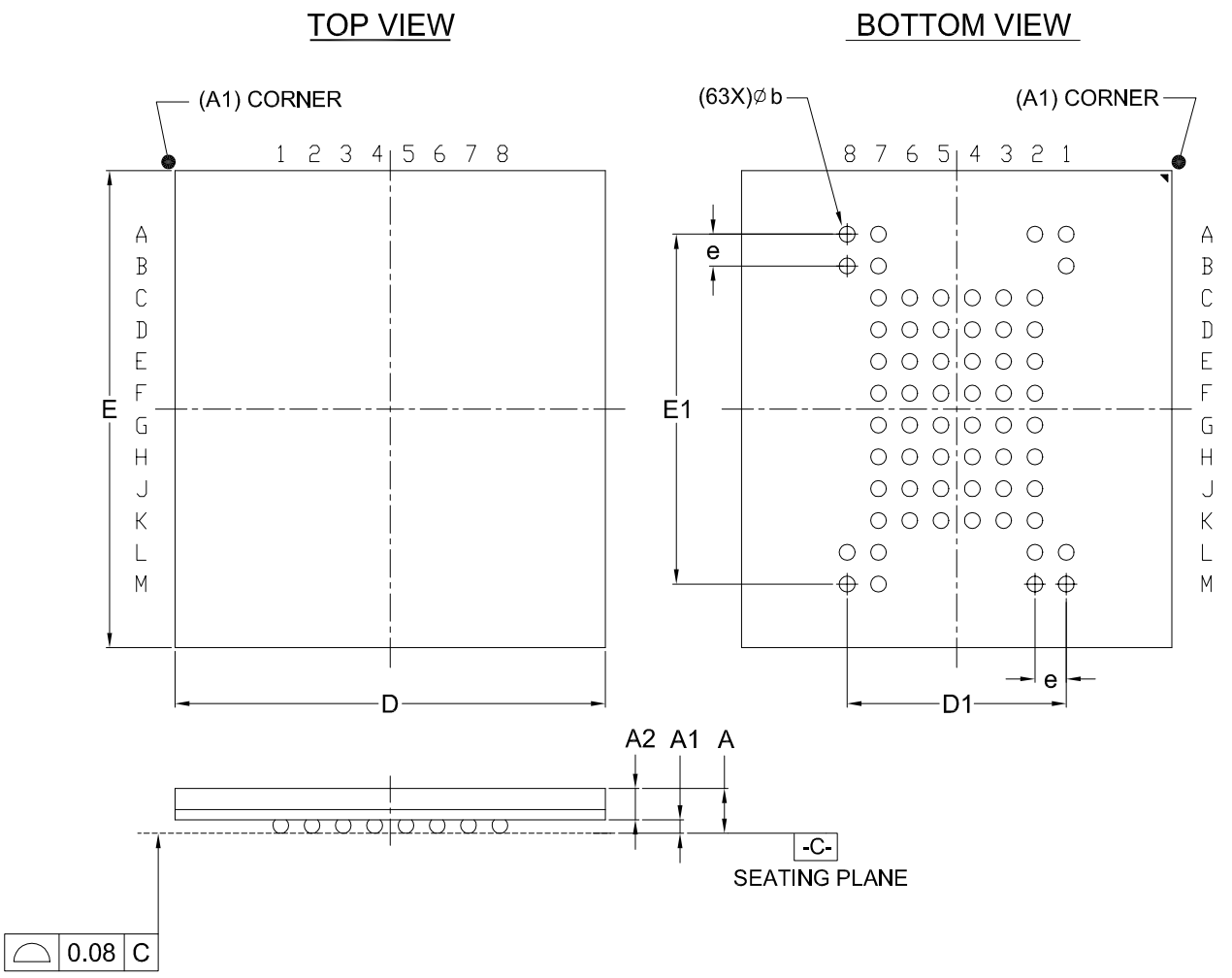
DETAIL"A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	6	MO-142			09-24-'02

Title: **Package Outline for CSP 63BALL(11X12X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.3MM)**

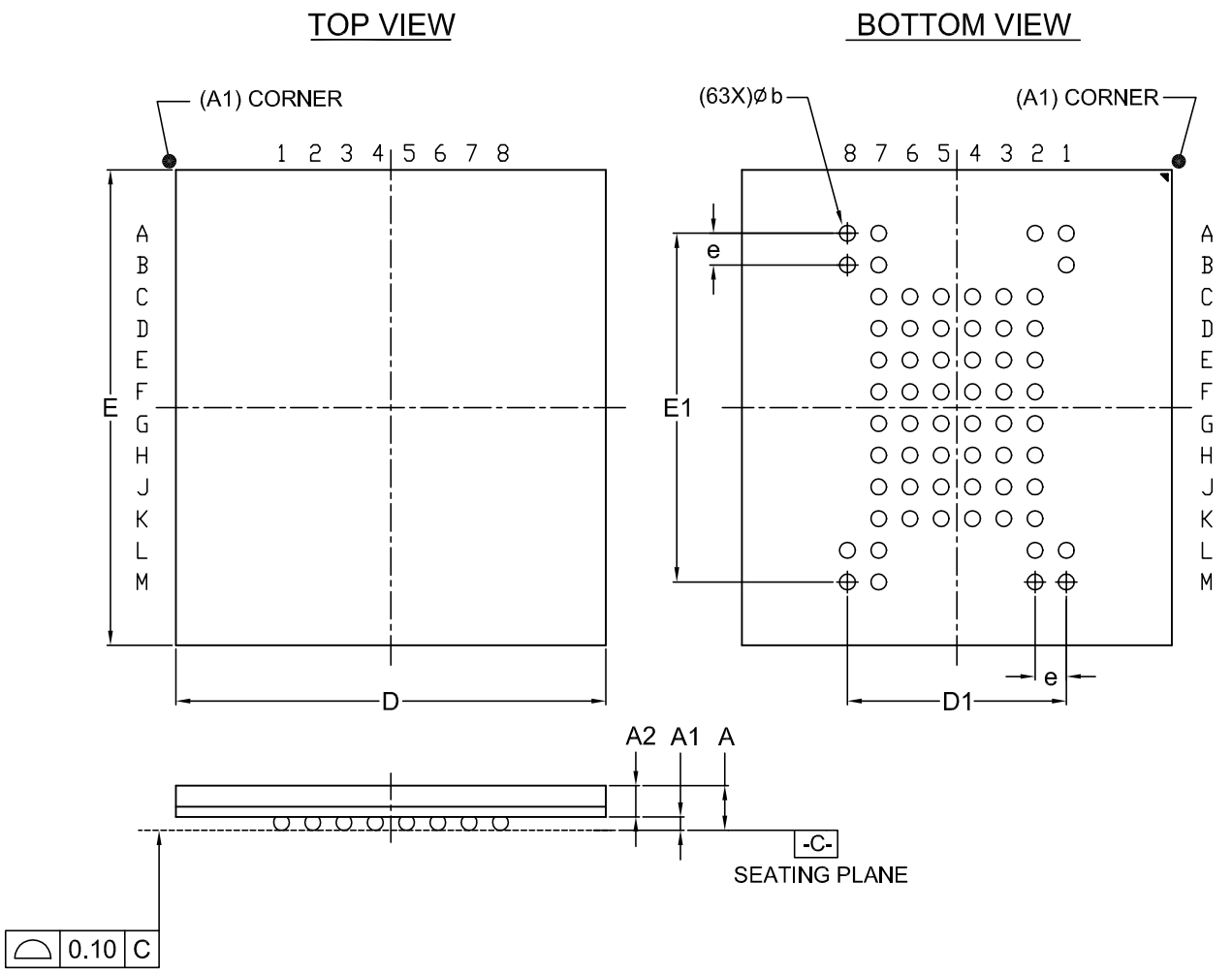


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.18	0.65	0.27	10.90		11.90		
	Nom.	---	0.23	---	0.30	11.00	5.60	12.00	8.80	0.80
	Max.	1.20	0.28	---	0.37	11.10		12.10		
Inch	Min.	---	0.007	0.026	0.011	0.429		0.469		
	Nom.	---	0.009	---	0.012	0.433	0.220	0.472	0.346	0.031
	Max.	0.047	0.011	---	0.015	0.437		0.476		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4226	3	MO-210			11-08-'02

Title: **Package Outline for CSP 63BALL(11X12X1.3MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)**

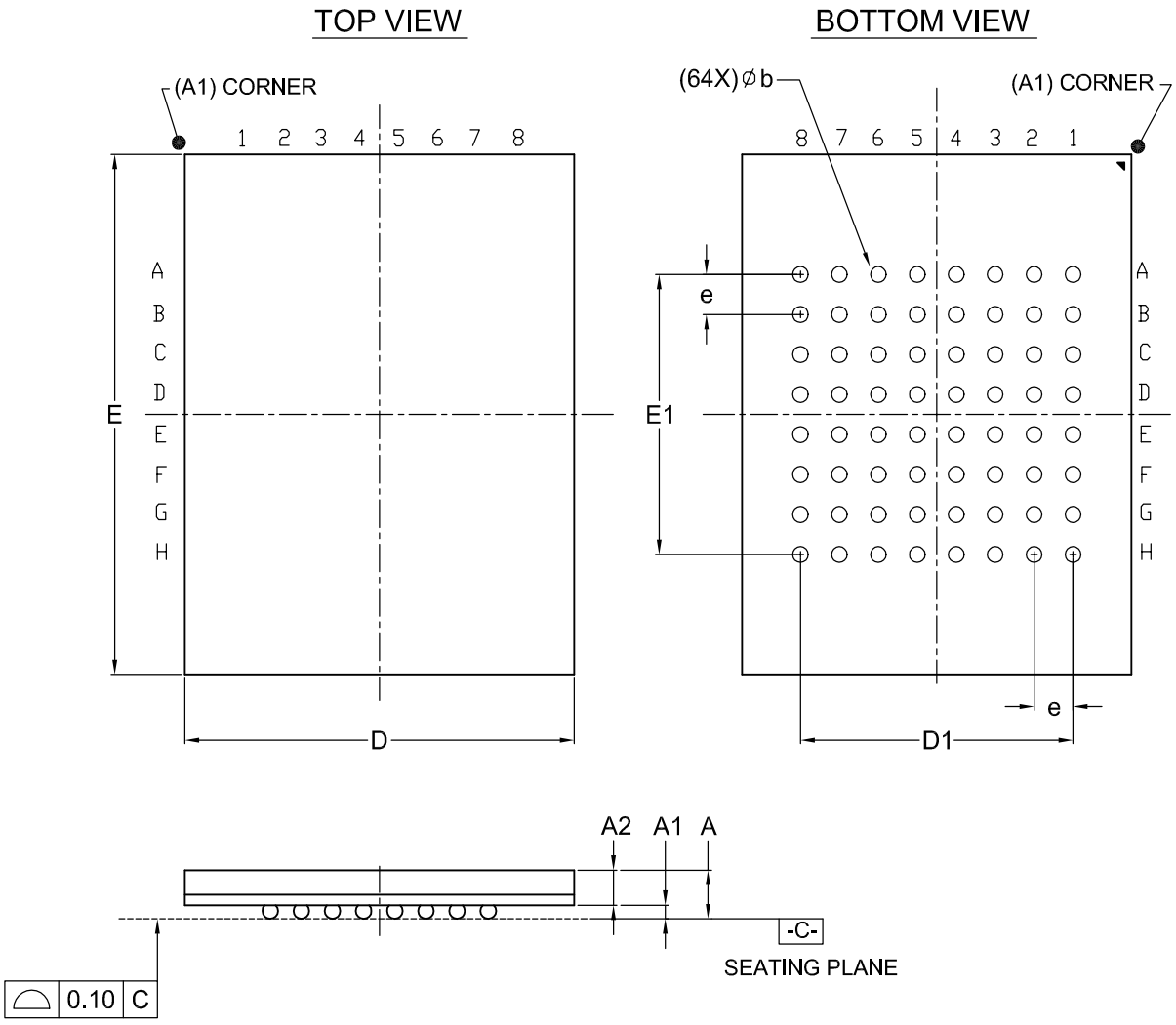


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	10.90		11.90		
	Nom.	---	0.30	---	0.40	11.00	5.60	12.00	8.80	0.80
	Max.	1.30	0.35	---	0.45	11.10		12.10		
Inch	Min.	---	0.010	0.026	0.014	0.429		0.469		
	Nom.	---	0.012	---	0.016	0.433	0.220	0.472	0.346	0.031
	Max.	0.051	0.014	---	0.018	0.437		0.476		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4235	0	MO-219			06-19-'03

Title: **Package Outline for CSP 64BALL(10X13X1.2MM,BALL PITCH 1.00MM,BALL DIAMETER 0.4MM)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	9.90		12.90		
	Nom.	---	0.30	---	0.40	10.00	7.00	13.00	7.00	1.00
	Max.	1.20	0.35	---	0.45	10.10		13.10		
Inch	Min.	---	0.010	0.026	0.014	0.390		0.508		
	Nom.	---	0.012	---	0.016	0.394	0.276	0.512	0.276	0.039
	Max.	0.047	0.014	---	0.018	0.398		0.516		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4220	2	MO-216			09-24-'02

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. To modified the max. ICC current from 5uA to 15uA	P33	JUL/22/2003
	2. To added 63CSP with 0.4mm ball size package information	P63,66	
1.1	1. To corrected CFI code in table 4-3 device geometry data values	P27	OCT/28/2003
	2. To added pb-free part no. for 48-TSOP package	P64	
1.2	1. Removed "Preliminary" from title	P1	NOV/05/2003

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