



Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

General Description

The MAX4130–MAX4134 family of operational amplifiers combines 10MHz gain-bandwidth product and excellent DC accuracy with Rail-to-Rail® operation at the inputs and outputs. These devices require only 900µA per amplifier, and operate from either a single supply (+2.7V to +6.5V) or dual supplies ($\pm 1.35V$ to $\pm 3.25V$) with a common-mode voltage range that extends 250mV beyond V_{EE} and V_{CC} . They are capable of driving 250Ω loads and are unity-gain stable. In addition, the MAX4131/ MAX4133 feature a shutdown mode in which the outputs are placed in a high-impedance state and the supply current is reduced to only 25µA per amplifier.

With their rail-to-rail input common-mode range and output swing, the MAX4130–MAX4134 are ideal for low-voltage, single-supply operation. Although the minimum operating voltage is specified at 2.7V, the devices typically operate down to 1.8V. In addition, low offset voltage and high speed make them the ideal signal-conditioning stages for precision, low-voltage data-acquisition systems. The MAX4130 is offered in the space-saving 5-pin SOT23 package. The MAX4131 is offered in the ultra-small 6-bump, 1mm x 1.5mm chip-scale package (UCSP™).

Selector Guide

PART	AMPS PER PACKAGE	SHUTDOWN MODE	PIN-PACKAGE
MAX4130	1	—	5 SOT23
MAX4131	1	Yes	6 UCSP, 8 µMAX/SO
MAX4132	2	—	8 µMAX/SO
MAX4133	2	Yes	14 SO
MAX4134	4	—	14 SO

Applications

Battery-Powered Instruments
 Portable Equipment
 Data-Acquisition Systems
 Signal Conditioning
 Low-Power, Low-Voltage Applications

Pin Configurations appear at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.
 UCSP is a trademark of Maxim Integrated Products, Inc.



Features

- ◆ 6-Bump UCSP (MAX4131)
- ◆ +2.7V to +6.5V Single-Supply Operation
- ◆ Rail-to-Rail Input Common-Mode Voltage Range
- ◆ Rail-to-Rail Output Voltage Swing
- ◆ 10MHz Gain-Bandwidth Product
- ◆ 900µA Quiescent Current per Amplifier
- ◆ 25µA Shutdown Function (MAX4131/MAX4133)
- ◆ 200µV Offset Voltage
- ◆ No Phase Reversal for Overdriven Inputs
- ◆ Drive 250Ω Loads
- ◆ Stable with 160pF Capacitive Loads
- ◆ Unity-Gain Stable

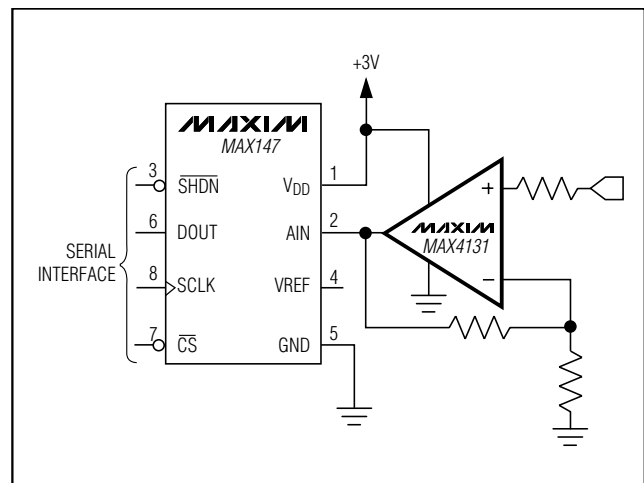
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4130EUK-T	-40°C to +85°C	5 SOT23-5	AABB
MAX4131C/D	0°C to +70°C	Dice*	—
MAX4131EBT-T	-40°C to +85°C	6 UCSP-6	AAX
MAX4131EUA	-40°C to +85°C	8 µMAX	—
MAX4131ESA	-40°C to +85°C	8 SO	—

*Dice are specified at $T_A = +25^\circ\text{C}$. DC parameters only.

Ordering Information continued at end of data sheet.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{CC} - V_{EE}$)	7.5V	8-Pin μ MAX (derate 4.10mW/°C above +70°C)	330mW
$IN+$, $IN-$, \overline{SHDN} Voltage	($V_{CC} + 0.3V$) to ($V_{EE} - 0.3V$)	14-Pin SO (derate 8.00mW/°C above +70°C)	640mW
Output Short-Circuit Duration (Note 1)	Continuous (short to either supply)	Operating Temperature Range	
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)		MAX413_E__	-40°C to +85°C
5-Pin SOT23 (derate 7.1mW/°C above +70°C)	571mW	Maximum Junction Temperature	+150°C
6-Bump UCSP (derate 2.9mW/°C above +70°C)	308mW	Storage Temperature Range	-65°C to +160°C
8-Pin SO (derate 5.88mW/°C above +70°C)	471mW	Lead Temperature (soldering, 10s)	+300°C
		Bump Reflow Temperature	+235°C

Note 1: Provided that the maximum package power-dissipation rating is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_{CM} = V_{EE}$ to V_{CC}	MAX4130EUK	± 0.35	± 1.50	mV
			MAX4131ESA	± 0.20	± 0.60	
			MAX4131EUA/ MAX4131EBT	± 0.35	± 1.20	
			MAX4132ESA/ MAX4133ESD	± 0.25	± 0.75	
			MAX4132EUA	± 0.40	± 1.50	
			MAX4134ESD	± 0.35	± 1.50	
Input Bias Current	I_B	$V_{CM} = V_{EE}$ to V_{CC}		± 50	± 150	nA
Input Offset Current	I_{OS}	$V_{CM} = V_{EE}$ to V_{CC}	MAX4131EBT		± 15	nA
			All other packages		± 12	
Differential Input Voltage	R_{IN}	$-1.5V < V_{DIFF} < 1.5V$		500		k Ω
Common-Mode Input Voltage Range	CMVR		$V_{EE} - 0.25$		$V_{CC} - 0.25$	V
Common-Mode Rejection Ratio	CMRR	$V_{EE} - 0.25V < V_{CM} < V_{CC} + 0.25V$	MAX4130EUK	67	90	dB
			MAX4131ESA	78	98	
			MAX4131EUA/ MAX4131EBT	68	88	
			MAX4132ESA/ MAX4133ESD	74	94	
			MAX4132EUA	66	86	
			MAX4134ESD	64	84	
Power-Supply Rejection Ratio	PSRR	$V_{CC} = 2.7V$ to $6.5V$	78	100		dB
Output Resistance	R_{OUT}	$A_V = 1$		0.1		Ω
Off-Leakage Current	I_{LKG}	$\overline{SHDN} < 0.8V$, $V_{OUT} = 0V$ to V_{CC}		± 0.1	± 1	μA

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Large-Signal Voltage Gain	A_v	$V_{CC} = 2.7V$	$V_{OUT} = 0.25V$ to $2.45V$, $R_L = 100k\Omega$	92	108		dB
			$V_{OUT} = 0.4V$ to $2.3V$, $R_L = 250\Omega$	72	82		
		$V_{CC} = 5V$	$V_{OUT} = 0.25V$ to $4.75V$, $R_L = 100k\Omega$	94	108		
			$V_{OUT} = 0.4V$ to $4.6V$, $R_L = 250\Omega$	75	86		
Output Voltage Swing	V_O	MAX4130/ MAX4131	$R_L = 100k\Omega$	$V_{CC} - V_{OH}$	12	20	mV
				$V_{OL} - V_{EE}$	20	35	
			$R_L = 250\Omega$	$V_{CC} - V_{OH}$	240	290	
				$V_{OL} - V_{EE}$	125	170	
		MAX4132/ MAX4133/ MAX4134	$R_L = 100k\Omega$	$V_{CC} - V_{OH}$	15	30	
				$V_{OL} - V_{EE}$	25	40	
			$R_L = 250\Omega$	$V_{CC} - V_{OH}$	280	330	
				$V_{OL} - V_{EE}$	180	230	
Output Short-Circuit Current	I_{SC}			50			mA
\overline{SHDN} Logic Threshold	V_{IL}	MAX4131-MAX4134	Low			0.8	V
	V_{IH}		High	2.0			
\overline{SHDN} Input Current	I_{IL}	MAX4131-MAX4134		± 1	± 3		μA
Operating Supply Voltage Range	V_{CC}			2.7		6.5	V
Supply Current per Amplifier	I_{CC}	$V_{CM} = V_{OUT} = V_{CC}/2$	$V_{CC} = 2.7V$	900	1050		μA
			$V_{CC} = 5V$	1000	1150		
Shutdown Supply Current per Amplifier	$I_{\overline{SHDN}}$	$\overline{SHDN} > 0.8V$, MAX4131-MAX4134	$V_{CC} = 2.7V$	25	40		μA
			$V_{CC} = 5V$	40	60		

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_{CM} = V_{EE}$ to V_{CC}	MAX4130EUK			± 3.50	mV
			MAX4131ESA			± 0.75	
			MAX4131EUA/MAX4131EBT			± 4.40	
			MAX4132ESA/MAX4133ESD			± 0.95	
			MAX4132EUA			± 4.70	
			MAX4134ESD			± 4.00	
Input Offset Voltage Tempco	TCV_{OS}				± 2		$\mu V/^\circ C$
Input Bias Current	I_B	$V_{CM} = V_{EE}$ to V_{CC}				± 160	nA

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DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Current	I_{OS}	$V_{CM} = V_{EE}$ to V_{CC}	MAX4131EBT			± 24	nA
			All other packages			± 18	
Common-Mode Input Voltage Range	CMVR			$V_{EE} - 0.20$		$V_{CC} - 0.20$	V
Common-Mode Rejection Ratio	CMRR	$V_{EE} - 0.2V < V_{CM} < V_{CC} + 0.2V$	MAX4130EUK	62			dB
			MAX4131ESA	76			
			MAX4131EUA/MAX4131EBT	60			
			MAX4132ESA/MAX4133ESD	74			
			MAX4132EUA	58			
MAX4134ESD	60						
Power-Supply Rejection Ratio	PSRR	$V_{CC} = 2.7V$ to $6.5V$		74			dB
Off-Leakage Current	I_{LKG}	$\overline{SHDN} < 0.8V$, $V_{OUT} = 0V$ to V_{CC}				± 12	μA
Large-Signal Voltage Gain	A_V	$V_{CC} = 2.7V$	$V_{OUT} = 0.25V$ to $2.45V$, $R_L = 100k\Omega$	84			dB
			$V_{OUT} = 0.4V$ to $2.3V$, $R_L = 250\Omega$	66			
		$V_{CC} = 5V$	$V_{OUT} = 0.25V$ to $4.75V$, $R_L = 100k\Omega$	86			
			$V_{OUT} = 0.4V$ to $4.6V$, $R_L = 250\Omega$	68			
Output Voltage Swing	V_O	MAX4130/ MAX4131ESA/ MAX4131EUA	$R_L = 100k\Omega$	$V_{CC} - V_{OH}$		25	mV
				$V_{OL} - V_{EE}$		40	
			$R_L = 250\Omega$	$V_{CC} - V_{OH}$		300	
				$V_{OL} - V_{EE}$		190	
		MAX4131EBT	$R_L = 100k\Omega$	$V_{CC} - V_{OH}$		25	
				$V_{OL} - V_{EE}$		40	
			$R_L = 250\Omega$	$V_{CC} - V_{OH}$		350	
				$V_{OL} - V_{EE}$		190	
		MAX4132/ MAX4133/ MAX4134	$R_L = 100k\Omega$	$V_{CC} - V_{OH}$		35	
				$V_{OL} - V_{EE}$		50	
$R_L = 250\Omega$	$V_{CC} - V_{OH}$			350			
	$V_{OL} - V_{EE}$			250			

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
\overline{SHDN} Logic Threshold	V_{IL}	MAX4131-MAX4134	Low			0.8	V
	V_{IH}		High	2.0			
\overline{SHDN} Input Current	I_{IL}	MAX4131-MAX4134				± 3	μA
Operating Supply Voltage Range	V_{CC}			2.7		6.5	V
Supply Current per Amplifier	I_{CC}	$V_{CM} = V_{OUT} = V_{CC}/2$	MAX4131EBT	$V_{CC} = 2.7V$		1200	μA
				$V_{CC} = 5V$		1350	
			All other devices	$V_{CC} = 2.7V$		1100	
				$V_{CC} = 5V$		1200	
Shutdown Supply Current per Amplifier	$I_{\overline{SHDN}}$	$\overline{SHDN} > 0.8V$, MAX4131-MAX4134	$V_{CC} = 2.7V$		50	μA	
			$V_{CC} = 5V$		70		

Note 2: All devices are 100% tested at $T_A = +25^\circ C$. MAX4130EUK/MAX4131EBT temperature limits are guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

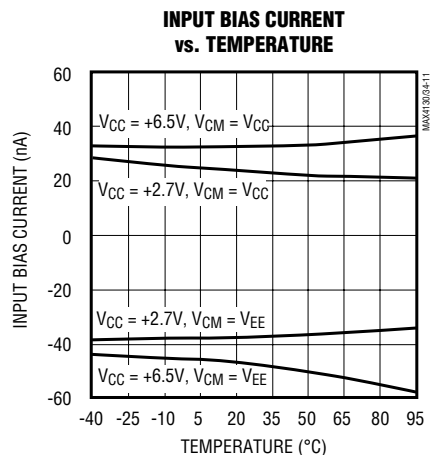
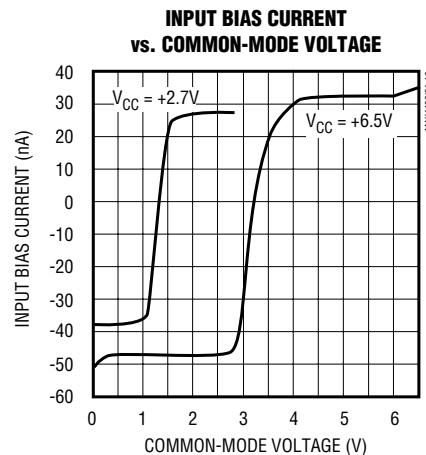
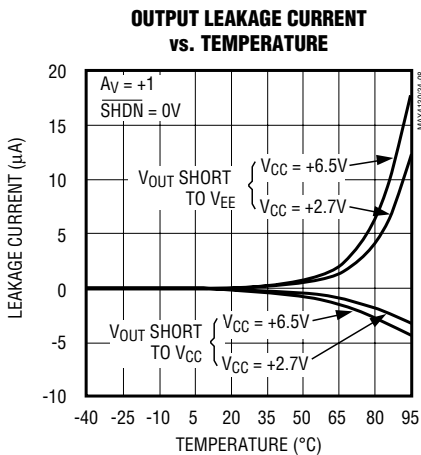
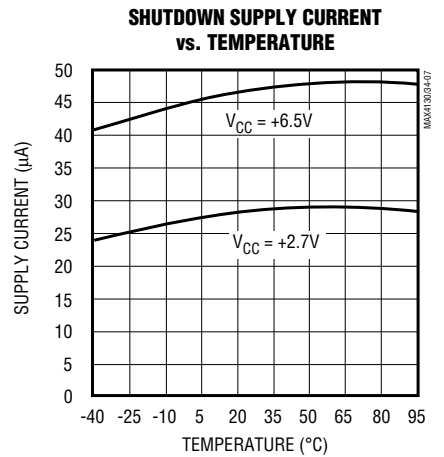
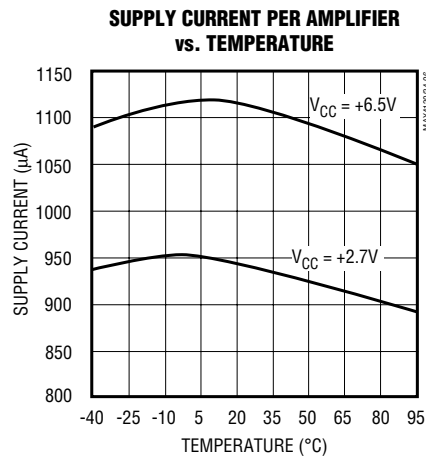
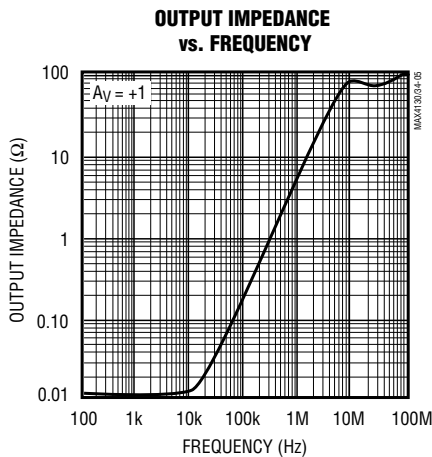
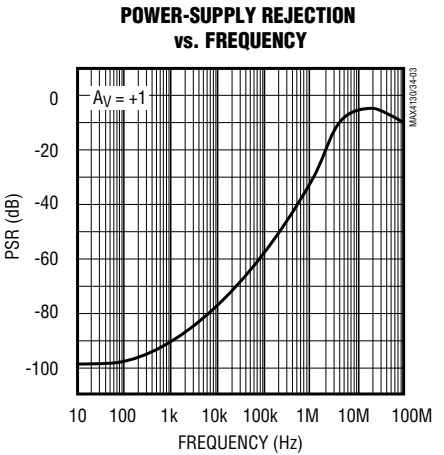
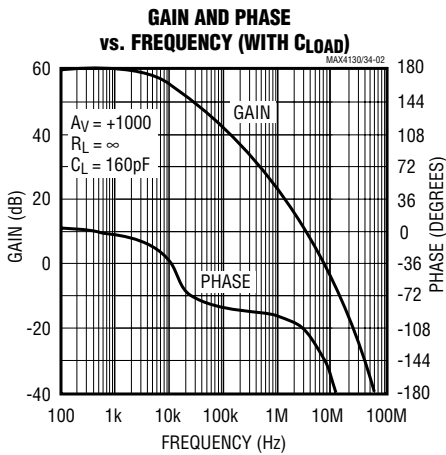
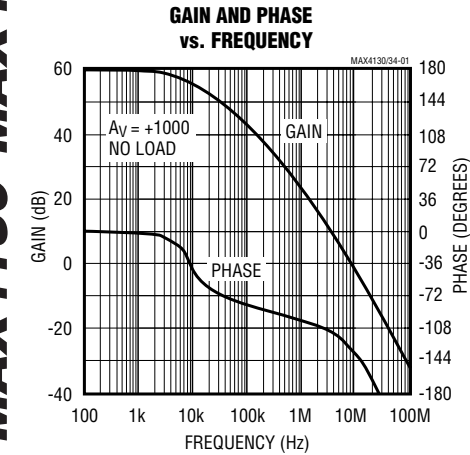
($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $\overline{SHDN} \geq 2V$ (or open), $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP				10		MHz
Phase Margin	θ_M				62		Degrees
Gain Margin	G_M				12		dB
Total Harmonic Distortion	THD	$f = 10kHz$, $V_{OUT} = 2V_{P-P}$ ($A_V = 1$)			0.003		%
Slew Rate	SR				4		V/ μs
Settling Time to 0.01%	t_S	$A_V = 1$, $V_{OUT} = 2V$ step			2.0		μs
Turn-On Time	t_{ON}	$V_{CC} = 0V$ to $3V$ step, $V_{OUT} = V_{CC}/2$			1		μs
\overline{SHDN} Delay		MAX4131-MAX4134, $V_{CC} = 3V$, $V_{OUT} = V_{CC}/2$	Enable		1		μs
			Disable		0.2		
Input Capacitance	C_{IN}				3		pF
Input Noise-Voltage Density	e_n	$f = 1kHz$			22		nV/\sqrt{Hz}
Input Noise-Current Density	i_n	$f = 1kHz$			0.4		pA/\sqrt{Hz}
Capacitive-Load Stability	C_L	$A_V = 1$			160		pF

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Typical Operating Characteristics

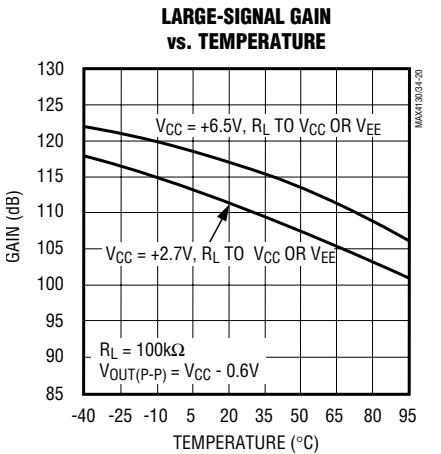
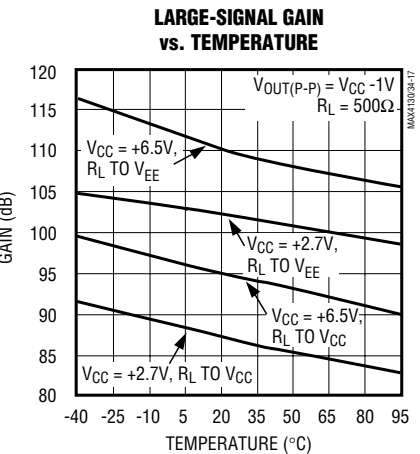
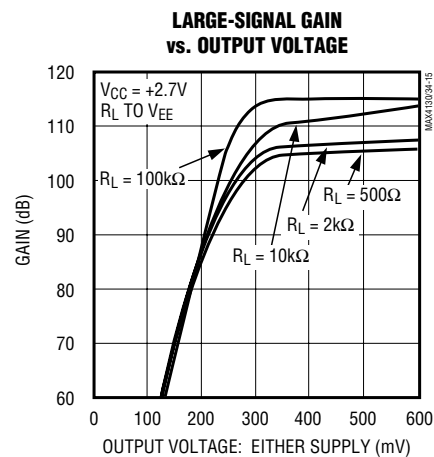
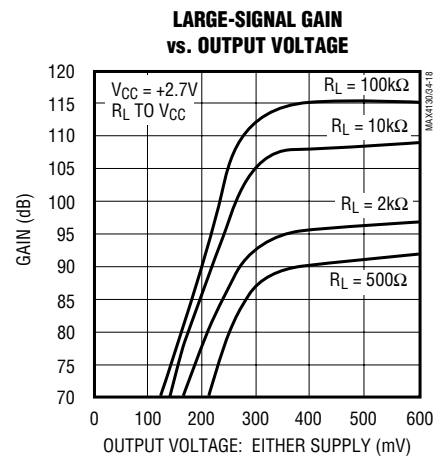
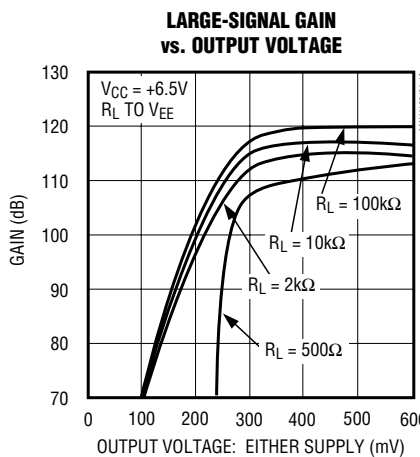
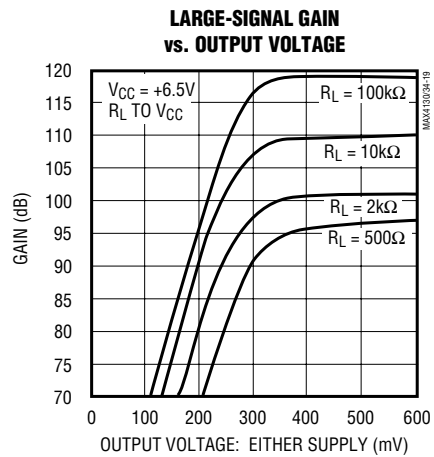
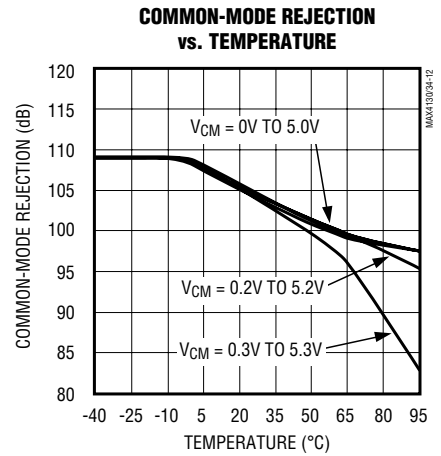
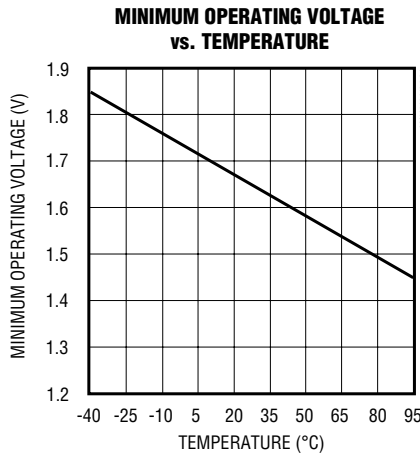
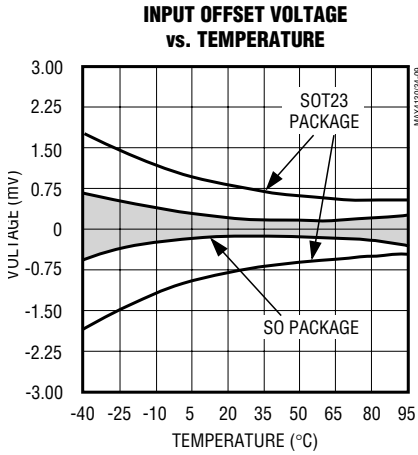
($V_{CC} = +5V$, $V_{EE} = 0V$, $V_{CM} = V_{CC} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)



Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Typical Operating Characteristics (continued)

($V_{CC} = +5V$, $V_{EE} = 0V$, $V_{CM} = V_{CC} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)

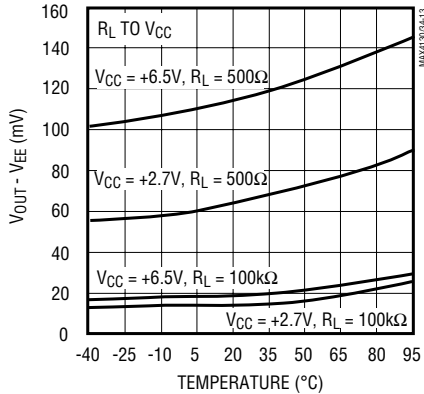


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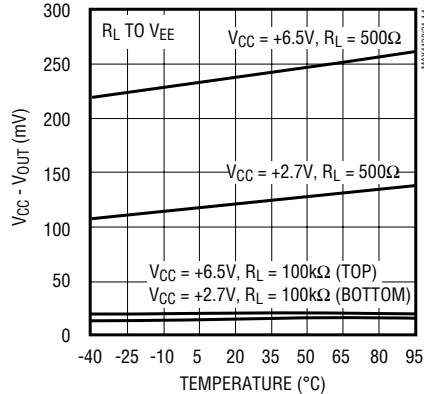
Typical Operating Characteristics (continued)

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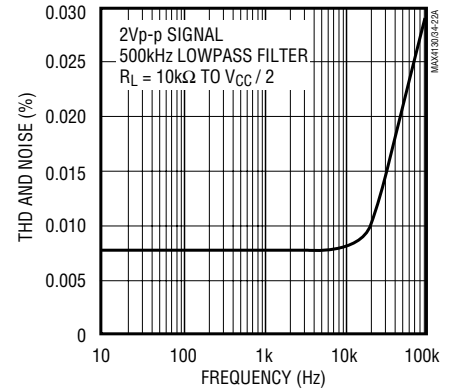
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE



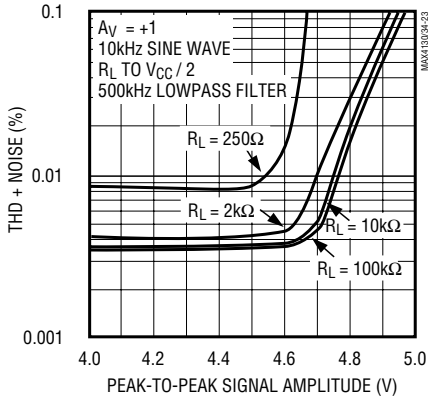
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



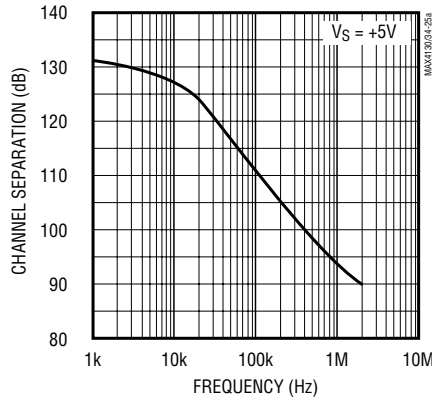
TOTAL HARMONIC DISTORTION AND NOISE vs. FREQUENCY



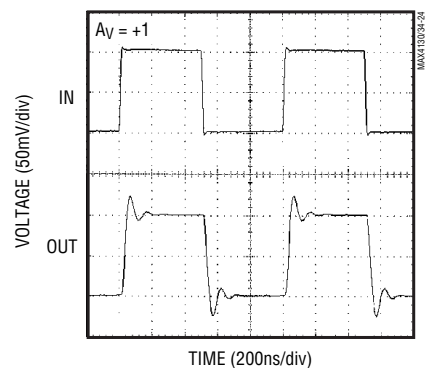
TOTAL HARMONIC DISTORTION AND NOISE vs. PEAK-TO-PEAK SIGNAL AMPLITUDE



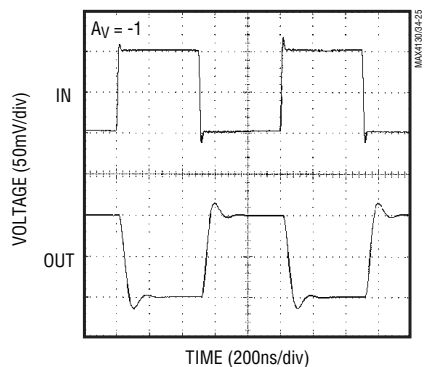
CHANNEL SEPARATION vs. FREQUENCY



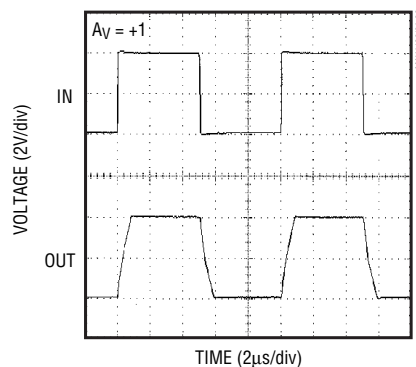
MAX4131 SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



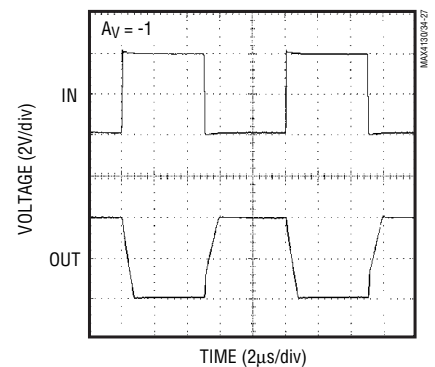
MAX4131 SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



MAX4131 LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



MAX4131 LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



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Pin Description

MAX4130-MAX4134

MAX4130	PIN					NAME	FUNCTION
	SO/ μ MAX	UCSP	MAX4132	MAX4133	MAX4134		
1	6	A2	—	—	—	OUT	Output
2	4	A1	4	4	11	V _{EE}	Negative Supply. Connect to GND for single-supply operation.
3	3	B1	—	—	—	IN+	Noninverting Input
4	2	B2	—	—	—	IN-	Inverting Input
5	7	A3	8	14	4	V _{CC}	Positive Supply
—	1, 5	—	—	5, 7, 8, 10	—	N.C.	No Connection. Not internally connected.
—	8	B3	—	—	—	$\overline{\text{SHDN}}$	Shutdown Control. Connect to V _{CC} or leave floating to enable amplifier.
—	—	—	1, 7	1, 13	1, 7	OUT1, OUT2	Outputs for Amps 1 and 2
—	—	—	2, 6	2, 12	2, 6	IN1-, IN2-	Inverting Inputs for Amps 1 and 2
—	—	—	3, 5	3, 11	3, 5	IN1+, IN2+	Noninverting Inputs for Amps 1 and 2
—	—	—	—	6, 9	—	$\overline{\text{SHDN1}}$, $\overline{\text{SHDN2}}$	Shutdown Control. Provides independent shutdown control for amps 1 and 2. Connect to V _{CC} or leave floating to enable amplifiers.
—	—	—	—	—	8, 14	OUT3, OUT4	Outputs for Amps 3 and 4
—	—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for Amps 3 and 4
—	—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for Amps 3 and 4

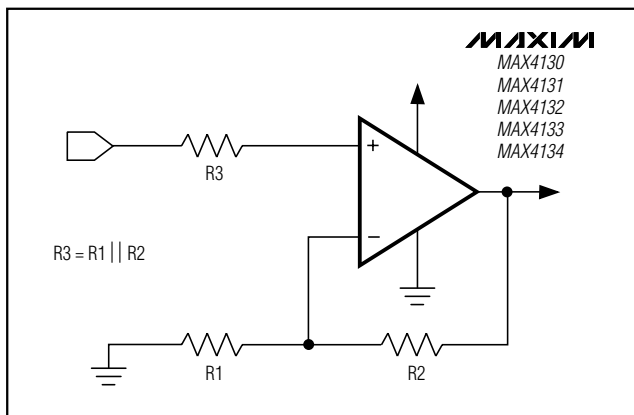


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

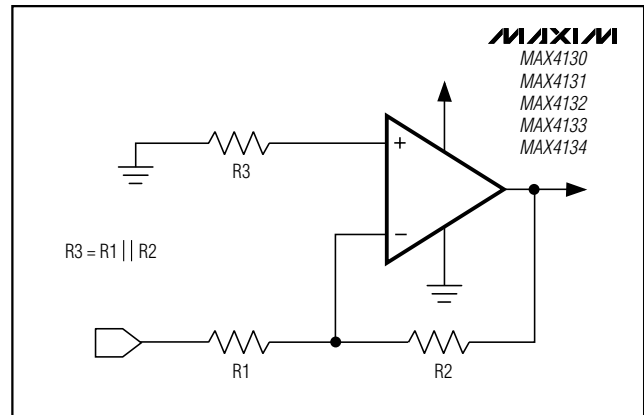


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Applications Information

Rail-to-Rail Input Stage

Devices in the MAX4130–MAX4134 family of high-speed amplifiers have rail-to-rail input and output stages designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages that combine to provide an input common-mode range that extends 0.2V beyond the supply rails. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages near the positive rail. The input offset voltage is typically below 200 μ V. The switchover transition region, which occurs near $V_{CC} / 2$, has been extended to minimize the slight degradation in common-mode rejection ratio caused by the mismatch of the input pairs. Their low offset voltage, high bandwidth, and rail-to-rail common-mode range make these op amps excellent choices for precision, low-voltage data-acquisition systems.

Since the input stage switches between the NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the transition region.

Reduce the offset error caused by input bias currents flowing through external source impedances by matching the effective impedance seen by each input (Figures 1a, 1b). High source impedances, together with input capacitance, can create a parasitic pole that produces an underdamped signal response. Reducing the input impedance or placing a small (2pF to 10pF) capacitor across the feedback resistor improves response.

The MAX4130–MAX4134s' inputs are protected from large differential input voltages by 1k Ω series resistors and back-to-back triple diodes across the inputs (Figure 2). For differential input voltages less than 1.8V, input resistance is typically 500k Ω . For differential input voltages greater than 1.8V, input resistance is approximately 2k Ω . The input bias current is given by the following equation:

$$I_{BIAS} = \frac{V_{DIFF} - 1.8V}{2k\Omega}$$

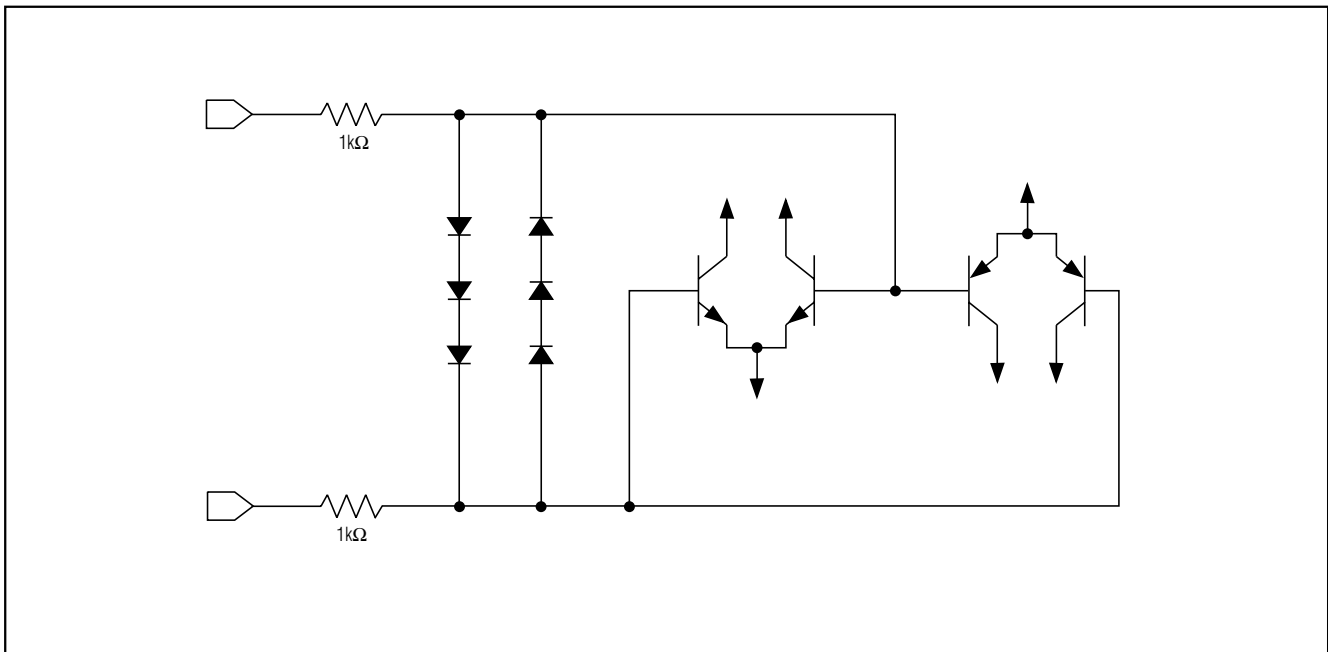


Figure 2. Input Protection Circuit

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Rail-to-Rail Output Stage

The minimum output voltage is within millivolts of ground for single-supply operation where the load is referenced to ground (V_{EE}). Figure 3 shows the input voltage range and output voltage swing of a MAX4131 connected as a voltage follower. With a +3V supply and the load tied to ground, the output swings from 0.00V to 2.90V. The maximum output voltage swing depends on the load, but will be within 150mV of a +3V supply, even with the maximum load (500Ω to ground).

Driving a capacitive load can cause instability in most high-speed op amps, especially those with low quiescent current. The MAX4130-MAX4134 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 160pF. Figure 4 gives the stable operating region for capacitive loads. Figures 5 and 6 show the response with capacitive loads and the results of adding an isolation resistor in series with the output (Figure 7). The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

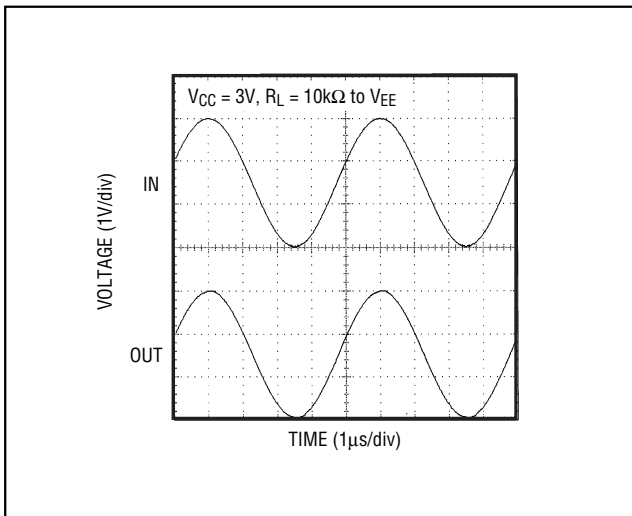


Figure 3. Rail-to-Rail Input/Output Voltage Range

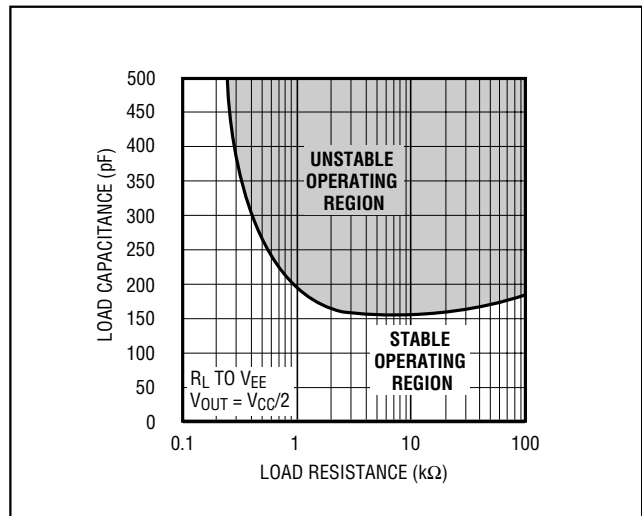


Figure 4. Capacitive-Load Stability

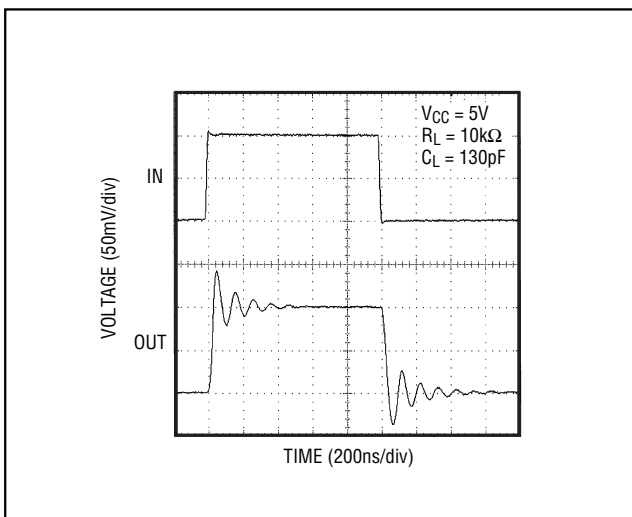


Figure 5. MAX4131 Small-Signal Transient Response with Capacitive Load

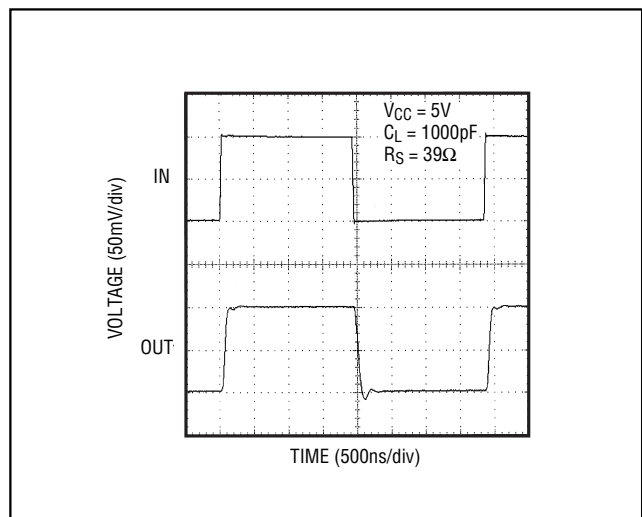


Figure 6. MAX4131 Transient Response to Capacitive Load with Isolation Resistor

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Power-Up and Shutdown Mode

The MAX4130-MAX4134 amplifiers typically settle within 1 μ s after power-up. Figures 9 and 10 show the output voltage and supply current on power-up, using the test circuit of Figure 8.

The MAX4131 and MAX4133 have a shutdown option. When the shutdown pin (SHDN) is pulled low, the supply current drops below 25 μ A per amplifier and the

amplifiers are disabled with the outputs in a high-impedance state. Pulling SHDN high or leaving it floating enables the amplifier. In the dual-amplifier MAX4133, the shutdown functions operate independently. Figures 11 and 12 show the output voltage and supply current responses of the MAX4131 to a shutdown pulse, using the test circuit of Figure 8.

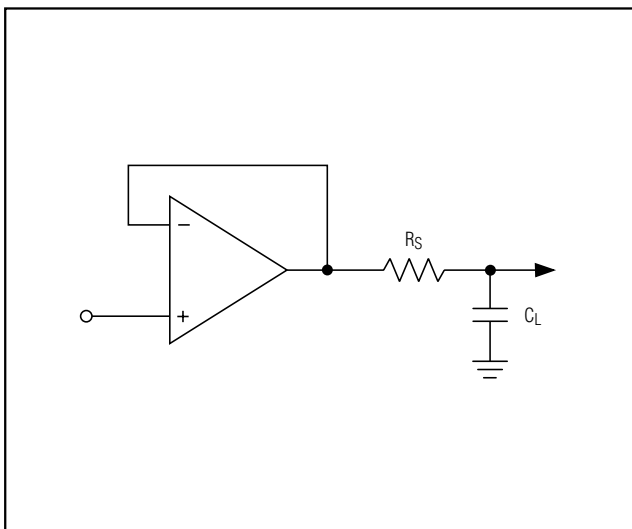


Figure 7. Capacitive-Load Driving Circuit

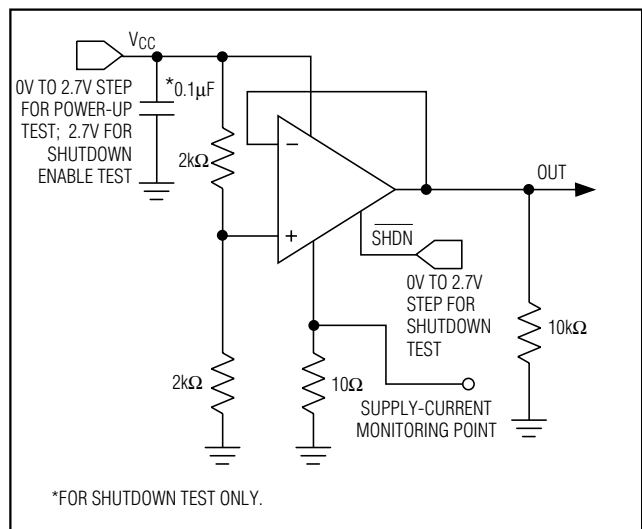


Figure 8. Power-Up/Shutdown Test Circuit

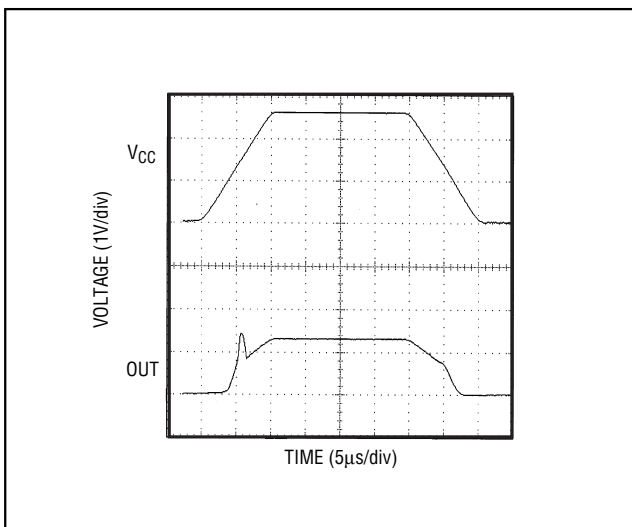


Figure 9. Power-Up Output Voltage

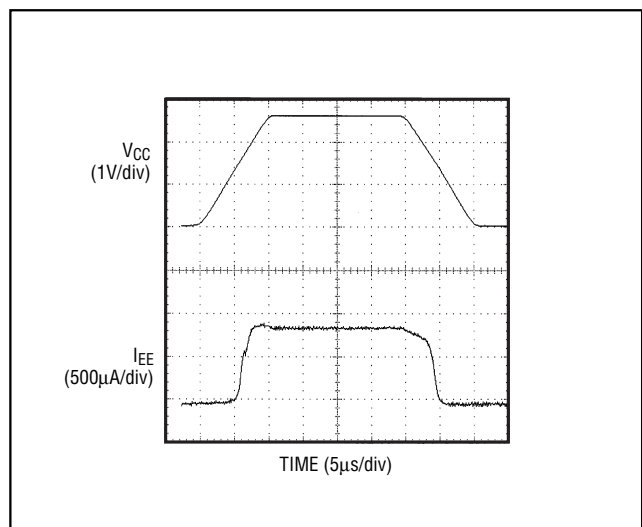


Figure 10. Power-Up Supply Current

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

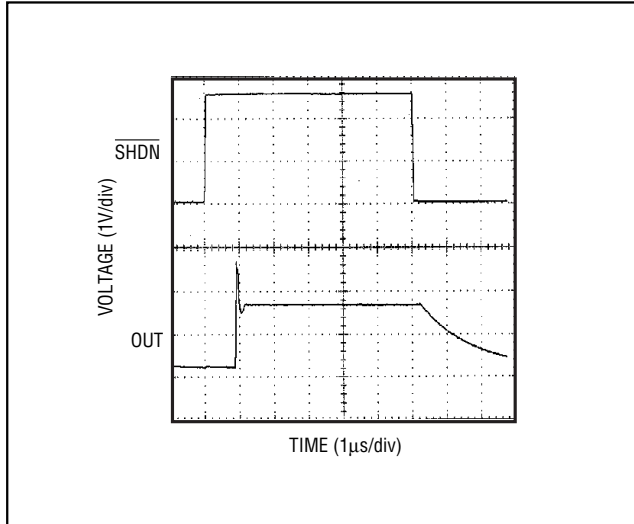


Figure 11. Shutdown Output Voltage

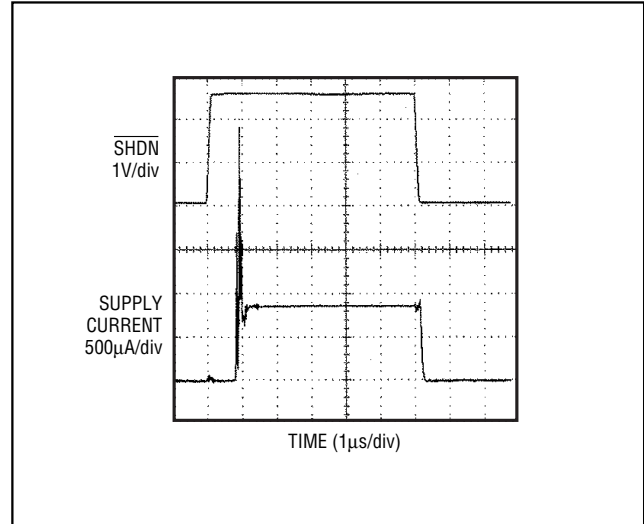


Figure 12. Shutdown Enable/Disable Supply Current

Power Supplies and Layout

The MAX4130–MAX4134 operate from a single +2.7V to +6.5V power supply, or from dual supplies of $\pm 1.35\text{V}$ to $\pm 3.25\text{V}$. For single-supply operation, bypass the power supply with a $0.1\mu\text{F}$ ceramic capacitor in parallel with at least $1\mu\text{F}$. For dual supplies, bypass each supply to ground.

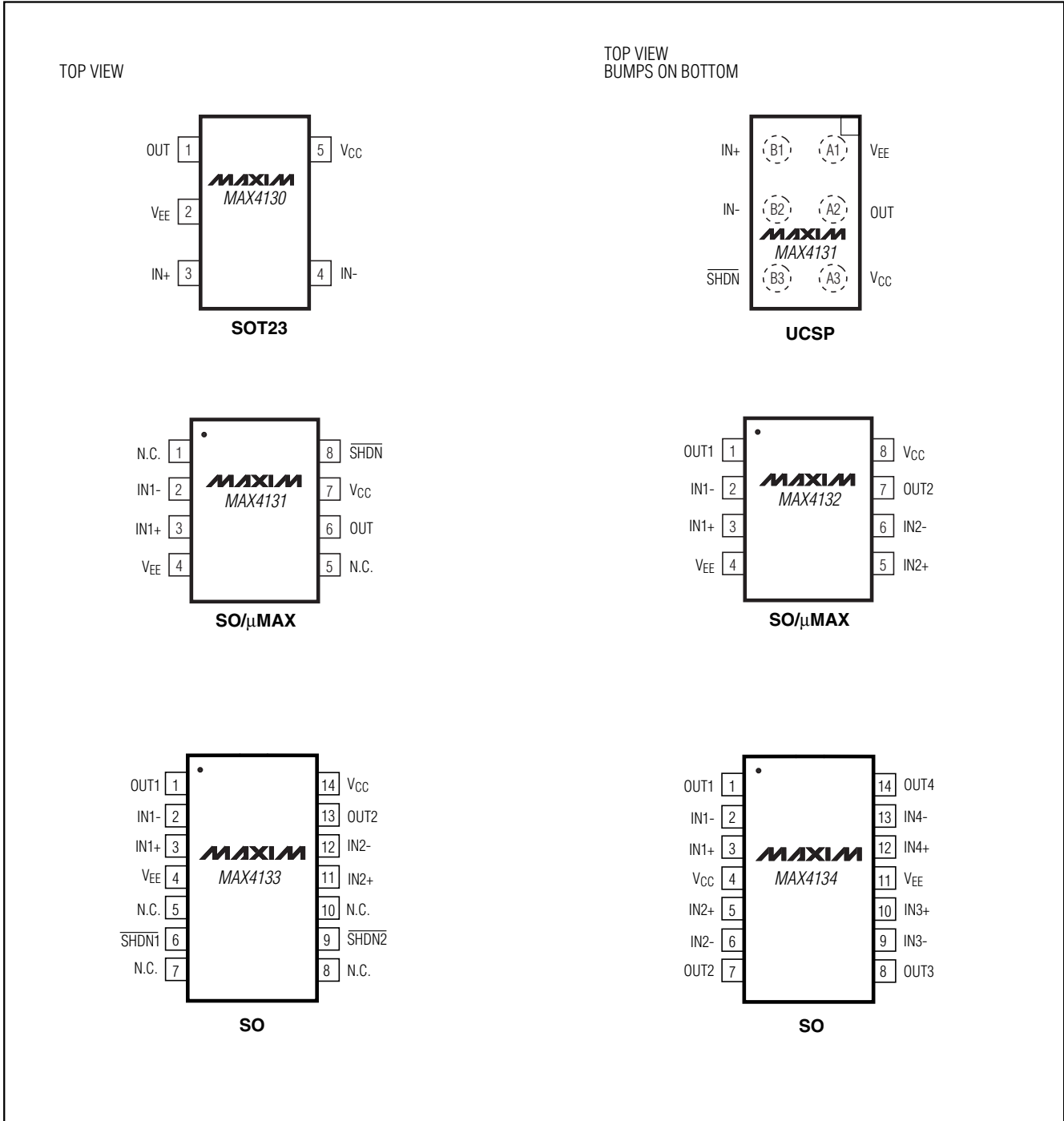
Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. Decrease stray capacitance by placing external components close to the op amp's pins, minimizing trace lengths and resistor leads.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and the recommended reflow temperature profile, as well as the latest information on reliability testing results, go to Maxim's website at www.maxim-ic.com/ucsp and search for the Application Note: *UCSP–A Wafer-Level Chip-Scale Package*.

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Pin Configurations



Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4132 ESA	-40°C to +85°C	8 SO	—
MAX4132EUA	-40°C to +85°C	8 μ MAX	—
MAX4133 C/D	0°C to +70°C	Dice*	—
MAX4133ESD	-40°C to +85°C	14 SO	—
MAX4134 ESD	-40°C to +85°C	14 SO	—

*Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

Chip Information

MAX4130 TRANSISTOR COUNT: 170
 MAX4131 TRANSISTOR COUNT: 170
 MAX4132 TRANSISTOR COUNT: 340
 MAX4134 TRANSISTOR COUNT: 680

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

TOP VIEW

SIDE VIEW

FRONT VIEW

SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60	REF
e	0.95	BSC.
e1	1.90	BSC.
α	0°	8°

SOT-23 5L .EPS

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
- PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
- PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
- MEETS JEDEC MO178, VARIATION AA.
- LEADS TO BE COPLANAR WITHIN 0.10 mm.
- SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 5L

APPROVAL	DOCUMENT CONTROL NO. 21-0057	REV. E	1/1
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Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.30	0.60
L2	0.25 BSC.	
e	0.65 BSC.	
e1	1.95 REF.	
θ	0	8

NOTE:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- △ FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
- PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
- PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
- COPLANARITY 4 MILS. MAX.
- PIN 1 I.D. DOT IS 0.3 MM MIN. LOCATED ABOVE PIN 1.
- SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
- MEETS JEDEC MO178.

DETAIL "A"

SEATING PLANE C

GAUGE PLANE

SOT23, 8L, EPS

<small>PROPRIETARY INFORMATION</small>		
TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY		
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small> 21-0078	<small>REV.</small> D 1/1

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX4130-MAX4134

TOP VIEW

COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	∅0.35±0.03
D1	0.50 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B6-1	1.00±0.05	1.52±0.05	NONE
B6-2	1.00±0.05	1.52±0.05	B2
B6-3	1.05±0.05	1.57±0.05	NONE
B6-4	1.05±0.05	1.57±0.05	B2
B6-5	0.97±0.05	1.46±0.05	NONE
B6-6	1.16±0.05	1.57±0.05	NONE

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

BOTTOM VIEW

SIDE VIEW

DALLAS SEMICONDUCTOR		MAXIM	
<small>PROPRIETARY INFORMATION</small>			
<small>TITLE:</small>			
PACKAGE OUTLINE, 3x2 UCSP			
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small>	<small>REV.</small>	<small>1/1</small>
	21-0097	G	

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

TOP VIEW

FRONT VIEW

SIDE VIEW

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

SOICN EFS

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

PROPRIETARY INFORMATION	
TITLE: PACKAGE OUTLINE, .150" SOIC	
APPROVAL	DOCUMENT CONTROL NO. 21-0041
REV.	1/1

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