

TQFP
Commercial Temp
Industrial Temp

256K x 18, 128K x 32, 128K x 36
4Mb Sync Burst SRAMs

8 ns – 12 ns
3.3 V V_{DD}
3.3 V and 2.5 V I/O

Features

- Flow Through mode operation
- 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{\text{LBO}}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipelined mode
- Byte Write ($\overline{\text{BW}}$) and/or Global Write ($\overline{\text{GW}}$) operation
- Common data inputs and data outputs
- Clock Control, registered, address, data, and control
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC standard 100-lead TQFP
- RoHS-compliant 100-lead TQFP package available

Functional Description

Applications

The GS840F18/32/36A is a 4,718,592-bit (4,194,304-bit for x32 version) high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support. The GS840F18/32/36A is available in a JEDEC standard 100-lead TQFP package.

Controls

Addresses, data I/Os, chip enables ($\overline{\text{E}}_1, \text{E}_2, \overline{\text{E}}_3$), address burst control inputs ($\overline{\text{ADSP}}, \overline{\text{ADSC}}, \overline{\text{ADV}}$) and write control inputs ($\overline{\text{Bx}}, \overline{\text{BW}}, \overline{\text{GW}}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{\text{G}}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either ADSP or $\overline{\text{ADSC}}$ inputs. In

Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{\text{ADV}}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{\text{LBO}}$) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Designing For Compatibility

The JEDEC Standard for Burst RAMS calls for a $\overline{\text{FT}}$ mode pin option (pin 14 on TQFP). Board sites for Flow Through Burst RAMS should be designed with V_{SS} connected to the $\overline{\text{FT}}$ pin location to ensure the broadest access to multiple vendor sources. Boards designed with $\overline{\text{FT}}$ pin pads tied low may be stuffed with GSI's Pipeline/Flow Through-configurable Burst RAMS or any vendor's Flow Through or configurable Burst SRAM. Bumps designed with the $\overline{\text{FT}}$ pin location tied high or floating must employ a non-configurable Flow Through Burst RAM, like this RAM, to achieve flow through functionality.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable ($\overline{\text{BW}}$) input combined with one or more individual byte write signals ($\overline{\text{Bx}}$). In addition, Global Write ($\overline{\text{GW}}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (high) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

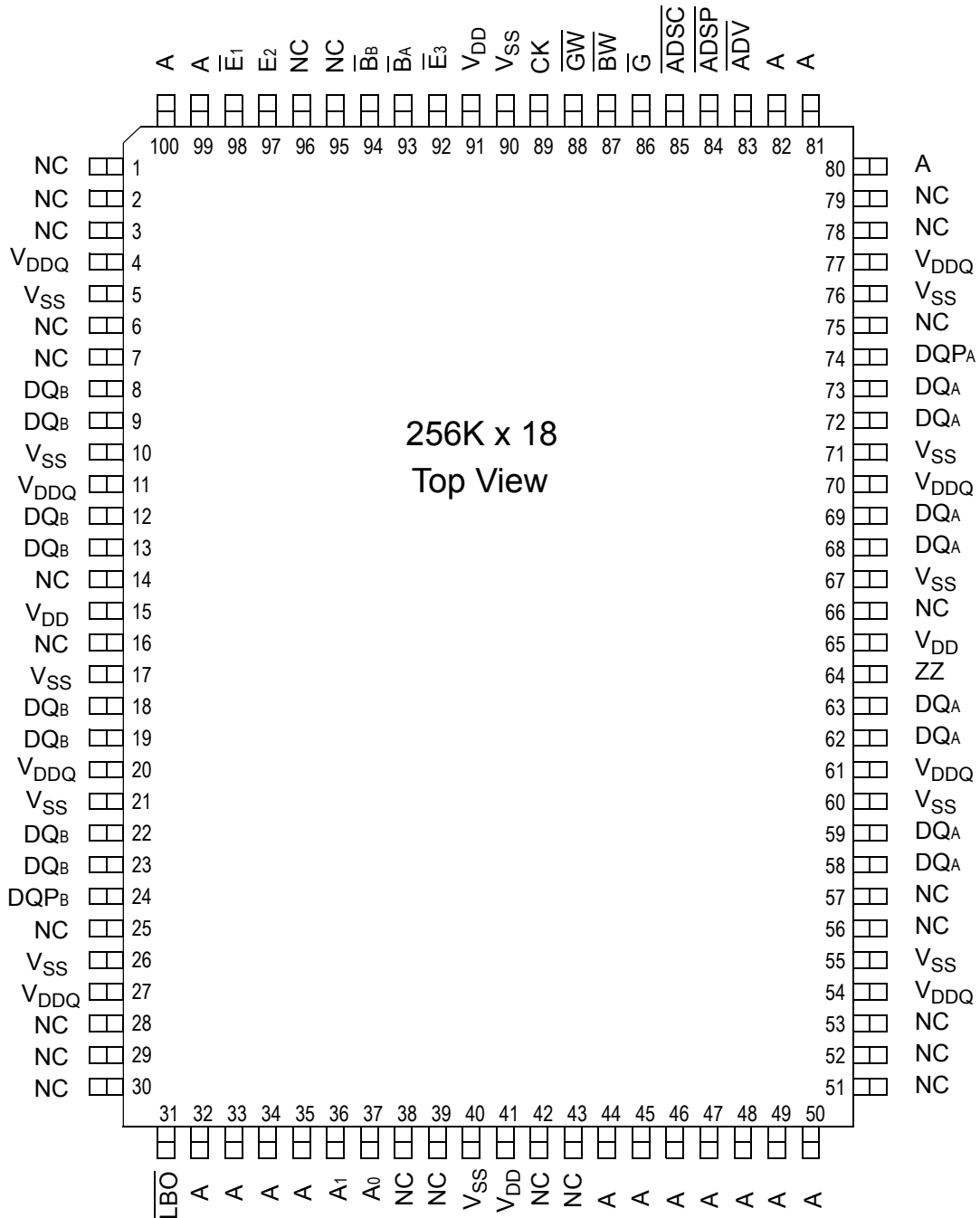
Core and Interface Voltages

The GS840F18/32/36A operates on a 3.3 V power supply and all inputs/outputs are 3.3 V- and 2.5 V-compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuit.

Parameter Synopsis

| | | -8 | -8.5 | -10 | -12 |
|---------|--------------------|--------|--------|--------|--------|
| Flow | t _Q | 8 ns | 8.5 ns | 10 ns | 12 ns |
| Through | t _{Cycle} | 9 ns | 10 ns | 12 ns | 15 ns |
| 2-1-1-1 | I _{DD} | 210 mA | 190 mA | 165 mA | 135 mA |

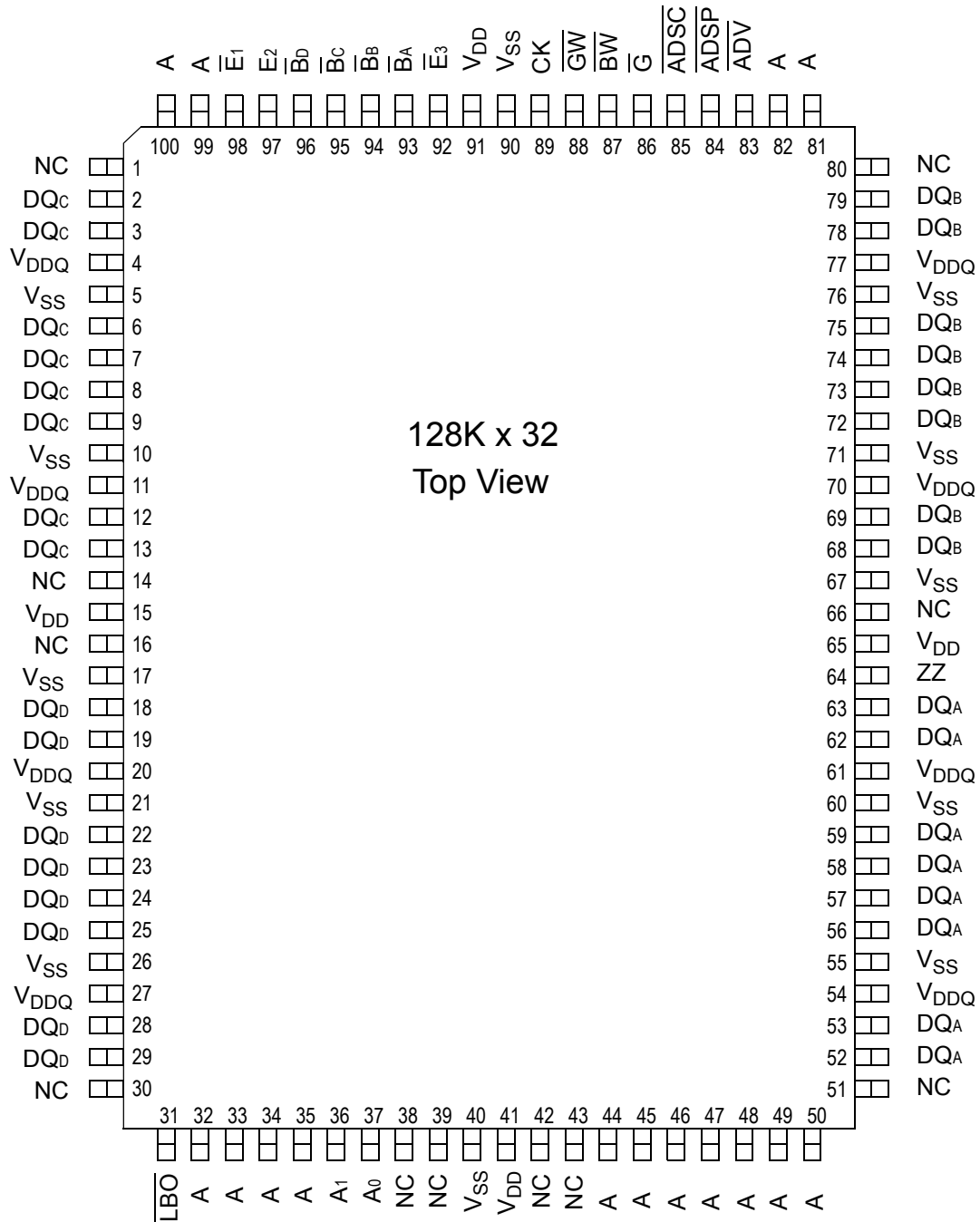
GS840F18A 100-Pin TQFP Pinout



Note:

Pins marked with NC can be tied to either V_{DD} or V_{SS} . These pins can also be left floating.

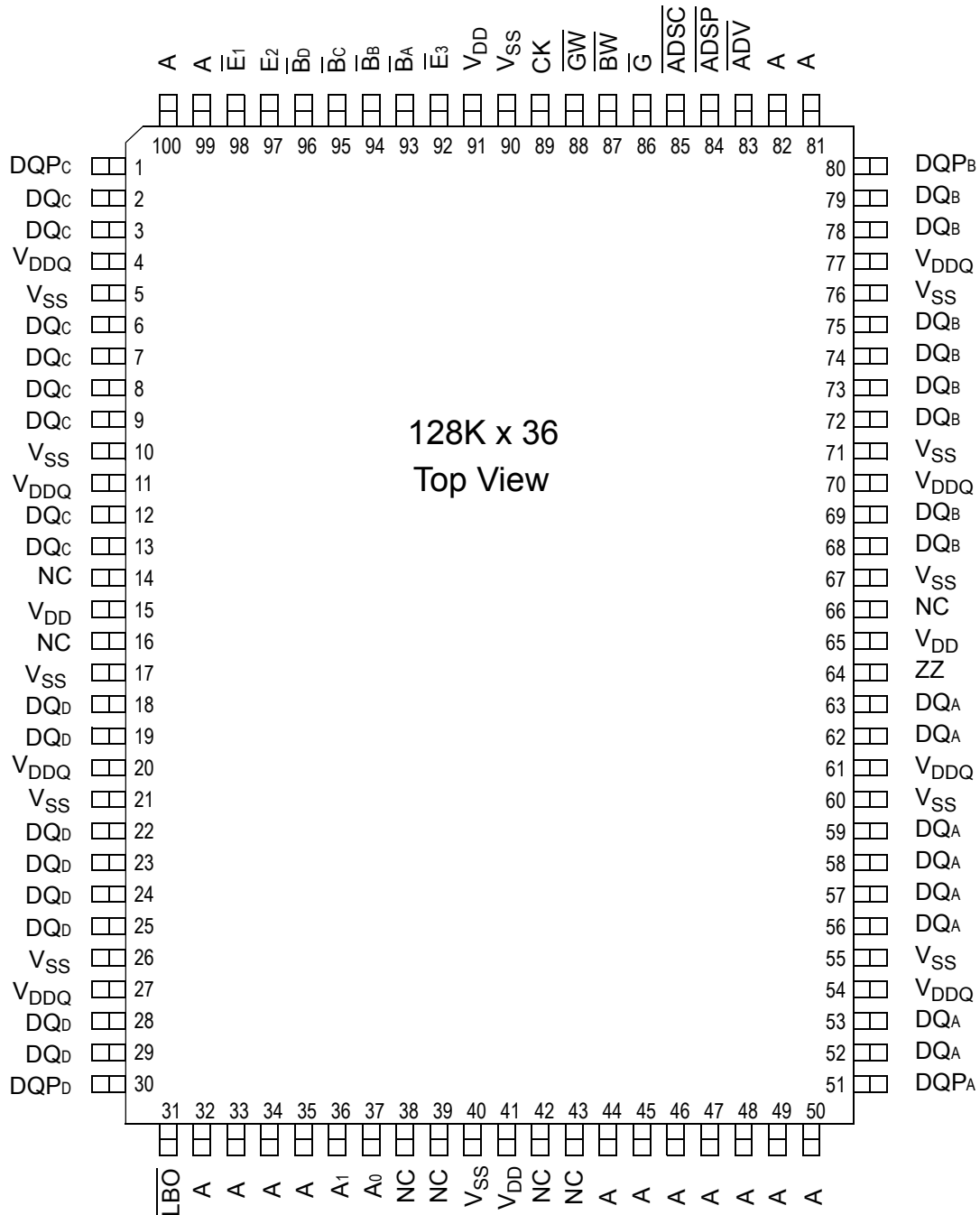
GS840F32A 100-Pin TQFP Pinout



Note:

Pins marked with NC can be tied to either V_{DD} or V_{SS} . These pins can also be left floating.

GS840F36A 100-Pin TQFP Pinout



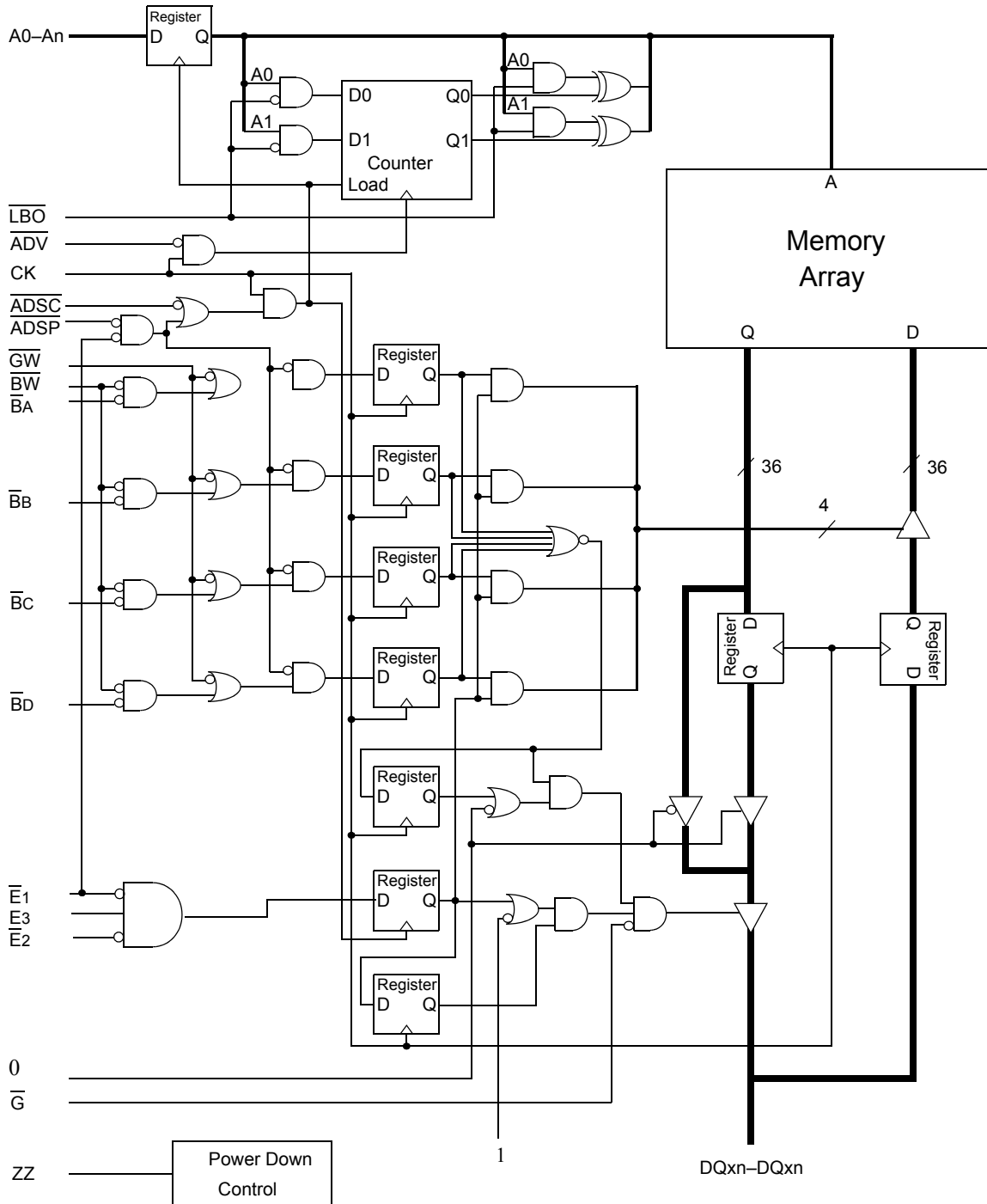
Note:

Pins marked with NC can be tied to either V_{DD} or V_{SS} . These pins can also be left floating.

TQFP Pin Description

| Symbol | Type | Description |
|---------------------------------------|-------------|--|
| A ₀ , A ₁ | I | Address field LSBs and Address Counter preset Inputs |
| A | I | Address Inputs |
| \overline{B}_A | In | Byte Write signal for data inputs DQ _A ; active low |
| \overline{B}_B | In | Byte Write signal for data inputs DQ _B ; active low |
| \overline{B}_C | In | Byte Write signal for data inputs DQ _C ; active low |
| \overline{B}_D | In | Byte Write signal for data inputs DQ _D ; active low |
| \overline{B}_W | I | Byte Write—Writes all enabled bytes; active low |
| CK | I | Clock Input Signal; active high |
| \overline{G}_W | I | Global Write Enable—Writes all bytes; active low |
| \overline{E}_1 , \overline{E}_3 | I | Chip Enable; active low |
| E ₂ | I | Chip Enable; active high |
| \overline{G} | I | Output Enable; active low |
| \overline{ADV} | I | Burst address counter advance enable; active low |
| \overline{ADSP} , \overline{ADSC} | I | Address Strobe (Processor, Cache Controller); active low |
| DQ _A | I/O | Byte A Data Input and Output pins |
| DQ _B | I/O | Byte B Data Input and Output pins |
| DQ | I/O | Byte C Data Input and Output pins |
| DQ _D | I/O | Byte D Data Input and Output pins |
| DQP _A | I/O | 9th Data I/O Pin; Byte A |
| DQP _B | I/O | 9th Data I/O Pin; Byte B |
| DQP _C | I/O | 9th Data I/O Pin; Byte C |
| DQP _D | I/O | 9th Data I/O Pin; Byte D |
| ZZ | I | Sleep Mode control; active high |
| \overline{LBO} | I | Linear Burst Order mode; active low |
| V _{DD} | I | Core power supply |
| V _{SS} | I | I/O and Core Ground |
| V _{DDQ} | I | Output driver power supply |
| NC | — | No Connect |

GS840F18/32/36A Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

| Mode Name | Pin Name | State | Function |
|---------------------|-------------------------|---------|----------------------------|
| Burst Order Control | $\overline{\text{LBO}}$ | L | Linear Burst |
| | | H or NC | Interleaved Burst |
| Power Down Control | ZZ | L or NC | Active |
| | | H | Standby, $I_{DD} = I_{SB}$ |

Note:

There is a pull-up device on the $\overline{\text{LBO}}$ pin and a pull-down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

| | A[1:0] | A[1:0] | A[1:0] | A[1:0] |
|-------------|--------|--------|--------|--------|
| 1st address | 00 | 01 | 10 | 11 |
| 2nd address | 01 | 10 | 11 | 00 |
| 3rd address | 10 | 11 | 00 | 01 |
| 4th address | 11 | 00 | 01 | 10 |

Note:

The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

| | A[1:0] | A[1:0] | A[1:0] | A[1:0] |
|-------------|--------|--------|--------|--------|
| 1st address | 00 | 01 | 10 | 11 |
| 2nd address | 01 | 00 | 11 | 10 |
| 3rd address | 10 | 11 | 00 | 01 |
| 4th address | 11 | 10 | 01 | 00 |

Note:

The burst counter wraps to initial state on the 5th clock.

Byte Write Truth Table

| Function | GW | BW | B _A | B _B | B _C | B _D | Notes |
|-----------------|----|----|----------------|----------------|----------------|----------------|---------|
| Read | H | H | X | X | X | X | 1 |
| Read | H | L | H | H | H | H | 1 |
| Write byte A | H | L | L | H | H | H | 2, 3 |
| Write byte B | H | L | H | L | H | H | 2, 3 |
| Write byte c | H | L | H | H | L | H | 2, 3, 4 |
| Write byte D | H | L | H | H | H | L | 2, 3, 4 |
| Write all bytes | H | L | L | L | L | L | 2, 3, 4 |
| Write all bytes | L | X | X | X | X | X | |

Notes:

- All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
- Byte Write Enable inputs $\overline{\text{B}}_A$, $\overline{\text{B}}_B$, $\overline{\text{B}}_C$, and/or $\overline{\text{B}}_D$ may be used in any combination with BW to write single or multiple bytes.
- All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
- Bytes "c" and "d" are only available on the x32 and x36 versions.

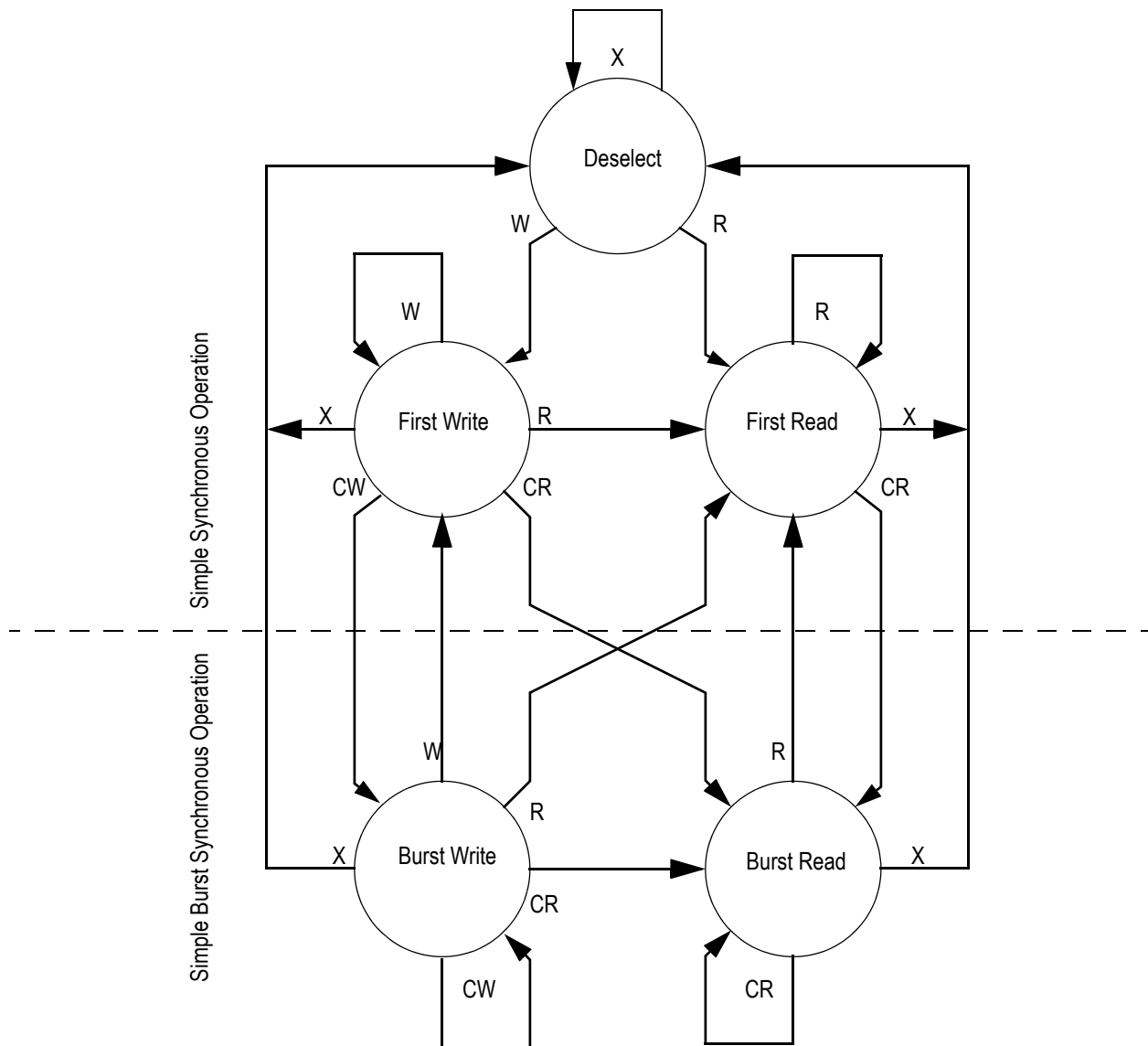
Synchronous Truth Table

| Operation | Address Used | State Diagram Key ⁵ | \bar{E}_1 | E^2 | \overline{ADSP} | \overline{ADSC} | \overline{ADV} | W^3 | DQ^4 |
|------------------------------------|-----------------|--------------------------------|-------------|----------|-------------------|-------------------|------------------|----------|---------------|
| Deselect Cycle, Power Down | None | X | H | X | X | L | X | X | High-Z |
| Deselect Cycle, Power Down | None | X | L | F | L | X | X | X | High-Z |
| Deselect Cycle, Power Down | None | X | L | F | H | L | X | X | High-Z |
| Read Cycle, Begin Burst | External | R | L | T | L | X | X | X | Q |
| Read Cycle, Begin Burst | External | R | L | T | H | L | X | F | Q |
| Write Cycle, Begin Burst | External | W | L | T | H | L | X | T | D |
| <i>Read Cycle, Continue Burst</i> | <i>Next</i> | <i>CR</i> | <i>X</i> | <i>X</i> | <i>H</i> | <i>H</i> | <i>L</i> | <i>F</i> | <i>Q</i> |
| Read Cycle, Continue Burst | Next | CR | H | X | X | H | L | F | Q |
| <i>Write Cycle, Continue Burst</i> | <i>Next</i> | <i>CW</i> | <i>X</i> | <i>X</i> | <i>H</i> | <i>H</i> | <i>L</i> | <i>T</i> | <i>D</i> |
| Write Cycle, Continue Burst | Next | CW | H | X | X | H | L | T | D |
| Read Cycle, Suspend Burst | Current | | X | X | H | H | H | F | Q |
| Read Cycle, Suspend Burst | Current | | H | X | X | H | H | F | Q |
| Write Cycle, Suspend Burst | Current | | X | X | H | H | H | T | D |
| Write Cycle, Suspend Burst | Current | | H | X | X | H | H | T | D |

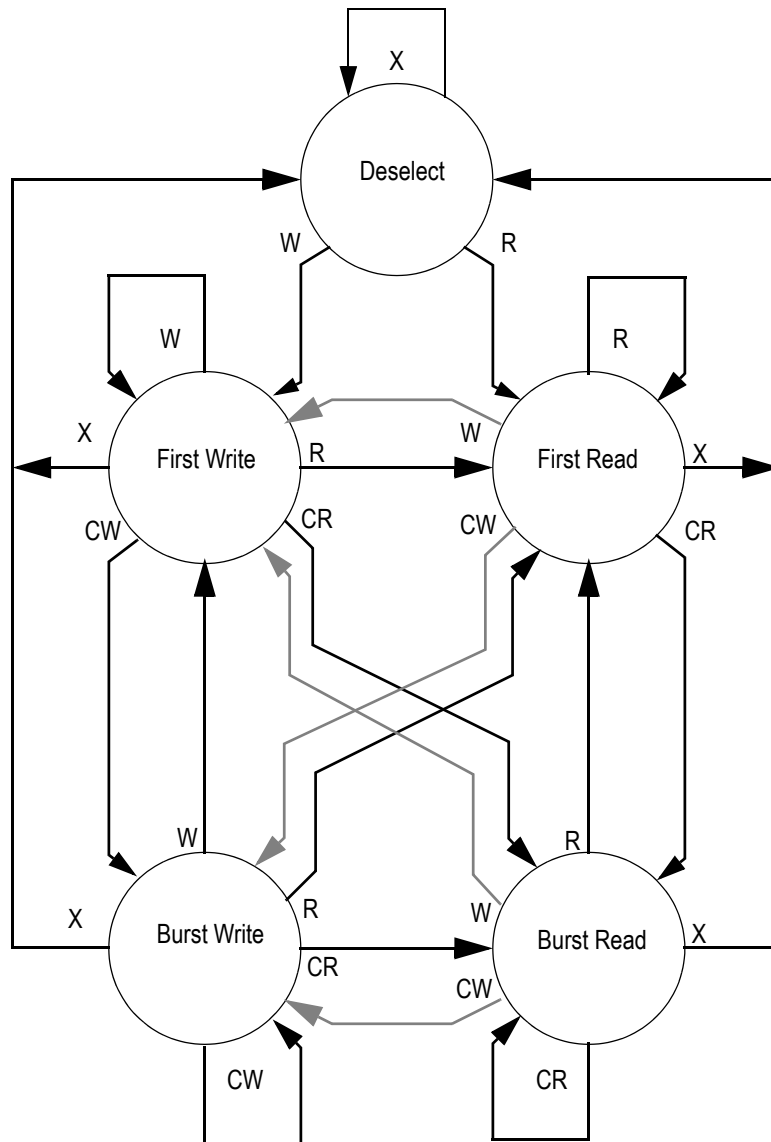
Notes:

1. X = Don't Care, H = High, L = Low.
2. E = T (True) if $E_2 = 1$ and $\bar{E}_3 = 0$; E = F (False) if $E_2 = 0$ or $\bar{E}_3 = 1$.
3. W = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. \bar{G} is an asynchronous input. \bar{G} can be driven high at any time to disable active output drivers. \bar{G} low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying \overline{ADSP} high and \overline{ADSC} low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying \overline{ADSP} high and \overline{ADV} low while using \overline{ADSC} to load new addresses allows simple burst operations. See *ITALIC* items above.

Simplified State Diagram


Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes \overline{G} is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E}_1, \overline{E}_2, \overline{E}_3$) and Write ($\overline{B}_A, \overline{B}_B, \overline{B}_C, \overline{B}_D, \overline{B}_W$, and \overline{G}_W) control inputs, and that \overline{ADSP} is tied high and \overline{ADSC} is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and \overline{ADSC} control inputs, and assumes \overline{ADSP} is tied high and \overline{ADV} is tied low.

Simplified State Diagram with \bar{G}

Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of \bar{G} .
2. Use of "Dummy Reads" (Read Cycles with \bar{G} High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal Read cycles.
3. Transitions shown in grey tone assume \bar{G} has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

 (All voltages reference to V_{SS})

| Symbol | Description | Value | Unit |
|------------|-------------------------------|--|------|
| V_{DD} | Voltage on V_{DD} Pins | -0.5 to 4.6 | V |
| V_{DDQ} | Voltage in V_{DDQ} Pins | -0.5 to 4.6 | V |
| $V_{I/O}$ | Voltage on I/O Pins | -0.5 to $V_{DDQ} + 0.5$ (≤ 4.6 V max.) | V |
| V_{IN} | Voltage on Other Input Pins | -0.5 to $V_{DD} + 0.5$ (≤ 4.6 V max.) | V |
| I_{IN} | Input Current on Any Pin | +/-20 | mA |
| I_{OUT} | Output Current on Any I/O Pin | +/-20 | mA |
| P_D | Package Power Dissipation | 1.5 | W |
| T_{STG} | Storage Temperature | -55 to 125 | °C |
| T_{BIAS} | Temperature Under Bias | -55 to 125 | °C |

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|------------------------------------|------------|------|------|------|------|-------|
| 3.3 V Supply Voltage | V_{DD} | 3.0 | 3.3 | 3.6 | V | |
| 3.3 V V_{DDQ} I/O Supply Voltage | V_{DDQ3} | 3.0 | 3.3 | 3.6 | V | |
| 2.5 V V_{DDQ} I/O Supply Voltage | V_{DDQ2} | 2.3 | 2.5 | 2.7 | V | |

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Logic Levels

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|-----------------------------------|------------|--------------------|------|--------------------|------|-------|
| V_{DD} Input High Voltage | V_{IH} | 2.0 | — | $V_{DD} + 0.3$ | V | 1 |
| V_{DD} Input Low Voltage | V_{IL} | -0.3 | — | 0.8 | V | 1 |
| V_{DDQ3} I/O Input High Voltage | V_{IHQ3} | 2.0 | — | $V_{DDQ} + 0.3$ | V | 1,3 |
| V_{DDQ3} I/O Input Low Voltage | V_{ILQ3} | -0.3 | — | 0.8 | V | 1,3 |
| V_{DDQ2} I/O Input High Voltage | V_{IHQ2} | $0.6 \cdot V_{DD}$ | — | $V_{DDQ} + 0.3$ | V | 1,3 |
| V_{DDQ2} I/O Input Low Voltage | V_{ILQ2} | -0.3 | — | $0.3 \cdot V_{DD}$ | V | 1,3 |

Notes:

- The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
- Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.
- V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

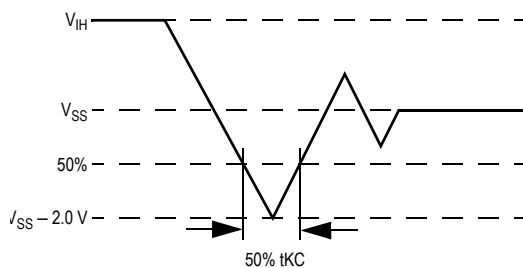
Recommended Operating Temperatures

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|--------|------|------|------|------|-------|
| Ambient Temperature (Commercial Range Versions) | T_A | 0 | 25 | 70 | °C | 2 |
| Ambient Temperature (Industrial Range Versions) | T_A | -40 | 25 | 85 | °C | 2 |

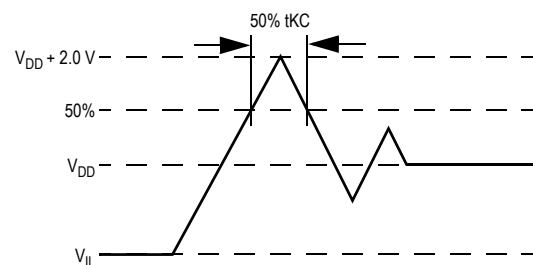
Notes:

- The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
- Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 2.5\text{ V}$)

| Parameter | Symbol | Test conditions | Typ. | Max. | Unit |
|--------------------------|-----------|------------------------|------|------|------|
| Input Capacitance | C_{IN} | $V_{IN} = 0\text{ V}$ | 4 | 5 | pF |
| Input/Output Capacitance | $C_{I/O}$ | $V_{OUT} = 0\text{ V}$ | 6 | 7 | pF |

Note:

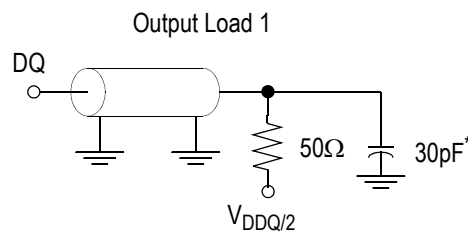
These parameters are sample tested.

AC Test Conditions

| Parameter | Conditions |
|------------------------|-------------------------|
| Input high level | $V_{DD} - 0.2\text{ V}$ |
| Input low level | 0.2 V |
| Input slew rate | 1 V/ns |
| Input reference level | $V_{DD}/2$ |
| Output reference level | $V_{DDQ}/2$ |
| Output load | Fig. 1 |

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.



* Distributed Test Jig Capacitance

DC Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Max |
|---|-----------|---|----------------------------|--------------------------|
| Input Leakage Current (except mode pins) | I_{IL} | $V_{IN} = 0$ to V_{DD} | -1 μ A | 1 μ A |
| ZZ Input Current | I_{IN1} | $V_{DD} \geq V_{IN} \geq V_{IH}$ $0 V \leq V_{IN} \leq V_{IH}$ | -1 μ A -1 μ A | 1 μ A 100 μ A |
| \overline{FT} , SCD, ZQ Input Current | I_{IN2} | $V_{DD} \geq V_{IN} \geq V_{IL}$ $0 V \leq V_{IN} \leq V_{IL}$ | -100 μ A -1 μ A | 1 μ A 1 μ A |
| Output Leakage Current | I_{OL} | Output Disable, $V_{OUT} = 0$ to V_{DD} | -1 μ A | 1 μ A |
| Output High Voltage | V_{OH2} | $I_{OH} = -8$ mA, $V_{DDQ} = 2.375$ V | 1.7 V | — |
| Output High Voltage | V_{OH3} | $I_{OH} = -8$ mA, $V_{DDQ} = 3.135$ V | 2.4 V | — |
| Output Low Voltage | V_{OL} | $I_{OL} = 8$ mA | — | 0.4 V |

Operating Currents

| Parameter | Test Conditions | Symbol | -8 | | -8.5 | | -10 | | -12 | | Unit |
|-------------------|---|--------------------------|-----------|-------------|-----------|-------------|-----------|-------------|-----------|-------------|------|
| | | | 0 to 70°C | -40 to 85°C | 0 to 70°C | -40 to 85°C | 0 to 70°C | -40 to 85°C | 0 to 70°C | -40 to 85°C | |
| Operating Current | All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open | I_{DD} Flow Through | 210 | 220 | 190 | 200 | 165 | 175 | 135 | 145 | mA |
| Standby Current | $ZZ \geq V_{DD} - 0.2$ V | I_{SB} Flow Through | 20 | 30 | 20 | 30 | 20 | 30 | 20 | 30 | mA |
| Deselect Current | Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ | I_{DD} Flow Through | 40 | 50 | 40 | 50 | 35 | 45 | 35 | 45 | mA |

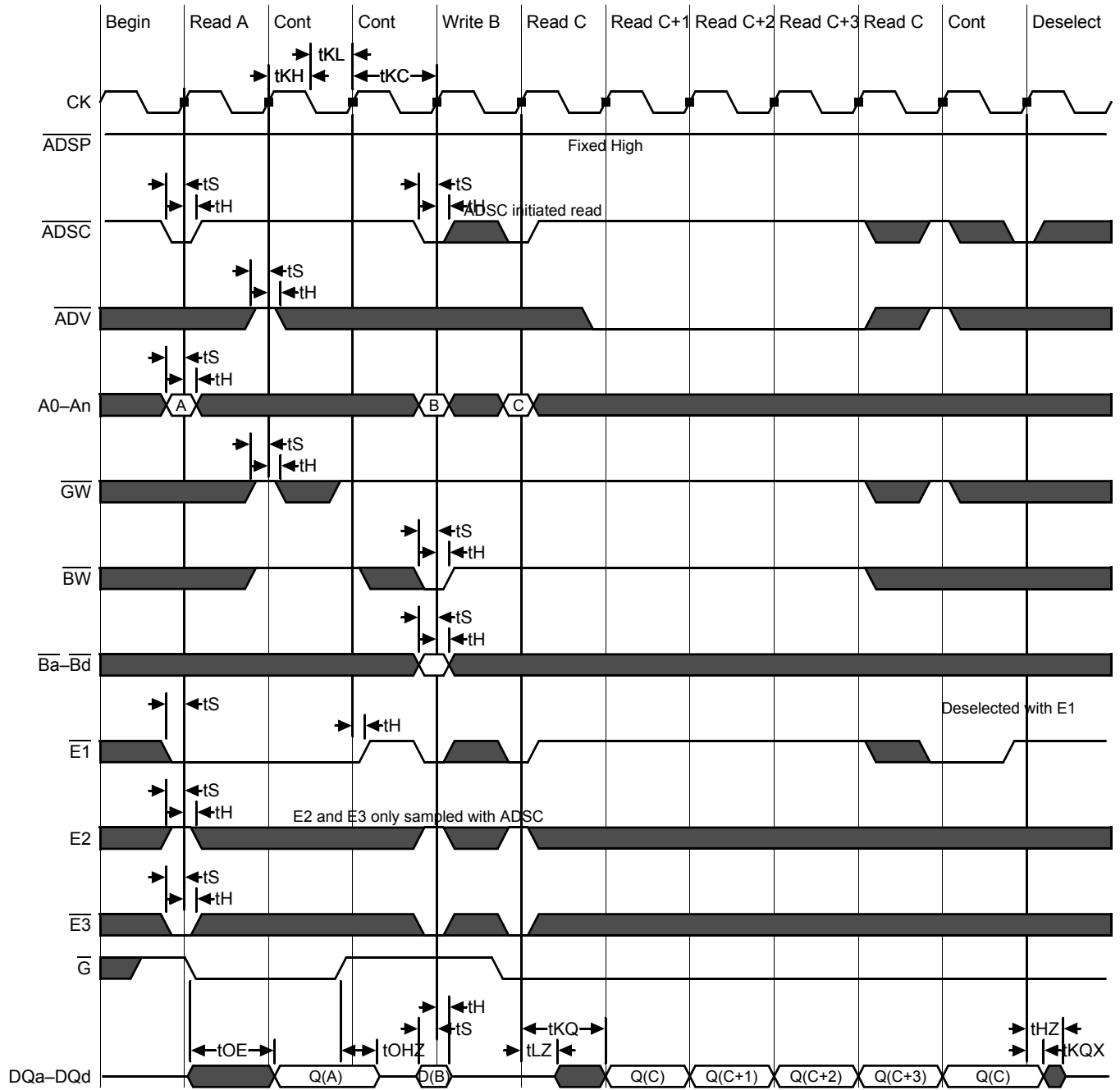
AC Electrical Characteristics

| | Parameter | Symbol | -8 | | -8.5 | | -10 | | -12 | | Unit |
|---------------------|-------------------------------|-------------------------------|-----|-----|------|-----|------|-----|------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Flow Through | Clock Cycle Time | t _{KC} | 9.0 | — | 10.0 | — | 10.0 | — | 15.0 | — | ns |
| | Clock to Output Valid | t _{KQ} | — | 8.0 | — | 8.5 | — | 10 | — | 12 | ns |
| | Clock to Output Invalid | t _{KQX} | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns |
| | Clock to Output in Low-Z | t _{LZ} ¹ | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns |
| | Clock HIGH Time | t _{KH} | 1.3 | — | 1.3 | — | 1.3 | — | 1.3 | — | ns |
| | Clock LOW Time | t _{KL} | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| | Clock to Output in High-Z | t _{HZ} ¹ | 1.5 | 3.2 | 1.5 | 3.5 | 1.5 | 3.8 | 1.5 | 5 | ns |
| | \bar{G} to Output Valid | t _{OE} | — | 3.2 | — | 3.5 | — | 3.8 | — | 5 | ns |
| | \bar{G} to output in Low-Z | t _{OLZ} ¹ | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| | \bar{G} to output in High-Z | t _{OHZ} ¹ | — | 3.2 | — | 3.5 | — | 3.8 | — | 5 | ns |
| | Setup time | t _S | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| | Hold time | t _H | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| | ZZ setup time | t _{ZZS} ² | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| | ZZ hold time | t _{ZZH} ² | 1 | — | 1 | — | 1 | — | 1 | — | ns |
| | ZZ recovery | t _{ZZR} | 20 | — | 20 | — | 20 | — | 20 | — | ns |

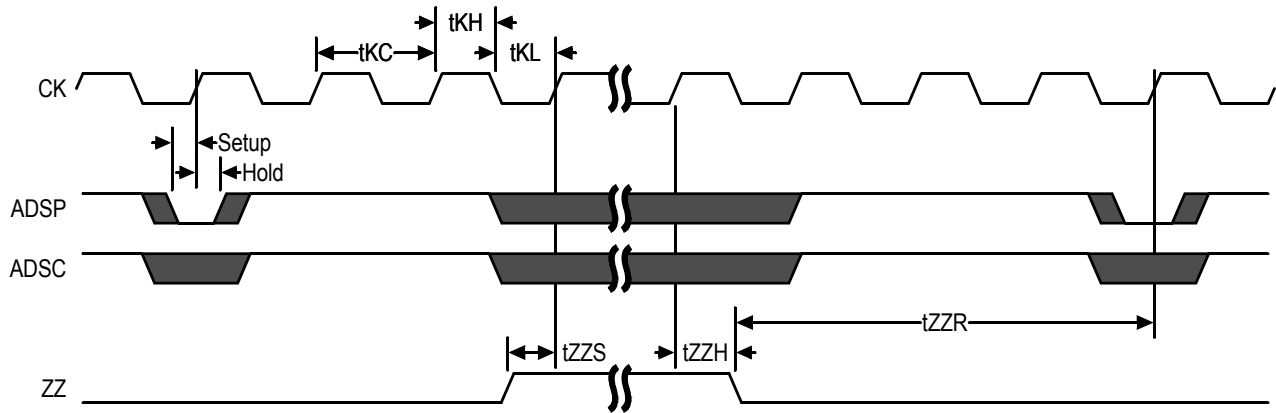
Notes:

1. These parameters are sampled and are not 100% tested
2. ZZ is an asynchronous signal. However, In order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

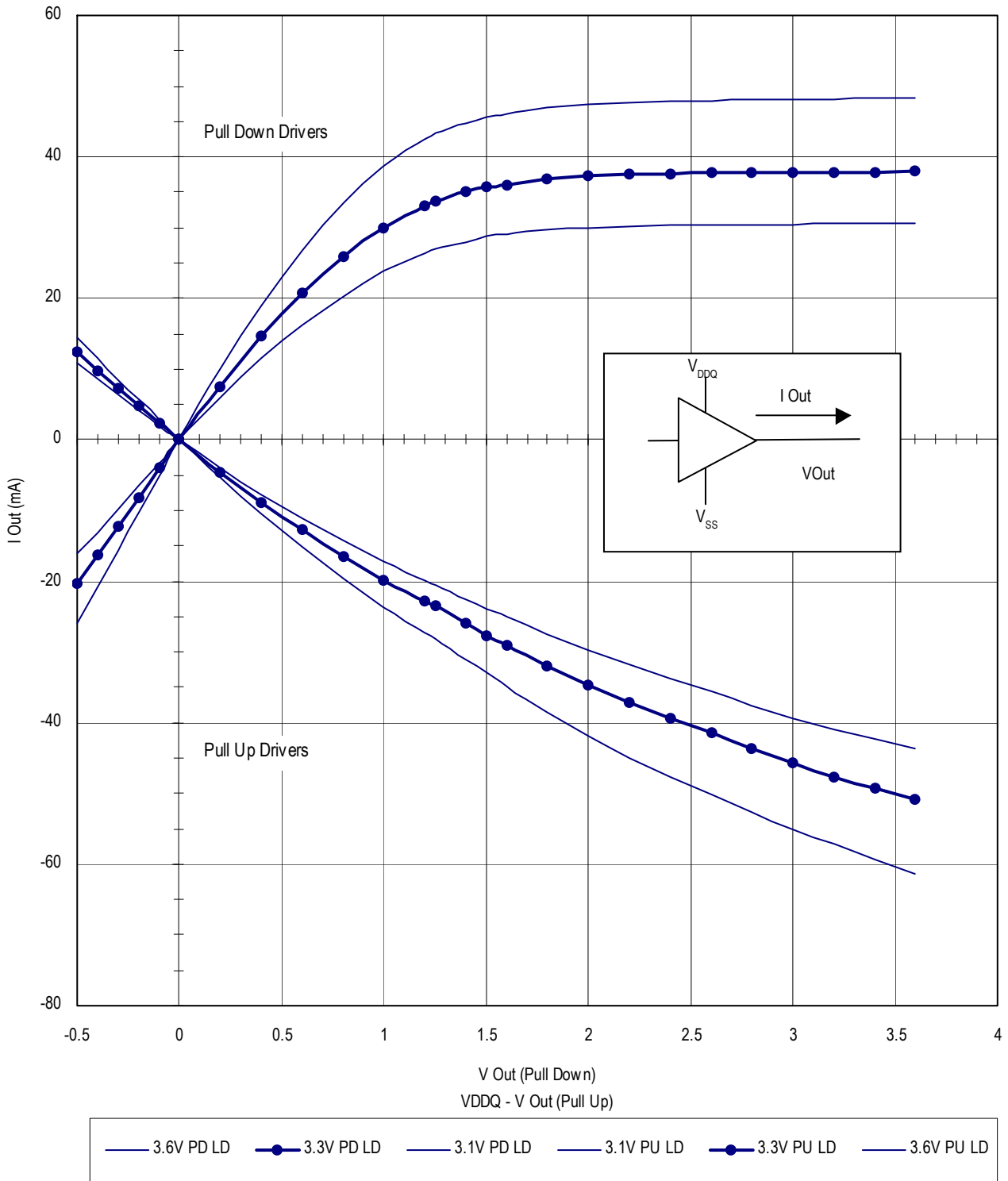
Flow Through Mode Timing



Sleep Mode Timing Diagram

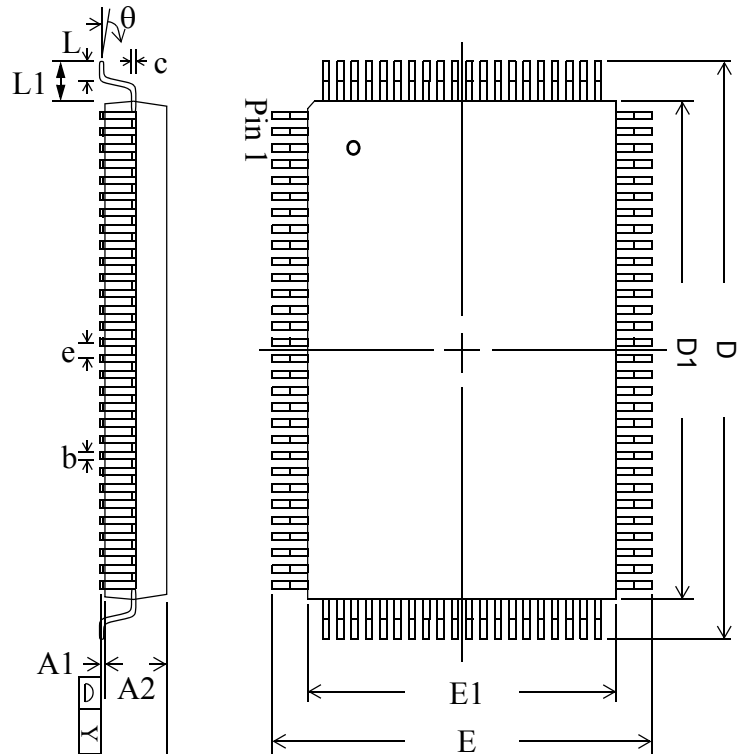


GS840F18/32/36A Output Driver Characteristics



TQFP Package Drawing (Package T)

| Symbol | Description | Min. | Nom. | Max |
|----------|--------------------|------|------|------|
| A1 | Standoff | 0.05 | 0.10 | 0.15 |
| A2 | Body Thickness | 1.35 | 1.40 | 1.45 |
| b | Lead Width | 0.20 | 0.30 | 0.40 |
| c | Lead Thickness | 0.09 | — | 0.20 |
| D | Terminal Dimension | 21.9 | 22.0 | 22.1 |
| D1 | Package Body | 19.9 | 20.0 | 20.1 |
| E | Terminal Dimension | 15.9 | 16.0 | 16.1 |
| E1 | Package Body | 13.9 | 14.0 | 14.1 |
| e | Lead Pitch | — | 0.65 | — |
| L | Foot Length | 0.45 | 0.60 | 0.75 |
| L1 | Lead Length | — | 1.00 | — |
| Y | Coplanarity | | | 0.10 |
| θ | Lead Angle | 0° | — | 7° |


Notes:

1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

Ordering Information for GSI Synchronous Burst RAMs

| Org | Part Number ¹ | Type | Package | Speed ² (Mhz/ns) | T _A ³ |
|-----------|--------------------------|--------------|---------------------|--------------------------------|-----------------------------|
| 256K x 18 | GS840F18AT-8 | Flow Through | TQFP | 8 | C |
| 256K x 18 | GS840F18AT-8.5 | Flow Through | TQFP | 8.5 | C |
| 256K x 18 | GS840F18AT-10 | Flow Through | TQFP | 10 | C |
| 256K x 18 | GS840F18AT-12 | Flow Through | TQFP | 12 | C |
| 128K x 32 | GS840F32AT-8 | Flow Through | TQFP | 8 | C |
| 128K x 32 | GS840F32AT-8.5 | Flow Through | TQFP | 8.5 | C |
| 128K x 32 | GS840F32AT-10 | Flow Through | TQFP | 10 | C |
| 128K x 32 | GS840F32AT-12 | Flow Through | TQFP | 12 | C |
| 128K x 36 | GS840F36AT-8 | Flow Through | TQFP | 8 | C |
| 128K x 36 | GS840F36AT-8.5 | Flow Through | TQFP | 8.5 | C |
| 128K x 36 | GS840F36AT-10 | Flow Through | TQFP | 8.5 | C |
| 128K x 36 | GS840F36AT-12 | Flow Through | TQFP | 8.5 | C |
| 256K x 18 | GS840F18AT-8I | Flow Through | TQFP | 8 | I |
| 256K x 18 | GS840F18AT-8.5I | Flow Through | TQFP | 8.5 | I |
| 256K x 18 | GS840F18AT-10I | Flow Through | TQFP | 10 | I |
| 256K x 18 | GS840F18AT-12I | Flow Through | TQFP | 12 | I |
| 128K x 32 | GS840F32AT-8I | Flow Through | TQFP | 8 | I |
| 128K x 32 | GS840F32AT-8.5I | Flow Through | TQFP | 8.5 | I |
| 128K x 32 | GS840F32AT-10I | Flow Through | TQFP | 10 | I |
| 128K x 32 | GS840F32AT-12I | Flow Through | TQFP | 12 | I |
| 128K x 36 | GS840F36AT-8I | Flow Through | TQFP | 8 | I |
| 128K x 36 | GS840F36AT-8.5I | Flow Through | TQFP | 8.5 | I |
| 128K x 36 | GS840F36AT-10I | Flow Through | TQFP | 10 | I |
| 128K x 36 | GS840F36AT-12I | Flow Through | TQFP | 12 | I |
| 256K x 18 | GS840F18AGT-8 | Flow Through | RoHS-compliant TQFP | 8 | C |
| 256K x 18 | GS840F18AGT-8.5 | Flow Through | RoHS-compliant TQFP | 8.5 | C |
| 256K x 18 | GS840F18AGT-10 | Flow Through | RoHS-compliant TQFP | 10 | C |
| 256K x 18 | GS840F18AGT-12 | Flow Through | RoHS-compliant TQFP | 12 | C |
| 128K x 32 | GS840F32AGT-8 | Flow Through | RoHS-compliant TQFP | 8 | C |
| 128K x 32 | GS840F32AGT-8.5 | Flow Through | RoHS-compliant TQFP | 8.5 | C |

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS840F32AT-8T.
- The speed column indicates the cycle frequency (MHz) of the device in Pipelined mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
- T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
- GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsistechnology.com) for a complete listing of current offerings.

Ordering Information for GSI Synchronous Burst RAMs

| Org | Part Number ¹ | Type | Package | Speed ² (Mhz/ns) | T _A ³ |
|-----------|--------------------------|--------------|---------------------|--------------------------------|-----------------------------|
| 128K x 32 | GS840F32AGT-10 | Flow Through | RoHS-compliant TQFP | 10 | C |
| 128K x 32 | GS840F32AGT-12 | Flow Through | RoHS-compliant TQFP | 12 | C |
| 128K x 36 | GS840F36AGT-8 | Flow Through | RoHS-compliant TQFP | 8 | C |
| 128K x 36 | GS840F36AGT-8.5 | Flow Through | RoHS-compliant TQFP | 8.5 | C |
| 128K x 36 | GS840F36AGT-10 | Flow Through | RoHS-compliant TQFP | 8.5 | C |
| 128K x 36 | GS840F36AGT-12 | Flow Through | RoHS-compliant TQFP | 8.5 | C |
| 256K x 18 | GS840F18AGT-8I | Flow Through | RoHS-compliant TQFP | 8 | I |
| 256K x 18 | GS840F18AGT-8.5I | Flow Through | RoHS-compliant TQFP | 8.5 | I |
| 256K x 18 | GS840F18AGT-10I | Flow Through | RoHS-compliant TQFP | 10 | I |
| 256K x 18 | GS840F18AGT-12I | Flow Through | RoHS-compliant TQFP | 12 | I |
| 128K x 32 | GS840F32AGT-8I | Flow Through | RoHS-compliant TQFP | 8 | I |
| 128K x 32 | GS840F32AGT-8.5I | Flow Through | RoHS-compliant TQFP | 8.5 | I |
| 128K x 32 | GS840F32AGT-10I | Flow Through | RoHS-compliant TQFP | 10 | I |
| 128K x 32 | GS840F32AGT-12I | Flow Through | RoHS-compliant TQFP | 12 | I |
| 128K x 36 | GS840F36AGT-8I | Flow Through | RoHS-compliant TQFP | 8 | I |
| 128K x 36 | GS840F36AGT-8.5I | Flow Through | RoHS-compliant TQFP | 8.5 | I |
| 128K x 36 | GS840F36AGT-10I | Flow Through | RoHS-compliant TQFP | 10 | I |
| 128K x 36 | GS840F36AGT-12I | Flow Through | RoHS-compliant TQFP | 12 | I |

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS840F32AT-8T.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipelined mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
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4Mb Burst Datasheet Revision History

| Rev. Code: Old; New | Types of Changes Format or Content | Page /Revisions;Reason |
|--|---------------------------------------|---|
| GS84018/32/362/2000G; 840F18A_r1_02 | Content | • Updated pin description table |
| 840F18A_r1_02; 840F18A_r1_03 | Content/Format | • Added “non-A” speed bins to Operating Currents table, AC Electrical Characteristics table, and Ordering Information table • Updated format to fit Technical Documentation standards |
| 840F18A_r1_03; 840F18A_r1_04 | Content/Format | • Updated table on page 1 • Updated Operating Currents table on page 14 • Updated AC Electrical Characteristics table on page 14 • Updated format to comply with present Technical Documentation standards |
| 840F18A_r1_04; 840F18A_r1_05 | Content | • Reduced I_{DD} by 20 mA in table on page 1 and Operating Currents table |
| 840F18A_r1_05; 840F18A_r1_06 | Content | • Removed 7.5 ns references from entire datasheet |
| 840F18A_r1_06; 840F18A_r1_07 | Content | • Updated format • Added 7.5 ns speed bin |
| 840F18A_r1_07; 840F18A_r1_08 | Content | • Updated format • Matched current numbers to NBT parts • Removed Preliminary banner |
| 840F18A_r1_08; 840F18A_r1_09 | Content | • Added Pb-free TQFP information |
| 840F18A_r1_09; 840F18A_r1_10 | Content | • Added note to TQFP pinouts (pg. 2, 3, 4) • Updated Power Supply Voltage Ranges table (pg. 11) • Updated Logic Level tables (pg. 12) • Changed Pb-free to RoHS-compliant (entire document) |
| 840F18A_r1_10; 840F18A_r1_11 | Content | • Removed 7.5 ns references from entire datasheet |