

**100-Pin TQFP**  
**Commercial Temp**  
**Industrial Temp**
**2M x 18, 1M x 32, 1M x 36**  
**36Mb Sync Burst SRAMs**
**250 MHz–133 MHz**  
**2.5 V or 3.3 V V<sub>DD</sub>**  
**2.5 V or 3.3 V I/O**

### Features

- $\overline{FT}$  pin for user-configurable flow through or pipeline operation
- Single Cycle Deselect (SCD) operation
- 2.5 V or 3.3 V +10%/–10% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$  pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipeline mode
- Byte Write ( $\overline{BW}$ ) and/or Global Write ( $\overline{GW}$ ) operation
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC-standard 100-lead TQFP package
- RoHS-compliant 100-lead TQFP package available

### Functional Description

#### Applications

The GS832018/32/36T is a 37,748,736-bit high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

#### Controls

Addresses, data I/Os, chip enables ( $\overline{E1}$ ,  $E2$ ,  $\overline{E3}$ ), address burst control inputs ( $\overline{ADSP}$ ,  $\overline{ADSC}$ ,  $\overline{ADV}$ ), and write control inputs ( $\overline{Bx}$ ,  $\overline{BW}$ ,  $\overline{GW}$ ) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ( $\overline{G}$ ) and power down control (ZZ) are asynchronous inputs. Burst

cycles can be initiated with either  $\overline{ADSP}$  or  $\overline{ADSC}$  inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by  $\overline{ADV}$ . The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ( $\overline{LBO}$ ) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

#### Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the  $\overline{FT}$  mode pin (Pin 14). Holding the  $\overline{FT}$  mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding  $\overline{FT}$  high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

#### Byte Write and Global Write

Byte write operation is performed by using Byte Write enable ( $\overline{BW}$ ) input combined with one or more individual byte write signals ( $\overline{Bx}$ ). In addition, Global Write ( $\overline{GW}$ ) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

#### Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

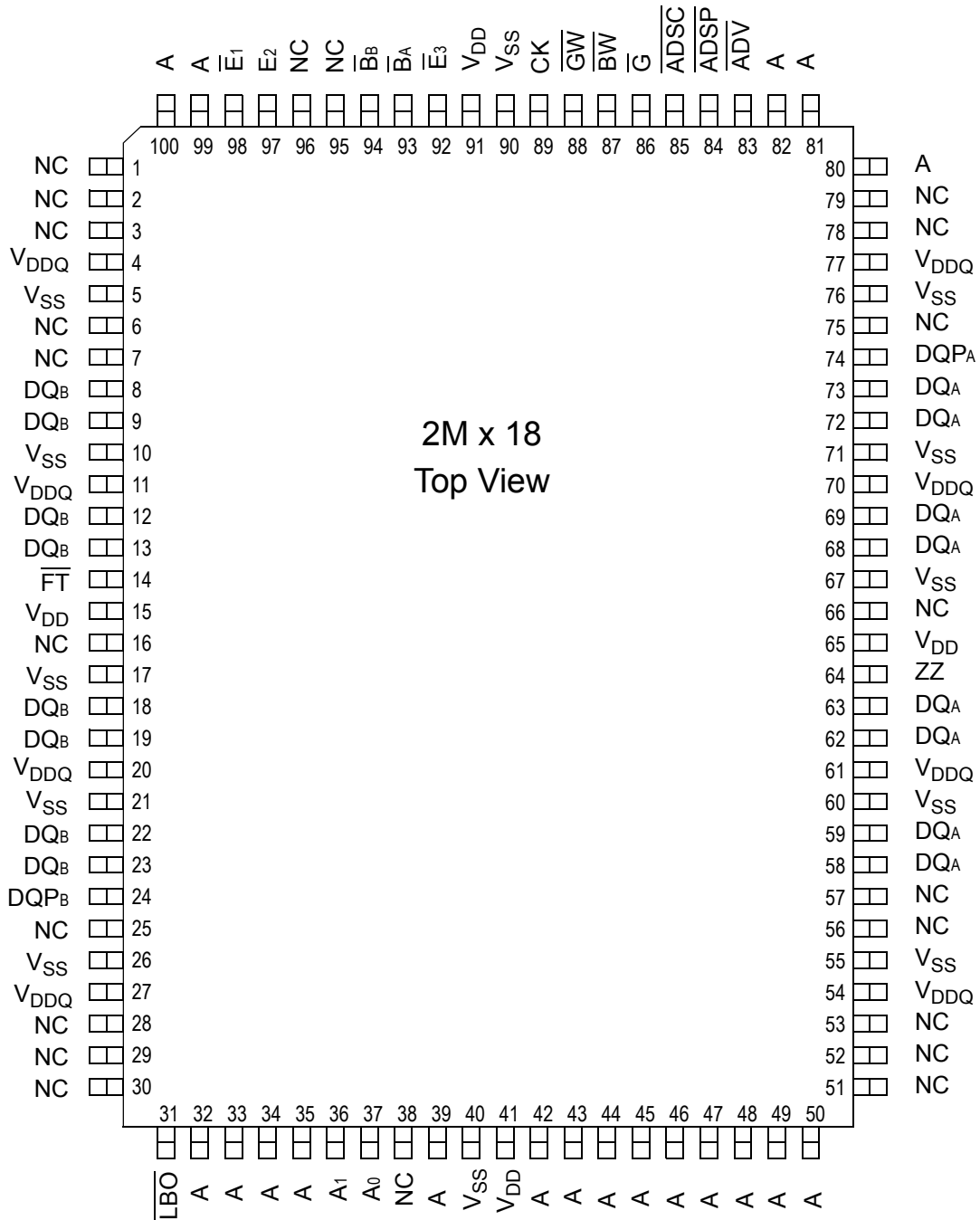
#### Core and Interface Voltages

The GS832018/32/36T operates on a 2.5 V or 3.3 V power supply. All input are 3.3 V and 2.5 V compatible. Separate output power ( $V_{DDQ}$ ) pins are used to decouple output noise from the internal circuits and are 3.3 V and 2.5 V compatible.

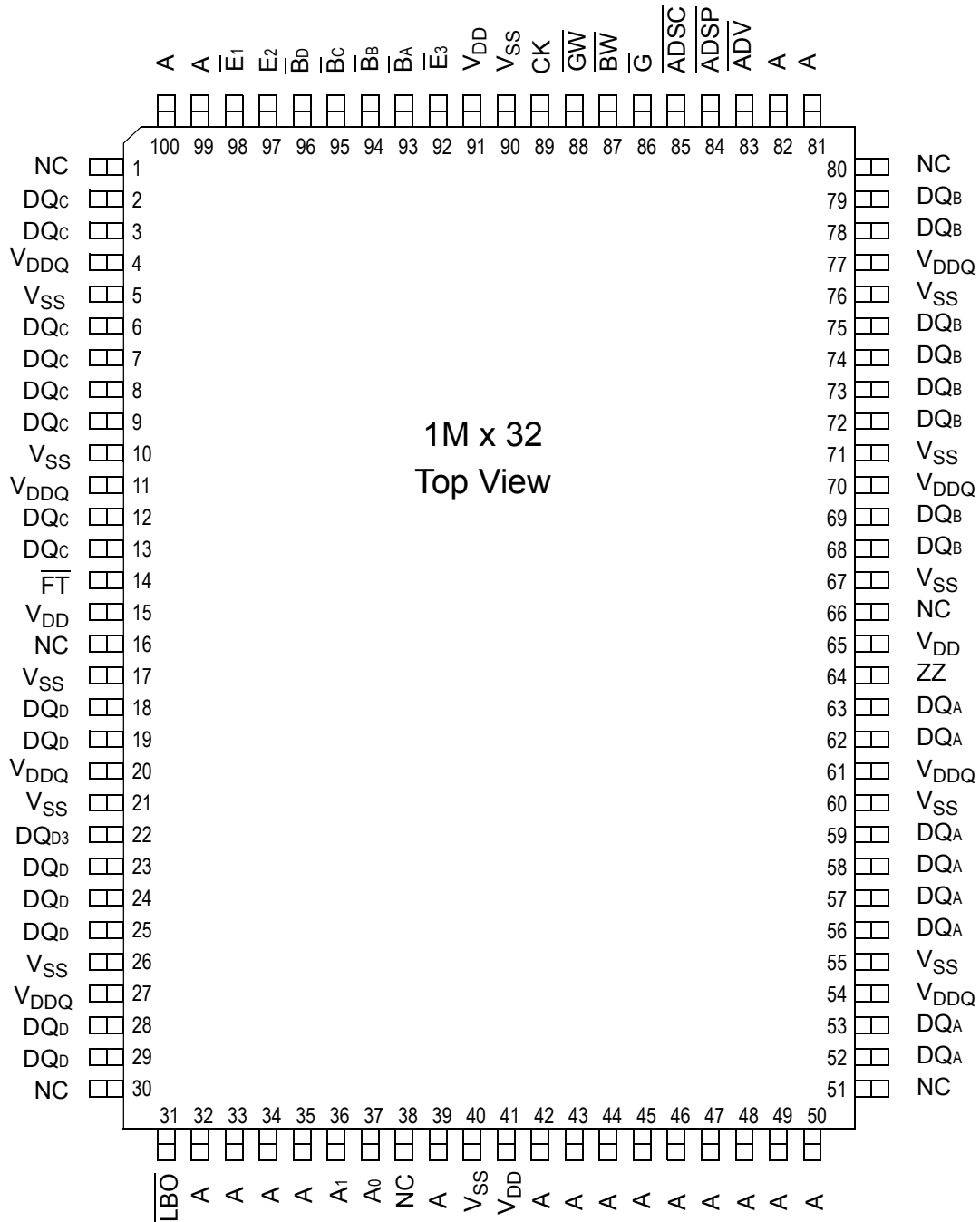
### Parameter Synopsis

		-250	-225	-200	-166	-150	-133	Unit
<b>Pipeline</b> <b>3-1-1-1</b>	$t_{kQ}$	2.5	2.7	3.0	3.5	3.8	4.0	ns
	tCycle	4.0	4.4	5.0	6.0	6.6	7.5	ns
	Curr (x18)	285	265	245	220	210	185	mA
	Curr (x32/x36)	350	320	295	260	240	215	mA
<b>Flow</b> <b>Through</b> <b>2-1-1-1</b>	$t_{kQ}$	6.5	7.0	7.5	8.0	8.5	8.5	ns
	tCycle	6.5	7.0	7.5	8.0	8.5	8.5	ns
	Curr (x18)	205	195	185	175	165	155	mA
	Curr (x32/x36)	235	225	210	200	190	175	mA

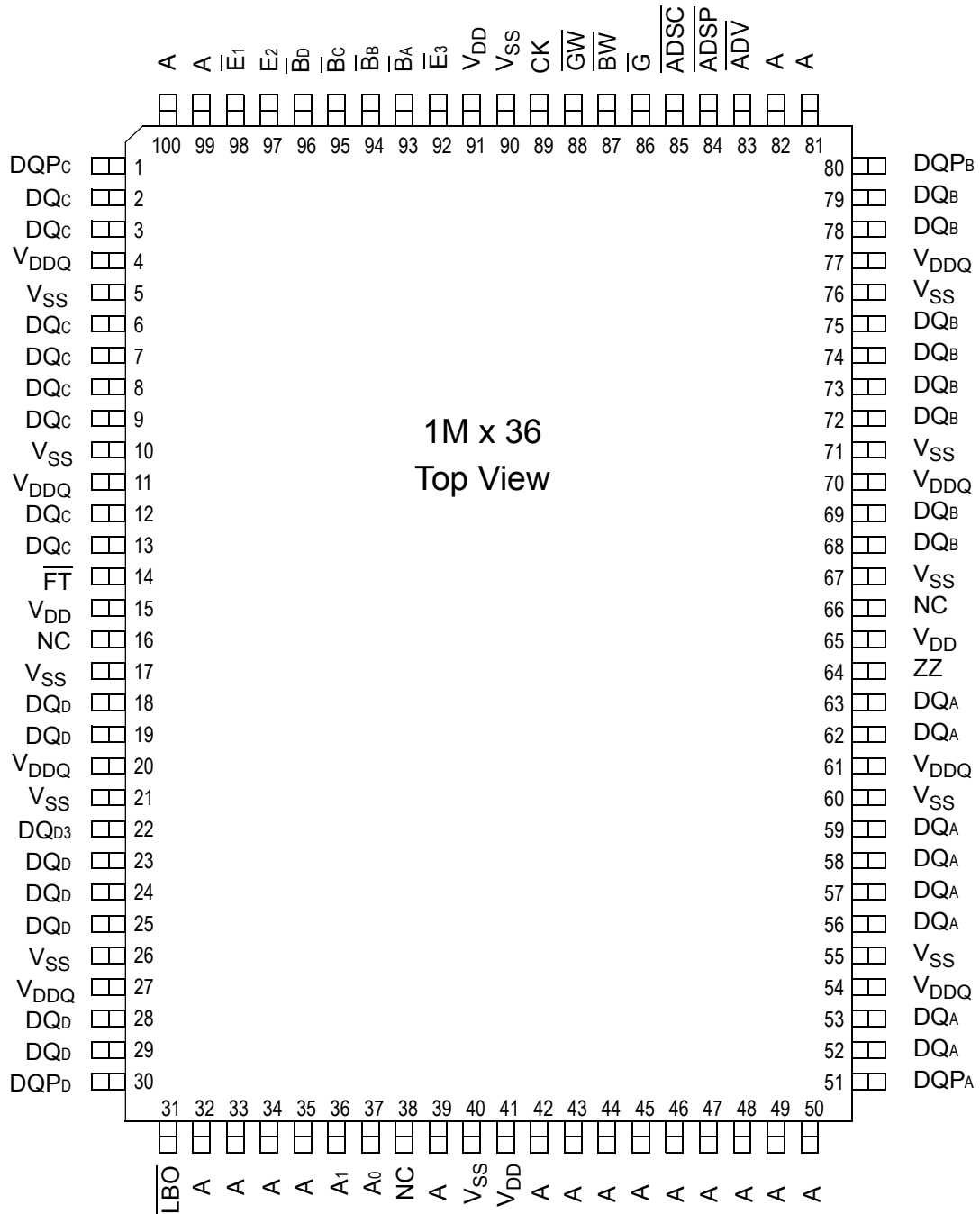
GS832018 100-Pin TQFP Pinout



GS832032 100-Pin TQFP Pinout



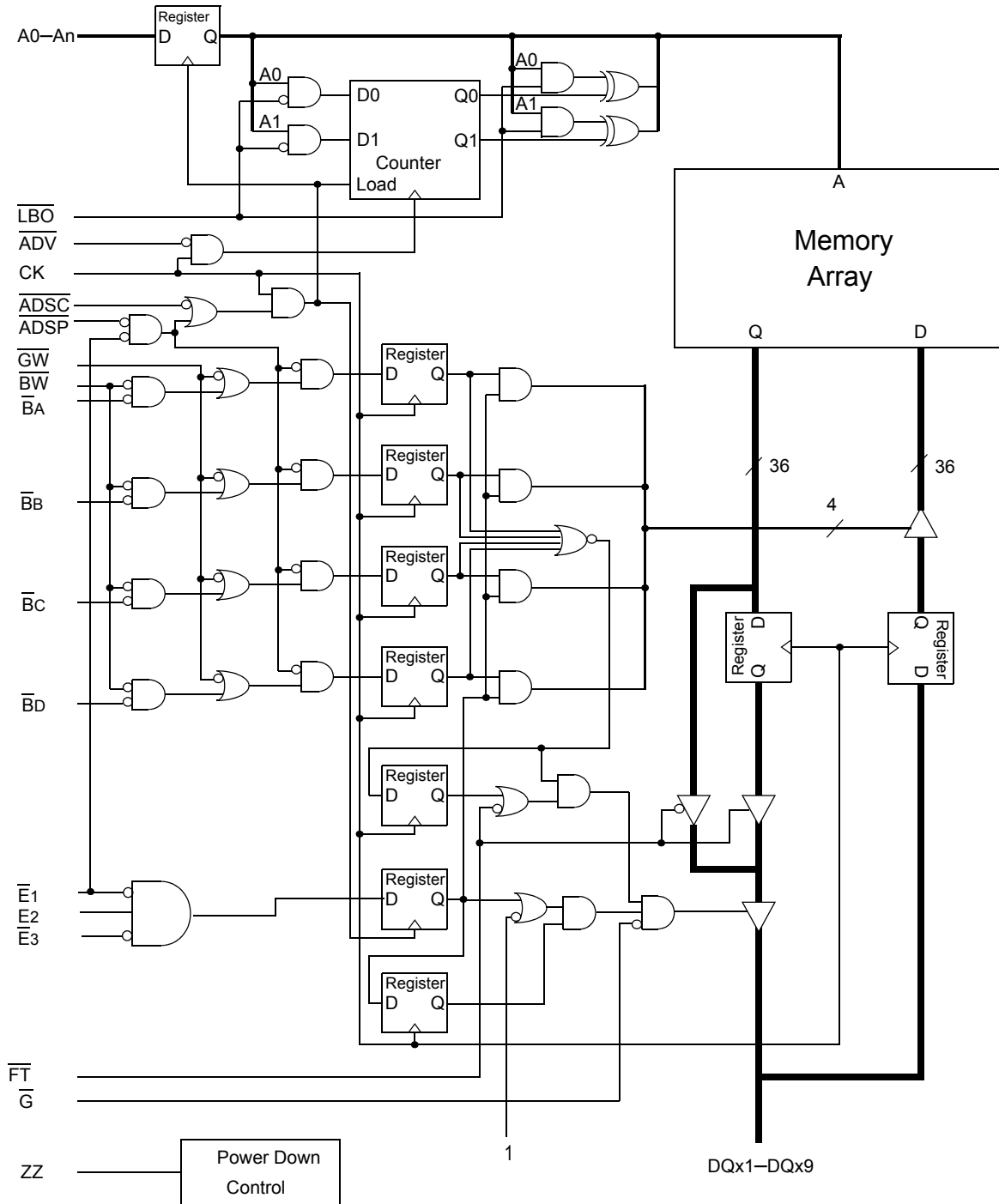
GS832036 100-Pin TQFP Pinout



**TQFP Pin Description**

<b>Symbol</b>	<b>Type</b>	<b>Description</b>
A <sub>0</sub> , A <sub>1</sub>	I	Address field LSBs and Address Counter preset Inputs
A	I	Address Inputs
DQ <sub>A</sub> DQ <sub>B1</sub> DQ <sub>C</sub> DQ <sub>D</sub>	I/O	Data Input and Output pins
NC		No Connect
$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
$\overline{B_A}$ , $\overline{B_B}$	I	Byte Write Enable for DQ <sub>A</sub> , DQ <sub>B</sub> Data I/Os; active low
$\overline{B_C}$ , $\overline{B_D}$	I	Byte Write Enable for DQ <sub>C</sub> , DQ <sub>D</sub> Data I/Os; active low
CK	I	Clock Input Signal; active high
$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E_1}$ , $\overline{E_3}$	I	Chip Enable; active low
E <sub>2</sub>	I	Chip Enable; active high
$\overline{G}$	I	Output Enable; active low
$\overline{ADV}$	I	Burst address counter advance enable; active low
$\overline{ADSP}$ , $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
ZZ	I	Sleep Mode control; active high
$\overline{FT}$	I	Flow Through or Pipeline mode; active low
$\overline{LBO}$	I	Linear Burst Order mode; active low
V <sub>DD</sub>	I	Core power supply
V <sub>SS</sub>	I	I/O and Core Ground
V <sub>DDQ</sub>	I	Output driver power supply

GS832018/32/36 Block Diagram



Note: Only x36 version shown for simplicity.

## Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$
Single/Dual Cycle Deselect Control	SCD	L	Dual Cycle Deselect
		H or NC	Single Cycle Deselect
FLXDrive Output Impedance Control	ZQ	L	High Drive (Low Impedance)
		H or NC	Low Drive (High Impedance)
9th Bit Enable	$\overline{\text{PE}}$	L or NC	Activate DQPx I/Os (x18/x3672 mode)
		H	Deactivate DQPx I/Os (x16/x3272 mode)

### Note:

There is a are pull-up devices on the ZQ, SCD, and  $\overline{\text{FT}}$  pins and a pull-down device on the ZZ pin, so those this input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

## Burst Counter Sequences

### Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

### Note:

The burst counter wraps to initial state on the 5th clock.

### Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

### Note:

The burst counter wraps to initial state on the 5th clock.

**Byte Write Truth Table**

Function	$\overline{GW}$	$\overline{BW}$	$\overline{BA}$	$\overline{BB}$	$\overline{BC}$	$\overline{BD}$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

**Notes:**

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs  $\overline{BA}$ ,  $\overline{BB}$ ,  $\overline{BC}$  and/or  $\overline{BD}$  may be used in any combination with  $\overline{BW}$  to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x32 and x36 versions.



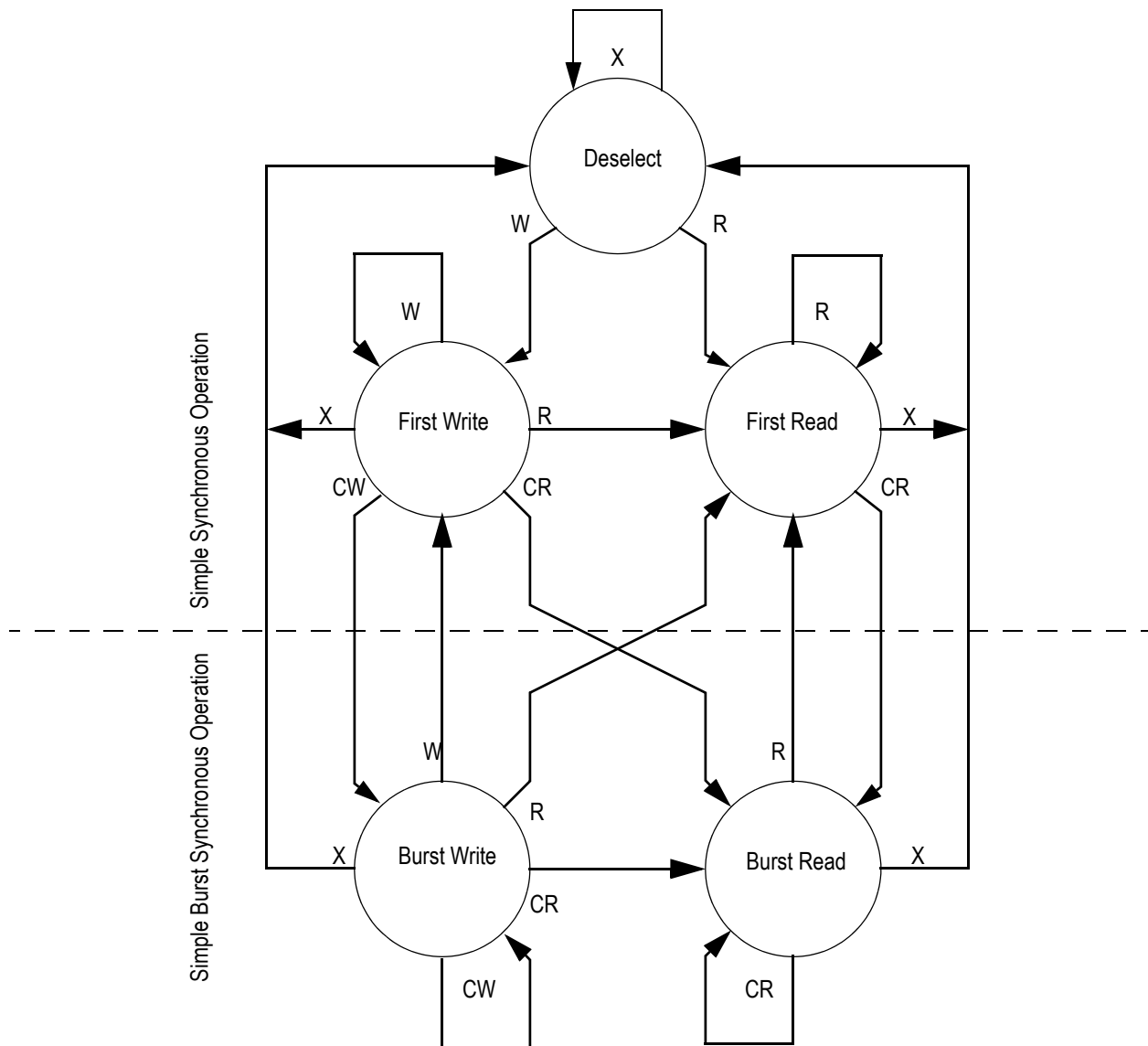
**Synchronous Truth Table**

Operation	Address Used	State Diagram Key <sup>5</sup>	$\bar{E}_1$	$E^2$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\bar{W}^3$	DQ <sup>4</sup>
<b>Deselect Cycle, Power Down</b>	<b>None</b>	<b>X</b>	<b>H</b>	<b>X</b>	<b>X</b>	<b>L</b>	<b>X</b>	<b>X</b>	<b>High-Z</b>
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
<b>Deselect Cycle, Power Down</b>	<b>None</b>	<b>X</b>	<b>L</b>	<b>F</b>	<b>H</b>	<b>L</b>	<b>X</b>	<b>X</b>	<b>High-Z</b>
Read Cycle, Begin Burst	External	R	L	T	L	X	X	X	Q
<b>Read Cycle, Begin Burst</b>	<b>External</b>	<b>R</b>	<b>L</b>	<b>T</b>	<b>H</b>	<b>L</b>	<b>X</b>	<b>F</b>	<b>Q</b>
<b>Write Cycle, Begin Burst</b>	<b>External</b>	<b>W</b>	<b>L</b>	<b>T</b>	<b>H</b>	<b>L</b>	<b>X</b>	<b>T</b>	<b>D</b>
<i>Read Cycle, Continue Burst</i>	<i>Next</i>	<i>CR</i>	<i>X</i>	<i>X</i>	<i>H</i>	<i>H</i>	<i>L</i>	<i>F</i>	<i>Q</i>
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
<i>Write Cycle, Continue Burst</i>	<i>Next</i>	<i>CW</i>	<i>X</i>	<i>X</i>	<i>H</i>	<i>H</i>	<i>L</i>	<i>T</i>	<i>D</i>
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

**Notes:**

1. X = Don't Care, H = High, L = Low
2. E = T (True) if  $E_2 = 1$  and  $\bar{E}_3 = 0$ ; E = F (False) if  $E_2 = 0$  or  $\bar{E}_3 = 1$
3. W = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4.  $\bar{G}$  is an asynchronous input.  $\bar{G}$  can be driven high at any time to disable active output drivers.  $\bar{G}$  low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying  $\overline{ADSP}$  high and  $\overline{ADSC}$  low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying  $\overline{ADSP}$  high and  $\overline{ADV}$  low while using  $\overline{ADSC}$  to load new addresses allows simple burst operations. See *ITALIC* items above.

## Simplified State Diagram


**Notes:**

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes  $\overline{G}$  is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ( $\overline{E1}$ ,  $E2$ , and  $E3$ ) and Write ( $\overline{BA}$ ,  $\overline{BB}$ ,  $\overline{BC}$ ,  $\overline{BD}$ ,  $\overline{BW}$ , and  $\overline{GW}$ ) control inputs, and that  $\overline{ADSP}$  is tied high and  $\overline{ADSC}$  is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and  $\overline{ADSC}$  control inputs, and assumes  $\overline{ADSP}$  is tied high and  $\overline{ADV}$  is tied low.

Simplified State Diagram with  $\overline{G}$ 

**Notes:**

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of  $\overline{G}$ .
2. Use of "Dummy Reads" (Read Cycles with  $\overline{G}$  High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in gray tone assume  $\overline{G}$  has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

**Absolute Maximum Ratings**

 (All voltages reference to  $V_{SS}$ )

Symbol	Description	Value	Unit
$V_{DD}$	Voltage on $V_{DD}$ Pins	-0.5 to 4.6	V
$V_{DDQ}$	Voltage in $V_{DDQ}$ Pins	-0.5 to 4.6	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to $V_{DDQ} + 0.5$ ( $\leq 4.6$ V max.)	V
$V_{IN}$	Voltage on Other Input Pins	-0.5 to $V_{DD} + 0.5$ ( $\leq 4.6$ V max.)	V
$I_{IN}$	Input Current on Any Pin	+/-20	mA
$I_{OUT}$	Output Current on Any I/O Pin	+/-20	mA
$P_D$	Package Power Dissipation	1.5	W
$T_{STG}$	Storage Temperature	-55 to 125	°C
$T_{BIAS}$	Temperature Under Bias	-55 to 125	°C

**Note:**

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

**Power Supply Voltage Ranges**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
3.3 V Supply Voltage	$V_{DD3}$	3.0	3.3	3.6	V	
2.5 V Supply Voltage	$V_{DD2}$	2.3	2.5	2.7	V	
3.3 V $V_{DDQ}$ I/O Supply Voltage	$V_{DDQ3}$	3.0	3.3	3.6	V	
2.5 V $V_{DDQ}$ I/O Supply Voltage	$V_{DDQ2}$	2.3	2.5	2.7	V	

**Notes:**

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be  $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$  not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

**V<sub>DDQ3</sub> Range Logic Levels**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V <sub>DD</sub> Input High Voltage	V <sub>IH</sub>	2.0	—	V <sub>DD</sub> + 0.3	V	1
V <sub>DD</sub> Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.8	V	1
V <sub>DDQ</sub> I/O Input High Voltage	V <sub>IHQ</sub>	2.0	—	V <sub>DDQ</sub> + 0.3	V	1,3
V <sub>DDQ</sub> I/O Input Low Voltage	V <sub>ILQ</sub>	-0.3	—	0.8	V	1,3

**Notes:**

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be  $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$  not to exceed 4.6 V maximum, with a pulse width not to exceed 20% t<sub>KC</sub>.
3. V<sub>IHQ</sub> (max) is voltage on V<sub>DDQ</sub> pins plus 0.3 V.

**V<sub>DDQ2</sub> Range Logic Levels**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V <sub>DD</sub> Input High Voltage	V <sub>IH</sub>	0.6*V <sub>DD</sub>	—	V <sub>DD</sub> + 0.3	V	1
V <sub>DD</sub> Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.3*V <sub>DD</sub>	V	1
V <sub>DDQ</sub> I/O Input High Voltage	V <sub>IHQ</sub>	0.6*V <sub>DD</sub>	—	V <sub>DDQ</sub> + 0.3	V	1,3
V <sub>DDQ</sub> I/O Input Low Voltage	V <sub>ILQ</sub>	-0.3	—	0.3*V <sub>DD</sub>	V	1,3

**Notes:**

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be  $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$  not to exceed 4.6 V maximum, with a pulse width not to exceed 20% t<sub>KC</sub>.
3. V<sub>IHQ</sub> (max) is voltage on V<sub>DDQ</sub> pins plus 0.3 V.

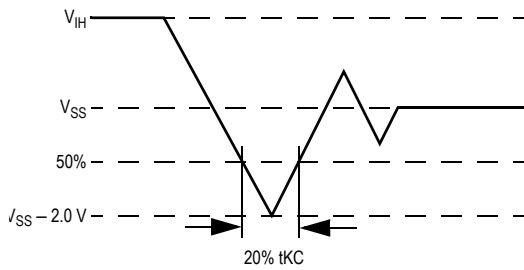
**Recommended Operating Temperatures**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature (Commercial Range Versions)	T <sub>A</sub>	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T <sub>A</sub>	-40	25	85	°C	2

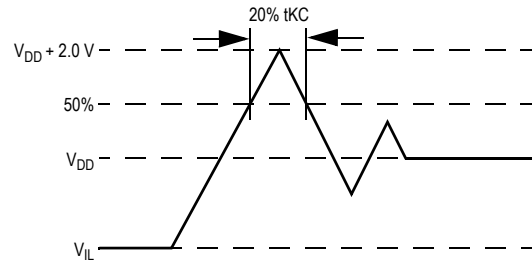
**Notes:**

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be  $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$  not to exceed 4.6 V maximum, with a pulse width not to exceed 20% t<sub>KC</sub>.

### Undershoot Measurement and Timing



### Overshoot Measurement and Timing



### Capacitance

( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{DD} = 2.5\text{ V}$ )

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$	4	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0\text{ V}$	6	7	pF

**Note:**

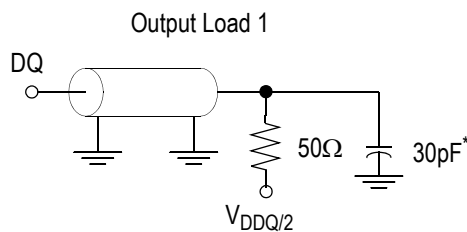
These parameters are sample tested.

### AC Test Conditions

Parameter	Conditions
Input high level	$V_{DD} - 0.2\text{ V}$
Input low level	$0.2\text{ V}$
Input slew rate	$1\text{ V/ns}$
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$
Output load	<b>Fig. 1</b>

**Notes:**

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Device is deselected as defined by the Truth Table.



\* Distributed Test Jig Capacitance

**DC Electrical Characteristics**

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	$I_{IL}$	$V_{IN} = 0$ to $V_{DD}$	-2 $\mu$ A	2 $\mu$ A
ZZInput Current	$I_{IN1}$	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0 V \leq V_{IN} \leq V_{IH}$	-1 $\mu$ A -1 $\mu$ A	1 $\mu$ A 100 $\mu$ A
$\overline{FT}$ Input Current	$I_{IN2}$	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0 V \leq V_{IN} \leq V_{IL}$	-100 $\mu$ A -1 $\mu$ A	1 $\mu$ A 1 $\mu$ A
Output Leakage Current (x36/x72)	$I_{OL}$	Output Disable, $V_{OUT} = 0$ to $V_{DD}$	-1 $\mu$ A	1 $\mu$ A
Output Leakage Current (x18)	$I_{OL}$	Output Disable, $V_{OUT} = 0$ to $V_{DD}$	-1 $\mu$ A	1 $\mu$ A
Output High Voltage	$V_{OH2}$	$I_{OH} = -8$ mA, $V_{DDQ} = 2.375$ V	1.7 V	—
Output High Voltage	$V_{OH3}$	$I_{OH} = -8$ mA, $V_{DDQ} = 3.135$ V	2.4 V	—
Output Low Voltage	$V_{OL}$	$I_{OL} = 8$ mA	—	0.4 V

### Operating Currents

Parameter	Test Conditions	Mode	Symbol	-250		-225		-200		-166		-150		-133		Unit	
				0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C				
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x32/ x36)	$I_{DD}$	300	320	275	295	255	275	225	245	210	230	190	210	mA	
			$I_{DDQ}$	50	50	45	45	40	40	35	35	30	30	25	25		
		(x18)	$I_{DD}$	210	220	200	210	190	200	180	190	170	180	160	170	150	mA
			$I_{DDQ}$	25	25	25	25	20	20	20	20	20	20	15	15		
Standby Current	$ZZ \geq V_{DD} - 0.2 V$	—	$I_{DD}$	260	280	240	260	225	245	200	220	190	210	170	190	mA	
			$I_{DDQ}$	25	25	25	25	20	20	20	20	20	20	15	15		
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	$I_{SB}$	60	80	60	80	60	80	60	80	60	80	60	80	mA	
			$I_{DD}$	100	115	95	110	90	105	85	100	85	100	80	95		
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	$I_{SB}$	60	80	60	80	60	80	60	80	60	80	60	80	mA	
			$I_{DD}$	85	100	85	100	80	95	80	95	75	90	70	85		

**Notes:**

1.  $I_{DD}$  and  $I_{DDQ}$  apply to any combination of  $V_{DD3}$ ,  $V_{DD2}$ ,  $V_{DDQ3}$ , and  $V_{DDQ2}$  operation.
2. All parameters listed are worst case scenario.



**AC Electrical Characteristics**

	Parameter	Symbol	-250		-225		-200		-166		-150		-133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	t <sub>KC</sub>	4.0	—	4.4	—	5.0	—	6.0	—	6.7	—	7.5	—	ns
	Clock to Output Valid	t <sub>KQ</sub>	—	2.5	—	2.7	—	3.0	—	3.5	—	3.8	—	4.0	ns
	Clock to Output Invalid	t <sub>KQX</sub>	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	t <sub>LZ</sub> <sup>1</sup>	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Setup time	t <sub>S</sub>	1.2	—	1.3	—	1.4	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	t <sub>H</sub>	0.2	—	0.3	—	0.4	—	0.5	—	0.5	—	0.5	—	ns
Flow Through	Clock Cycle Time	t <sub>KC</sub>	6.5	—	7.0	—	7.5	—	8.0	—	8.5	—	8.5	—	ns
	Clock to Output Valid	t <sub>KQ</sub>	—	6.5	—	7.0	—	7.5	—	8.0	—	8.5	—	8.5	ns
	Clock to Output Invalid	t <sub>KQX</sub>	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	t <sub>LZ</sub> <sup>1</sup>	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Setup time	t <sub>S</sub>	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	t <sub>H</sub>	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	t <sub>KH</sub>	1.3	—	1.3	—	1.3	—	1.3	—	1.5	—	1.7	—	ns
	Clock LOW Time	t <sub>KL</sub>	1.5	—	1.5	—	1.5	—	1.5	—	1.7	—	2	—	ns
	Clock to Output in High-Z	t <sub>HZ</sub> <sup>1</sup>	1.5	2.5	1.5	2.7	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	ns
	$\bar{G}$ to Output Valid	t <sub>OE</sub>	—	2.5	—	2.7	—	3.0	—	3.5	—	3.8	—	4.0	ns
	$\bar{G}$ to output in Low-Z	t <sub>OLZ</sub> <sup>1</sup>	0	—	0	—	0	—	0	—	0	—	0	—	ns
	$\bar{G}$ to output in High-Z	t <sub>OHZ</sub> <sup>1</sup>	—	2.5	—	2.7	—	3.0	—	3.0	—	3.0	—	3.0	ns
	ZZ setup time	t <sub>ZZS</sub> <sup>2</sup>	5	—	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	t <sub>ZZH</sub> <sup>2</sup>	1	—	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	t <sub>ZZR</sub>	20	—	20	—	20	—	20	—	20	—	20	—	ns

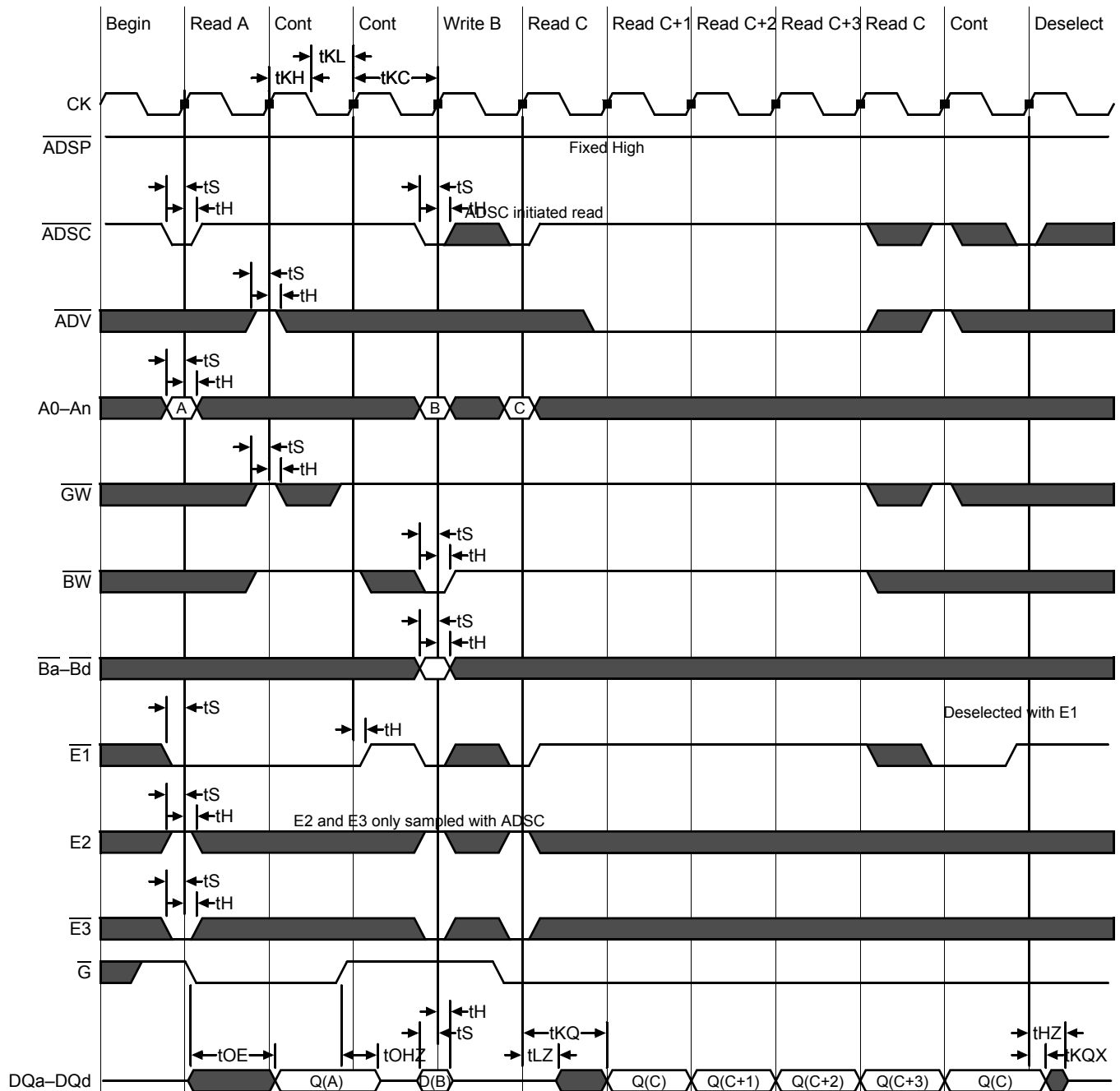
**Notes:**

1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

### Pipeline Mode Timing



## Flow Through Mode Timing

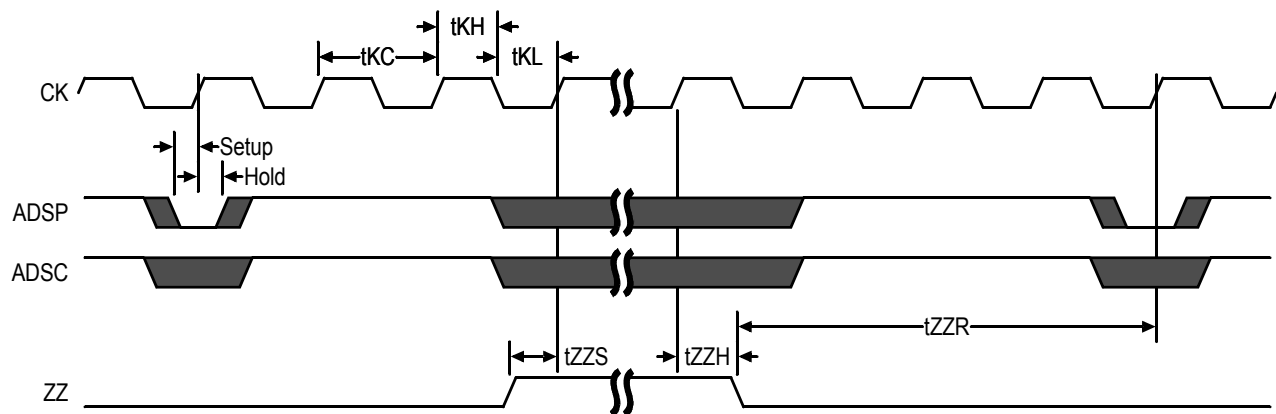


## Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after 2 cycles of wake up time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to  $I_{SB2}$ . The duration of Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z. The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high,  $I_{SB2}$  is guaranteed after the time  $t_{ZZI}$  is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during  $t_{ZZR}$ , only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

**Sleep Mode Timing Diagram**



## TQFP Package Drawing (Package T)

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
$\theta$	Lead Angle	0°	—	7°


**Notes:**

1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

**Ordering Information for GSI Synchronous Burst RAMs**

Org	Part Number <sup>1</sup>	Type	Package	Speed <sup>2</sup> (MHz/ns)	T <sub>A</sub> <sup>3</sup>
2M x 18	GS832018T-250	Pipeline/Flow Through	TQFP	250/6.5	C
2M x 18	GS832018T-225	Pipeline/Flow Through	TQFP	225/7	C
2M x 18	GS832018T-200	Pipeline/Flow Through	TQFP	200/7.5	C
2M x 18	GS832018T-166	Pipeline/Flow Through	TQFP	166/8	C
2M x 18	GS832018T-150	Pipeline/Flow Through	TQFP	150/8.5	C
2M x 18	GS832018T-133	Pipeline/Flow Through	TQFP	133/8.5	C
1M x 32	GS832032T-250	Pipeline/Flow Through	TQFP	250/6.5	C
1M x 32	GS832032T-225	Pipeline/Flow Through	TQFP	225/7	C
1M x 32	GS832032T-200	Pipeline/Flow Through	TQFP	200/7.5	C
1M x 32	GS832032T-166	Pipeline/Flow Through	TQFP	166/8	C
1M x 32	GS832032T-150	Pipeline/Flow Through	TQFP	150/8.5	C
1M x 32	GS832032T-133	Pipeline/Flow Through	TQFP	133/8.5	C
1M x 36	GS832036T-250	Pipeline/Flow Through	TQFP	250/6.5	C
1M x 36	GS832036T-225	Pipeline/Flow Through	TQFP	225/7	C
1M x 36	GS832036T-200	Pipeline/Flow Through	TQFP	200/7.5	C
1M x 36	GS832036T-166	Pipeline/Flow Through	TQFP	166/8	C
1M x 36	GS832036T-150	Pipeline/Flow Through	TQFP	150/8.5	C
1M x 36	GS832036T-133	Pipeline/Flow Through	TQFP	133/8.5	C
2M x 18	GS832018T-250I	Pipeline/Flow Through	TQFP	250/6.5	I
2M x 18	GS832018T-225I	Pipeline/Flow Through	TQFP	225/7	I
2M x 18	GS832018T-200I	Pipeline/Flow Through	TQFP	200/7.5	I
2M x 18	GS832018T-166I	Pipeline/Flow Through	TQFP	166/8	I
2M x 18	GS832018T-150I	Pipeline/Flow Through	TQFP	150/8.5	I
2M x 18	GS832018T-133I	Pipeline/Flow Through	TQFP	133/8.5	I
1M x 32	GS832032T-250I	Pipeline/Flow Through	TQFP	250/6.5	I
1M x 32	GS832032T-225I	Pipeline/Flow Through	TQFP	225/7	I
1M x 32	GS832032T-200I	Pipeline/Flow Through	TQFP	200/7.5	I
1M x 32	GS832032T-166I	Pipeline/Flow Through	TQFP	166/8	I
1M x 32	GS832032T-150I	Pipeline/Flow Through	TQFP	150/8.5	I

**Notes:**

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS832018T-150IT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T<sub>A</sub> = C = Commercial Temperature Range. T<sub>A</sub> = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site ([www.gsistechnology.com](http://www.gsistechnology.com)) for a complete listing of current offerings.

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1M x 36	GS832036T-250I	Pipeline/Flow Through	TQFP	250/6.5	I
1M x 36	GS832036T-225I	Pipeline/Flow Through	TQFP	225/7	I
1M x 36	GS832036T-200I	Pipeline/Flow Through	TQFP	200/7.5	I
1M x 36	GS832036T-166I	Pipeline/Flow Through	TQFP	166/8	I
1M x 36	GS832036T-150I	Pipeline/Flow Through	TQFP	150/8.5	I
1M x 36	GS832036T-133I	Pipeline/Flow Through	TQFP	133/8.5	I
2M x 18	GS832018GT-250	Pipeline/Flow Through	RoHS-compliant TQFP	250/6.5	C
2M x 18	GS832018GT-225	Pipeline/Flow Through	RoHS-compliant TQFP	225/7	C
2M x 18	GS832018GT-200	Pipeline/Flow Through	RoHS-compliant TQFP	200/7.5	C
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2M x 18	GS832018GT-225I	Pipeline/Flow Through	RoHS-compliant TQFP	225/7	I
2M x 18	GS832018GT-200I	Pipeline/Flow Through	RoHS-compliant TQFP	200/7.5	I
2M x 18	GS832018GT-166I	Pipeline/Flow Through	RoHS-compliant TQFP	166/8	I
2M x 18	GS832018GT-150I	Pipeline/Flow Through	RoHS-compliant TQFP	150/8.5	I
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1M x 32	GS832032GT-133I	Pipeline/Flow Through	RoHS-compliant TQFP	133/8.5	I
1M x 36	GS832036GT-250I	Pipeline/Flow Through	RoHS-compliant TQFP	250/6.5	I
1M x 36	GS832036GT-225I	Pipeline/Flow Through	RoHS-compliant TQFP	225/7	I
1M x 36	GS832036GT-200I	Pipeline/Flow Through	RoHS-compliant TQFP	200/7.5	I
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1M x 36	GS832036GT-150I	Pipeline/Flow Through	RoHS-compliant TQFP	150/8.5	I
1M x 36	GS832036GT-133I	Pipeline/Flow Through	RoHS-compliant TQFP	133/8.5	I

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**36Mb Sync SRAM Datasheet Revision History**

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
832018_r1		• Creation of new datasheet
832018_r1; 832018_r1_01	Content	<ul style="list-style-type: none"> <li>• Updated AC Characteristics table</li> <li>• Updated FT power numbers</li> <li>• Corrected Absolute Maximum Ratings table</li> <li>• Corrected Capacitance table</li> <li>• Updated tKQ (PL) numbers in table on page 1</li> <li>• Updated DC Electrical Characteristics table</li> <li>• Removed Output Load 2 diagram on page 15</li> <li>• Updated standby current numbers in Operating Currents table</li> </ul>
832018_r1_01; 832018_r1_02	Content/Format	<ul style="list-style-type: none"> <li>• Updated format</li> <li>• Added RoHS-compliant information for TQFP package</li> <li>• (Rev. 1.02b: Removed status column from ordering information table)</li> </ul>
832018_r1_02; 832018_r1_03	Content/Format	<ul style="list-style-type: none"> <li>• Updated format</li> <li>• (Rev. 1.03b: Removed status column from ordering information table)</li> </ul>