Freescale Semiconductor
Advance Information

Document Number: MC33903_4_5
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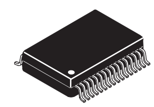
RoHS

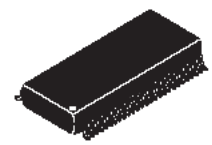
SBC Gen2 with CAN High Speed and LIN Interface

33903/4/5

SYSTEM BASIS CHIP



EK SUFFIX (PB-FREE)
98ASA10556D
32-PIN SOIC



EK SUFFIX (PB-FREE)
98ASA10506D
54-PIN SOIC

ORDERING INFORMATION
See Device Variations on page 2

The 33903/4/5 is the second generation family of System Basis Chips, which combines several features and enhances present module designs. The device works as an advanced power management unit for the MCU, additional integrated circuits such as sensors, and CAN transceivers. It has a built-in enhanced high speed CAN interface (ISO11898-2 and -5), with local and bus failure diagnostics, protection, and fail safe operation mode. The SBC may include one or two LIN 2.1 interfaces with LIN output pin switches. It includes up to four wake-up input pins than can also be configured as output drivers for flexibility.

This device implements multiple Low Power modes, with very low-current consumption. In addition, the device is part of a family concept where pin compatibility, among the various devices with and without LIN interfaces, add versatility to module design.

The 33903/4/5 also implements an innovative and advanced fail-safe state machine and concept solution.

Features

- Voltage regulator for MCU, 5.0 or 3.3 V, part number selectable, with possibility of usage external PNP to extend current capability and share power dissipation
- Voltage, current, and temperature protection
- Extremely low quiescent current in low power modes
- Fully-protected embedded 5.0 V regulator for the CAN driver
- Multiple under-voltage detections to address various MCU specifications and system operation modes (i.e. cranking)
- Auxiliary 5.0 or 3.3 V SPI configurable regulator, for additional ICs, with over-current detection and under-voltage protection
- MUX output pin for device internal analog signal monitoring and power supply monitoring
- Advanced SPI, MCU, ECU power supply, and critical pins diagnostics and monitoring.
- Multiple wake-up sources in low power modes: CAN or LIN bus, I/O transition, automatic timer, SPI message, and V_{DD} over-current detection.
- ISO11898-5 high speed CAN interface compatibility for baud rates of 40 kb/s to 1.0 Mb/s
- Pb-free packaging designated by suffix code EK

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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DEVICE VARIATIONS

Table 1. Device Variations - (All devices rated at T_A = -40 TO 125 °C)

Freescale Part Number	V_{DD} output voltage	CAN interface	LIN interface(s)	Wake-up input / LIN master termination	Package	V_{AUX}	V_{SENSE}	MUX
MC33905D (Dual LIN)								
MCZ33905D3EK/R2	3.3 V	1	2	2 wake-up + 2 LIN terms or 3 wake-up + 1 LIN terms or 4 wake-up + no LIN terms	SOIC 54 pins exposed pad	Yes	Yes	Yes
*MCZ33905BD3EK/R2								
MCZ33905D5EK/R2	5.0 V							
*MCZ33905BD5EK/R2								
MC33905S (Single LIN)								
MCZ33905S3EK/R2	3.3 V	1	1	3 wake-up + 1 LIN terms or 4 wake-up + no LIN terms	SOIC 32 pins exposed pad	Yes	Yes	Yes
*MCZ33905BS3EK/R2								
MCZ33905S5EK/R2	5.0 V							
*MCZ33905BS5EK/R2								
MC33904								
MCZ33904A3EK/R2	3.3 V	1	no	4 wake-up	SOIC 32 pins exposed pad	Yes	Yes	Yes
*MCZ33904B3EK/R2								
MCZ33904A5EK/R2	5.0 V							
*MCZ33904B5EK/R2								
MC33903								
*MCZ33903B3EK/R2	3.3 V(1)	1	no	1 wake-up	SOIC 32 pins exposed pad	No	No	No
*MCZ33903B5EK/R2	5.0 V(1)							

Notes

1. V_{DD} does not allow usage of an external PNP on the 33903. Output current limited to 100 mA.

* "B" versions are recommended for new design. Changes resolved V_{SUP} slow ramp up behavior, enhanced device current consumption and improved oscillator.

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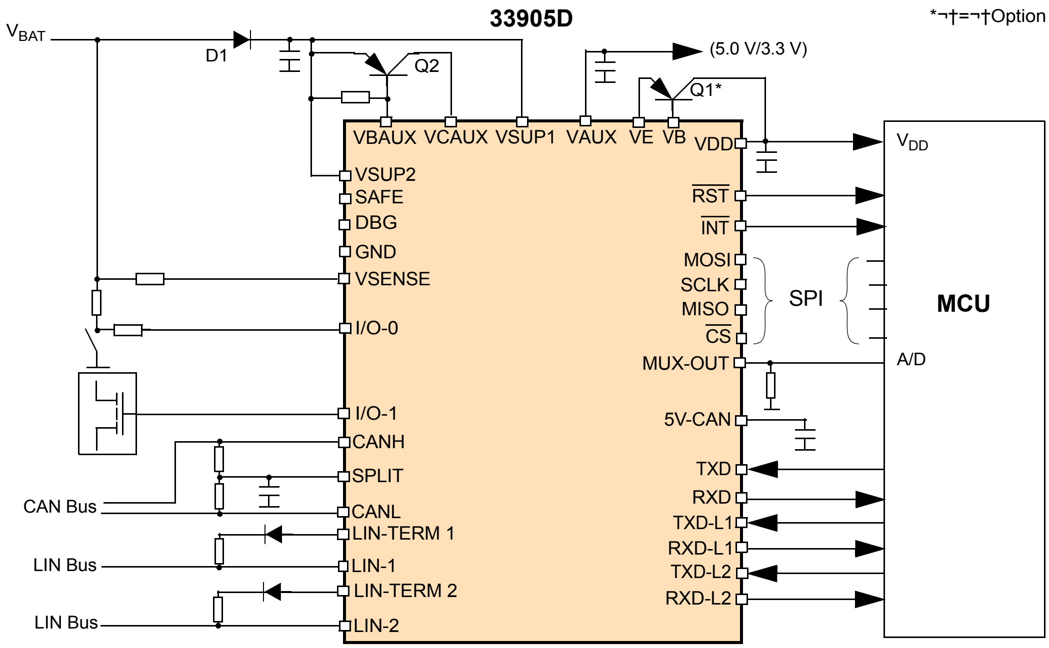


Figure 1. 33905D Simplified Application Diagram

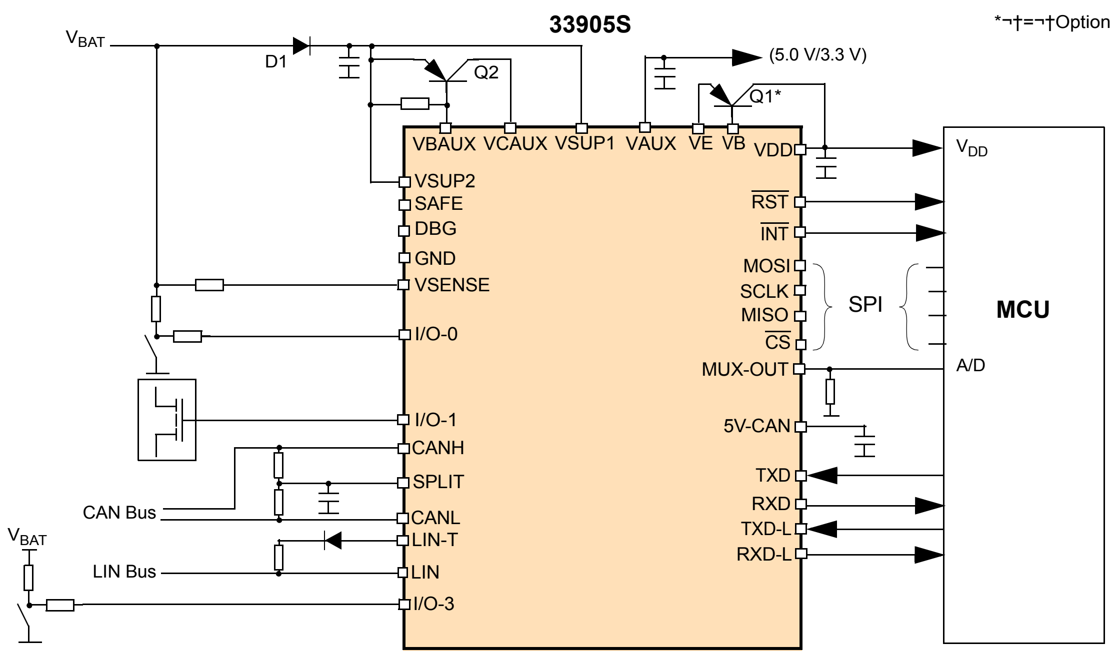


Figure 2. 33905S Simplified Application Diagram

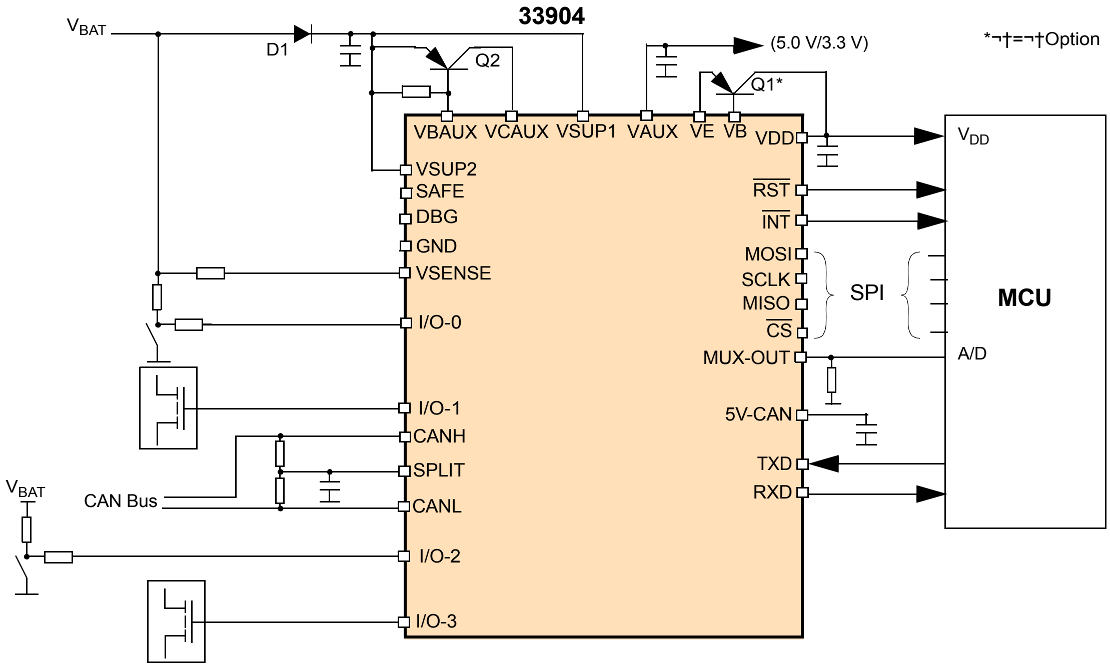


Figure 3. 33904 Simplified Application Diagram

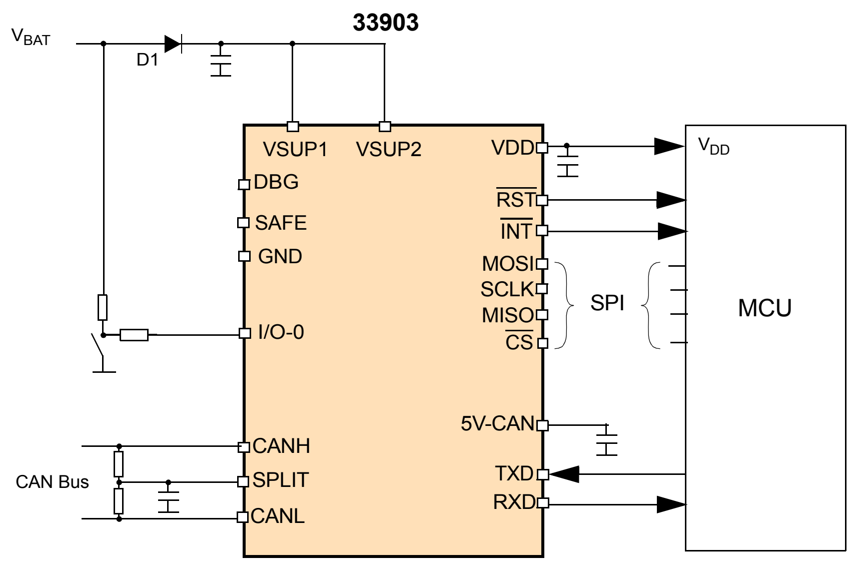


Figure 4. 33903 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

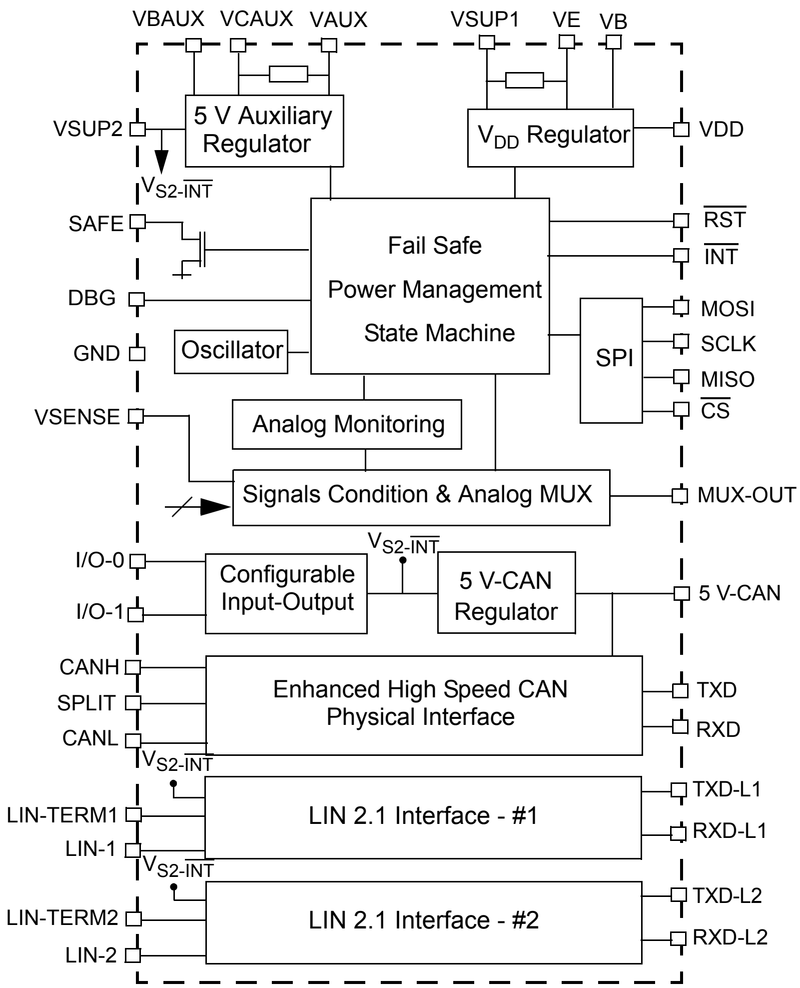


Figure 5. 33905D Internal Block Diagram

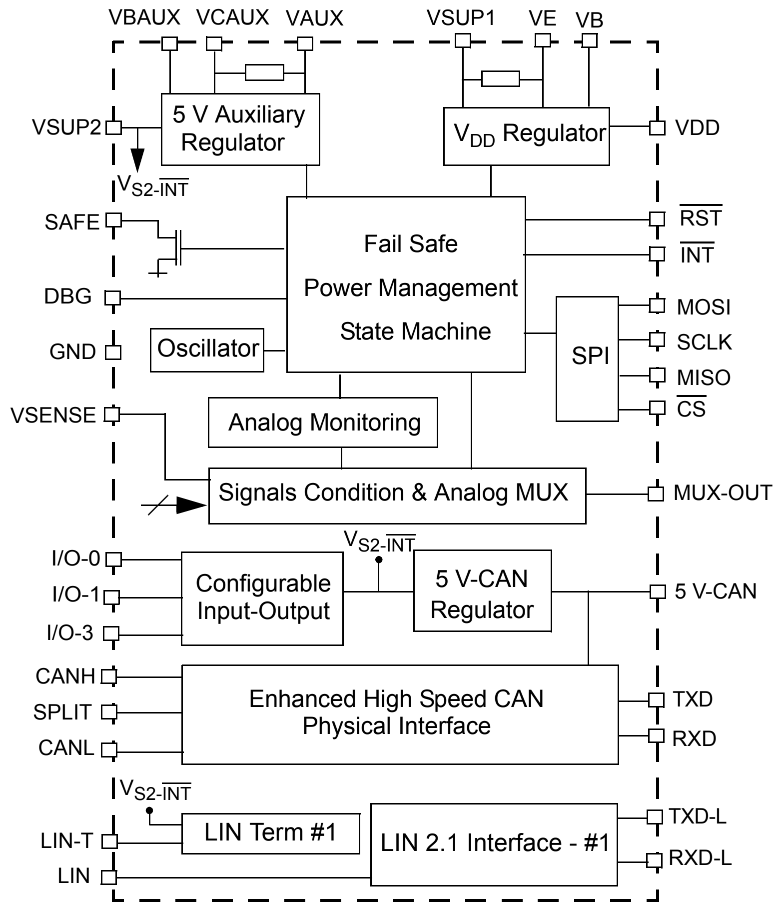


Figure 6. 33905S Internal Block Diagram

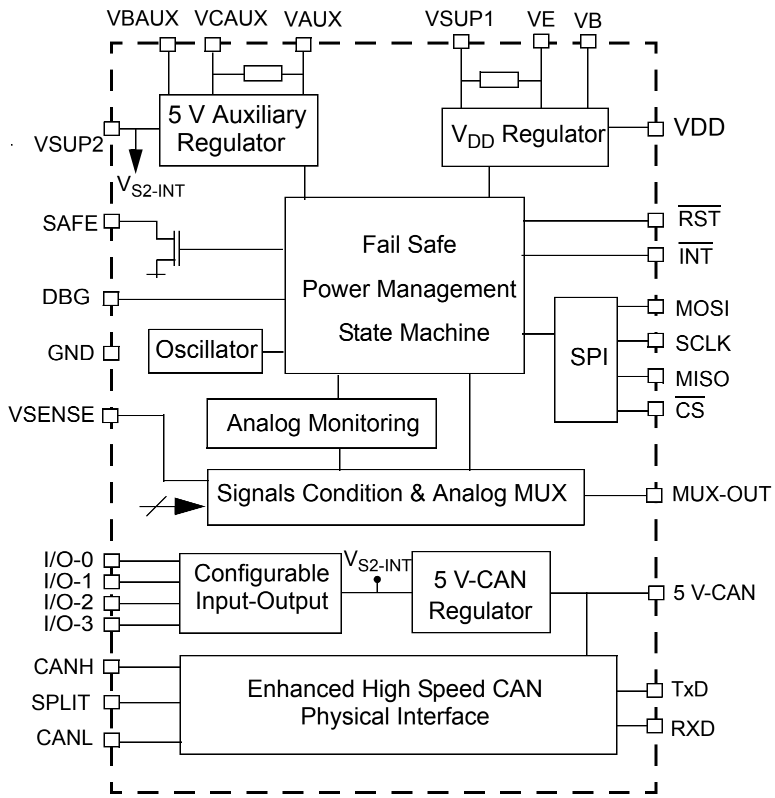


Figure 7. 33904 Internal Block Diagram

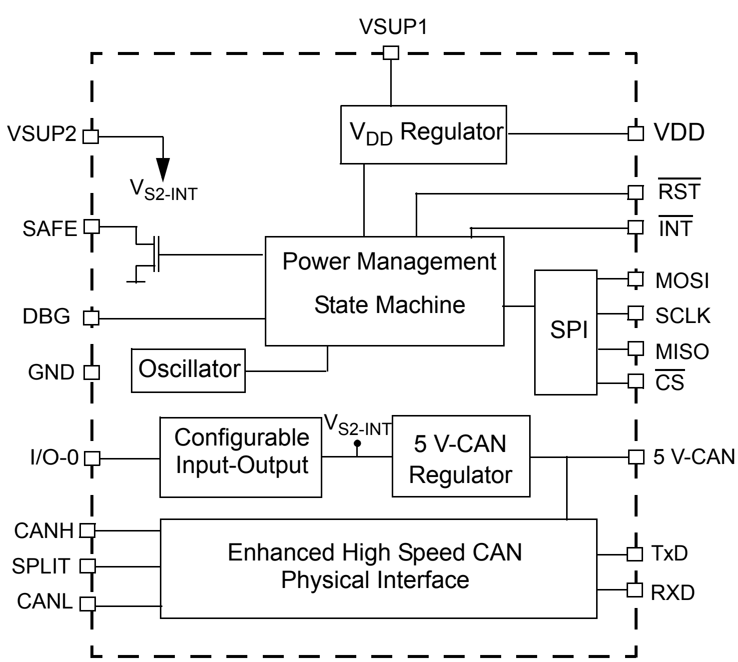
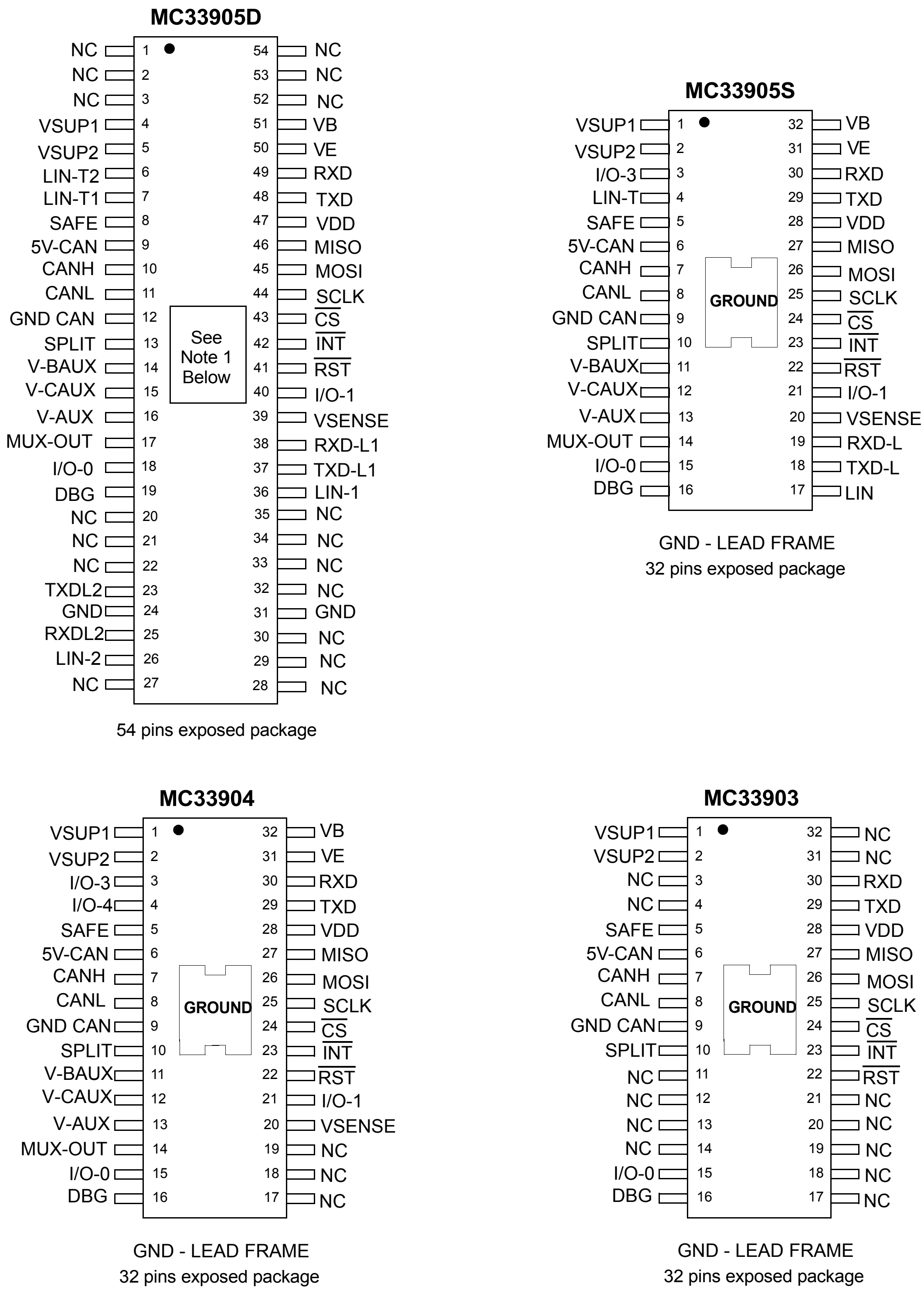


Figure 8. 33903 Internal Block Diagram

PIN CONNECTIONS



Note 1: Exposed pad should be connected to electrical ground

Figure 9. 33903/4/5 Pin Connections

Table 2. 33903/4/5 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 30.

Pin # 33905D	Pin # 33905S	Pin # 33904	Pin # 33903	Pin Name	Pin Function	Formal Name	Definition
1-3,20-22,27-30,32-35,52-54	N/A	17, 18, 19	2-4,11-13, 17-21, 31, 32	N/C	No Connect	-	No Connection
4	1	1	1	VSUP1	Power	Battery Voltage Supply 1	Supply input for the device internal supplies, power on reset circuitry and the V_{DD} regulator.
5	2	2	2	VSUP2	Power	Battery Voltage Supply 2	Supply input for 5 V-CAN regulator, V_{AUX} regulator, I/O and LIN pins.
6	3	3	N/A	LIN-T2 or I/O-3	Output or Input/Output	LIN Termination 2 or Input/Output 3	33905D, Output pin for the LIN2 master node termination resistor. or 33904/33905S, Configurable pin as an input or high side output, for connection to external circuitry (switched or small load). The input can be used as a programmable wake-up input in Low Power mode. When used as a high side, no over-temperature protection is implemented. A basic short to GND protection function, based on switch drain-source over-voltage detection, is available.
7	4	4	N/A	LIN-T1 or LIN-T I/O-2	Output or Input/Output	LIN Termination 1 or Input/Output 2 I/O-2	33905D, Output pin for the LIN1 master node termination resistor. or 33905S, 33905D, Configurable pin as an input or high side output, for connection to external circuitry (switched or small load). The input can be used as a programmable wake-up input in Low Power mode. When used as a high side, no over-temperature protection is implemented. A basic short to GND protection function, based on switch drain-source over-voltage detection, is available. 33904, Configurable pin as input or high side output, for connection to external circuitry (switched or small load). Input can be used as a programmable wake-up input from Low Power mode. When used as high side, no over-temperature protection is implemented. A basic short to GND protection function based on switch drain-source over-voltage detection is available.
8	5	5	5	SAFE	Output	Safe Output (Active LOW)	Output of the safe circuitry. The pin is asserted LOW in case of a safe condition is detected (e.g.: software watchdog is not triggered, V_{DD} low, issue on the RESET pin, etc.). Open drain structure.
9	6	6	6	5 V-CAN	Output	5V-CAN	Output voltage for the embedded CAN interface. A capacitor must be connected to this pin.
10	7	7	7	CANH	Output	CAN High	CAN high output.
11	8	8	8	CANL	Output	CAN Low	CAN low output.
12	9	9	9	GND-CAN	Ground	GND-CAN	Power GND of the embedded CAN interface
13	10	10	10	SPLIT	Output	SPLIT Output	Output pin for connection to the middle point of the split CAN termination
14	11	11	N/A	VBAUX	Output	VB Auxiliary	Output pin for external path PNP transistor base

Table 2. 33903/4/5 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 30.

Pin # 33905D	Pin # 33905S	Pin # 33904	Pin # 33903	Pin Name	Pin Function	Formal Name	Definition
15	12	12	N/A	VCAUX	Output	VCOLLECTOR Auxiliary	Output pin for external path PNP transistor collector
16	13	13	N/A	VAUX	Output	VOUT Auxiliary	Output pin for the auxiliary voltage.
17	14	14	N/A	MUX-OUT	Output	Multiplex Output	Multiplexed output to be connected to an MCU A/D input. Selection of the analog parameter available at MUX-OUT is done via the SPI. A switchable internal pull-down resistor is integrated for V_{DD} current sense measurements.
18	15	15	15	I/O-0	Input/Output	Input/Output 0	Configurable pin as an input or output, for connection to external circuitry (switched or small load). The voltage level can be read by the SPI and via the MUX output pin. The input can be used as a programmable wake-up input in Low Power mode. In low power, when used as an output, the high side or low side can be activated for a cyclic sense function.
19	16	16	16	DBG	Input	Debug	Input to activate the Debug mode. In Debug mode, no watchdog refresh is necessary. Outside of Debug mode, connection of a resistor between DBG and GND allows the selection of Safe mode functionality.
23	N/A	N/A	N/A	TXD-L2	Input	LIN Transmit Data 2	LIN bus transmit data input. Includes an internal pull-up resistor to VDD.
24,31	N/A	N/A	N/A	GND	Ground	Ground	Ground of the IC.
25	N/A	N/A	N/A	RXD-L2	Output	LIN Receive Data	LIN bus receive data output.
26	N/A	N/A	N/A	LIN2	Input/Output	LIN bus	LIN bus input output connected to the LIN bus.
36	17	17	N/A	33905D LIN-1 33905S LIN	Input/Output	LIN bus	LIN bus input output connected to the LIN bus.
37	18	18	N/A	33905D TXD-L1 33905S TXD-L	Input	LIN Transmit Data	LIN bus transmit data input. Includes an internal pull-up resistor to VDD.
38	19	19	N/A	33905D RXD-L1 33905S RXD-L	Output	LIN Receive Data	LIN bus receive data output.
39	20	20	N/A	VSENSE	Input	Sense input	Direct battery voltage input sense. A serial resistor is required to limit the input current during high voltage transients.
40	21	21	N/A	I/O-1	Input/Output	Input Output 1	Configurable pin as an input or output, for connection to external circuitry (switched or small load). The voltage level can be read by the SPI and via the MUX output pin. The input can be used as a programmable wake-up input in Low Power mode. Can be used in association with I/O-0 for a cyclic sense function in Low Power mode.
41	22	22	22	RST	Output	Reset Output (Active LOW)	This is the device reset output whose main function is to reset the MCU. This pin has an internal pull-up to VDD. The reset input voltage is also monitored in order to detect external reset and safe conditions.

Table 2. 33903/4/5 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 30.

Pin # 33905D	Pin # 33905S	Pin # 33904	Pin # 33903	Pin Name	Pin Function	Formal Name	Definition
42	23	23	23	INT	Output	Interrupt Output (Active LOW)	This output is asserted low when an enabled interrupt condition occurs. This pin is a open drain structure with an internal pull up resistor to VDD.
43	24	24	24	CS	Input	Chip Select (Active LOW)	Chip select pin for the SPI. When the $\overline{CS}$ is low, the device is selected. In Low Power mode with V_{DD} ON, a transition on $\overline{CS}$ is a wake-up condition
44	25	25	25	SCLK	Input	Serial Data Clock	Clock input for the Serial Peripheral Interface (SPI) of the device
45	26	26	26	MOSI	Input	Master Out/ Slave In	SPI data received by the device
46	27	27	27	MISO	Output	Master In/Slave Out	SPI data sent to the MCU. When the $\overline{CS}$ is high, MISO is high-impedance
47	28	28	28	VDD	Output	Voltage Digital Drain	5.0 or 3.3 V output pin of the main regulator for the Microcontroller supply.
48	29	29	29	TXD	Input	Transmit Data	CAN bus transmit data input. Internal pull-up to VDD
49	30	30	30	RXD	Output	Receive Data	CAN bus receive data output
50	31	31	N/A	VE		Voltage Emitter	Connection to the external PNP path transistor. This is an intermediate current supply source for the V_{DD} regulator
51	32	32	N/A	VB	Output	Voltage Base	Base output pin for connection to the external PNP pass transistor
EX PAD	EX PAD	EX PAD	EX PAD	GND	Ground	Ground	Ground

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS[3]			
Supply Voltage at VSUP1 and VSUP2 Normal Operation (DC) Transient Conditions (Load Dump)	$V_{SUP1/2}$ $V_{SUP1/2TR}$	-0.3 to 27 -0.3 to 40	V
DC voltage on LIN, LIN1 and LIN2 Normal Operation (DC) Transient Conditions (Load Dump)	V_{BUSLIN} $V_{BUSLINTR}$	-27 to 27 -27 to 40	V
DC voltage on CANL, CANH, SPLIT Normal Operation (DC) Transient Conditions (Load Dump)	V_{BUS} V_{BUSTR}	-27 to 27 -32 to 40	V
DC Voltage at SAFE Normal Operation (DC) Transient Conditions (Load Dump)	V_{SAFE} V_{SAFETR}	-0.3 to 27 -0.3 to 40	V
DC Voltage at I/O-0, I/O-1, I/O-2, I/O-3 (LIN-pin Pins) Normal Operation (DC) Transient Conditions (Load Dump)	$V_{I/O}$ $V_{I/OTR}$	-0.3 to 27 -0.3 to 40	V
DC voltage on TXDL1 TXDL2, RXDL2, RXDL2	V_{DIGLIN}	-0.3 to V_{DD} +0.3	V
DC voltage on TXD, RXD	V_{DIG}	-0.3 to V_{DD} +0.3	V
DC Voltage at $\overline{\text{INT}}$	$V_{\overline{INT}}$	-0.3 to 10	V
DC Voltage at $\overline{\text{RST}}$	$V_{\overline{RST}}$	-0.3 to V_{DD} +0.3	V
DC Voltage at MOSI, MSIO, SCLK and $\overline{\text{CS}}$	$V_{\overline{RST}}$	-0.3 to V_{DD} +0.3	V
DC Voltage at MUX-OUT	V_{MUX}	-0.3 to V_{DD} +0.3	V
DC Voltage at DBG	V_{DBG}	-0.3 to 10	V
Continuous current on CANH and CANL	ILH	200	mA
DC voltage at VDD, 5V-CAN, VAUX, VCAUX	V_{REG}	-0.3 to 5.5	V
DC voltage at VBASE, VE, VBAUX	V_{REG}	-0.3 to 40	V
DC voltage at VSENSE	V_{SENSE}	-27 to 40	V

Table 3. Maximum Ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ESD Capability			V
AECQ100[2]			
Human Body Model - JESD22/A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω)			
CANH and CANL. LIN1 and LIN2, Pins versus all GND pins	V_{ESD1-1}	±8000	
all other Pins including CANH and CANL	V_{ESD1-2}	±2000	
Charge Device Model - JESD22/C101 (C_{ZAP} = 4.0 pF)			
Corner Pins (Pins 1, 16, 17, and 32)	V_{ESD2-1}	±750	
All other Pins (Pins 2-15, 18-31)	V_{ESD2-2}	±500	
Tested per IEC 61000-4-2 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω)			
Device unpowered, CANH and CANL pin without capacitor, versus GND	V_{ESD3-1}	±15000	
Device unpowered, LIN, LIN1 and LIN2 pin, versus GND	V_{ESD3-2}	±15000	
Device unpowered, VS1/VS2 (100 nF to GND), versus GND	V_{ESD3-3}	±15000	
Tested per specific OEM EMC requirements for CAN and LIN with additional capacitor on VSUP1/VSUP2 pins (See Typical Applications on page 86)			
CANH, CANL without bus filter	V_{ESD4-1}	±9000	
LIN, LIN1 and LIN2 with and without bus filter	V_{ESD4-2}	±12000	
I/O with external components (22 k - 10 nF)	V_{ESD4-3}	±7000	

THERMAL RATINGS4

Ratings	Symbol	Value	Unit
Junction temperature	T_J	150	°C
Ambient temperature	T_A	-40 to 125	°C
Storage temperature	T_{ST}	-55 to 165	°C

THERMAL RESISTANCE

Ratings	Symbol	Value	Unit
Thermal resistance junction to ambient	$R_{\theta JA}$	50[5]	°C/W
Peak package reflow temperature during reflow[2], [4]	T_{PPRT}	Note 4	°C

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Charge Device Model (CDM), and Robotic (C_{ZAP} = 4.0 pF).
3. The voltage on non-VSUP pins should never exceed the V_{SUP} voltage at any time or permanent damage to the device may occur. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
5. This parameter was measured according to Figure 10:

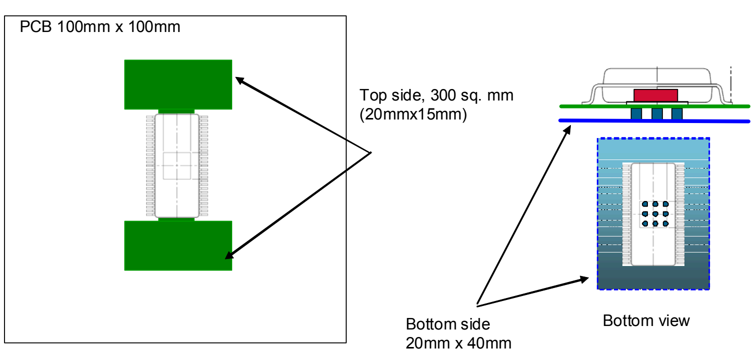


Figure 10. PCB with Top and Bottom Layer Dissipation Area (Dual Layer)

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Nominal DC Voltage Range[(6)]	V_{SUP1}/V_{SUP2}	5.5	-	27	V
Extended DC Low Voltage Range[(7)]	V_{SUP1}/V_{SUP2}	4.0	-	5.5	V
Under-voltage Detector Thresholds, at the VSUP1 pin, Low threshold (V_{SUP1} ramp down) High threshold (V_{SUP1} ramp up) Hysteresis Note: function not active in Low Power modes	V_{S1_LOW}	 5.5 - 0.22	 6.0 - 0.35	 6.5 6.6 0.5	V
Under-voltage Detector Thresholds, at the VSUP2 pin: Low threshold (V_{SUP2} ramp down) High threshold (V_{SUP2} ramp up) Hysteresis Note: function not active in Low Power modes	V_{S2_LOW}	 5.5 - 0.22	 6.0 - 0.35	 6.5 6.6 0.5	V
V_{SUP} Over-voltage Detector Thresholds, at the VSUP1 pin: Not active in Low Power modes	V_{S_HIGH}	16.5	17	18.5	V
Battery loss detection threshold, at the VSUP1 pin.	BATFAIL	2.0	2.8	4.0	V
VSUP1 to turn V_{DD} ON, VSUP1 rising	$V_{SUP\text{-}TH1}$	-	4.1	4.5	V
VSUP1 to turn V_{DD} ON, hysteresis (guaranteed by design)	$V_{SUP\text{-}TH1HYST}$	150	180		mV
Supply current[(8)] - from VSUP1 - from VSUP2, (5V-CAN V_{AUX}, I/O OFF)	I_{SUP1}	 - -	 2.0 0.05	 4.0 0.85	mA
Supply current, I_{SUP1} + I_{SUP2}, Normal mode, V_{DD} ON - 5 V-CAN OFF, V_{AUX} OFF - 5 V-CAN ON, CAN interface in Sleep Mode, V_{AUX} OFF - 5 V-CAN OFF, Vaux ON - 5 V-CAN ON, CAN interface in TxD/RxD mode, V_{AUX} OFF, I/O-x disabled	I_{SUP1+2} N1	 - - - -	 2.8 - - -	 4.5 5.0 5.5 8.0	mA
Low Power mode V_{DD} OFF. Wake-up from CAN, I/O-x inputs V_{SUP} ≤ 18 V, -40 to 25 °C V_{SUP} ≤ 18 V, 125 °C	I_{LPM_OFF}	 - -	 15 -	 35 50	µA
Low Power mode V_{DD} ON (5.0 V) with V_{DD} under-voltage and V_{DD} over-current monitoring, wake-up from CAN, I/O-x inputs V_{SUP} ≤ 18 V, -40 to 25 °C, I_{DD} = 1.0 µA V_{SUP} ≤ 18 V, -40 to 25 °C, I_{DD} = 100 µA V_{SUP} ≤ 18 V, 125 °C, I_{DD} = 100 µA	I_{LPM_ON}	- -	 20 40 -	 - 65 85	µA
Low Power mode, additional current for oscillator (used for: cyclic sense, forced wake-up, and in Low Power V_{DD} ON mode cyclic interruption and watchdog) V_{SUP} ≤ 18 V, -40 to 125 °C	I_{OSC}	-	5.0	9.0	µA

Notes

6. All parameters in spec (ex: V_{DD} regulator tolerance).
7. Device functional, some parameters could be out of spec. V_{DD} is active, device is not in Reset mode if the lowest V_{DD} under-voltage reset threshold is selected (approx. 3.4 V). CAN and I/Os are not operational.
8. In Run mode, CAN interface in Sleep mode, 5 V-CAN and V_{AUX} turned off. I_{OUT} at V_{DD} < 50 mA. Ballast: turned off or not connected.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V $\le V_{SUP} \le$ 27 V, -40 °C $\le T_A \le$ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
V_{DD} VOLTAGE REGULATOR, VDD PIN					
Output Voltage V_{DD} = 5.0 V, V_{SUP} 5.5 to 27 V, I_{OUT} 0 to 150 mA V_{DD} = 3.3 V, V_{SUP} 5.5 to 27 V, I_{OUT} 0 to 150 mA	 $V_{OUT-5.0}$ $V_{OUT-3.3}$	 4.9 3.234	 5.0 3.3	 5.1 3.366	V
Drop voltage without external PNP pass transistor[(9)] V_{DD} = 5.0 V, I_{OUT} = 100 mA V_{DD} = 5.0 V, I_{OUT} = 150 mA	V_{DROP}	 - -	 330 -	 450 500	mV
Drop voltage with external transistor[(9)] I_{OUT} = 200 mA ($I_{\_BALLAST}$ + $I_{\_INTERNAL}$)	V_{DROP-B}	 -	 350	 500	mV
VSUP1 to maintain V_{DD} within $V_{OUT-3.3}$ specified voltage range V_{DD} = 3.3 V, I_{OUT} = 150 mA V_{DD} = 3.3 V, I_{OUT} = 200 mA, external transistor implemented	$V_{SUP1-3.3}$	 4.0 4.0	 - -	 - -	V
External ballast versus internal current ratio ($I_{\_BALLAST}$ = K x Internal current)	K	1.5	2.0	2.5	
Output Current limitation, without external transistor MC33904, 33905 MC33903	I_{LIM}	 150 100	 350 -	 550 -	mA
Temperature prewarning (guaranteed by design)	T_{PW}	-	140	-	°C
Thermal shutdown (guaranteed by design)	T_{SD}	160	-	-	°C
Range of decoupling capacitor (guaranteed by design)[(10)]	C_{EXT}	4.7	-	100	µF
Low Power mode V_{DD} ON, output voltage -5.0 V, $I_{OUT} \le$ 50 mA (time limited) V_{DD} = 5.0 V, 5.6 V $\le V_{SUP} \le$ 27 V V_{DD} = 3.3 V, 5.6 V $\le V_{SUP} \le$ 27 V	V_{DDLP}	 4.75 3.135	 5.0 3.3	 5.25 3.465	V
Low Power mode V_{DD} ON, dynamic output current capability (Limited duration. Ref to device description).	$L_{P-IOUTDC}$	-	-	50	mA
Low Power V_{DD} ON mode: Over-current wake-up threshold. Hysteresis	L_{P-ITH}	 1.0 0.1	 3.0 1.0	 - -	mA
Low Power mode V_{DD} ON, drop voltage, at I_{OUT} = 30 mA (Limited duration. Ref to device description).	$L_{P-VDROP}$	-	200	400	mV
Low Power mode V_{DD} ON, min V_{SUP} operation (Below this value, a V_{DD}, under-voltage reset may occur)	$L_{P-MINVS}$	5.5	-	-	V
V_{DD} when V_{SUP} < $V_{SUP-TH1}$, at $I\_V_{DD} \le$ 10 µA (guaranteed by design)	V_{DD_OFF}	-	-	0.3	V
V_{DD} when $V_{SUP} \ge V_{SUP-TH1}$, at $I\_V_{DD} \le$ 40 mA (guaranteed with parameter $V_{SUP-TH1}$	$V_{DD\_START\ UP}$	3.0	-	-	V

Notes

9. For 3.3 V V_{DD} devices, the drop-out voltage test condition leads to a V_{SUP} below the min V_{SUP} threshold (4.0 V). As a result, the dropout voltage parameter cannot be specified.
10. The regulator is stable without external capacitor. Usage of external capacitor recommended for AC performance.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V $\leq V_{SUP} \leq$ 27 V, -40 °C $\leq T_A \leq$ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR FOR CAN INTERFACE SUPPLY, 5.0 V-CAN PIN					
Output voltage, V_{SUP2} = 5.5 to 40 V I_{OUT} 0 to 160 mA	$5V_{-C\ OUT}$	4.75	5.0	5.25	V
Output Current limitation [11]	$5V_{-C\ ILIM}$	160	280	-	mA
Under-voltage threshold	$5V_{-C\ UV}$	4.1	4.5	4.7	V
Thermal shutdown (guaranteed by design)	$5V_{-CTS}$	160	-	-	°C
External capacitance (guaranteed by design)	$C_{EXT-CAN}$	1.0	-	100	µF
V AUXILIARY OUTPUT, 5.0 AND 3.3 V SELECTABLE PIN VB-AUX, VC-AUX, VAUX					
VAUX output voltage V_{AUX} = 5.0 V, V_{SUP} = V_{SUP2} 5.5 to 40 V, I_{OUT} 0 to 150 mA V_{AUX} = 3.3 V, V_{SUP} = V_{SUP2} 5.5 to 40 V, I_{OUT} 0 to 150 mA	V_{AUX}	 4.75 3.135	 5.0 3.3	 5.25 3.465	V
VAUX under-voltage detector (VAUX configured to 5.0 V) Low Threshold Hysteresis VAUX under-voltage detector (VAUX configured to 3.3 V, default value)	$V_{AUX-UVTH}$	 4.2 0.06 2.75	 4.5 - 3.0	 4.70 0.12 3.135	V
VAUX over-current threshold detector V_{AUX} set to 3.3 V V_{AUX} set to 5.0 V	$V_{AUX-ILIM}$	 250 230	 360 330	 450 430	mA
External capacitance (guaranteed by design)	$V_{AUX\ CAP}$	2.2	-	100	µF
UNDER-VOLTAGE RESET AND RESET FUNCTION, $\overline{RST}$ PIN					
V_{DD} under-voltage threshold down - 90% V_{DD} (V_{DD} 5.0 V)[12], [14] V_{DD} under-voltage threshold up - 90% V_{DD} (V_{DD} 5.0 V) V_{DD} under-voltage threshold down - 90% V_{DD} (V_{DD} 3.3 V)[12], [14] V_{DD} under-voltage threshold up - 90% V_{DD} (V_{DD} 3.3 V)	$V_{RST-TH1}$	4.5 - 2.75 -	4.65 - 3.0 -	4.85 4.90 3.135 3.135	V
V_{DD} under-voltage reset threshold down - 70% V_{DD} (V_{DD} 5.0 V)[13], [14]	$V_{RST-TH2-5}$	2.95	3.2	3.45	V
Hysteresis for threshold 90% V_{DD}, 5.0 V device for threshold 70% V_{DD}, 5.0 V device Hysteresis 3.3 V V_{DD} for threshold 90% V_{DD}, 5.0 V device	$V_{RST-HYST}$	 20 10 10	 - - -	 150 150 150	mV
V_{DD} under-voltage reset threshold down - Low Power V_{DD} ON mode (note: device change to Normal Request mode). V_{DD} 5.0 V (note: device change to Normal Request mode). V_{DD} 3.3 V	V_{RST-LP}	 4.0 2.75	 4.5 3.0	 4.85 3.135	V

Notes

11. Current limitation will report into a flag.
12. Generate a reset or an $\overline{INT}$. SPI programmable
13. Generate a reset
14. In Run mode

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
UNDER-VOLTAGE RESET AND RESET FUNCTION, $\overline{RST}$ PIN (CONTINUED)					
Reset V_{OL} @ 1.5 mA, V_{SUP} 4.1 to 40 V	V_{OL}	-	300	500	mV
Current limitation, Reset activated, V_{RESET} = 0.9 x V_{DD}	$I_{RESET\ LOW}$	2.5	7.0	10	mA
Pull-up resistor (to VDD pin)	$R_{PULL-UP}$	8.0	11	15	kΩ
V_{SUP} to guaranteed reset low level(15)	$V_{SUP-RSTL}$	2.5	-	-	V
Reset input threshold Low threshold, V_{DD} = 5.0 V High threshold, V_{DD} = 5.0 V Low threshold, V_{DD} = 3.3 V High threshold, V_{DD} = 3.3 V	$V_{RST-VTH}$	 1.5 2.5 0.99 1.65	 1.9 3.0 1.17 2.0	 2.2 3.5 1.32 2.31	V
Reset input hysteresis	V_{HYST}	0.5	1.0	1.5	V
I/O PINS WHEN FUNCTION SELECTED IS OUTPUT					
I/O-0 high side switch drop @ I = -12 mA, V_{SUP} = 10.5 V	$V_{I/O-0\ HSDRP}$	-	0.5	1.4	V
I/O-2 and I/O-3 high side switch drop @ I = -20 mA, V_{SUP} = 10.5 V	$V_{I/O-2-3\ HSDRP}$	-	0.5	1.4	V
I/O-1, high side switch drop @ I = -400 μA, V_{SUP} = 10.5 V	$V_{I/O-1\ HSDRP}$	-	0.4	1.4	V
I/O-0, I/O-1 low side switch drop @ I = 400 μA, V_{SUP} = 10.5 V	$V_{I/O-01\ LSDRP}$	-	0.4	1.4	V
Leakage current	I_{I/O_LEAK}	-	0.1	3.0	μA
I/O PINS WHEN FUNCTION SELECTED IS INPUT					
Negative threshold	V_{I/O_NTH}	1.4	2.0	2.9	V
Positive threshold	V_{I/O_PTH}	2.1	3.0	3.8	V
Hysteresis	V_{I/O_HYST}	0.2	1.0	1.4	V
Input current	I_{I/O_IN}	-5.0	1.0	5.0	μA
I/O-0 and I/O-1 input resistor. I/O-0 (or I/O-1) selected in MUX register, 2.0 V < $V_{I/O-X}$ <16 V (guaranteed by design).	$R_{I/O-X}$	-	100	-	kΩ
VSENSE INPUT					
VSENSE under-voltage threshold (Not active in Low Power modes) Low Threshold High threshold Hysteresis	V_{SENSE_TH}	 8.1 - 0.1	 8.6 - 0.25	 9.0 9.1 0.5	V
Input resistor to GND. In all modes except in Low Power modes. (guaranteed by design).	R_{VSENSE}	-	125	-	kΩ

Notes

15. Reset must be maintained low

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ANALOG MUX OUTPUT					
Output Voltage Range, with external resistor to GND >2.0 kΩ	V_{OUT_MAX}	0.0	-	V_{DD} - 0.5	V
Internal pull-down resistor for regulator output current sense	R_{MI}	0.8	1.9	2.8	kΩ
External capacitor at MUX OUTPUT[(16)] (guaranteed by design)	C_{MUX}	-	-	1.0	nF
Chip temperature sensor coeff (guaranteed by design and device characterization)	$TEMP_{-COEFF}$	20	21	22	mv/°C
Chip temperature: MUX-OUT voltage T_A = 25 °C, guaranteed by design and characterization V_{DD} = 5.0 V, T_A = 125 °C V_{DD} = 3.3 V, T_A = 125 °C	V_{TEMP}	 1.5 3.6 2.45	 1.65 3.75 2.58	 1.8 3.9 2.65	V
Gain for V_{SENSE}, with external 1.0 k 1% resistor V_{DD} = 5.0 V V_{DD} = 3.3 V	V_{SENSE} GAIN	 5.13 8.1	 5.48 8.2	 5.67 8.3	
Offset for V_{SENSE}, with external 1.0 k 1% resistor	V_{SENSE} OFFSET	-20	-	20	mV
Divider ratio for V_{SUP1} V_{DD} = 5.0 V V_{DD} = 3.3 V	V_{SUP1} RATIO	 5.335 7.95	 5.5 8.18	 5.665 8.45	
Divider ratio for I/O-0 and I/O-1 actual voltage - with attenuation selected (MUX-OUT register bit 3 set to 1); V_{DD} =5.0 V, V_{SUP} = 16 V V_{DD} =5.0 V, - with gain selected (MUX-OUT register bit 3 set to 0) V_{DD} =3.3 V, V_{SUP} = 16 V V_{DD} =3.3 V, - with gain selected (MUX-OUT register bit 3 set to 0)	VI/O RATIO	 3.8 - 5.6 -	 4.0 2.0 5.8 2.0	 4.2 - 6.2 -	
Internal reference voltage V_{DD} =5.0 V V_{DD} =3.3 V	V_{REF}	 2.45 1.64	 2.5 1.67	 2.55 1.7	V
Current ratio between VDD output & I_{OUT} at MUX-OUT (I_{OUT} at MUX-OUT = I_{DD} out / I_{DD_RATIO}) At I_{OUT} = 50 mA $I_{\_OUT}$ from 25 to 150 mA	I_{DD_RATIO}	 80 62.5	 97 97	 115 117	
SAFE OUTPUT					
SAFE low level, at I = 500 µA	V_{OL}	0.0	0.2	1.0	V
Safe leakage current (V_{DD} low, or device unpowered). V_{SAFE} 0 to 27 V.	$I_{SAFE-IN}$	-	0.0	1.0	µA

Notes

16. When C is higher than CMUX, a serial resistor must be inserted

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INTERRUPT					
Output low voltage, I_{OUT} = 1.5 mA	V_{OL}	-	0.2	1.0	V
Pull-up resistor	R_{PU}	6.5	10	14	kΩ
Output high level in Low Power V_{DD} ON mode (guaranteed by design)	$V_{OH\text{-}LPVDDON}$	3.9	4.3		V
Leakage current $\overline{INT}$ voltage = 10 V (to allow high-voltage on MCU $\overline{INT}$ pin)	V_{MAX}	-	35	100	μA
Sink current, $V_{\overline{INT}}$ > 5.0 V, $\overline{INT}$ low state	I_{SINK}	2.5	6.0	10	mA
MISO, MOSI, SCLK, $\overline{CS}$ PINS					
Output low voltage, I_{OUT} = 1.5 mA (MISO)	V_{OL}	-	-	1.0	V
Output high voltage, I_{OUT} = -0.25 mA (MISO)	V_{OH}	V_{DD} -0.9	-		V
Input low voltage (MOSI, SCLK,$\overline{CS}$)	V_{IL}	-	-	0.3 x V_{DD}	V
Input high voltage (MOSI, SCLK,$\overline{CS}$)	V_{IH}	0.7 x V_{DD}	-	-	V
Tri-state leakage current (MISO)	I_{HZ}	-2.0	-	2.0	μA
Pull-up current ($\overline{CS}$)	I_{PU}	200	370	500	μA
CAN LOGIC INPUT PINS (TXD)					
High Level Input Voltage	V_{IH}	0.7 x V_{DD}	-	V_{DD} + 0.3	V
Low Level Input Voltage	V_{IL}	-0.3	-	0.3 x V_{DD}	V
Pull-up Current, TxD, V_{IN} = 0 V V_{DD} =5.0 V V_{DD} =3.3 V	I_{PDWN}	 -850 -500	 -650 -250	 -200 -175	μA
CAN DATA OUTPUT PINS (RXD)					
Low Level Output Voltage I_{RXD} = 5.0 mA	$VOUT_{LOW}$	 0.0	 -	 0.3 x V_{DD}	V
High Level Output Voltage I_{RX} = -3.0 mA	$VOUT_{HIGH}$	 0.7 x V_{DD}	 -	 V_{DD}	V
High Level Output Current V_{RXD} = V_{DD} - 0.4 V	$IOUT_{HIGH}$	 2.5	 5.0	 9.0	mA
Low Level Input Current V_{RXD} = 0.4 V	$IOUT_{LOW}$	 2.5	 5.0	 9.0	mA

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CAN OUTPUT PINS (CANH, CANL)					
Bus pins common mode voltage for full functionality	V_{COM}	-12	-	12	V
Differential input voltage threshold	$V_{CANH-VCANL}$	500	-	900	mV
Differential input hysteresis	$V_{DIFF-HYST}$	50	-	-	mV
Input resistance	R_{IN}	5.0	-	50	kΩ
Differential input resistance	$R_{IN-DIFF}$	10	-	100	kΩ
Input resistance matching	$R_{IN-MATCH}$	-3.0	0.0	3.0	%
CANH output voltage (45 Ω < R_{BUS} < 65 Ω) TxD dominant state TxD recessive state	V_{CANH}	 2.75 2.0	 3.5 2.5	 4.5 3.0	V
CANL output voltage (45 Ω < R_{BUS} < 65 Ω) TxD dominant state TxD recessive state	V_{CANL}	 0.5 2.0	 1.5 2.5	 2.25 3.0	V
Differential output voltage (45 Ω < R_{BUS} < 65 Ω) TxD dominant state TxD recessive state	V_{OH}-V_{OL}	 1.5 -0.5	 2.0 0.0	 3.0 0.05	V
CAN H output current capability - Dominant state	I_{CANH}	-	-	-30	mA
CAN L output current capability - Dominant state	I_{CANL}	30	-	-	mA
CANL over-current detection - Error reported in register	$I_{CANL-OC}$	75	120	195	mA
CANH over-current detection - Error reported in register	$I_{CANH-OC}$	-195	-120	-75	mA
CANH, CANL input resistance to gnd, device supplied, CAN in Sleep mode, V_CANH, V_CANL from 0 to 5.0 V	$R_{INSLEEP}$	5.0	-	50	kΩ
CANL, CANH output voltage in Low Power V_{DD} OFF and Low Power V_{DD} ON modes	V_{CANLP}	-0.1	0.0	0.1	V
CANH, CANL input current, VCANH, VCANL = 0 to 5.0 V, device unpowered (VSUP, VDD, 5V-CAN: open).[17]	I_{CAN-UN_SUP1}	-	3.0	10	μA
CANH, CANL input current, VCANH, VCANL = -2.0 to 7.0 V, device unpowered (VSUP, VDD, 5V-CAN: open).[17]	I_{CAN-UN_SUP2}	-	-	250	μA
Differential voltage for recessive bit detection in LP mode[18]	$V_{DIFF-R-LP}$	-	-	0.4	V
Differential voltage for dominant bit detection in LP mode[18]	$V_{DIFF-D-LP}$	1.15	-	-	V
CANH AND CANL DIAGNOSTIC INFORMATION					
CANL to GND detection threshold	V_{LG}	1.6	1.75	2.0	V
CANH to GND detection threshold	V_{HG}	1.6	1.75	2.0	V
CANL to VBAT detection threshold, V_{SUP1} and V_{SUP2} > 8.0 V	V_{LVB}	-	V_{SUP} -2.0	-	V
CANH to VBAT detection threshold, V_{SUP1} and V_{SUP2} > 8.0 V	V_{HVB}	-	V_{SUP} -2.0	-	V
CANL to VDD detection threshold	V_{L5}	4.0	V_{DD} -0.43	-	V
CANH to VDD detection threshold	V_{H5}	4.0	V_{DD} -0.43	-	V

Notes

17. VSUP, VDD, 5V-CAN: shorted to GND, or connected to GND via a 47 k resistor instances are guaranteed by design and device characterization.
18. Guaranteed by design and device characterization.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPLIT					
Output voltage Loaded condition I_{SPLIT} = ±500 μA Unloaded condition Rmeasure > 1.0 MΩ	V_{SPLIT}	 0.3 x V_{DD} 0.45 x V_{DD}	 0.5 x V_{DD} 0.5 x V_{DD}	 0.7 x V_{DD} 0.55 x V_{DD}	V
Leakage current -12 V < V_{SPLIT} < +12 V -22 to -12 V < V_{SPLIT} < +12 to +35 V	I_{LSPLIT}	 - -	 0.0 -	 5.0 200	μA
LIN TERM1, LIN TERM2					
LIN-T1, LIN-T2, high side switch drop @ I = -20 mA, V_{SUP} > 10.5 V	V_{LT_HSDRP}	-	1.0	1.4	V
LIN1 AND LIN 2 MC33905D PIN - LIN1 MC33905S PIN (Parameters guaranteed for V_{SUP1}, V_{SUP2} 7.0 V ≤ V_{SUP} ≤ 18 V)					
Operating Voltage Range	V_{BAT}	8.0	-	18	V
Supply Voltage Range	V_{SUP}	7.0	-	18	V
Current Limitation for Driver Dominant State Driver ON, V_{BUS} = 18 V	I_{BUS_LIM}	40	90	200	mA
Input Leakage Current at the receiver Driver off; V_{BUS} = 0 V; V_{BAT} = 12 V	$I_{BUS\_PAS\_DOM}$	-1.0	-	-	mA
Leakage Output Current to GND Driver Off; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	$I_{BUS\_PAS\_REC}$	-	-	20	μA
Control unit disconnected from ground (Loss of local ground must not affect communication in the residual network) GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V (guaranteed by design)	$I_{BUS\_NO\_GND}$	-1.0	-	1.0	mA
V_{BAT} Disconnected; V_{SUP_DEVICE} = GND; 0 < V_{BUS} < 18 V (Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition)	I_{BUSNO_BAT}	-	-	100	μA
Receiver Dominant State	V_{BUSDOM}	-	-	0.4	V_{SUP}
Receiver Recessive State	V_{BUSREC}	0.6	-	-	V_{SUP}
Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	V_{BUS_CNT}	0.475	0.5	0.525	V_{SUP}
Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	V_{HYS}	-	-	0.175	V_{SUP}
LIN Wake-up threshold from Low Power V_{DD} ON or Low Power V_{DD} OFF mode	V_{BUSWU}	-	5.3	5.8	V
LIN Pull-up Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
Over-temperature Shutdown (guaranteed by design)	T_{LINSD}	140	160	180	°C
Over-temperature Shutdown Hysteresis (guaranteed by design)	T_{LINSD_HYS}	-	10	-	°C

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_{A} = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI TIMING					
SPI Operation Frequency (MISO cap = 50 pF)	FREQ	0.25	-	4.0	MHz
SCLK Clock Period	t_{PCLK}	250	-	N/A	ns
SCLK Clock High Time	t_{WSCLKH}	125	-	N/A	ns
SCLK Clock Low Time	t_{WSCLKL}	125	-	N/A	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}	30	-	N/A	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$	t_{LAG}	30	-	N/A	ns
MOSI to Falling Edge of SCLK	t_{SISU}	30	-	N/A	ns
Falling Edge of SCLK to MOSI	t_{SIH}	30	-	N/A	ns
MISO Rise Time (CL = 50 pF)	t_{RSO}	-	-	30	ns
MISO Fall Time (CL = 50 pF)	t_{FSO}	-	-	30	ns
Time from Falling to MISO Low-impedance Time from Rising to MISO High-impedance	t_{SOEN} t_{SODIS}	- -	- -	30 30	ns
Time from Rising Edge of SCLK to MISO Data Valid	t_{VALID}	-	-	30	ns
Delay between rising and falling edge on $\overline{CS}$	$t_{D2\overline{CS}}$	1.0	-	-	µs
$\overline{CS}$ low timeout detection	$t_{\overline{CS}-TO}$	2.5	-	-	ms
SUPPLY, VOLTAGE REGULATOR, RESET					
V_{SUP} under-voltage detector threshold deglitcher	$t_{VS\_LOW1/2\_DGLT}$	30	50	100	µs
Rise time at turn ON. V_{DD} from 1.0 to 4.5 µV. 2.2 µF at the VDD pin.	$t_{RISE-ON}$	50	250	800	µs
Deglitcher time to set RESET pin low	$t_{RST-DGLT}$	20	30	40	µs
RESET PULSE DURATION					
V_{DD} under-voltage (SPI selectable) short, default at power on when BATFAIL bit set medium medium long long	$t_{RST-PULSE}$	 0.9 4.0 8.5 17	 1.0 5.0 10 20	 1.4 6.0 12 24	ms
Watchdog reset	t_{RST-WD}	0.9	1.0	1.4	ms
VSENSE INPUT					
Under-voltage deglitcher time	t_{BFT}	30	-	100	µs
INTERRUPT					
$\overline{INT}$ pulse duration (refer to SPI for selection. Guaranteed by design) short (25 to 125 °C) short (-40 °C) long (25 to 125 °C) long (-40 °C)	$t_{\overline{INT}-PULSE}$	 20 20 90 90	 25 25 100 100	 35 40 130 140	µs

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions $5.5\text{ V} \leq V_{SUP} \leq 27\text{ V}$, $-40\text{ °C} \leq T_A \leq 125\text{ °C}$, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ °C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
STATE DIGRAM TIMINGS					
Delay for SPI Timer A, Timer B or Timer C write command after entering Normal mode (No command should occur within t_{D_NM}. t_{D_NM} delay definition: from $\overline{CS}$ rising edge of "Go to Normal mode (i.e 0x5A00)" command to $\overline{CS}$ falling edge of "Timer write" command)	t_{D_NM}	60	-	-	µs
Tolerance for: W/D period in all modes, FWU delay, Cyclic sense period and active time, Cyclic Interrupt period, LP mode over-current (unless otherwise noted)[22]	$t_{TIMING-ACC}$	-10	-	10	%
CAN DYNAMIC CHARACTERISTICS					
TXD Dominant State Timeout	t_{DOUT}	300	600	1000	µs
Bus dominant clamping detection	t_{DOM}	300	600	1000	µs
Propagation loop delay TXD to RXD, recessive to dominant (Fast slew rate)	t_{LRD}	60	120	210	ns
Propagation delay TXD to CAN, recessive to dominant	t_{TRD}	-	70	110	ns
Propagation delay CAN to RXD, recessive to dominant	t_{RRD}	-	45	140	ns
Propagation loop delay TXD to RXD, dominant to recessive (Fast slew rate)	t_{LDR}	100	120	200	ns
Propagation delay TXD to CAN, dominant to recessive	t_{TDR}	-	75	150	ns
Propagation delay CAN to RXD, dominant to recessive	t_{RDR}	-	50	140	ns
Loop time TXD to RXD, Medium Slew rate (Selected by SPI) Rec to Dom Dom to Rec	$t_{LOOP-MSL}$	 - -	 200 200	 - -	ns
Loop time TXD to RXD, Slow Slew rate (Selected by SPI) Rec to Dom Dom to Rec	$t_{LOOP-SSL}$	 - -	 300 300	 - -	ns
CAN wake-up filter time, single dominant pulse detection[19] (See Figure 32)	$t_{CAN-WU1-F}$	0.5	2.0	5.0	µs
CAN wake-up filter time, 3 dominant pulses detection[20]	$t_{CAN-WU3-F}$	300	-	-	ns
CAN wake-up filter time, 3 dominant pulses detection timeout[21] (See Figure 33)	$t_{CAN-WU3-TO}$	-	-	120	µs

Notes

19. No wake-up for single pulse shorter than $t_{CAN-WU1}$ min. Wake-up for single pulse longer than $t_{CAN-WU1}$ max.
20. Each pulse should be greater than $t_{CAN-WU3-F}$ min. Guaranteed by design, and device characterization.
21. The 3 pulses should occur within $t_{CAN-WU3-TO}$. Guaranteed by design, and device characterization.
22. Guaranteed by design.

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 27 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN 1 AND LIN 2 PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. See Figure 15, page 27.					
Duty Cycle 1: $TH_{REC(MAX)}$ = 0.744 * V_{SUP} $TH_{DOM(MAX)}$ = 0.581 * V_{SUP} D1 = $t_{BUS\_REC(MIN)}/(2 \times t_{BIT})$, t_{BIT} = 50 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	D1	0.396	-	-	
Duty Cycle 2: $TH_{REC(MIN)}$ = 0.422 * V_{SUP} $TH_{DOM(MIN)}$ = 0.284 * V_{SUP} D2 = $t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$, t_{BIT} = 50 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	D2	-	-	0.581	
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds. See Figure 16, page 28.					
Duty Cycle 3: $TH_{REC(MAX)}$ = 0.778 * V_{SUP} $TH_{DOM(MAX)}$ = 0.616 * V_{SUP} D3 = $t_{BUS\_REC(MIN)}/(2 \times t_{BIT})$, t_{BIT} = 96 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	D3	0.417	-	-	
Duty Cycle 4: $TH_{REC(MIN)}$ = 0.389 * V_{SUP} $TH_{DOM(MIN)}$ = 0.251 * V_{SUP} D4 = $t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$, t_{BIT} = 96 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	D4	-	-	0.590	
LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR FAST SLEW RATE					
LIN Fast Slew Rate (Programming mode)	SR_{FAST}	-	20	-	V/µs
LIN PHYSICAL LAYER: CHARACTERISTICS AND WAKE-UP TIMINGS V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. See Figure 15, page 27.					
Propagation Delay and Symmetry (See Figure 15, page 27 and Figure 16, page 28) Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF}) Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	 t_{REC_PD} t_{REC_SYM}	 - -2.0	 4.2 -	 6.0 2.0	µs
Bus Wake-up Deglitcher (Low Power V_{DD} OFF and Low Power V_{DD} ON modes) (See Figure 17, page 27 for Low Power V_{DD} OFF mode and Figure 18, page 28 for Low Power mode)	t_{PROPWL}	42	70	95	µs
Bus Wake-up Event Reported From Low Power V_{DD} OFF mode From Low Power V_{DD} ON mode	 $t_{WAKE\_LPVDD OFF}$ $t_{WAKE\_LPVDD ON}$	 - 1.0	 - -	 1500 12	µs
TXD Permanent Dominant State Delay (guaranteed by design)	t_{TXDDOM}	0.65	1.0	1.35	s

TIMING DIAGRAMS

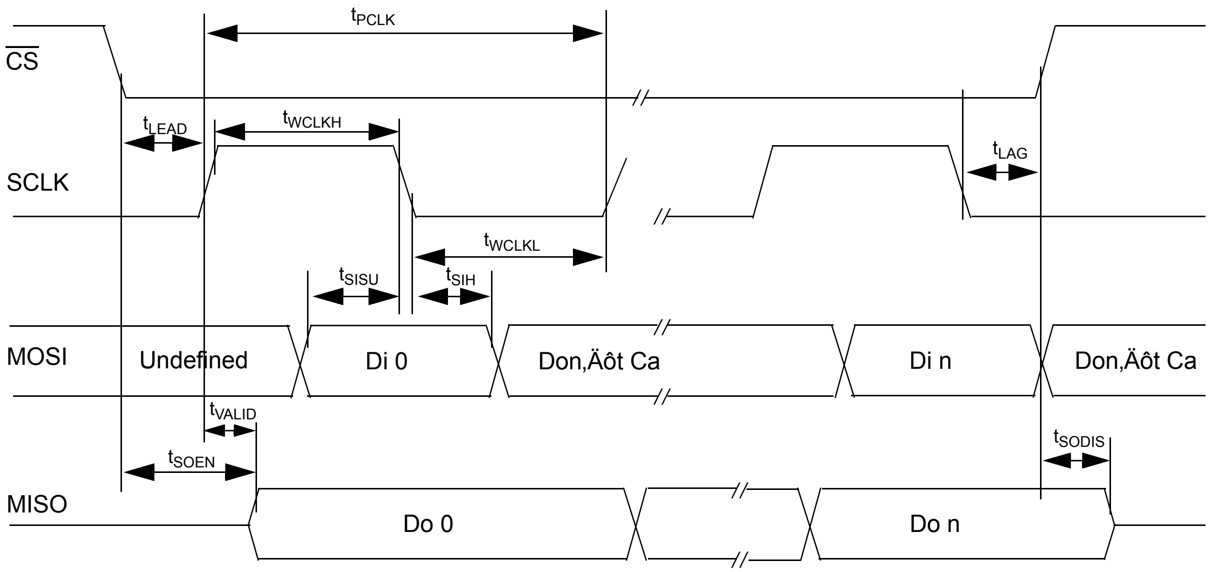


Figure 11. SPI Timings

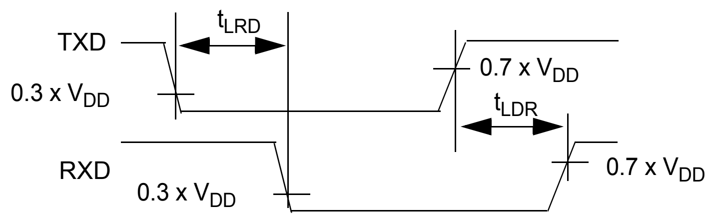


Figure 12. CAN Signal Propagation Loop Delay TXD to RXD

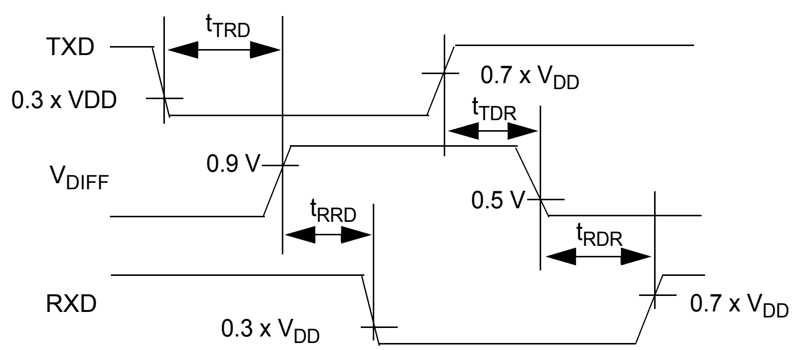


Figure 13. CAN Signal Propagation Delays TXD to CAN and CAN to RXD

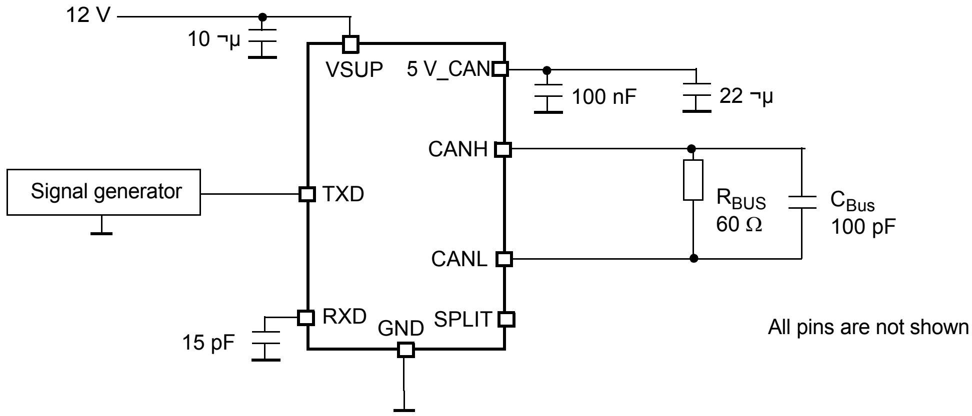


Figure 14. Test Circuit for CAN Timing Characteristics

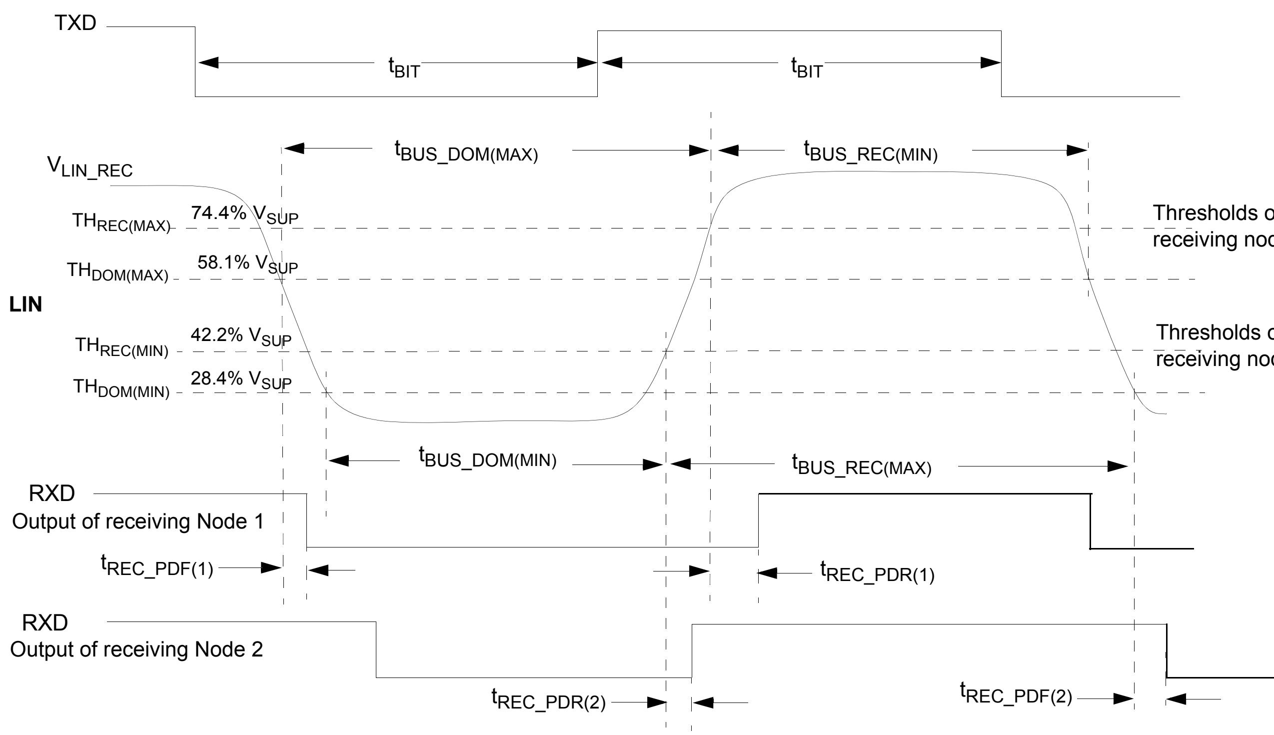


Figure 15. LIN Timing Measurements for Normal Slew Rate

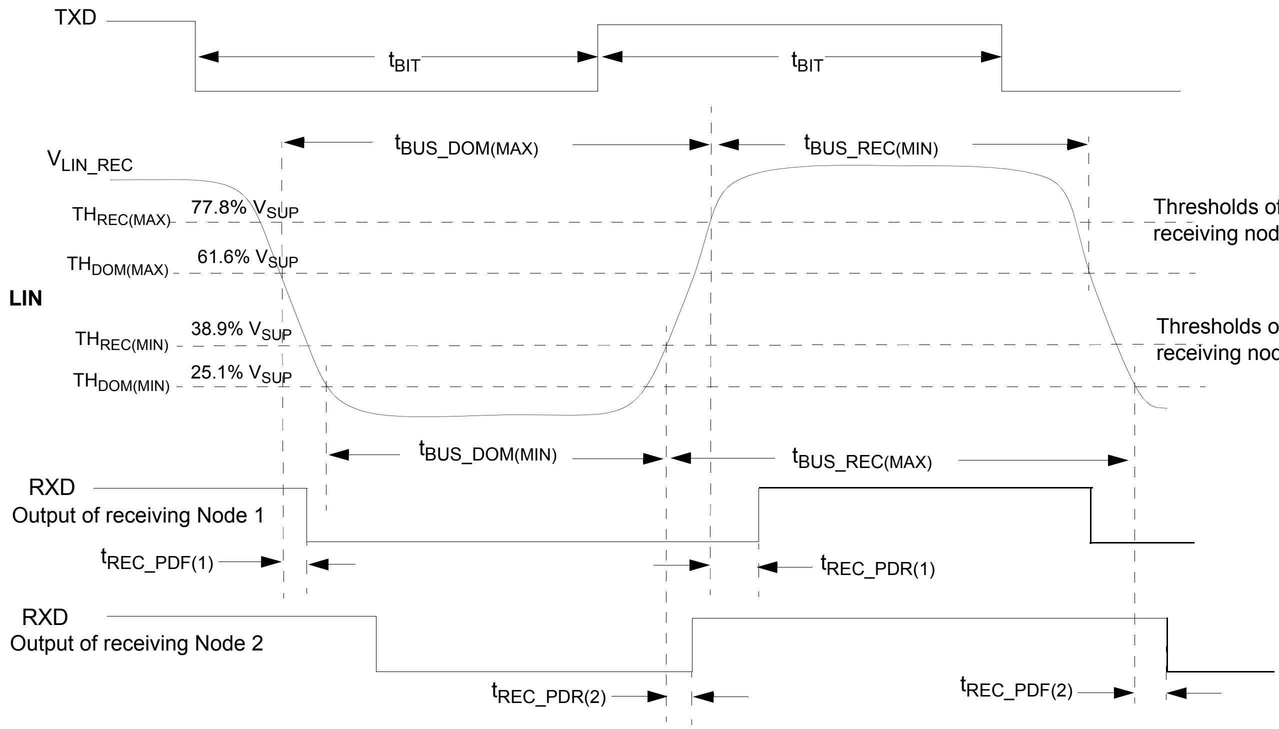


Figure 16. LIN Timing Measurements for Slow Slew Rate

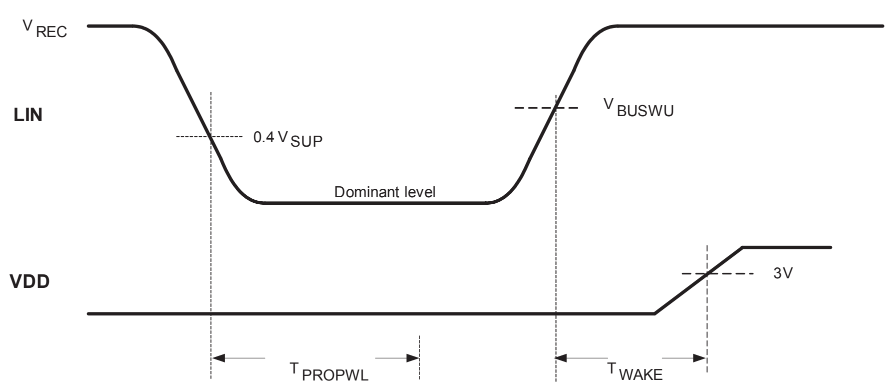


Figure 17. LIN Wake-up Low Power V_{DD} OFF Mode Timing

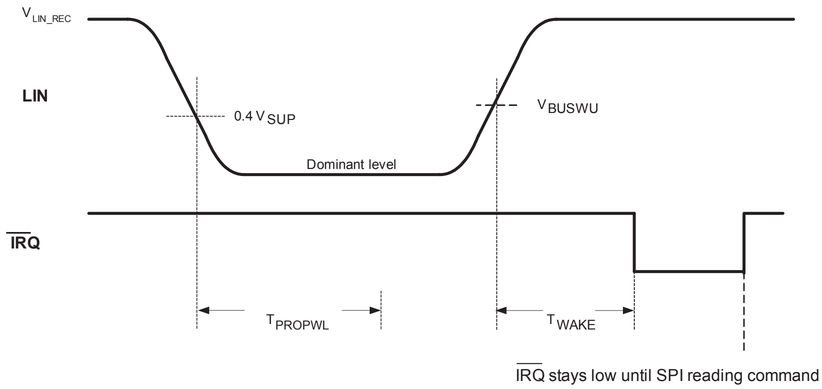


Figure 18. LIN Wake-up Low Power V_{DD} ON Mode Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The MC33903_4_5 is the second generation of System Basis Chip, combining:

- Advanced power management unit for the MCU, the integrated CAN interface and for additional ICs such as sensors, CAN transceiver.

- Built in enhanced high speed CAN interface (ISO11898-2 and -5), with local and bus failure diagnostic, protection and fail safe operation mode.

- Built in LIN interface, compliant to LIN 2.1 and J2602-2 specification, with local and bus failure diagnostic and protection.

- Innovative and hardware configurable fail safe state machine solution.

- Multiple low power modes, with low current consumption.

- Family concept; with and without LIN interface devices with pin compatibility.

FUNCTIONAL PIN DESCRIPTION

POWER SUPPLY (VSUP1 AND VSUP2)

VSUP1 is the input pin for the device internal supply and the VDD regulator. VSUP2 is the input pin for the 5 V-CAN regulator, LINs interfaces and I/O functions. The VSUP block includes over and under-voltage detections which can generate interrupt. The device includes a loss of battery detector connected to VSUP1.

Loss of battery is reported through a bit (called BATFAIL). This generates a POR (Power On Reset).

VDD VOLTAGE REGULATOR (VDD)

The regulator has two main modes of operation (Normal mode and Low Power mode). It can operate with or without an external PNP transistor.

In Normal mode, without external PNP, the max DC capability is 150 mA. Current limitation, temperature prewarning flag and over-temperature shutdown features are included. When V_{DD} is turned ON, rise time from 0 to 5.0 V is controlled. Output voltage is 5.0 V. A 3.3 V option is available via dedicated part number.

If current higher than 150 mA is required, an external PNP transistor must be connected to VEM (PNP emitter) and VB (PNP base) pins, in order to increase total current capability and share the power dissipation between internal VDD transistor and the external transistor. See External Transistor Q1 (VE and VB). The PNP can be used even if current is less than 150 mA, depending upon ambient temperature, maximum supply and thermal resistance. Typically, above 100-200 mA, an external ballast transistor is recommended.

VDD REGULATOR IN LOW POWER MODE

When the device is set in Low Power V_{DD} ON mode, the V_{DD} regulator is able to supply the MCU with a DC current below typ 1.5 mA ($L_{P\text{-}ITH}$). Transient current can also be supplied up to a tenth of a mA. Current in excess of 1.5 mA is detected, and this event is managed by the device logic (wake-up detection, timer start for over-current duration monitoring or watchdog refresh).

EXTERNAL TRANSISTOR Q1 (VE AND VB)

The device has a dedicated circuit to allow usage of an external P type transistor, with the objective to share the power dissipation between the internal transistor of the V_{DD} regulator and the external transistor. The bipolar PNP recommended transistor are MJD42C or BCP52-16.

When the external PNP is connected, the current is shared between the internal path transistor and the external PNP, with the following typical ratio: 1/3 in the internal transistor and 2/3 in the external PNP. The PNP activation and control is done by SPI.

The device is able to operate without an external transistor. In this case, the VEM and VB pins must remain open.

5 V-CAN VOLTAGE REGULATOR FOR CAN AND ANALOG MUX

This regulator is supplied from the VSUP2 pin. A capacitor is required at 5 V-CAN pin. Analog MUX and part of the LIN interfaces are supplied from 5 V-CAN. Consequently, the 5 V-CAN must be ON in order to have Analog MUX operating and to have the LIN interface operating in TxD/RxD mode.

5 V-CAN regulator is OFF by default and must be turn ON by SPI. In Debug mode 5 V-CAN is ON be default.

V AUXILIARY OUTPUT, 5.0 AND 3.3 V SELECTABLE (VB-AUX, VC-AUX, AND VCAUX) - Q2

The VAUX block is used to provide an auxiliary voltage output, 5.0 or 3.3 V, selectable by the SPI. It uses an external PNP pass transistor for flexibility and power dissipation constraints. The external recommended bipolar transistors are MJD42C or BCP52-16.

An over-current and under-voltage detectors are provided.

V_{AUX} is controlled via the SPI, and can be turned ON or OFF. V_{AUX} low threshold detection and over-current information will disable V_{AUX}, and are reported in the SPI and can generate $\overline{INT}$.

V_{AUX} is OFF by default and must be turned ON by the SPI.

UNDER-VOLTAGE RESET AND RESET FUNCTION (RST)

The RESET pin is an open drain structure with an internal pull-up resistor. The low side driver has limited current capability when asserted low, in order to tolerate a short to 5.0 V.The RESET pin voltage is monitored in order to detect failure (e.g. RESET pin shorted to 5.0 V or GND).

The RESET pin reports to the MCU under-voltage condition at the VDD pin, as well as failure in watchdog refresh operation. V_{DD} under-voltage reset operate also in Low Power V_{DD} ON mode.

Two V_{DD} under-voltage threshold are included. The upper on (typ 4.65 V, $R_{ST\text{-}TH1\text{-}5}$) can lead to a Reset or an Interrupt. This is selected by the SPI. When “$R_{ST\text{-}TH2\text{-}5}$“is selected, in Normal mode, an INT is asserted when VDD falls below “$R_{ST\text{-}TH1\text{-}5}$“, then when V_{DD} falls below “$R_{ST\text{-}TH2\text{-}5}$” a Reset will occur. This will allow the MCU to operate in a degraded mode, for example, with 4.0 V V_{DD}.

I/O PINS (I/O-0: I/O-3)

I/O s are configurable input output pins. They can be used for small load or to drive external transistors. When used as output drivers, the I/Os are high side or low side type. They can also be set to high-impedance. I/Os are controlled by the SPI and at power on, the I/Os are set as inputs. They include over load protection by temperature or excess of drop voltage.

In Low Power mode, state of the I/O can be turned on or off, with extremely low extra consumption (except load). Protection is disabled in low power mode.

When cyclic sense is used, I/O-0 is the high side/low side switch, I/O-1, -2 and -3 and the wake inputs.

I/O-2 and I/O-3 pins share also the LIN Master pin function.

VSENSE INPUT (VSENSE)

This pin can be connected to the battery line (before the reverse battery protection diode), via a serial resistor and a capacitor to gnd. It incorporates a threshold detector to sense the battery voltage and provide a battery early warning. It also includes a resistor divider to measure the V_{SENSE} voltage via the MUX-OUT pin.

MUX-OUTPUT (MUXOUT)

The MUX-OUT pin (Figure 19) delivers an analog voltage to the MCU A/D input. The voltage to be delivered to MUX-OUT is selected via the SPI, from one of the following functions: V_{SUP1}, V_{SENSE}, I/O-0, I/O-1, Internal 2.5 V reference, die temperature sensor, V_{DD} current copy.

Voltage divider or amplifier are inserted in the chain, as shown in Figure 19.

For the V_{DD} current copy, a resistor must be added to the MUX-OUT pin, to convert current into voltage. Device includes an internal 2.0 k resistor selectable by the SPI.

Voltage range at MUX-OUT is from GND to VDD. It is automatically limited to V_{DD} (max 3.3 V for 3.3 V part numbers).

The MUX-OUT buffer is supplied from 5 V-CAN regulator, so the 5 V-CAN regulator must be ON in order to have:

1) MUX-OUT functionality and

2) SPI selection of the analog function.

If 5 V-CAN is OFF, MUX-OUT voltage is near gnd and the SPI command that selects one of the analog input is ignored.

Delay must be respected between SPI commands for 5 V-CAN turn ON and SPI to select MUX-OUT function. The delay depends mainly upon the 5 V-CAN capacitor and load on 5 V-CAN.

The delay can be estimated using the following formula: delay = C(5 V-CAN) x U (5.0 V) / I_lim 5 V-CAN.

C = cap at 5 V-CAN regulator, U = 5.0 V,

$I_{\_LIM}$ 5 V-CAN = min current limit of 5 V-CAN regulator (parameter 5 $V_{\text{-C ILIM}}$).

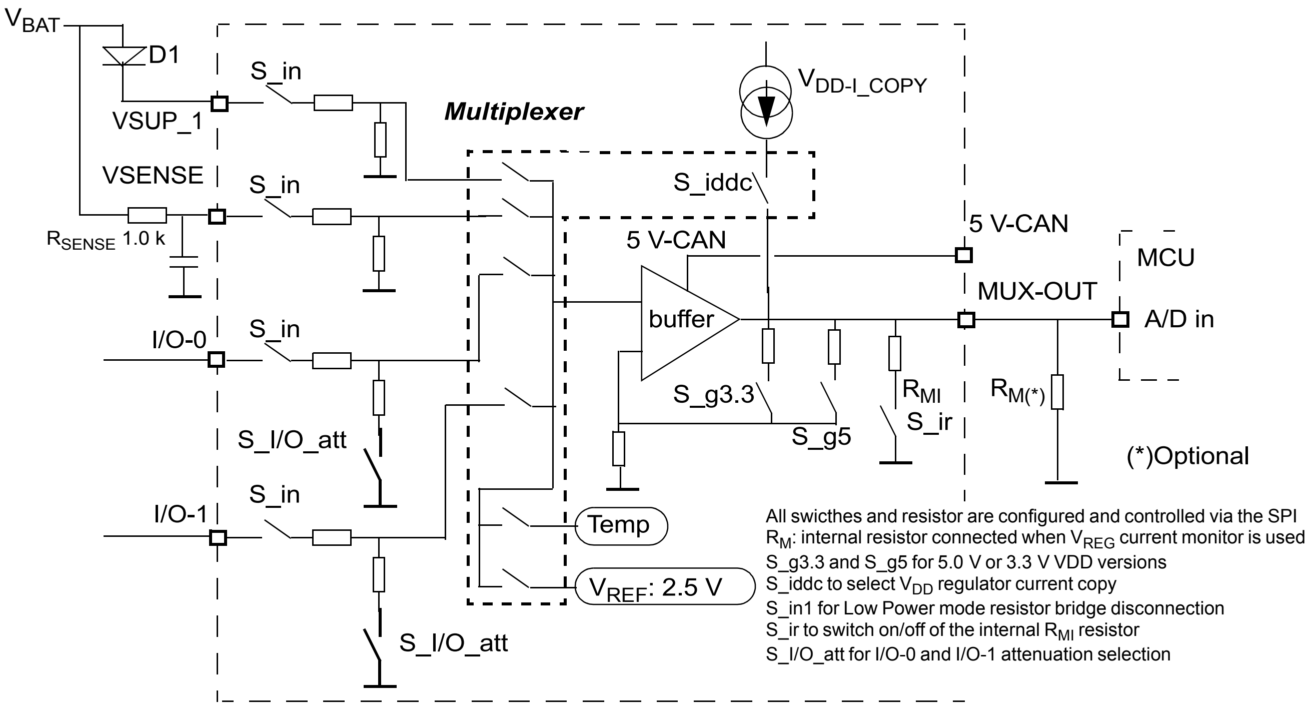


Figure 19. Analog Multiplexer Block Diagram

DGB (DGB) AND DEBUG MODE

The DBG pin has 2 functions:

Primary function:

It is an input used to set the device in Debug mode. This is achieved by applying a voltage between 8.0 and 10 V, at the DEBUG pin, and then powering up the device (ref to state diagram). When device leaves the INIT reset mode and enter in INIT mode, device detects that voltage at DEBUG pin is within the 8.0 to 10 V range, and activate the debug mode.

When debug mode is detected, no watchdog SPI refresh commands is necessary. This allow easy debug of the hardware and software routines (i.e SPI commands).

Device is in debug mode is reported by SPI flag. While in debug mode, when voltage at DBG pin falls below the 8.0 to 10 V range, the debug mode is left, and device start W/D operation, and expect proper W/D refresh. Debug mode can be left by SPI. Such command is recommended to avoid staying in debug mode in case of unwanted debug mode selection (FMEA pin). SPI command to leave debug has higher priority than providing 8.0 to 10 V at the DEBUG pin.

Secondary function:

The resistor connected between DBG pin and GND selects the Fail Safe mode operation. DBG pin can also be connected directly to GND (this prevent usage of debug mode).

Flexibility is provided to the user to select SAFE output operation via a resistor at the DBG pin or via a SPI command. The SPI command has higher priority than the hardware selection via Debug resistor.

When the Debug mode is selected, the SAFE modes can not be configured via the resistor connected at DBG pin.

SAFE

Safe output pin

This pin is an output which is asserted low in case a fault event occurs. The objective is to drive electrical safe circuitry and set the ECU in a know sate independent of the MCU and SBC, once a failure has been detected.

The SAFE output structure is an open drain, without a pull-up.

INTERRUPT ($\overline{\text{INT}}$)

The $\overline{\text{INT}}$ output is asserted low or generate a low pulse when an interrupt condition occurs. The $\overline{\text{INT}}$ condition is enabled in the $\overline{\text{INT}}$ register. The selection of low level or pulse as well as pulse duration are selected by SPI.

No current will flow inside the $\overline{\text{INT}}$ structure when V_{DD} is low, in Low Power V_{DD} OFF mode. This allows the connection of an external pull-up resistor, and connection of an $\overline{\text{INT}}$ pin from other ICs without extra consumption in unpowered mode.

$\overline{\text{INT}}$ has an internal pull-up structure to V_{DD}. In Low Power V_{DD} ON mode, a diode is inserted in series with the pull-up, so the high level is slightly lower than in other modes.

CANH, CANL, SPLIT, RXD, TXD

These are the pins of the high speed CAN physical interface, between the CAN bus and the micro controller. A detail description is provided in the document.

LIN, TXDL, RXDL AND LINTERM

These are the pins of the LIN physical interface. Device contains zero, one or two LIN interfaces.

The MC33903 and MC33904 do not have a LIN interface. However, the MC33905S (S = Single) and MC33905D (D = Dual) contain 1 and 2 LIN interfaces, respectively.

LIN1 and LIN2 pins are the connection to the LIN sub buses.

LIN interfaces are connected to the MCU via the TxDL1 (TxDL2) and RxDL1 (RxDL2) pins.

The device also include one or two high side switches to VSUP2 pin which can be used as a LIN master termination switch. Pins LINT-1 and LINT-2 are the same as I/O-2 and I/O-3.

A detail description is provided in the document

FUNCTIONAL DEVICE OPERATION

MODE AND STATE DESCRIPTION

The device has several operation modes. The transitions and conditions to enter or leave each modes are illustrated in the state diagram.

INIT RESET

This mode is automatically entered after device “power on”. In this mode, the RST pin is asserted low, for a duration of typ 1.0 ms. Control bits and flags are “set” to their default reset condition. The BATFAIL is set to indicated that the device is coming from an unpowered condition, and that all previous device configuration are lost and “reset” the default value. The duration of the INIT reset is typ 1.0 ms.

INIT reset mode is also entered from INIT mode in case the expected SPI command does not occur in due time (ref. INIT mode), and if device is not in debug mode.

INIT

This mode is automatically entered from “INIT reset” mode. In this mode, the device must be configured via SPI within a time of 256 ms max.

Four registers called INIT Wdog, INIT REG, INIT LIN I/O and INIT MISC must be and can only be configured during INIT mode.

Other registers can be written in this mode, however they can be also written in other modes.

Once the INIT registers configuration is done, a SPI Watchdog Refresh command must be send in order to set the device into Normal mode. If the SPI W/D refresh does not occur within the 256 ms period, the device will return into INIT reset mode for typ 1.0 ms, and then re enter into INIT mode.

Register read operation is allowed in INIT mode to collect device status or to read back the INIT register configuration

When INIT mode is left by a SPI W/D refresh command, it is only possible to re enter the INIT mode using a secured SPI command. In INIT mode, the CAN, LIN1, LIN2, VAUX, I/O_x and Analog MUX functions are not operating. The 5V-CAN is also not operating, except if the Debug mode is detected.

RESET

In this mode, the RST pin is asserted low. Reset mode is entered from Normal mode, Normal Request mode, LP V_{DD} on mode and from Flash mode, when the W/D is not triggered, or if a V_{DD} low condition is detected.

The duration of reset is typ 1.0 ms by default. The user can defined a longer Reset pulse activation only for the case the reset mode is entered following a V_{DD} low condition. Reset pulse is always 1.0 ms, in case reset mode is entered due to wrong a watchdog refresh command.

Reset mode can be entered via secured SPI command.

NORMAL REQUEST

This mode is automatically entered after RESET mode, or after a wake-up from Low Power V_{DD} ON mode.

A watchdog refresh SPI command is necessary to transition to NORMAL mode. The duration of the Normal request mode is 256 ms when Normal Request mode is entered after RESET mode. Different duration can be selected by SPI for the case when normal request is entered from LP V_{DD} ON mode.

If the watchdog refresh SPI command does not occur within the 256 ms (or the shorter user defined time out), then the device will enter into RESET mode, for a duration of typ 1.0 ms.

Note: in init reset, init, reset and normal request modes as well as in low power modes, the V_{DD} external PNP is disabled.

NORMAL

In this mode, all device functions are available. This mode is entered by a SPI watchdog refresh command from Normal Request mode, or from INIT mode.

During Normal mode, the device watchdog function is operating, and a periodic watchdog refresh must occurs. In case of incorrect or missing watchdog refresh command device will enter into Reset mode.

From Normal mode, the device can be set by SPI command into Low Power modes (Low Power V_{DD} ON or Low Power V_{DD} OFF modes). Dedicated secured SPI commands must be used to enter from Normal mode in Reset mode, INIT mode or Flash mode.

FLASH

In this mode, the software watchdog period is extended up to typ 32 seconds. This allow programming of the MCU flash memory while minimizing the software over head to refresh the watchdog. The flash mode is entered by Secured SPI command and is left by SPI command. Device will enter into Reset mode. In case of incorrect or missing watchdog refresh command device will enter into Reset mode. An interrupt can be generated at 50% of the watchdog period.

CAN interface operates in Flash mode to allow flash via CAN bus, inside the vehicle.

DEBUG

Debug is a special operation mode of the device which allows system easy software and hardware debugging. The debug operation is detected after power up if the DBG pin is set in the 8.0 to 10 V range.

When debug is detected, all the software watchdog operations are disabled: 256 ms of INIT mode, watchdog refresh of Normal mode and Flash mode, Normal Request time out (256 ms or user defined value) are not operating and will not lead to transition into INIT reset or Reset mode.

When device is in Debug, SPI command can be send without any time constraints with respect to watchdog operation, MCU program can be “halted” or “paused” to verify proper operation.

Debug can be left by removing 8 to 10 V from the DEBUG pin, or by SPI command (ref to MODE register).

5 V-CAN regulator is ON by default in debug mode.

LOW POWER MODES

The device has two main Low Power modes: Low Power mode with V_{DD} OFF, and Low Power mode with V_{DD} on.

Prior to entering into Low Power mode, I/O and CAN wake up flags must be cleared (ref to mode register). If the wake-up flags are not cleared, the device will not enter into Low Power mode. In addition, the CAN failure flags (i.e CAN_F and CAN_UF) must be cleared, in order to meet the Low Power current consumption specification.

LOW POWER - V_{DD} OFF

In this mode, V_{DD} is turned off and the MCU connected to VDD is unsupplied. This mode is entered by the SPI. It can also be entered by automatic transition due to fail safe management. 5 V-CAN and V_{AUX} regulators are also turned OFF.

When the device is in Low Power V_{DD} OFF mode, it monitors external events to wake-up and leave the LP mode. The wake-up events can occurs from:

- CAN
- LIN interface, depending upon device part number
- Expiration of an internal timer
- I/O-0, and I/O-1 inputs, and depending upon device part number and configuration, I/O-2 and/or -3 input
- Cyclic sense of I/O-1 input, associated by I/O-0 activation, and depending upon device part number and configuration, cyclic sense of I/O-2 and -3 input, associated by I/O-0 activation

When a wake-up event is detected, the device enters into reset mode and then into Normal Request mode. The wake-up source are reported into the device SPI registers. In summary, a wake-up event from LP V_{DD} OFF, lead to V_{DD} regulator turn ON, and MCU operation restart.

LOW POWER - V_{DD} ON

In this mode, the voltage at the VDD pin remains at 5.0 V (or 3.3 V, depending upon device part number). The objective is to maintain the MCU powered, with reduced consumption. In such mode, the DC output current is expected to be limited to 100 μA or a few mA, as the ECU is in reduced power operation mode.

During this mode, the 5 V-CAN and V_{AUX} regulators are OFF. The optional external PNP at VDD will also be automatically disabled when entering this mode.

The same wake-up events as in LP V_{DD} OFF mode (CAN, LIN, I/O, timer, cyclic sense) are available in LP V_{DD} on mode.

In addition, two additional wake-up conditions are available.

- Dedicated SPI command. When device is in LP V_{DD} ON mode, the wake-up by SPI command uses a write to “Normal Request mode”, 0x5C10.
- Output current from VDD exceeding $L_{P\text{-}ITH}$ threshold.

In Low Power V_{DD} ON mode, the device is able to source several tenths of mA DC. The current source capability can be time limited, by a selectable internal timer. Timer duration is up to 32 ms, and is triggered when the output current exceed the output current threshold typ 1.5 mA.

This allow for instance a periodic activation of the MCU, while the device remains in LP V_{DD} on mode. If the duration exceed the selected time (ex 32 ms), the device will detect a wake-up.

Wake-up events are reported to the MCU via a low level pulse at $\overline{INT}$ pulse. The MCU will detect the $\overline{INT}$ pulse and resume operation.

Watchdog Function in LP V_{DD} ON mode

It is possible to enable the watchdog function in Low Power V_{DD} ON mode. In this case, the principle is timeout.

Refresh of the watchdog is done either by:

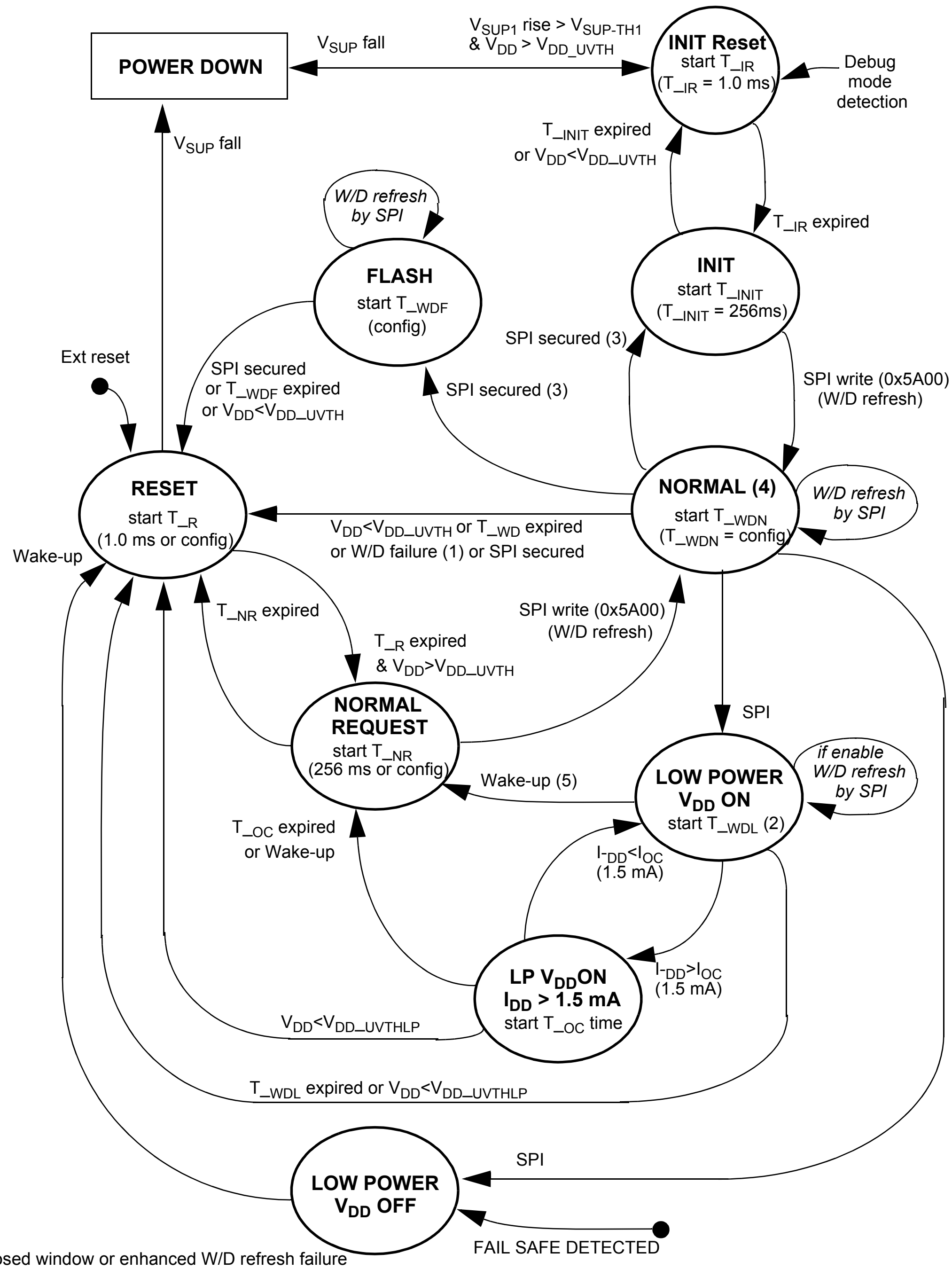
- a dedicated SPI command (different from any other SPI command or simple $\overline{CS}$ activation which would wake-up - ref to the previous paragraph)
- or by a temporary (less than 32 ms max) V_{DD} over current wake-up (I_{DD} > 1.5 mA typ).

As long as the watchdog refresh occurs, the device remains in LP V_{DD} on mode.

MODE transition

Mode transitions are either done automatically (i.e after timeout expired or voltage conditions), or via a SPI command, or by external event such as a wake-up. Some mode change are performed via “secured” SPI commands.

STATE DIAGRAM



(1) W/D refresh in closed window or enhanced W/D refresh failure

(2) If enable by SPI, prior to enter LP V_{DD} ON mode

(3) Ref to ‚ÄúSPI secure‚Äù descrip

(4) V_{DD} external PNP is disable in all mode except Normal and Flash modes.

(5) Wake-up from LP V_{DD} ON mode by SPI command is done by a SPI mode change: 0X5C10

Figure 20. State Diagram

MODE CHANGE

"SECURED SPI" DESCRIPTION:

A request is done by a SPI command, the device provide on MISO an unpredictable "random code". Software must perform a logical change on the code and return it to the device with the new SPI command to perform the desired action.

The "random code" is different at every exercise of the secured procedure and can be read back at any time.

The secured SPI uses the Special MODE register for the following transitions:

- from Normal mode to $\overline{\text{INT}}$ mode

- from Normal mode to Flash mode

- from Normal mode to Reset mode (reset request).

"Random code" is also used when the "advance watchdog" is selected.

CHANGING OF DEVICE CRITICAL PARAMETERS

Some critical parameters are configured one time at device power on only, while the batfail flag is set in the INIT mode. If a change is required while device is no longer in INIT mode, device must be set back in INIT mode using the "SPI secure" procedure.

WATCHDOG OPERATION

IN NORMAL REQUEST MODE

In Normal Request mode, the device expects to receive a watchdog configuration before the end of the normal request time out period. This period is reset to a long (256 ms) after power on and when BATFAIL is set.

The device can be configured to a different (shorter) time out period which can be used after wake-up from LP V_{DD} on mode.

After a software watchdog reset, the value is restored to 256 ms, in order to allow for a complete software initialization, similar to a device power up.

In Normal Request mode the watchdog operation is "timeout" only and can be triggered/served any time within the period.

WATCHDOG TYPE SELECTION

Three types of W/D operation can be used:

- Window watchdog (default)
- Timeout operation
- Advanced

The selection of W/D is performed in INIT mode. This is done after device power up and when the BATFAIL flag is set. W/D configuration is done via the SPI. Then, the W/D mode selection content is locked and can be changed only via a secured SPI procedure.

Window Watchdog Operation

The window watchdog is available in Normal mode only. The watchdog period selection can be kept (SPI is selectable in INIT mode), while the device enters into Low Power V_{DD} ON mode. The watchdog period is reset to the default long period after BATFAIL.

The period and the refresh of watchdog is done by the SPI. A refresh must be done in the open window of the period, which starts at 50% of the selected period and ends at the end of the period.

If the watchdog is triggered before 50%, or not triggered before end of period, a reset has occurred. The device enters into Reset mode.

Watchdog in Debug Mode

When the device is in Debug mode (entered via the DBG pin), the watchdog continues to operate but does not affect the device operation by asserting a reset. For the user, operation appears without the watchdog.

When debug is left by software (SPI mode reg) the watchdog period starts at the end of the SPI command.

When debug mode is left by hardware (DBG pin below 8-10 V), the device enters into Reset mode.

Watchdog in Flash Mode

During Flash mode operation, the watchdog can be set to a long timeout period. Watchdog is timeout only and an $\overline{\text{INT}}$ pulse can be generated at 50% of the time window.

Advance Watchdog Operation

When the Advance watchdog is selected (at INIT mode), the refresh of the watchdog must be done using a random number and with 1, 2, or 4 SPI commands. The number for the SPI command is selected in INIT mode.

The software must read a random byte from the device, and then must return the random byte inverted to clear the watchdog. The random byte write can be performed in 1, 2, or 4 different SPI commands.

If one command is selected, all eight bits are written at once.

If two commands are selected, first write command must include four of the eight bits of the inverted random byte. The second command must include the next four bits. This complete the watchdog refresh.

If four commands are selected, the first write command must include two of the eight bits of the inverted random byte. The second command must include the next two bits, the 3rd command the next two, and the last command, the last two. This complete the watchdog refresh.

When multiple writes are used, the most significant bits are send first. The latest SPI command needs to be done inside the open window time frame, if window watchdog is selected.

DETAIL SPI OPERATION AND SPI COMMANDS FOR ALL WATCHDOG TYPES.

All SPI commands and examples given in this document do not make use of the parity functions.

In INIT mode, the watchdog type (window, timeout, advance and number of SPI commands) is selected using register Init W/D, bits 1, 2 and 3. The watchdog period is selected via TIM_A register. The watchdog period selection can also be done in Normal mode or in Normal Request mode.

Transition from INIT mode to Normal mode or from Normal Request mode to Normal mode is done via a single W/D refresh command (SPI 0x 5A00).

While in Normal mode, the watchdog refresh command depends upon the watchdog type selected in INIT mode. They are detailed in the paragraph below:

Simple Watchdog:

Refresh command is 0x5A00. It can be send any time within the watchdog period, if the timeout watchdog operation is selected (INIT-watchdog register, bit 1 WD N/Win = 0).

It must be send in the open window (second half of the period) if the Window Watchdog operation was selected (INIT-watchdog register, bit 1 WD N/Win = 1).

Advance Watchdog:

The first time device enters in Normal mode (entry on Normal mode using the 0x5A00 command), Random (RNDM) code must be read using SPI command 0x1B00. Device returns on MISO second byte the RNDM code. The full 16 bits MISO is called 0x XXRD. $\overline{RD}$ is the complement of the RD byte.

Advance Watchdog, Refresh by 1 SPI Command:

The refresh command is 0x5A$\overline{RD}$. During each refresh command device returns on MISO a new Random Code. This new random code must be inverted and send along with the next refresh command and so on.

It must be done in the open window if the Window operation was selected.

Advance Watchdog, Refresh by two SPI Commands:

The refresh command is splitted in two SPI commands.

The first partial refresh command is 0x5Aw1, and the second is 0x5Aw2. Byte w1 contains the first four inverted bits of the RD byte plus the last four bits equal to zero. Byte w2 contains four bits equal to zero plus the last four inverted bits of the RD byte.

During this second refresh command device return on MISO a new Random Code. This new random code must be inverted and send along with the next two refresh commands and so on.

The second command must be done in the open window if the Window operation was selected.

Advance Watchdog, Refresh by four SPI Commands:

The refresh command is splitted in four SPI commands.

The first partial refresh command is 0x5Aw1, the second is 0x5Aw2, the third is 0x5Aw3, and the last is 0x5Aw4.

Byte w1 contains the first two inverted bits of the RD byte, plus the last six bits equal to zero.

Byte w2 contains two bits equal to zero, plus the next two inverted bits of the RD byte, plus four bits equal to zero.

Byte w3 contains four bits equal to zero, plus the next two inverted bits of the RD byte, plus two bits equal to zero.

Byte w4 contains six bits equal to zero, plus the next two inverted bits of the RD byte.

During this fourth refresh command device return on MISO a new Random Code. This new random code must be inverted and send along with the next four refresh commands.

The fourth command must be done in the open window if the Window operation was selected.

PROPER RESPONSE TO $\overline{INT}$

A device detect, that upon an $\overline{INT}$, the software handles the $\overline{INT}$ in a timely manner: Access of the $\overline{INT}$ register is done within two watchdog periods. Such feature must be enabled by SPI via the INIT watchdog register bit 7

FUNCTIONAL BLOCK OPERATION VERSUS MODE

Table 6. Device Block Operation for Each State

State	V_{DD}	5 V-CAN	I/O-x / WU	V_{AUX}	CAN	LIN1/2
Power down	OFF	OFF	OFF	OFF	High-impedance	High-impedance
Init Reset	ON	OFF	HS/LS off Wake-up disable	OFF	OFF: CAN termination 25 k to GND Transmitter / receiver /wake-up OFF	OFF: internal 30k pull-up active. Transmitter: receiver / wake-up OFF. LIN term OFF
INIT	ON	OFF[24]	SPI config WU disable	OFF	OFF	OFF
Reset	ON	Keep SPI config	HS/LS off WU disable	OFF	OFF	OFF
Normal Request	ON	Keep SPI config	HS/LS off WU disable	OFF	OFF	OFF
Normal	ON	SPI config	SPI config WU SPI config	SPI config	SPI config	SPI config
Low power V_{DD} OFF	OFF	OFF	user defined WU SPI config	OFF	OFF + wake-up en/dis	OFF + wake-up en/dis
Low power V_{DD} ON	ON[23]	OFF	user defined WU SPI config	OFF	OFF + wake-up en/dis	OFF + wake-up en/dis
SAFE output low: Safe case A	safe case A:ON safe case B: OFF	A: Keep SPI config, B: OFF	HS/LS off wake-up by change state	OFF	OFF + wake-up enable	OFF + wake-up enable
FLASH	ON	SPI config	SPI config	SPI config	SPI config	OFF

Notes
23. With limited current capability
24. 5 V-CAN is ON in Debug mode.

The 5 V-CAN default is ON when the device is powered-up and set in Debug mode. It is fully controllable via the SPI command.

ILLUSTRATION OF DEVICE MODE TRANSITIONS.

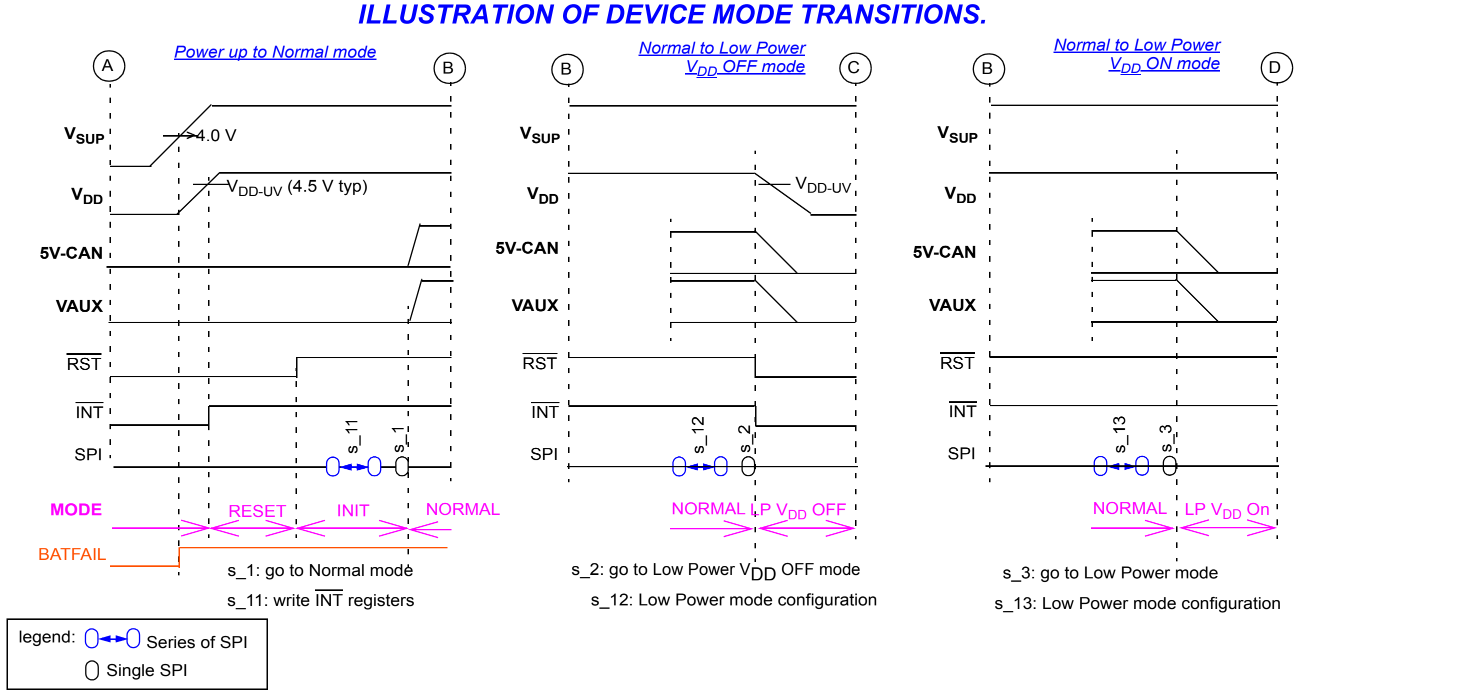


Figure 21. Power Up Normal and Low Power Modes

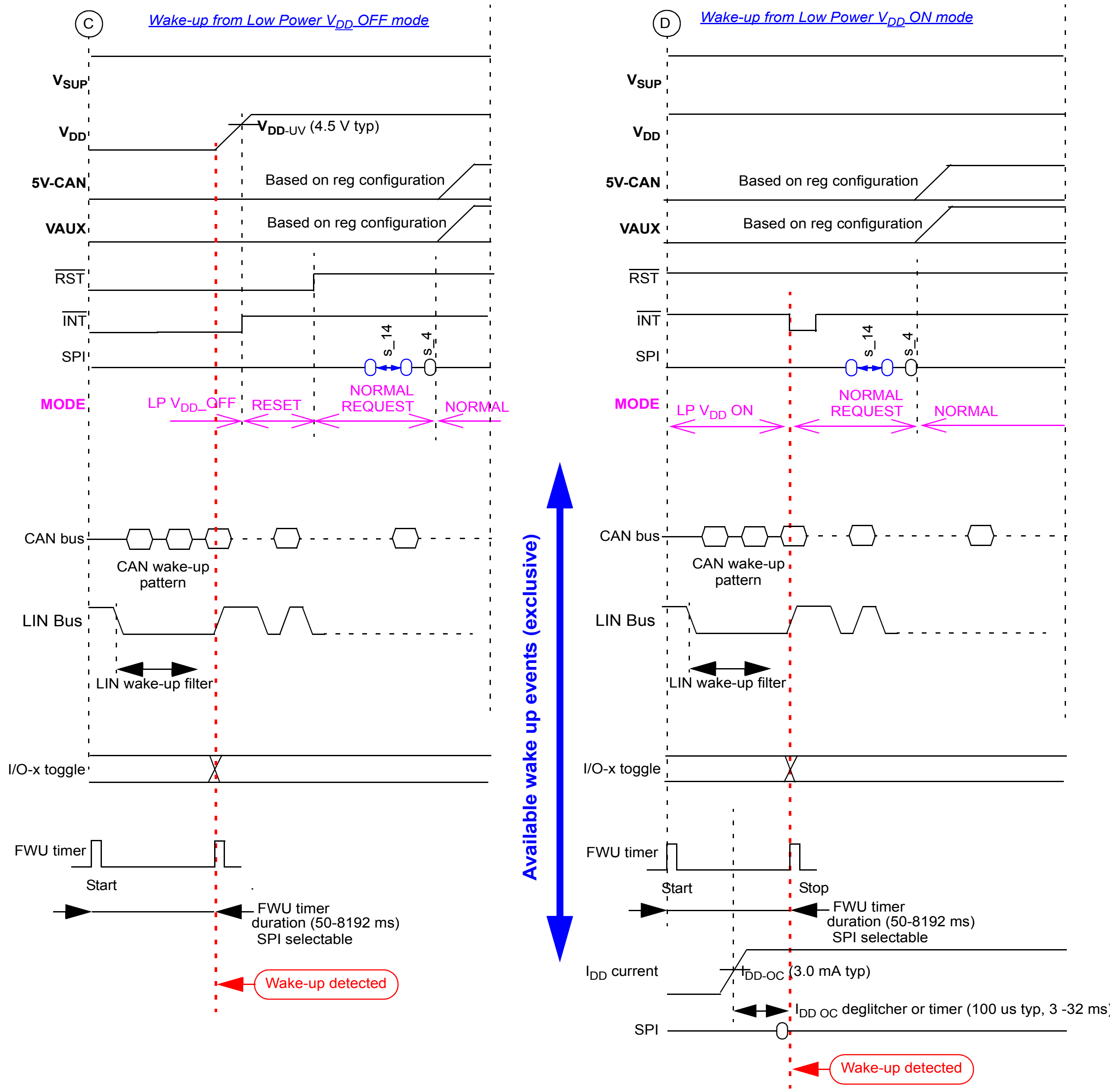


Figure 22. Wake-up from Low Power Modes

CYCLIC SENSE OPERATION DURING LOW POWER MODES

This function can be used in both Low Power (LP) modes: V_{DD} OFF and V_{DD} ON.

Cyclic sense is the periodic activation of I/O-0 to allow biasing of external contact swicthes. The contact switch state can be detected via I/O-1, -2, and -3, and device can wake-up from either LP mode.

Cyclic sense is optimized and designed primarily for closed contact switch in order to minimize consumption via the contact pull-up resistor.

Principle

A dedicated timer allows to select a cyclic sense period from 3.0 to 512 ms (selection in timer B).

At end of the period, the I/O-0 will be activated for a duration of $T_{\_CSON}$ (SPI selectable in INIT register, to 200 µs, 400 µs, 800 µs, or 1.6 ms). The I/O-0 high side transistor or low side transistor can be activated. The selection is done by the state of I/O-0 prior to enter in low power mode.

During the T_{-CSON} duration, the I/O-x are monitored. If one of them is high, the device will detect a wake-up. (Figure 23).

Cyclic sense period is selected by SPI configuration prior to enter in device low power mode. Upon entering LP mode, I/O-0 should be activated.

The level of I/O-1 is sense during the I/O-0 active time, and is deglitched for a duration of typ 30 µs. This mean that I/O-1 should be in the expected state for a duration longer than the deglitcher time.

The diagram below (Figure 23) illustrates the cyclic sense operation, with I/O-0 high side active and I/O-1 wake-up in case of high level.

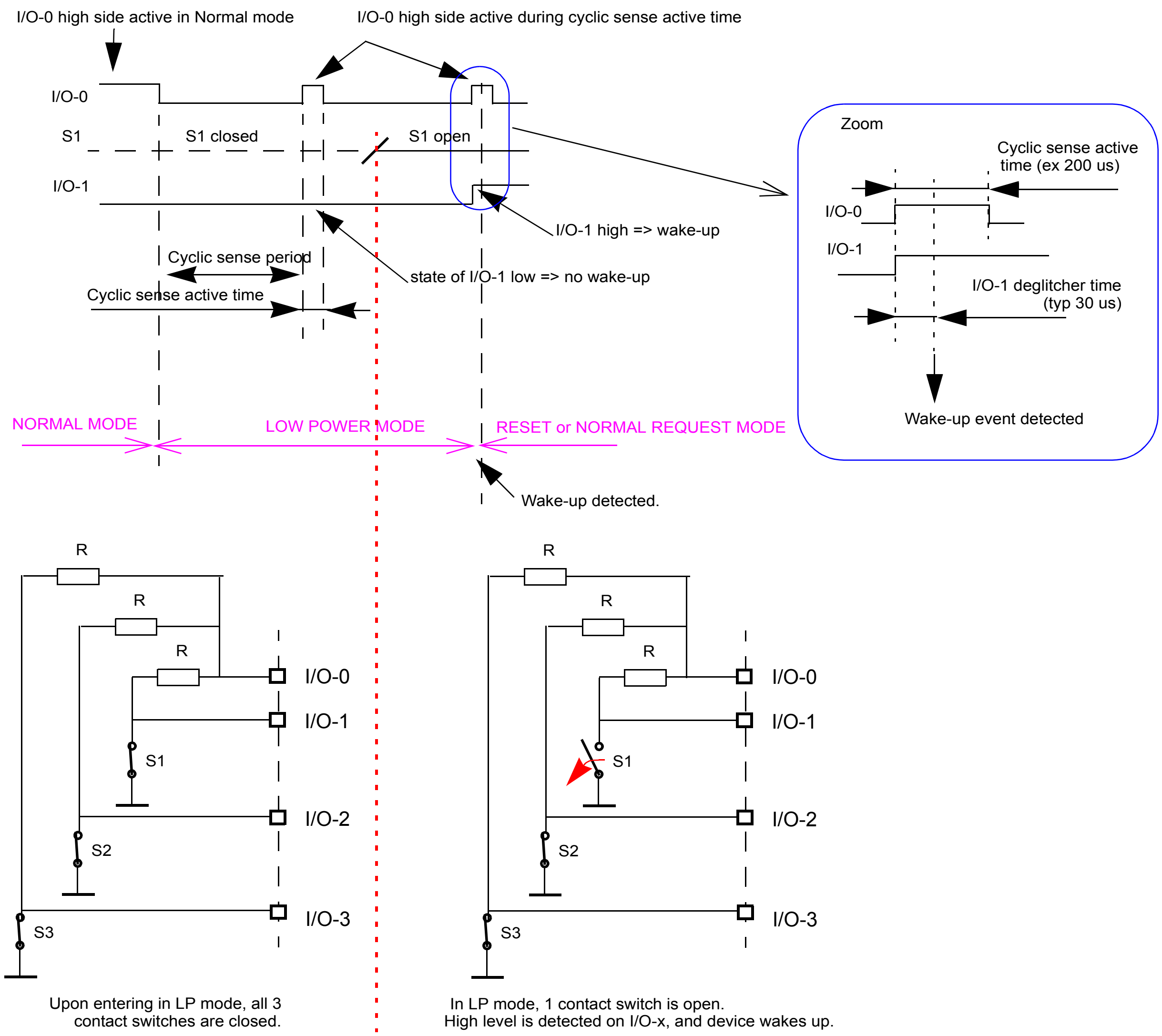


Figure 23. Cyclic Sense Operation - Switch to GND, Wake-up by Open Switch

CYCLIC INT OPERATION DURING LOW POWER VDD ON MODE

Principle

This function can be used only in Low Power V_{DD} ON mode (LP V_{DD} ON).

When Cyclic INT is selected and device is in LP V_{DD} ON mode, the device will generate a periodic INT pulse.

Upon reception of the INT pulse, the MCU must acknowledge the INT by sending SPI commands before the end of the next INT period in order to keep the process going.

When Cyclic INT is selected and operating, the device remains in LP V_{DD} ON mode, assuming the SPI commands are issued properly. When no/improper SPI commands are sent, the device will cease Cyclic INT operation and leave LP V_{DD} ON mode by issuing a reset. The device will then enter into Normal Request mode.

VDD current capability and VDD regulator behavior is similar as in LP V_{DD} ON mode.

Operation

Cyclic INT period selection: register timer B

SPI command in hex 0x56xx [example; 0x560E for 512ms cyclic Interrupt period (SPI command without parity bit)].

This command must be send while the device is in Normal Mode.

SPI commands to acknowledge INT: (2 commands)

- read the Random code via the W/D register address using the following command: MOSI 0x1B00 device report on MISO second byte the RNDM code (MISO bit 0-7).

- write W/D refresh command using the random code inverted: 0x5A RNDb.

These commands can occur at any time within the period.

Initial entry in LP mode with Cyclic INT: after the device is set in LP V_{DD} ON mode, with cyclic INT enable, no SPI command is necessary until the first INT pulse occurs. The acknowledge process must start only after the 1st INT pulse.

Leave Low Power Mode with Cyclic INT:

This is done by a SPI wake-up command, similar to SPI wake-up from LP V_{DD} ON mode: 0x5C10. The device will enter into Normal Request mode.

Improper SPI command while Cyclic INT operates:

When no/improper SPI commands are sent, while the device is in LP V_{DD} ON mode with Cyclic INT enable, the device will cease Cyclic INT operation and leave LP V_{DD} ON mode by issuing a reset. The device will then enter into Normal Request mode.

The figure below (Figure 24) describes the complete Cyclic Interrupt operation.

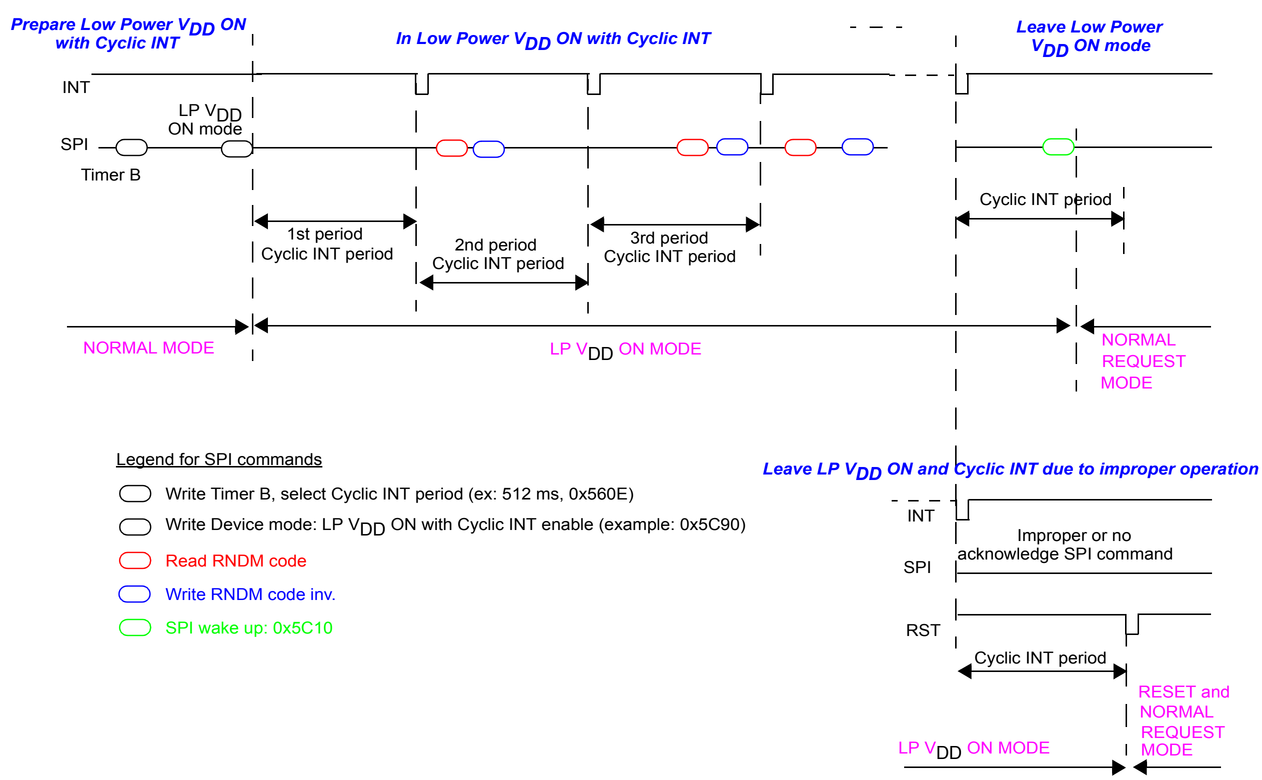


Figure 24. Cyclic Interrupt Operation

BEHAVIOR AT POWER UP AND POWER DOWN

DEVICE POWER UP:

This section describe the device behavior during ramp up, and ramp down of V_{SUP1}, and the flexibility offered mainly by the Crank bit and the two V_{DD} under-voltage reset thresholds.

The figures below illustrate the device behavior during V_{SUP1} ramp up. As the Crank bit is by default set to 0, V_{DD} is enable when V_{SUP1} is above $V_{SUP\ TH\ 1}$ parameters.

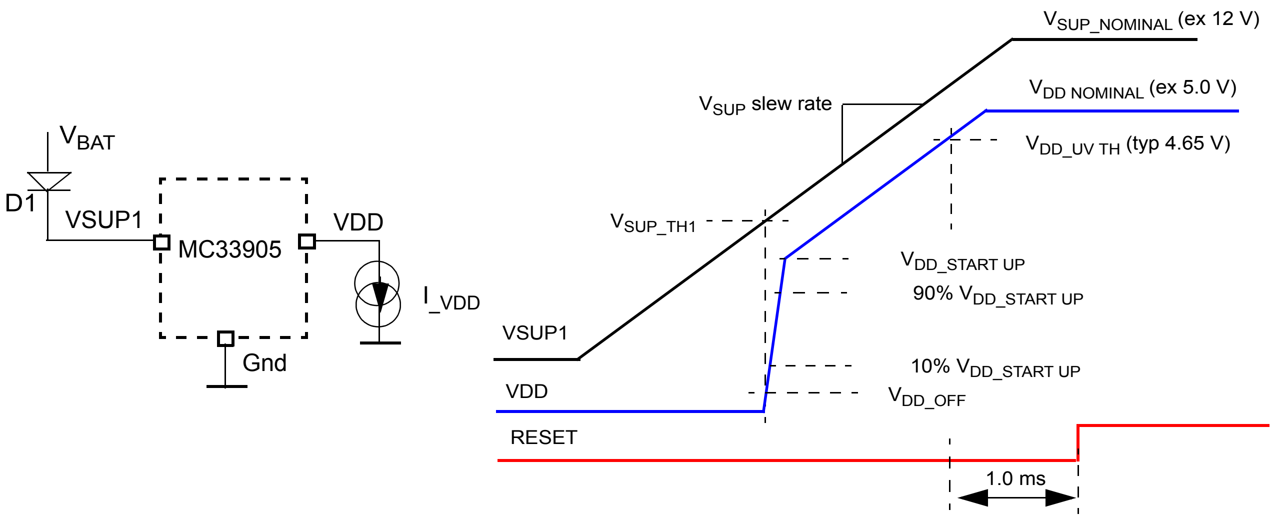


Figure 25. V_{DD} Start-up Versus V_{SUP1} Tramp

DEVICE POWER DOWN

The figures below illustrate the device behavior during V_{SUP1} ramp down, based on Crank bit configuration, and V_{DD} under-voltage reset selection.

Crank bit reset (INIT W/D register, bit 0 =0):

Bit 0 = 0 is the default state for this bit.

During V_{SUP} ramp down, V_{DD} remain ON until device enters in Reset mode due to a V_{DD} under-voltage condition (V_{DD} < 4.6 V or V_{DD} < 3.2 V typ, threshold selected by the SPI). When device is in Reset, if V_{SUP} is below “V_{SUP_TH1}”, V_{DD} is turned OFF.

Crank bit set (INIT Watchdog register, bit 0 =1):

The bit 0 is set by SPI write. During V_{SUP} ramp down, V_{DD} remains ON until device detects a POR and set BATFAIL. This occurs for a V_{SUP} approx 3.0 V.

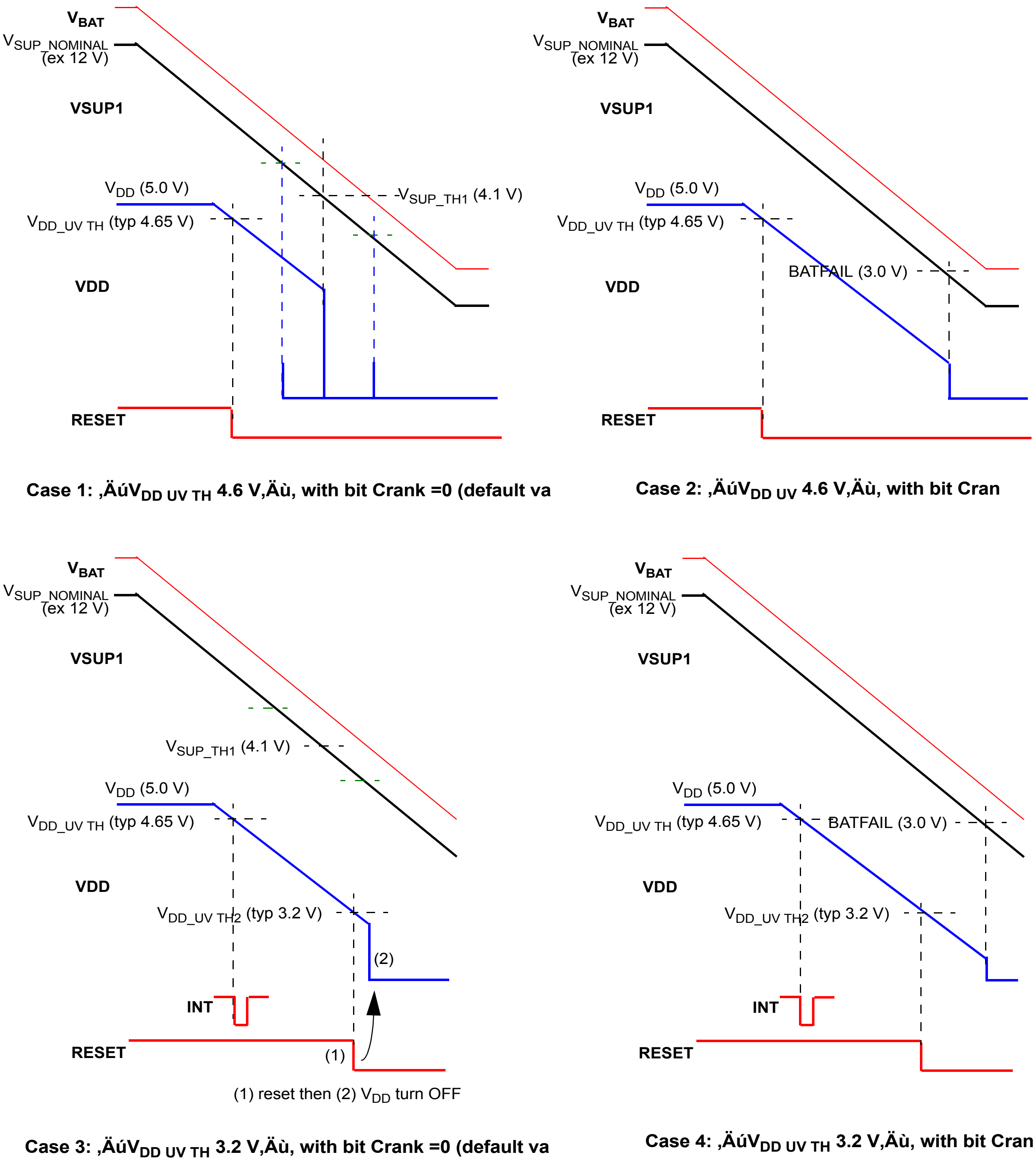


Figure 26. V_{DD} Behavior During V_{SUP1} Ramp Down

FAIL SAFE OPERATION

OVERVIEW

Fail safe mode is entered when specific fail conditions occur. The “Safe state” condition is defined by the resistor connected at the DGB pin. Safe mode is entered after additional event or conditions are met: time out for CAN communication and state at I/O-1 pin.

Exit of the safe state is always possible by a wake-up event: in the safe state the device is automatically wakeable CAN and I/O (if configured as inputs). Upon wake-up, the device operation is resumed: enter in Reset mode.

FAIL SAFE FUNCTIONALITY

Upon dedicated event or issue detected at a device pin (i.e RESET), the Safe mode can be entered. In this mode, the SAFE pin is active low.

Description

Upon activation of the SAFE pin, and if the failure condition that make the SAFE pin activated have not recovered, the device can help to reduce ECU consumption, assuming that the MCU is not able to set the whole ECU in low power mode. Two main cases are available:

Mode A:

Upon SAFE activation, the MCU remains powered (V_{DD} stays ON), until the failure condition recovers (i.e S/W is able to properly control the device and properly refresh the watchdog).

Modes B1, B2 and B3:

Upon SAFE activation, the system continues to monitor external event, and disable the MCU supply (turn V_{DD} OFF). The external events monitored are: CAN traffic, I/O-1 low level or both of them. 3 sub cases exist, B1, B2 and B3.

Note: no CAN traffic indicates that the ECU of the vehicle are no longer active, thus that the car is being parked and stopped. The I/O low level detection can also indicate that the vehicle is being shutdown, if the I/O-1 pin is connected for instance to a switched battery signal (ignition key on/off signal).

The selection of the monitored events is done by hardware, via the resistor connected at DBG pin, but can be over written by software, via a specific SPI command.

By default, after power up the device detect the resistor value at DBG pin (upon transition from INIT to Normal mode), and, if no specific SPI command related to Debug resistor change is send, operates according to the detected resistor.

The INIT MISC register allow to verify and change the device behaviour, to either confirm or change the hardware selected behaviour. Device will then operate according to the SAFE mode configured by the SPI.

Table 7 illustrates the complete options available:

Table 7. Fail Safe Options

Resistor at DBG pin	SPI coding - register INIT MISC bits [2,1,0] (higher priority that Resistor coding)	Safe mode code	V_{DD} status
<6.0 k	bits [2,1,0) = [111]: verification enable: resistor at DBG pin is typ 0 kohm (RA) - Selection of SAFE mode A	A	remains ON
typ 15 k	bits [2,1,0) = [110]: verification enable: resistor at DBG pin is typ 15 kohm (RB1) - Selection of SAFE mode B1	B1	Turn OFF 8.0 s after CAN traffic bus idle detection.
typ 33 k	bits [2,1,0) = [101]: verification enable: resistor at DBG pin is typ 33 kohm (RB2 - Selection of SAFE mode B2	B2	Turn OFF when I/O-1 low level detected.
typ 68 k	bits [2,1,0) = [100]: verification enable: resistor at DBG pin is typ 68 kohm (RB3) - Selection of SAFE mode B3	B3	Turn OFF 8.0 s after CAN traffic bus idle detection AND when I/O-1 low level detected.

Exit of Safe Mode

Exit of the safe state with V_{DD} OFF is always possible by a wake-up event: in this safe state the device is automatically wakeable by CAN and I/O (if I/O wake-up was enable by the SPI prior to enter in SAFE mode). Upon wake-up, the device operation is resumed, and device enters in Reset mode. The SAFE pin remains active, until a proper read and clear of the SPI flags reporting the SAFE conditions.

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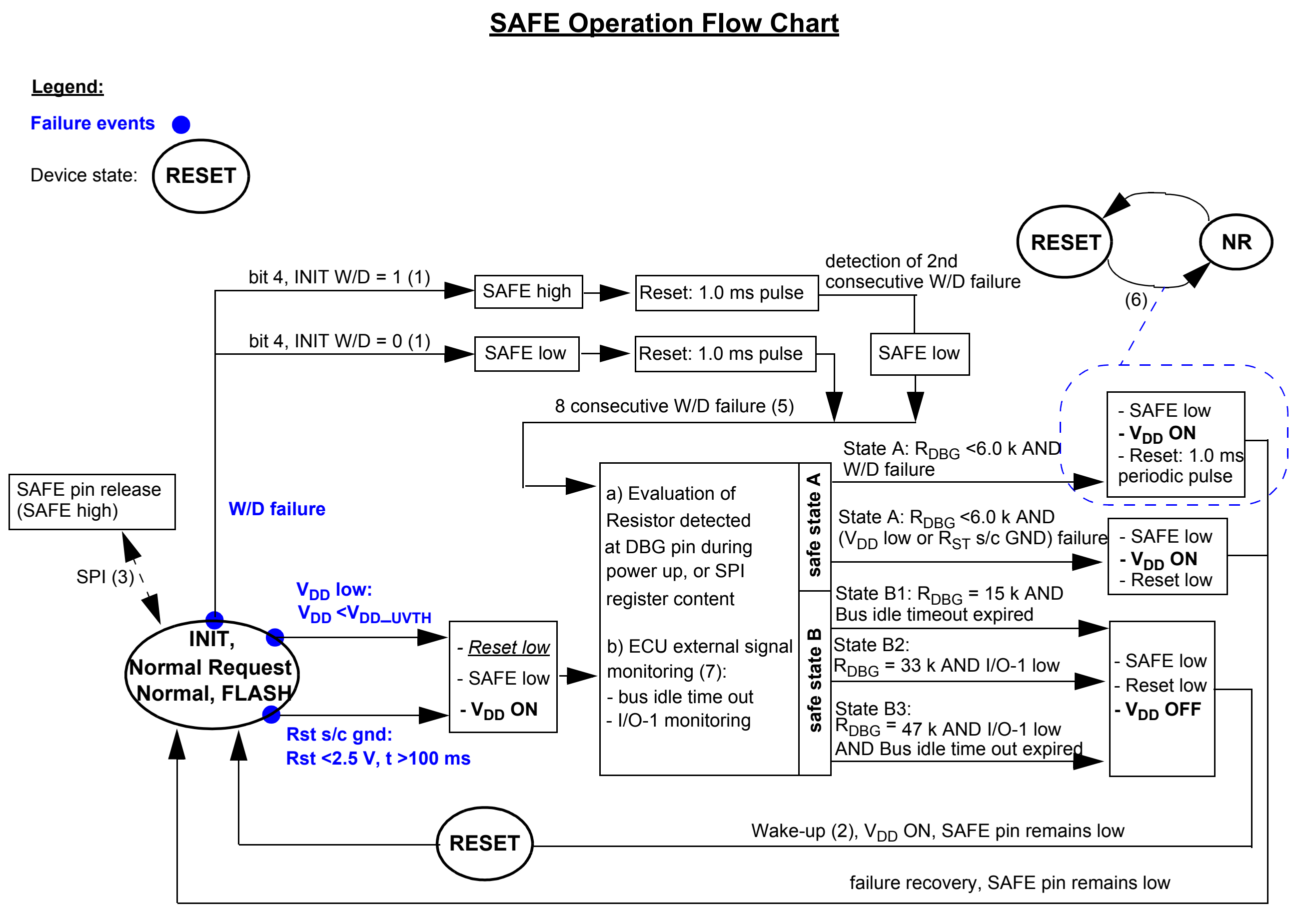

1) bit 4 of INIT Watchdog register
2) Wake-up event: CAN, LIN or I/O-1 high level (if I/O-1 wake-up previously enabled)
3) SPI commands: 0xDD00 or 0xDD80 to release SAFE pin
4) Recovery: reset low condition released, V_{DD} low condition released, correct SPI W/D refresh
5) detection of 8 consecutive W/D failures: no correct SPI W/D refresh command occurred for duration of 8 x 256 ms.
6) Dynamic behavior: 1.0 ms reset pulse every 256 ms, due to no W/D refresh SPI command, and device state transition between RESET and NORMAL REQUEST mode, or INIT RESET and INIT modes.
7) 8 second timer for bus idle timeout. I/O-1 high to low transition.

Figure 27. Safe Operation Flow Chart

Conditions to set SAFE pin active low:

Watchdog refresh issue: SAFE activated at 1st reset pulse or at the second consecutive reset pulse (selected by bit 4, INIT W/D register).

V_{DD} low: V_{DD} < R_{ST-TH}. SAFE pin is set low at same time as the RESET pin is set low.

The RESET pin is monitored to verify that reset is not clamped to a low level preventing the MCU to operate. If this is the case, the Safe mode is entered.

SAFE Mode A Illustration:

Figure 28 illustrates the event, and consequences when SAFE mode A is selected via the appropriate debug resistor or SPI configuration.

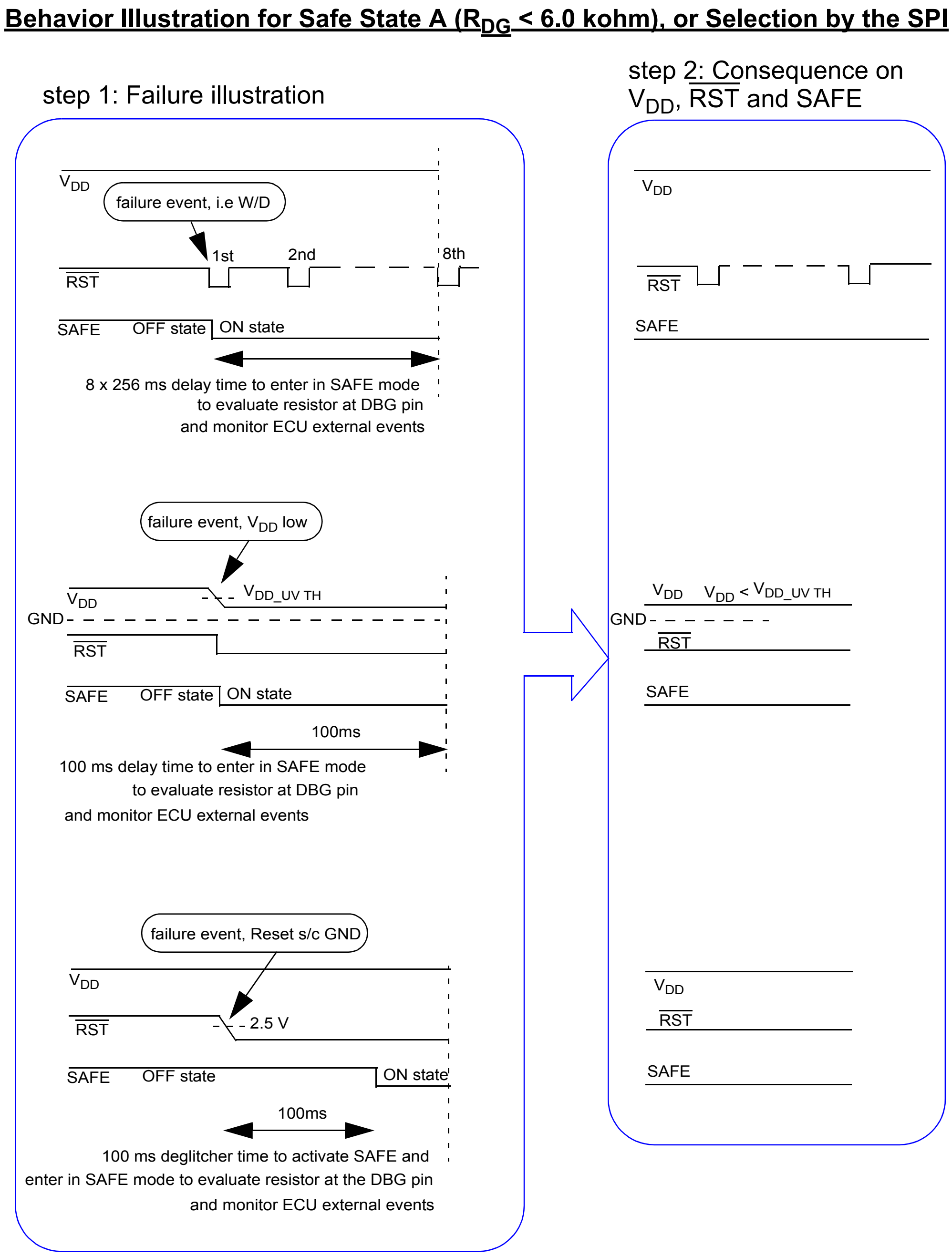

Figure 28. SAFE Mode A Behavior Illustration

SAFE mode B1, B2 and B3 illustration:

Figure 29 illustrates the event, and consequences when SAFE mode B1, B2, or B3 is selected via the appropriate debug resistor or SPI configuration.

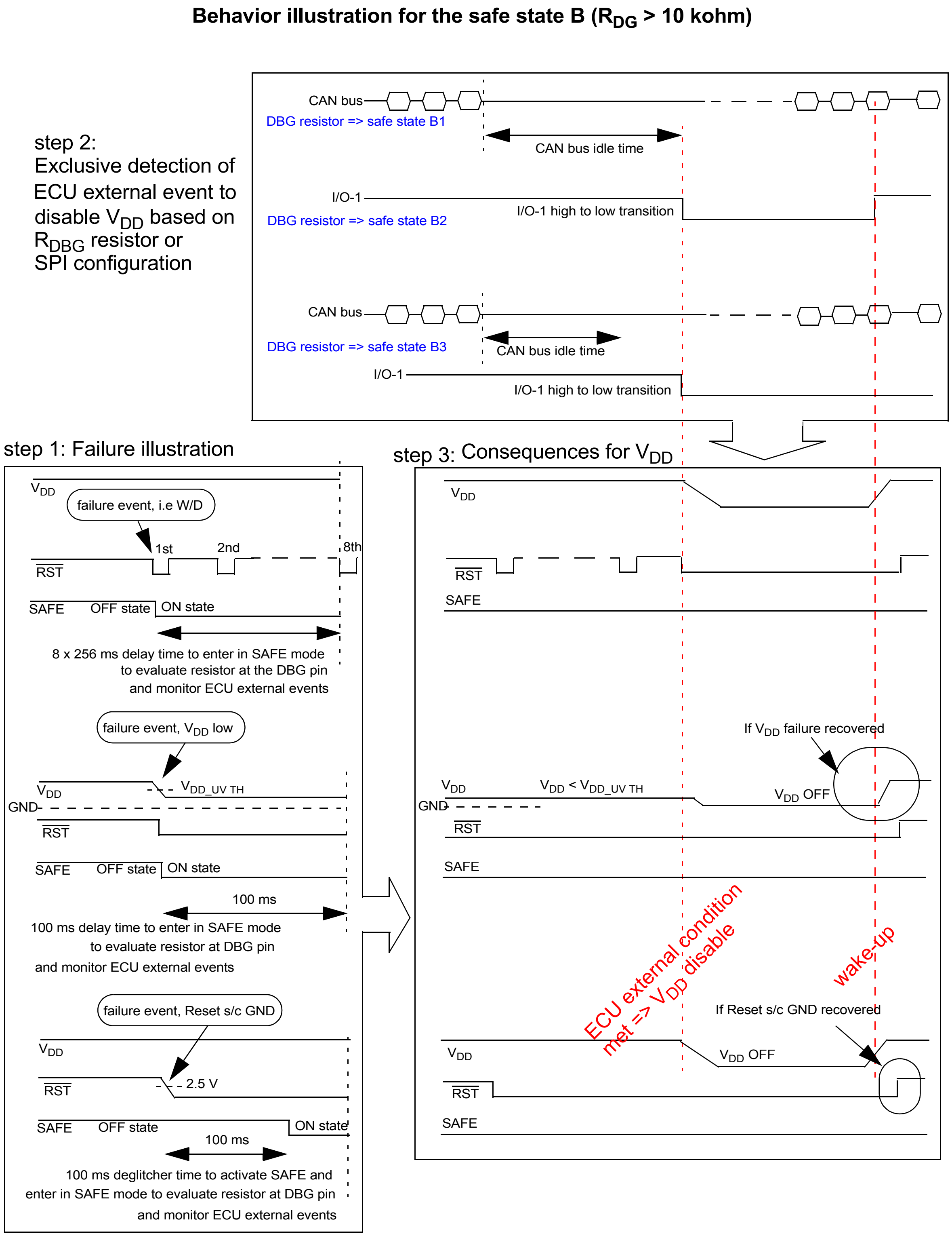

Figure 29. SAFE Modes B1, B2, or B3 Behavior Illustration

CAN INTERFACE

CAN INTERFACE DESCRIPTION

The figure below is a high level schematic of the CAN interface. It consist in a low side driver between CANL and gnd, and high side driver from CANH to 5 V-CAN. Two differential receivers are connected between CANH and CANL, to detect bus state and to wake up from CAN Sleep mode. An internal 2.5 V reference provide the 2.5 V recessive level via the matched R_{IN} resistors. The resistors can be switched to GND in CAN Sleep mode. A dedicated split buffer provide a low-impedance 2.5 V to the Split pin, for recessive level stabilization.

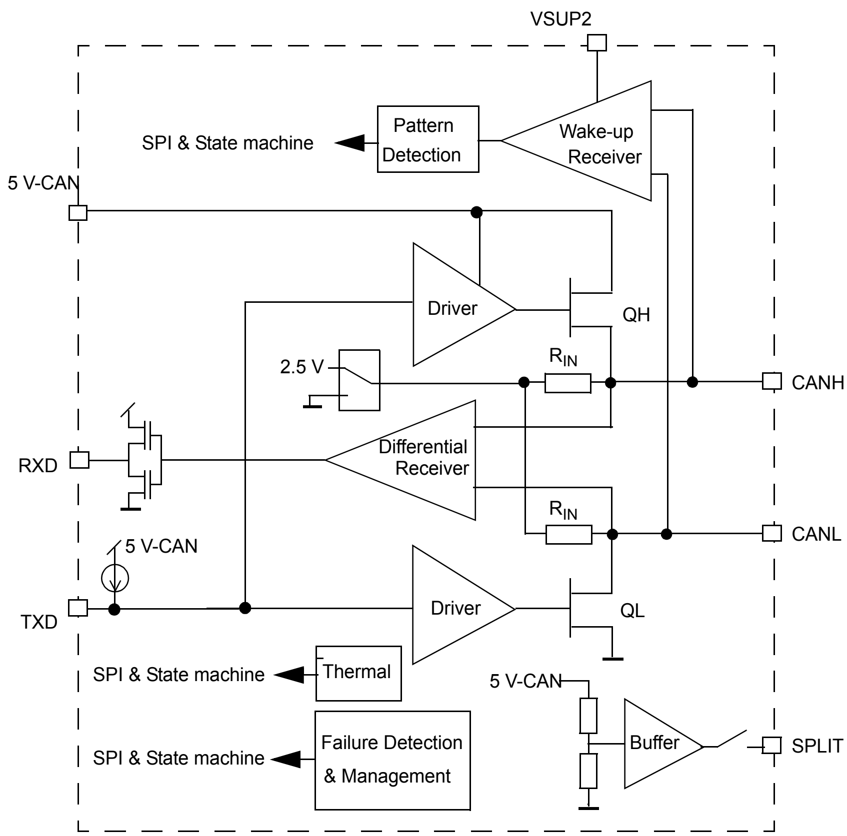

Figure 30. CAN Interface Block Diagram

CAN INTERFACE SUPPLY

The supply voltage for the CAN driver is the 5 V-CAN pin. The CAN interface also has a supply pass from the battery line, through the VSUP2 pin. This pass is used in CAN Sleep mode to allow wake-up detection.

During CAN communication (transmission and reception), the CAN interface current is sourced from the 5 V-CAN pin. During CAN Low Power mode, the current is sourced from the VSUP2 pin.

TXD/RXD MODE

In TxD/RxD mode, both the CAN driver and the receiver are ON. In this mode, the CAN lines are controlled by the TXD pin level, and the CAN bus state is reported on the RXD pin.

The 5 V-CAN regulator must be ON. It supplies the CAN driver and receiver.The SPLIT pin is active and a 2.5 V biasing is provided on the SPLIT output pin.

RECEIVE ONLY MODE

This mode is used to disable the CAN driver, but leave the CAN receiver active. In this mode, the device is only able to report the CAN state on the RXD pin. The TXD pin has no effect on CAN bus lines. The 5 V-CAN regulator must be ON. The SPLIT pin is active and a 2.5 V biasing is provided on the SPLIT output pin.

OPERATION in TXD/RXD Mode

The CAN driver will be enable as soon as the device is in Normal mode and the TXD pin is recessive.

When the CAN interface is in Normal mode, the driver has two states: recessive or dominant. The driver state is controlled by the TXD pin. The bus state is reported through the RXD pin.

When TXD is high, the driver is set in the recessive state, and CANH and CANL lines are biased to the voltage set with 5 V-CAN divided by 2, or approx. 2.5 V.

When TXD is low, the bus is set into the dominant state, and CANL and CANH drivers are active. CANL is pulled low and CANH is pulled high.

The RXD pin reports the bus state: CANH minus the CANL voltage is compared versus an internal threshold (a few hundred mV).

If "CANH minus CANL" is below the threshold, the bus is recessive and RXD is set high.

If "CANH minus CANL" is above the threshold, the bus is dominant and RXD is set low.

The SPLIT pin is active and provide a 2.5 V biasing to the SPLIT output.

TxD/RxD Mode and Slew Rate Selection

The CAN signal slew rate selection is done via the SPI. By default and if no SPI is used, the device is in the fastest slew rate. Three slew rates are available. The slew rate controls the recessive to dominant, and dominant to recessive transitions. This also affects the delay time from the TXD pin to the bus, and from the bus to the RXD. The loop time is thus affected by the slew rate selection.

Minimum Baud rate

The minimum baud is determined by the shortest TXD permanent dominant timing detection. The maximum number of consecutive dominant bits in a frame is 12 (6 bits of active error flag and its echo error flag).

The shortest TXD dominant detection time of 300 μs lead to a single bit time of: 300 μs / 12 = 25 μs.

So the minimum Baud rate is 1 / 25 μs = 40 kBaud.

SLEEP MODE

Sleep mode is a reduced current consumption mode. CANH and CANL driver are disabled and CANH and CANL lines are terminated to GND via the R_{IN} resistor, the SPLIT pin is high-impedance. In order to monitor bus activities, the CAN wake-up receiver can be enabled. It is supplied internally from V_{SUP2}.

Wake-up events occurring on the CAN bus pin are reporting by dedicated flags in SPI and by $\overline{INT}$ pulse, and results in a device wake-up if device was in Low Power mode.

When the device is set back into Normal mode, CANH and CANL are set back into the recessive level. This is illustrated in Figure 31.

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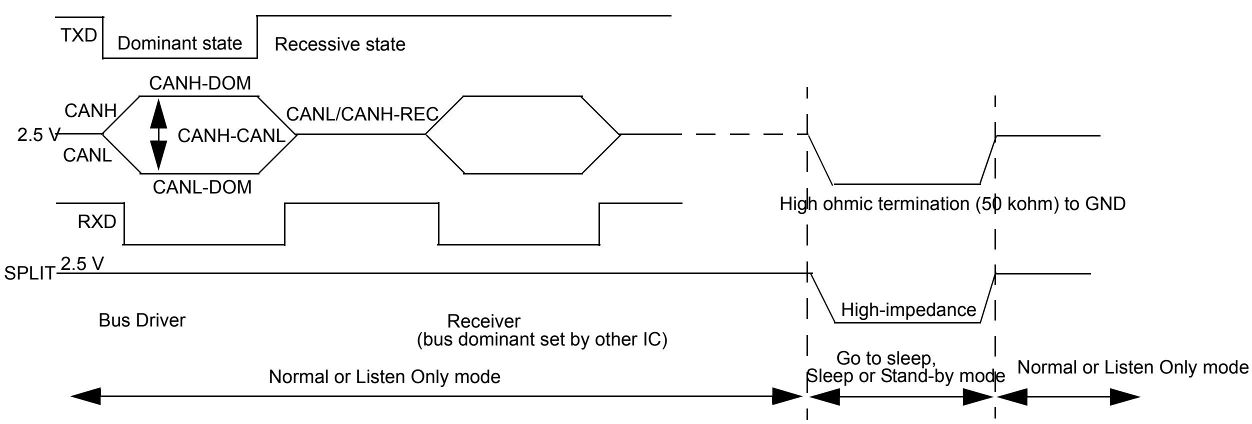

Figure 31. Bus Signal in TxD/RxD and Low Power Mode

Wake-up

When the CAN interface is in Sleep mode with wake-up enabled, the CAN bus traffic is detected. The CAN bus wake-up is a pattern wake-up. The wake-up by the CAN is enabled or disabled via the SPI.

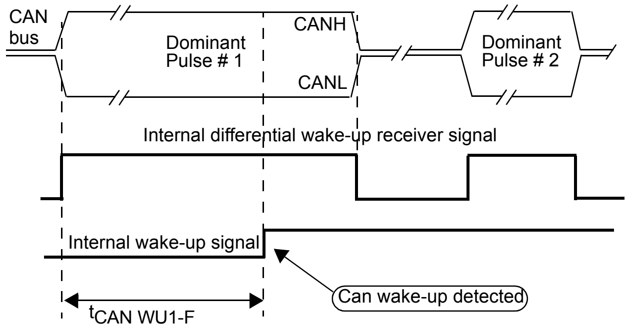

Figure 32. Single Dominant Pulse Wake-up

Pattern Wake-up

In order to wake-up the CAN interface, the wake-up receiver must receive a series of three consecutive valid dominant pulses, by default when the CANWU bit is low. CANWU bit can be set high by SPI and the wake-up will occur after a single pulse duration of 2.0 µs (typ).

A valid dominant pulse should be longer than 500 ns. The three pulses should occur in a time frame of 120 µs, to be considered valid. When three pulses meet these conditions, the wake signal is detected. This is illustrated by the following figure.

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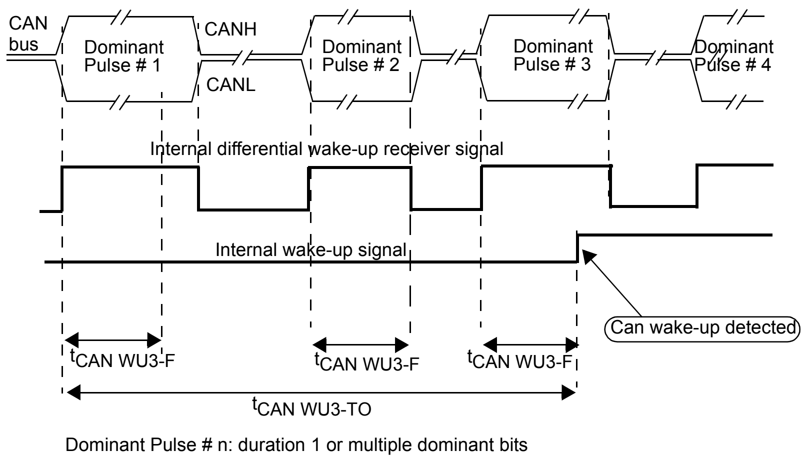


Figure 33. Pattern Wake-up - Multiple Dominant Detection

BUS TERMINATION

The device supports the two main types of bus terminations:

- Differential termination resistors between CANH and CANL lines.
- The figure below illustrate some of the most co
- SPLIT termination concept, with the mid point of the differential termination connected to GND through a capacitor and to the SPLIT pin.
- In application, device can also be used without termination.
- Figure 34 illustrates some of the most common terminations.

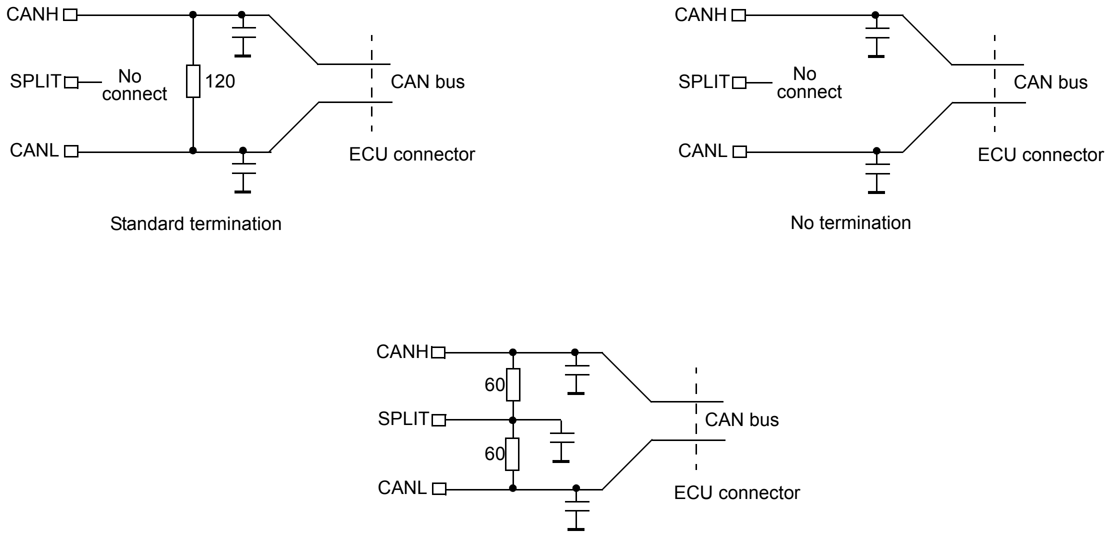


Figure 34. Bus Termination Options

CAN BUS FAULT DIAGNOSTIC

The device includes diagnostic of bus short-circuit to GND, VBAT, and internal ECU 5.0 V. Several comparators are implemented on CANH and CANL lines. These comparators monitor the bus level in the recessive and dominant states. The information is then managed by a logic circuitry to properly determine the failure and report it.

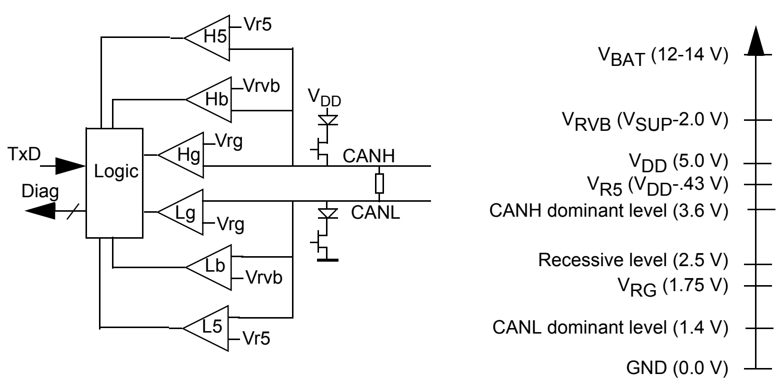


Figure 35. CAN Bus Simplified Structure Truth Table for Failure Detection

The following table indicates the state of the comparators in case of a bus failure, and depending upon the driver state.

Table 8. Failure Detection Truth Table

Failure Description	Driver Recessive State		Driver Dominant State	
	Lg (threshold 1.75 V)	Hg (threshold 1.75 V)	Lg (threshold 1.75 V)	Hg (threshold 1.75 V)
No failure	1	1	0	1
CANL to GND	0	0	0	1
CANH to GND	0	0	0	0
	Lb (threshold V_{SUP} -2.0 V)	Hb (threshold V_{SUP} -2.0 V)	Lb (threshold V_{SUP} -2.0 V)	Hb (threshold V_{SUP} -2.0 V)
No failure	0	0	0	0
CANL to VBAT	1	1	1	1
CANH to VBAT	1	1	0	1

Table 8. Failure Detection Truth Table

Failure Description	Driver Recessive State		Driver Dominant State	
	Lg (threshold 1.75 V)	Hg (threshold 1.75 V)	Lg (threshold 1.75 V)	Hg (threshold 1.75 V)
	L5 (threshold V_{DD} -0.43 V)	H5 (threshold V_{DD} -0.43 V)	L5 (threshold V_{DD} -0.43 V)	H5 (threshold V_{DD} -0.43 V)
No failure	0	0	0	0
CANL to 5.0 V	1	1	1	1
CANH to 5.0 V	1	1	0	1

DETECTION PRINCIPLE

In the recessive state, if one of the two bus lines are shorted to GND, VDD (5.0 V), or VBAT, the voltage at the other line follows the shorted line, due to the bus termination resistance. For example: if CANL is shorted to GND, the CANL voltage is zero, the CANH voltage measured by the Hg comparator is also close to zero.

In the recessive state, the failure detection to GND or VBAT is possible. However, it is not possible with the above implementation to distinguish which of the CANL or CANH lines are shorted to GND or VBAT. A complete diagnostic is possible once the driver is turned on, and in the dominant state.

Number of Samples for Proper Failure Detection

The failure detector requires at least one cycle of the recessive and dominant states to properly recognize the bus failure. The error will be fully detected after five cycles of the recessive-dominant states. As long as the failure detection circuitry has not detected the same error for five recessive-dominant cycles, the error is not reported.

BUS CLAMPING DETECTION

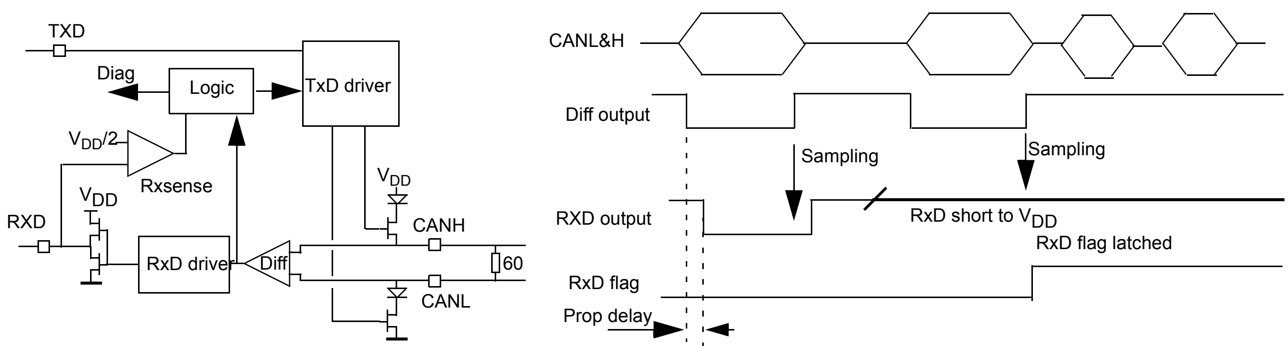
If the bus is detected to be in dominant for a time longer than (T_{DOM}), the bus failure flag is set and the error is reported in the SPI.

Such condition could occur in case the CANH line is shorted to a high-voltage. In this case, current will flow from the high-voltage short-circuit, through the bus termination resistors (60 Ω), into the SPLIT pin (if used), and into the device CANH and CANL input resistors, which are terminated to internal 2.5 V biasing or to GND (Sleep mode).

Depending upon the high-voltage short-circuit, the number of nodes, usage of the SPLIT pin, R_{IN} actual resistor and mode state (Sleep or Active) the voltage across the bus termination can be sufficient to create a positive dominant voltage between CANH and CANL, and the RXD pin will be low. This would prevent start of any CAN communication, and thus a proper failure identification (requires five pulses on TXD). The bus dominant clamp circuit will help to determine such failure situation.

RXD PERMANENT RECESSIVE FAILURE

The aim of this detection, is to diagnose an external hardware failure at the RxD output pin and ensure that a permanent failure at RxD does not disturb the network communication. If RxD is shorted to a logic high signal, the CAN protocol module within the MCU will not recognize any incoming message. In addition it will not be able to easily distinguish the bus idle state and can start communication at any time. In order to prevent this, an RxD failure detection is necessary.



The RxD flag is not the RXPR bit in the LPC register, and neither is the CANF in the INTR register.

Figure 36. RxD Path Simplified Schematic, RxD Short to V_{DD} Detection

Implementation for Detection

The implementation sense the RXD output voltage at each low to high transition of the differential receiver. Excluding the internal propagation delay, the RXD output should be low when the differential receiver is low. In case of an external short to VDD at the RXD output, RXD will be tied to a high level and can be detected at the next low to high transition of the differential receiver.

As soon as the RXD permanent recessive is detected, the RXD driver is deactivated.

Once the error is detected the driver is disabled and the error is reported via SPI in CAN register.

Recovery Condition

The internal recovery is done by sampling a correct low level at TXD as shown in the following illustration.

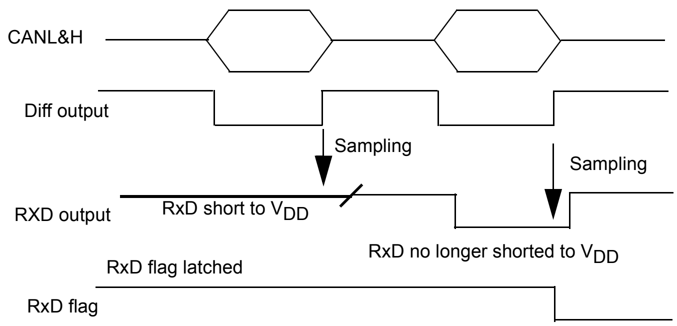


Figure 37. RxD Path Simplified Schematic, RxD Short to V_{DD} Detection

TXD PERMANENT DOMINANT

Principle

If the TXD is set to a permanent low level, the CAN bus is set into dominant level, and no communication is possible. The device has a TXD permanent timeout detector. After the timeout, the bus driver is disabled and the bus is released into a recessive state. The TXD permanent flag is set.

Recovery

The TXD permanent dominant is used and activated also in case of a TXD short to RXD. The recovery condition for a TXD permanent dominant (recovery means the re-activation of the CAN drivers) is done by entering into a Normal mode controlled by the MCU or when TXD is recessive while RXD change from recessive to dominant.

TXD TO RXD SHORT-CIRCUIT:

Principle

In case TXD is shorted to RXD during incoming dominant information, RXD is set low. Consequently, the TXD pin is low and drives CANH and CANL into a dominant state. Thus the bus is stuck in dominant. No further communication is possible.

Detection and Recovery

The TXD permanent dominant timeout will be activated and release the CANL and CANH drivers. However, at the next incoming dominant bit, the bus will then be stuck in dominant again. The recovery condition is same as the TXD dominant failure

IMPORTANT INFORMATION FOR BUS DRIVER REACTIVATION

The driver stays disabled until the failure is/are removed (TxD and/or RxD is no longer permanent dominant or recessive state or shorted) and the failure flags cleared (read). The CAN driver must be set by SPI in TxD/RxD mode in order to re enable the CAN bus driver.

LIN BLOCK

LIN INTERFACE DESCRIPTION

The physical interface is dedicated to automotive LIN sub-bus applications.

The interface has 20 kbps and 10 kbps baud rates, and includes as well as a fast baud rate for test and programming modes. It has excellent ESD robustness and immunity against disturbance, and radiated emission performance. It has safe behavior in case of a LIN bus short-to-ground, or a LIN bus leakage during low power mode.

Digital inputs are related to the device VDD pin.

POWER SUPPLY PIN (VSUP2)

The VSUP2 pin is the supply pin for the LIN interface. To avoid a false bus message, an under-voltage on VSUP2 disables the transmission path (from TXD to LIN) when V_{SUP} falls below 6.1 V.

GROUND PIN (GND)

In case of a ground disconnection at the module level, the LIN interface do not have significant current consumption on the LIN bus pin when in the recessive state.

LIN BUS PIN (LIN1, LIN2)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems, and is compliant to the LIN bus specification 2.1 and SAEJ2602-2.

The LIN interface is only active during Normal mode.

Driver Characteristics

The LIN driver is a low side MOSFET with internal over-current thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated so no external pull-up components are required for the application in a slave node. An additional pull-up resistor of 1.0 kΩ must be added when the device is used in the master node. The 1.0 kΩ pull-up resistor can be connected to the LIN pin or to the ECU battery supply.

The LIN pin exhibits no reverse current from the LIN bus line to VSUP2, even in the event of a GND shift or VSUP2 disconnection.

The transmitter has a 20 kbps, 10 kbps and fast baud rate, which are selected by SPI.

Receiver Characteristics

The receiver thresholds are ratiometric with the device V_{SUP2} voltage.

If the V_{SUP2} voltage goes below typ 6.1 V, the LIN bus enters into a recessive state even if communication is sent on TXD.

If LIN driver temperature reaches the over-temperature threshold, the transceiver and receiver are disabled. When the temperature falls below the over-temperature threshold, LIN driver and receiver will be automatically enabled.

DATA INPUT PIN (TXDL1, TXDL2)

The TXDl1 (TXDL2) input pin is the MCU interface to control the state of the LIN output. When TXDL is LOW (dominant), LIN output is LOW. When TXDL is HIGH (recessive), the LIN output transistor is turned OFF.

This pin has an internal pull-up current source to V_{DD} to force the recessive state if the input pin is left floating.

If the pin stays low (dominant sate) more than t_{TXDDOM}, the LIN transmitter goes automatically in recessive state. This is reported by flag in LIN register.

DATA OUTPUT PIN (RXDL1, RXDL2)

The RXDl output pin is the MCU interface, which reports the state of the LIN bus voltage.

LIN HIGH (recessive) is reported by a high voltage on RXD, LIN LOW (dominant) is reported by a low voltage on RXD.

LIN OPERATIONAL MODES

The LIN interface have two operational modes, Transmit receiver and LIN disable modes.

TRANSMIT RECEIVE

In the TxD/RxD mode, the LIN bus can transmit and receive information.

When the 20 kbps baud rate is selected, the slew rate and timing are compatible with LIN protocol specification 2.1.

When the 10 kbps baud rate is selected, the slew rate and timing are compatible with J2602-2.

When the fast baud rate is selected, the slew rate and timing are much faster than the above specification and allow fast data transition. The LIN interface can be set by the SPI command in TxD/RxD mode, only when TXDL is at a high level. When the SPI command is send while TXDL is low, the command is ignored.

SLEEP MODE

This mode is selected by SPI, and the transmission path is disabled. Supply current for LIN block from V_{SUP2} is very low (typ 3.0 μA). LIN bus is monitor to detect wake-up event. In the Sleep mode, the internal 725 kOhm pull-up resistor is connected and the 30 kOhm disconnected.

The LIN block can be awakened from Sleep mode by detection of LIN bus activity.

LIN Bus Activity Detection

The LIN bus wake-up is recognized by a recessive to dominant transition, followed by a dominant level with a duration greater than 70 μs, followed by a dominant to recessive transition. This is illustrated in Figures 17 and 18. Once the wake-up is detected, the event is reported to the device state machine. An INT is generated if device is in LP V_{DD} ON mode, or V_{DD} will restart if device was in LP V_{DD}OFF mode.

The wake-up can be enable or disable by the SPI.

Fail safe Features

Table 9 describes the LIN block behavior in case of failure.

Table 9. LIN Block Failure

FAULT	FUNCTIONNAL MODE	CONDITION	CONSEQUENCE	RECOVERY
LIN supply under-voltage	TxD RxD	LIN supply voltage < 6.0 V (typ)	LIN transmitter in recessive State	Condition gone
TXD Pin Permanent Dominant		TXD pin low for more than t_{TXDDOM}	LIN transmitter in recessive State	Condition gone
LIN Thermal Shutdown	TxD RxD	LIN driver temperature > 160°C (typ)	LIN transmitter and receiver disabled High Side turned off	Condition gone

SERIAL PERIPHERAL INTERFACE

HIGH LEVEL OVERVIEW

The device is using a 16 bits SPI, with the following arrangement:

MOSI, Master Out Slave In bits:

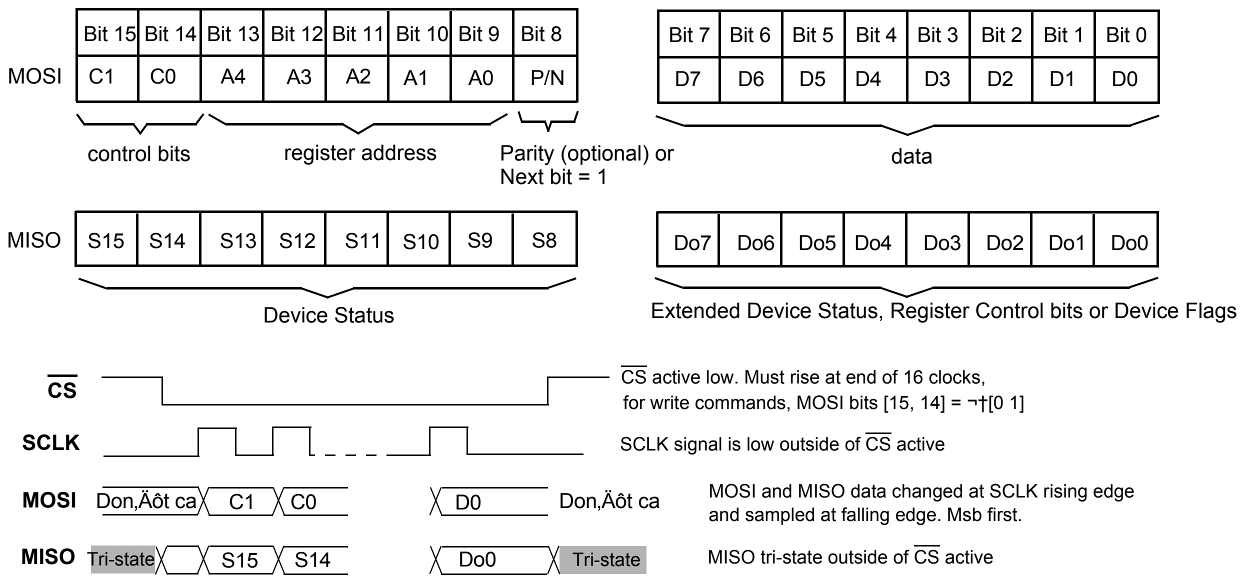
- bits 15 and 14 (called C1 and C0) are control bits to select the SPI operation mode (write control bit to device register, read back of the control bits, read of device flag).
- bit 13 to 9 (A4 to A0) to select the register address.
- bit 8 (P/N) has two functions: parity bit in write mode (optional, = 0 if not used), Next bit (= 1) in read mode.
- bit7 to 0 (D7 to D0): control bits

MISO, Master IN Slave Out bits:

- bits 15 to 8 (S15 to S8) are device status bits
- bits 7 to 0 (Do7 to Do0) are either extended device status bits, device internal control register content or device flags.

The SPI implementation does not support daisy chain capability.

Figure 38 is an overview of the SPI implementation.



SPI Wave Form, and Signals Polarity

Figure 38. Device SPI Overview

DETAIL OPERATION

BITS 15, 14 AND 8 FUNCTIONS

Table 10 summarizes the various SPI operation, depending upon bit 15, 14, and 8.

Table 10. SPI Operations (bits 8, 14 & 15)

Control Bits MOSI[15-14], C1-C0	Type of Command	Parity/Next MOSI[8] P/N	Note for Bit 8 P/N
00	Read back of register content and block (CAN, I/O, INT, LINs) real time state. See Table 37.	1	Bit 8 must be set to 1, independently of the parity function selected or not selected.
01	Write to register address, to control device operation	0	If bit 8 is set to “0”: means parity not selected OR parity is selected AND parity = 0
		1	if bit 8 is set to “1”: means parity is selected AND parity = 1
10	Reserved		
11	Read of device flags form a register address	1	Bit 8 must be set to 1, independently of the parity function selected or not selected.

BITS 13-9 FUNCTIONS

The device contains several registers. Their address is coded on five bits (bits 13 to 9).

Each register controls or reports part of the device function. Data can be written to the register, to control the device operation or set default value or behavior.

Every register can also be read back in order to ensure that its content (default setting or value previously written) is correct.

In addition some of the registers are used to report device flags.

Device status on MISO

When a write operation is performed to store data or control bit into the device, the MISO pin reports a 16 bits fixed device status composed of 2 bytes: Device Fixed Status (bits 15 to 8) + extended Device Status (bits 7 to 0). In a read operation, MISO will report the Fixed device status (bits 15 to 8) and the next eight bits will be the content of the selected register.

REGISTER ADRESS TABLE

Table 11 is the list of device registers and their associated address, coded with bits 13 to 9.

Table 11. Device Registers with Corresponding Address

Address MOSI[13-9] A4...A0	Description	Quick Ref. Name	Functionality
0_0000	Analog Multiplexer	MUX	1) Write “device control bits” to register address. 2) Read back register “control bits”
0_0001	Memory byte A	RAM_A	1) Write “data byte” to register address. 2) Read back “data byte” from register address
0_0010	Memory byte B	RAM_B	
0_0011	Memory byte C	RAM_C	
0_0100	Memory byte D	RAM_D	
0_0101	Initialization Regulators	Init REG	1) Write “device initialization control bits” to register address. 2) Read back “initialization control bits” from register address
0_0110	Initialization Watchdog	Init W/D	
0_0111	Initialization LIN and I/O	Init LIN I/O	
0_1000	Initialization Miscellaneous functions	Init MISC	
0_1001	Specific modes	SPE_MODE	1) Write to register to select device Specific mode, using “Inverted Random Code”. 2) Read “Random Code”

Table 11. Device Registers with Corresponding Address

0_1010	Timer_A: W/D & Low Power MCU consumption	TIM_A	1) Write “timing values” to register address. 2) Read back register “timing values”
0_1011	Timer_B: Cyclic Sense & Cyclic Interrupt	TIM_B	
0_1100	Timer_C: W/D Low Power & Forced Wake-up	TIM_C	
0_1101	Watchdog Refresh	W/D	Watchdog Refresh Commands
0_1110	Mode register	MODE	1) Write to register to select Low Power mode, with optional “Inverted Random code” and select wake-up functionality 2) Read operations: Read back device “Current mode” Read “Random Code”, Leave “Debug mode”
0_1111	Regulator Control	REG	1) Write “device control bits” to register address, to select device operation. 2) Read back register “control bits”. 3) Read device flags from each of the register addresses.
1_0000	CAN interface control	CAN	
1_0001	Input Output control	I/O	
1_0010	Interrupt Control	Interrupt	
1_0011	LIN1 interface control	LIN1	
1_0100	LIN2 interface control	LIN2	

COMPLETE SPI OPERATION

Table 12 is a compiled view of all the SPI capabilities and options. Both MOSI and MISO information are described.

Table 12. SPI Capabilities with Options

Type of Command	MOSI/ MISO	Control bits [15-14]	Address [13-9]	Parity/Next bits [8]	Bit 7	Bits [6-0]
Read back of “device control bits” (MOSI bit 7 = 0) OR Read specific device information (MOSI bit 7 = 1)	MOSI	00	address	1	0	000 0000
	MISO	Device Fixed Status (8 bits)			Register control bits content	
	MOSI	00	address	1	1	000 0000
	MISO	Device Fixed Status (8 bits)			Device ID and I/Os state	
Write device control bit to address selected by bits (13-9). MISO return 16 bits device status	MOSI	01	address	(note)	Control bits	
	MISO	Device Fixed Status (8 bits)			Device Extended Status (8 bits)	
Reserved	MOSI	10	Reserved			
	MISO	Reserved				
Read device flags and wake-up flags, from register address (bit 13-9), and sub address (bit 7). MISO return fixed device status (bit 15-8) + flags from the selected address and sub-address.	MISO	11	address	Reserved	0	Read of device flags form a register address, and sub address LOW (bit 7)
	MOSI	Device Fixed Status (8 bits)			Flags	
	MISO	11	address	1	1	Read of device flags form a register address, and sub address HIGH (bit 7)
	MOSI	Device Fixed Status (8 bits)			Flags	

Note: P = 0 if parity bit is not selected or parity = 0. P = 1 if parity is selected and parity = 1.

PARITY BIT 8

Calculation

The parity is used for write to register command (bit 15,14 = 01). It is calculated based on the number of logic one contained in bits 15-9,7-0 sequence (this is the whole 16 bits of the write command except bit 8).

Bit 8 must be set to 0 if the number of 1 is odd.

Bit 8 must be set to 1if the number of 1 is even.

Examples 1:

MOSI [bit 15-0] = 01 00 011 **P** 01101001, P should be 0, because the command contains 7 bits with logic 1.

Thus the Exact command will then be:

MOSI [bit 15-0] = 01 00 011 **0** 01101001

Examples 2:

MOSI [bit 15-0] = 01 00 011 P 0100 0000, P should be 1, because the command contains 4 bits with logic 1.

Thus the Exact command will then be:

MOSI [bit 15-0] = 01 00 011 **1** 0100 0000

Parity function selection:

All SPI commands and examples given in this document do not make use of the parity functions.

The parity function is optional. It is selected by bit 6 in INIT MISC register.

If parity function is not selected (bit 6 of INIT MISC = 0), then Parity bits in all SPI commands (bit 8) must be “0”.

DETAIL OF CONTROL BITS AND REGISTER MAPPING

The following tables contain register bit meaning arranged by register address, from address 0_000 to address 1_0100

MUX AND RAM REGISTERS

Table 13. MUX Register[(25)]

MOSI First Byte [15-8] [b_15 b_14] 0_0000 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 00 _ 000 P	MUX_2	MUX_1	MUX_0	Int 2K	I/O-att	0	0	0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR, 5 V-CAN off, any mode different from Normal							

Bits	Description
b7 b6 b5	**MUX_2, MUX_1, MUX_0** - Selection of external input signal or internal signal to be measured at MUX-OUT pin
000	All functions disable. No output voltage at MUX-OUT pin
001	V_{DD} regulator current recopy. Ratio is approx 1/97. Requires an external resistor or selection of Internal 2.0 K (bit 3)
010	Device internal voltage reference (approx 2.5 V)
011	Device internal temperature sensor voltage
100	Voltage at I/O-0. Attenuation or gain is selected by bit 3.
101	Voltage at I/O-1. Attenuation or gain is selected by bit 3.
110	Voltage at VSUP_1 pin. Refer to electrical table for attenuation ratio (approx 5)
111	Voltage at VSENSE pin. Refer to electrical table for attenuation ratio (approx 5)
b4	**INT 2k** - Select device internal 2.0 kohm resistor between AMUX and GND. This resistor allows the measurement of a voltage proportional to the V_{DD} output current.
0	Internal 2.0 kohm resistor disable. An external resistor must be connected between AMUX and GND.
1	Internal 2.0 kohm resistor enable.
b3	**I/O-att** - When I/O-0 (or I/O-1) is selected with b7,b6,b5 = 100 (or 101), b3 selects attenuation or gain between I/O-0 (or I/O-1) and MUX-OUT pin
0	Gain is approx 2 for device with V_{DD} = 5.0 V (Ref to electrical table for exact gain value) Gain is approx 1.3 for device with V_{DD} = 3.3 V (Ref to electrical table for exact gain value)
1	Attenuation is approx 6 for device with V_{DD} = 5.0 V (Ref to electrical table for exact attenuation value) Attenuation is approx 4 for device with V_{DD} = 3.3 V (Ref to electrical table for exact attenuation value)

Notes

25. The MUX register can be written and read only when the 5V-CAN regulator is ON. If the MUX register is written or read while 5V-CAN is OFF, the command is ignored, and the MXU register content is reset to default state (all control bits = 0).

Table 14. Internal Memory Registers A, B, C and D, RAM_A, RAM_B, RAM_C and RAM_D

MOSI First Byte [15-8] [b_15 b_14] 0_0xxx [P/N]	**MOSI Second Byte, bits 7-0**							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
01 00 _ 001 P	Ram a7	Ram a6	Ram a5	Ram a4	Ram a3	Ram a2	Ram a1	Ram a0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							
01 00 _ 010 P	Ram b7	Ram b6	Ram b5	Ram b4	Ram b3	Ram b2	Ram b1	Ram b0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							
01 00 _ 011 P	Ram c7	Ram c6	Ram c5	Ram c4	Ram c3	Ram c2	Ram c1	Ram c0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							
01 00 _ 100 P	Ram d7	Ram d6	Ram d5	Ram d4	Ram d3	Ram d2	Ram d1	Ram d0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

INIT REGISTERS

Note: these registers can be written only in INIT mode

Table 15. Initialization Regulator Registers, INIT REG (note: register can be written only in INIT mode)

MOSI First Byte [15-8] [b_15 b_14] 0_0101 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 00 _ 101 P	I/O-x sync	V_{DDL} rst[1]	V_{DDL} rst[0]	V_{DD} rstD[1]	V_{DD} rstD[0]	V_{AUX}5/3	Cyclic on[1]	Cyclic on[0]
Default state	1	0	0	0	0	0	0	0
Condition for default	POR							

Bit	Description
b7	**I/O-x sync** - Determine if I/O-1 is sensed during I/O-0 activation, when cyclic sense function is selected
0	I/O-1 sense anytime
1	I/O-1 sense during I/O-0 activation
b6, b5	**$V_{DDL\ RST}$[1] $V_{DDL\ RST}$[0] -** Select the V_{DD} under-voltage threshold, to activate RESET pin and/or INT
00	Reset at approx 0.9 V_{DD}.
01	INT at approx 0.9 V_{DD}, Reset at approx 0.7 V_{DD}
10	Reset at approx 0.7 V_{DD}
11	Reset at approx 0.9 V_{DD}.
b4, b3	**$V_{DD\ RST}$D[1] $V_{DD\ RST}$D[0] - Select the RESET pin low lev duration, after V_{DD} rises above the V_{DD} under-voltage threshold**
00	1.0 ms
01	5.0 ms
10	10 ms
11	20 ms

b2	**[V_{AUX} 5/3]** - Select Vauxilary output voltage
0	V_{AUX} = 3.3 V
1	V_{AUX} = 5.0 V

b1, b0	**Cyclic on[1] Cyclic on[0] - Determine I/O-0 activation time, when cyclic sense function is selected**
00	200 μs (typical value. ref to dynamic parameters for exact value)
01	400 μs (typical value. ref to dynamic parameters for exact value)
10	800 μs (typical value. ref to dynamic parameters for exact value)
11	1600 μs (typical value. ref to dynamic parameters for exact value)

Table 16. Initialization Watchdog Registers, INIT W/D (note: register can be written only in INIT mode)

MOSI First Byte [15-8] [b_15 b_14] 0_0110 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 00 _ 110 P	WD2INT	MCU_OC	OC-TIM	WD Safe	WD_spi[1]	WD_spi[0]	WD N/Win	Crank
Default state	0	1	0		0	0	1	0
Condition for default	POR							

Bit	**Description**
b7	**WD2INT -** Select the maximum time delay between INT occurrence and INT source read SPI command
0	Function disable. No constraint between INT occurrence and INT source read.
1	INT source read must occur before the remaining of the current W/D period plus 2 complete W/D periods.

b6, b5	**MCU_OC, OC-TIM -** In Low Power V_{DD} ON, select watchdog refresh and V_{DD} current monitoring functionality. $V_{DD\_OC\_LP}$ threshold is defined in device electrical parameters (approx 1.5 mA)
	In low power mode, when W/D is not selected
no W/D + 00	In Low Power V_{DD} ON mode, V_{DD} over-current has no effect
no W/D + 01	In Low Power V_{DD} ON mode, V_{DD} over-current has no effect
no W/D + 10	In Low Power V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time > 100 μs (typ) is a wake-up event
no W/D + 11	In Low Power V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time > I_mcu_OC is a wake-up event. I_mcu_OC time is selected in Timer register (selection range from 3.0 to 32 ms)
	In low power mode when W/D is selected
W/D + 00	In Low Power V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold has no effect. W/D refresh must occur by SPI command.
W/D + 01	In Low Power V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold has no effect. W/D refresh must occur by SPI command.
W/D + 10	In Low Power V_{DD} ON mode, V_{DD} over-current for a time > 100 μs (typ) is a wake-up event.
W/D + 11	In Low Power V_{DD} ON mode, V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time < I_mcu_OC is a W/D refresh condition. V_{DD} current > $V_{DD\_OC\_LP}$ threshold for a time > I_mcu_OC is wake-up event. I_mcu_OC time is selected in Timer register (selection range from 3.0 to 32 ms)

b4	**WD Safe -** Select the activation of the SAFE pin low, at first or second consecutive RESET pulse
0	SAFE pin is set low at the time of the RESET pin low activation
1	SAFE pin is set low at the second consecutive time RESET pulse

b3, b2	**WD_spi[1] WD_spi[0] -** Select the Watchdog (W/D) Operation
00	Simple Watchdog selection: W/D refresh done by a 8 bits or 16 bits SPI
01	Enhanced 1: Refresh is done using the Random Code, and by a single 16 bits.
10	Enhanced 2: Refresh is done using the Random Code, and by two 16 bits command.
11	Enhanced 4: Refresh is done using the Random Code, and by four 16 bits command.

b1	**WD N/Win -** Select the Watchdog (W/D) Window or Timeout operation
0	Watchdog operation is TIMEOUT, W/D refresh can occur anytime in the period
1	Watchdog operation is WINDOW, W/D refresh must occur in the open window (second half of period)

b0	**Crank -** Select the V_{SUP1} threshold to disable V_{DD}, while V_{SUP1} is falling toward GND
0	V_{DD} disable when V_{SUP1} is below typ 4.0 V (parameter $V_{SUP-TH1}$), and device in Reset mode
1	V_{DD} kept ON when V_{SUP1} is below typ 4.0 V (parameter V_{SUP_TH1})

Table 17. Initialization LIN and I/O Registers, INIT LIN I/O (note: register can be written only in INIT mode)

MOSI First Byte [15-8] [b_15 b_14] 0_0111 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 00 _ 111 P	I/O-1 ovoff	LIN_T2[1]	LIN_T2[0]	LIN_T1[1]	LIN_T1[0]	I/O-1 out-en	I/O-0 out-en	Cyc_Inv
Default state	0	0	0		0	0	0	0
Condition for default	POR							

Bit	**Description**
b7	**I/O-1 ovoff -** Select the deactivation of I/O-1 in case V_{DD} or V_{AUX} over-voltage condition is detected
0	Disable I/O-1 turn off.
1	Enable I/O-1 turn off, in case V_{DD} or V_{AUX} over-voltage condition is detected.

b6, b5	**LIN_T2[1], LIN_T2[0]** - Select pin operation as LIN Master pin switch or I/O
00	pin is OFF
01	pin operation as LIN Master pin switch
10	pin operation as I/O: high side switch and wake-up input
11	N/A

b4, b3	**LIN_T1[1], LIN_T1[0] -** Select pin operation as LIN Master pin switch or I/O
00	pin is OFF
01	pin operation as LIN Master pin switch
10	pin operation as I/O: high side switch and wake-up input
11	N/A

b2	**I/O-1 out-en**- Select the operation of the I/O-1 as output driver (high side, low side)
0	Disable high side and low side drivers of pin I/O-1. I/O-1 can only be used as input.
1	Enable high side and low side drivers of pin I/O-1. Pin can be used as input and output driver.

b1	**I/O-0 out-en -** Select the operation of the I/O-0 as output driver (high side, low side)
0	Disable high side and low side drivers of. I/O-0 can only be used as input.
1	Enable high side and low side drivers of the I/O-0 pin. Pin can be used as input and output driver.

b0	**Cyc_Inv -** Select I/O-0 operation in device Low Power mode, when cyclic sense is selected
0	During cyclic sense active time, I/O is set to the same state prior to enter in low power mode. During cyclic sense off time, I/O-0 is disable (high side and low side drivers OFF).
1	During cyclic sense active time, I/O is set to the same state prior to enter in low power mode. During cyclic sense off time, the opposite driver of I/O_0 is actively set. Example: If I/O_0 high side is ON during active time, then I/O_O low side is turned ON at expiration of the active time, for the duration of the cyclic sense period.

Table 18. Initialization Miscellaneous Functions, INIT MISC (Note: Register can be written only in INIT mode)

MOSI First Byte [15-8] [b_15 b_14] 0_1000 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 01_ 000 P	LPM w RNDM	SPI parity	INT pulse	INT width	INT flash	Dbg Res[2]	Dbg Res[1]	Dbg Res[0]
Default state	0	0	0		0	0	0	0
Condition for default	POR							

Bit	**Description**
b7	**LPM w RNDM -** This enables the usage of random bits 2, 1 and 0 of the MODE register to enter into Low Power VDD OFF or Low Power VDD ON.
0	Function disable: the Low Power mode can be entered without usage of Random Code
1	Function enabled: the Low Power mode is entered using the Random Code

b6	**SPI parity -** Select usage of the parity bit in SPI write operation
0	Function disable: the parity is not used. The parity bit must always set to logic 0.
1	Function enable: the parity is used, and parity must be calculated.

b5	**INT pulse -**Select INT pin operation: low level pulse or low level
0	INT pin will assert a low level pulse, duration selected by bit [b4]
1	INT pin assert a permanent low level (no pulse)

b4	**INT width -** Select the INT pulse duration
0	INT pulse duration is typ 100 μs. Ref to dynamic parameter table for exact value.
1	INT pulse duration is typ 25 μs. Ref to dynamic parameter table for exact value.

b3	**INT flash -** Select INT pulse generation at 50% of the Watchdog Period in Flash mode
	Function disable
	Function enable: an INT pulse will occur at 50% of the Watchdog Period when device in flash mode.

b2, b1, b0	**Dbg Res[2], Dbg Res[1], Dbg Res[0] -** Allow verification of the external resistor connected at DBG pin. Ref to parametric table for resistor range value.[(26)]
0xx	Function disable
100	100 verification enable: resistor at DBG pin is typ 68 kohm (RB3) - Selection of SAFE mode B3
101	101 verification enable: resistor at DBG pin is typ 33 kohm (RB2 - Selection of SAFE mode B2
110	110 verification enable: resistor at DBG pin is typ 15 kohm (RB1) - Selection of SAFE mode B1
111	111 verification enable: resistor at DBG pin is typ 0 kohm (RA) - Selection of SAFE mode A

Notes

26. Bits b2,1 and 0 allow the following operation:
First, check the resistor device has detected at the DEBUG pin. If the resistor is different, bit 5 (Debug resistor) is set in INTerrupt register (ref to device flag table).
Second, over write the resistor decoded by device, to set the SAFE mode operation by SPI. Once this function is selected by bit 2 = 1, this selection has higher priority than “hardware”, and device will behave according to b2,b1 and b0 setting

SPECIFIC MODE REGISTER

Table 19. Specific Mode Register, SPE_MODE

MOSI First Byte [15-8] [b_15 b_14] 01_001 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 01_ 001 P	Sel_Mod[1]	Sel_Mod[0]	Rnd_C5b	Rnd_C4b	Rnd_C3b	Rnd_C2b	Rnd_C1b	Rnd_C0b
Default state	0	0	0		0	0	0	0
Condition for default	POR							

Bit	**Description**
b7, b6	**Sel_Mod[1], Sel_Mod[0]** - Mode selection: these 2 bits are used to select which mode the device will enter upon a SPI command.
00	RESET mode
01	INIT mode
10	FLASH mode
11	N/A

b5....b0	**[Rnd_C4b... Rnd_C0b]** - Random Code inverted, these six bits are the inverted bits obtained from the SPE-MODE Register read command.

The SPE MODE register is used for the following operation:

- Set the device in RESET mode, to exercise or test the RESET functions.

- Go to INIT mode, using the Secure SPi command.

- Go to FLASH mode (in this mode the watchdog timer can be extended up to 32 s).

- Activate the SAFE pin by S/W.

These mode (called Special mode) are accessible via secured SPI command, which consist in 2 commands:

1) reading a random code and

2) then write the inverted random code plus mode selection or SAFE pin activation:

Return to INIT mode is done as follow (this is done from Normal mode only):

1) Read random code:

MOSI : 0001 0011 0000 0000 [Hex:0x 13 00]

MISO report 16 bits, random code are bits (5-0)

miso = xxxx xxxx xxR5 R4 R3 R2 R1 R0 (RxD = 6 bits random code)

2) Write INIT mode + random code inverted

MOSI : 0101 0010 01 Ri5 Ri4 Ri3 Ri2 Ri1 Ri0 [Hex 0x 52 HH] (R_{IX} = random code inverted)

MISO : xxxx xxxx xxxx xxxx (don’t care)

SAFE pin activation: SAFE pin can be set low, only in INIT mode, with following commands:

1) Read random code:

MOSI : 0001 0011 0000 0000 [Hex:0x 13 00]

MISO report 16 bits, random code are bits (5-0)

miso = xxxx xxxx xxR5 R4 R3 R2 R1 R0 (RxD = 6 bits random code)

2) Write INIT mode + random code bits 5:4 not inverted and random code bits 3:0 inverted

MOSI : 0101 0010 01 R5 R4 Ri3 Ri2 Ri1 Ri0 [Hex 0x 52 HH] (R_{IX} = random code inverted)

MISO : xxxx xxxx xxxx xxxx (don’t care)

Return to Reset or Flash mode is done similarly to the go to INIT mode, except that the b7, b6 are set according to table above (b7, b6 = 00 - go to reset, b7, b6 = 10 - go to Flash).

TIMER REGISTERS

Table 20. Timer Register A, Low Power V_{DD} Over-current & Watchdog Period Normal Mode, TIM_A

MOSI First Byte [15-8] [b_15 b_14] 01_010 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 01_ 010 P	I_mcu[2]	I_mcu[1]	I_mcu[1]	W/D Nor[4]	W/D_N[4]	W/D_Nor[3]	W/D_N[2]	W/D_Nor[0]
Default state	0	0	0	1	1	1	1	0
Condition for default	POR							

Low Power V_{DD} Over-current (ms)				
b7	**b6, b5**			
	00	01	10	11
0	3 (def)	6	12	24
1	4	8	16	32

Watchdog Period in Device Normal Mode (ms)								
b4, b3	**b2, b1, b0**							
	000	001	010	011	100	101	110	111
00	2.5	5	10	20	40	80	160	320
01	3	6	12	24	48	96	192	384
10	3.5	7	14	28	56	112	224	448
11	4	8	16	32	64	128	256 (def)	512

Table 21. Timer Register B, Cyclic Sense and Cyclic INT, in Device Low Power Mode, TIM_B

MOSI First Byte [15-8] [b_15 b_14] 01_011 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 01_ 011 P	Cyc-sen[3]	Cyc-sen[2]	Cyc-sen[1]	Cyc-sen[0]	Cyc-int[3]	Cyc-int[2]	Cyc-int[1]	Cyc-int[0]
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Cyclic Sense (ms)								
b7	**b6, b5, b4**							
	000	001	010	011	100	101	110	111
0	3	6	12	24	48	96	192	384
1	4	8	16	32	64	128	256	512

Cyclic Interrupt (ms)								
b3	**b2, b1, b0**							
	000	001	010	011	100	101	110	111
0	6 (def)	12	24	48	96	192	384	768
1	8	16	32	64	128	258	512	1024

Table 22. Timer Register C, Watchdog LP Mode or Flash Mode and Forced Wake-up Timer, TIM_C

MOSI First Byte [15-8] [b_15 b_14] 01_100 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 01_ 100 P	WD-LP-F[3]	WD-LP-F[2]	WD-LP-F[1]	WD-LP-F[0]	FWU[3]	FWU[2]	FWU[1]	FWU[0]
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Table 23. Typical Timing Values

Watchdog in Low Power V_{DD} ON Mode (ms)								
b7	**b6, b5, b4**							
	000	001	010	011	100	101	110	111
0	12	24	48	96	192	384	768	1536
1	16	32	64	128	256	512	1024	2048

Watchdog in Flash Mode (ms)								
b7	**b6, b5, b4**							
	000	001	010	011	100	101	110	111
0	48 (def)	96	192	384	768	1536	3072	6144
1	256	512	1024	2048	4096	8192	16384	32768

Forced Wake-up (ms)								
b3	**b2, b1, b0**							
	000	001	010	011	100	101	110	111
0	48 (def)	96	192	384	768	1536	3072	6144
1	64	128	258	512	1024	2048	4096	8192

WATCHDOG AND MODE REGISTERS

Table 24. Watchdog Refresh Register, W/D[27]

MOSI First Byte [15-8] [b_15 b_14] 01_101 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 01_ 101 P	0	0	0	0	0	0	0	0
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Notes
27. The Simple Watchdog Refresh command is in hexadecimal: 5A00. This command is used to refresh the W/D and also to transition from INIT mode to Normal mode, and from Normal Request mode to Normal mode (after a wake-up of a reset)

Table 25. MODE Register, MODE

MOSI First Byte [15-8] [b_15 b_14] 01_110 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 01_ 110 P	mode[4]	mode[3]	mode[2]	mode[1]	mode[0]	Rnd_b[2]	Rnd_b[1]	Rnd_b[0]
Default state	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 26. Low Power V_{DD} OFF Selection and FWU / Cyclic Sense Selection

b7, b6, b5, b4, b3	**FWU**	**Cyclic Sense**
0 1100	OFF	OFF
0 1101	OFF	ON
0 1110	ON	OFF
0 1111	ON	ON

Table 27. Low Power V_{DD} ON selection and operation mode

b7, b6, b5, b4, b3	**FWU**	**Cyclic Sense**	**Cyclic INT**	**Watchdog**
1 0000	OFF	OFF	OFF	OFF
1 0001	OFF	OFF	OFF	ON
1 0010	OFF	OFF	ON	OFF
1 0011	OFF	OFF	ON	ON
1 0100	OFF	ON	OFF	OFF
1 0101	OFF	ON	OFF	ON
1 0110	OFF	ON	ON	OFF
1 0111	OFF	ON	ON	ON
1 1000	ON	OFF	OFF	OFF
1 1001	ON	OFF	OFF	ON
1 1010	ON	OFF	ON	OFF
1 1011	ON	OFF	ON	ON
1 1100	ON	ON	OFF	OFF
1 1101	ON	ON	OFF	ON
1 1110	ON	ON	ON	OFF
1 1111	ON	ON	ON	ON
b2, b1, b0	Random Code inverted, these 3bits are the inverted bits obtained from the previous SPI command. The usage of these bits are optional and must be previously selected in the INIT MISC register [See bit 7 (LPM w RNDM) in Table 18]			

Prior to enter in LP V_{DD} ON or LP V_{DD} OFF, the wake-up flags must be cleared or read.

This is done by the following SPI commands (See Table 37, Device Flag, I/O Real Time and Device Identification):

0xE100 for CAN wake up clear

0xE380 for I/O wake up clear

0xE700 for LIN1 wake up clear

0xE900 for LIN2 wake up clear

If wake-up flags are not cleared, the device will enter into the selected low power mode and immediately wake up. In addition, the CAN failure flags (i.e CAN_F and CAN_UF) must be cleared in order to meet the low power current consumption specification. This is done by the following SPI command:

0xE180 (read CAN failure flags)

When the device is in LP V_{DD} ON mode, the wake-up by a SPI command uses a write to “Normal Request mode”, 0x5C10.

Mode Register Features

The mode register include specific function and “global SPI command” that allow the following:

- read device current mode
- read device Debug status
- read state of SAFE pin
- leave Debug state
- release or turn off SAFE pin
- read a 3 bit Random Code to enter in LP mode

These global commands are built using the MODE register adress bit [13-9], along with several combinations of bit [15-14] and bit [7]. Note, bit [8] is always set to 1.

Entering into LP Mode using Random Code

- LP Mode using Random Code must be selected in INIT mode via bit 7 of the INIT MISC register.

- In Normal Mode, read the Random Code using 0x1D00 or 0x1D80 command. The 3 Random Code bits are available on MISO bits 2,1 and 0.

- Write LP Mode by inverting the 3 random bits.

Example - Select LP VDD OFF without cyclic sense and FWU:

1. in hex: 0x5C60 to enter in LP VDD OFF mode without using the 3 random code bits.
2. if Random Code is selected, the commands are:

- Read Random Code: 0x1D00 or 0x1D80,

MISO report in binary: bits 15-8, bits 7-3, Rnd_[2], Rnd_[1], Rnd_[0].

- Write LP VDD OFF Mode, using Random Code inverted:

in binary: 0101 1100 0110 0 Rnd_b[2], Rnd_b[1], Rnd_b[0].

Table 28 summarizes these commands

Table 28. Device Modes

Global commands and effects								
Read device current mode, Leave debug mode. Keep SAFE pin as is. MOSI in hexadecimal: 1D 00	MOSI	**bits 15-14**	**bits 13-9**	**bit 8**	**bit 7**	**bits 6-0**		
		00	01 110	1	0	000 0000		
	MISO	**bit 15-8**		**bit 7-3**		**bit 2-0**		
		Fix Status		device current mode		Random code		
Read device current mode Release SAFE pin (turn OFF). MOSI in hexadecimal: 1D 80	MOSI	**bits 15-14**	**bits 13-9**	**bit 8**	**bit 7**	**bits 6-0**		
		00	01 110	1	1	000 0000		
	MISO	**bit 15-8**		**bit 7-3**		**bit 2-0**		
		Fix Status		device current mode		Random code		
Read device current mode, Leave debug mode. Keep SAFE pin as is. MOSI in hexadecimal: DD 00 MISO reports Debug and SAFE state (bits 1,0)	MOSI	**bits 15-14**	**bits 13-9**	**bit 8**	**bit 7**	**bits 6-0**		
		11	01 110	1	0	000 0000		
	MISO	**bit 15-8**		**bit 7-3**		**bit 2**	**bit 1**	**bit 0**
		Fix Status		device current mode		X	SAFE	DEBUG
Read device current mode, Keep DEBUG mode Release SAFE pin (turn OFF). MOSI in hexadecimal: DD 80 MISO reports Debug and SAFE state (bits 1,0)	MOSI	**bits 15-14**	**bits 13-9**	**bit 8**	**bit 7**	**bits 6-0**		
		11	01 110	1	1	000 0000		
	MISO	**bit 15-8**		**bit 7-3**		**bit 2**	**bit 1**	**bit 0**
		Fix Status		device current mode		X	SAFE	DEBUG

Tables below describe the meaning of MISO bits 7-0, that allow to decode the device current mode.

Table 29. MISO bits 7-3

Device current mode, any of the above command	
b7, b6, b5, b4, b3	**MODE**
0 0000	INIT
0 0001	FLASH
0 0010	Normal Request
0 0011	Normal mode

Table below describes the SAFE and DEBUG bit decoding.

Table 30. SAFE and DEBUG status

SAFE and DEBUG bits	
b1	**description**
0	SAFE pin OFF, not activated
1	SAFE pin ON, driver activated.
b0	**description**
0	Debug mode OFF
1	Debug mode Active

REGULATOR, CAN, I/O, INT AND LIN REGISTERS

Table 31. REGULATOR Register, REG

MOSI First Byte [15-8] [b_15 b_14] 01_111 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 01_ 111 P	$V_{AUX}[1]$	$V_{AUX}[0]$	-	5V-can[1]	5V-can[0]	V_{DD} bal en	V_{DD} bal auto	V_{DD} OFF en
Default state	0	0	N/A	0	0	N/A	N/A	N/A
Condition for default	POR			POR				

Bits	Description
b7 b6	**V_{AUX}[1], V_{AUX}[0]** - Vauxilary regulator control
00	Regulator OFF
01	Regulator ON. Under-voltage (UV) and Over-current (OC) monitoring flags not reported. V_{AUX} is disabled in case UV or OC detected after 1.0 ms blanking time.
10	Regulator ON. Under-voltage (UV) and over-current (OC) monitoring flags active. V_{AUX} is disabled in case UV or OC detected after 1.0 ms blanking time.
11	Regulator ON. Under-voltage (UV) and over-current (OC) monitoring flags active. V_{AUX} is disabled in case UV or OC detected after 25 µs blanking time.
b4 b3	**5 V-can[1], 5 V-can[0]** - 5V-CAN regulator control
00	Regulator OFF
01	Regulator ON. Thermal protection active. Under-voltage (UV) and over-current (OC) monitoring flags not reported. 1.0 ms blanking time for UV and OC detection.
10	Regulator ON. Thermal protection active. Under-voltage (UV) and over-current (OC) monitoring flags active. 1.0 ms blanking time for UV and OC detection.
11	Regulator ON. Thermal protection active. Under-voltage (UV) and over-current (OC) monitoring flags active. 5 V-CAN disable in case UV or OC detected after 25 µs blanking time.
b2	**V_{DD} bal en** - Control bit to Enable the V_{DD} external ballast transistor
0	External V_{DD} ballast disable
1	External V_{DD} ballast Enable
b1	**V_{DD} bal auto -** Control bit to automatically Enable the V_{DD} external ballast transistor, if V_{DD} is > typ 60 mA
0	Disable the automatic activation of the external ballast
1	Enable the automatic activation of the external ballast, if V_{DD} > typ 60 mA
b0	**V_{DD} OFF en -** Control bit to allow transition into Low Power V_{DD} OFF mode (to prevent V_{DD} turn OFF)

Bits	Description
0	Disable Usage of Low Power V_{DD} OFF mode
1	Enable Usage of Low Power V_{DD} OFF mode

Table 32. CAN Register, CAN[28]

MOSI First byte [15-8] [b_15 b_14] 10_000 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 10_ 000P	CAN mod[1]	CAN mod[0]	Slew[1]	Slew[0]	Wake up 1/3	-	-	CAN int
Default state	1	0	0	0	0	-	-	0
Condition for default	note		POR		POR			POR

Bits	Description
b7 b6	**CAN mod[1], CAN mod[0]** - CAN interface mode control, wake-up enable / disable
00	CAN interface in Sleep mode, CAN wake-up disable.
01	CAN interface in receive only mode, CAN driver disable.
10	CAN interface is in Sleep mode, CAN wake-up enable. In device low power mode, CAN wake-up is reported by device wake-up. In device normal mode, CAN wake-up reported by INT.
11	CAN interface in transmit and receive mode.
b5 b4	**Slew[1] Slew[0]** - CAN driver slew rate selection
00	FAST
01	MEDIUM
10	SLOW
11	SLOW
b3	**Wake-up 1/3** - Selection of CAN wake-up mechanism
0	3 dominant pulses wake-up mechanism
1	Single dominant pulse wake-up mechanism
b0	**CAN INT -** Select the CAN failure detection reporting
0	Select INT generation when a bus failure is fully identified and decoded (i.e after 5 dominant pulses on TxCAN)
1	Select INT generation as soon as a bus failure is detected, event if not fully identified

Notes

28. The first time the device is set in Normal mode, the CAN is in Sleep wake-up enable (bit7 = 1, bit 6 =0). The next time the device is set in Normal mode, the CAN state is controlled by bits 7 and 6.

Table 33. I/O Register, I/O

MOSI First byte [15-8] [b_15 b_14] 10_001 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 10_ 001P	I/O-3 [1]	I/O-3 [0]	I/O-2 [1]	I/O-2 [0]	I/O-1 [1]	I/O-1 [0]	I/O-0 [1]	I/O-0 [0]
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Bits	**Description**
b7 b6	I/O-3 [1], I/O-3 [0] - I/O-3 pin operation
00	I/O-3 driver disable, Wake-up capability disable
01	I/O-3 driver disable, Wake-up capability enable.
10	I/O-3 High Side driver enable.
11	I/O-3 High Side driver enable.
b5 b4	I/O-2 [1], I/O-2 [0] - I/O-2 pin operation
00	I/O-2 driver disable, Wake-up capability disable
01	I/O-2 driver disable, Wake-up capability enable.
10	I/O-2 High Side driver enable.
11	I/O-2 High Side driver enable.
b3 b2	I/O-1 [1], I/O-1 [0] - I/O-1 pin operation
00	I/O-1 driver disable, Wake-up capability disable
01	I/O-1 driver disable, Wake-up capability enable.
10	I/O-1 Low Side driver enable.
11	I/O-1 High Side driver enable.
b1 b0	I/O-0 [1], I/O-0 [0] - I/O-0 pin operation
00	I/O-0 driver disable, Wake-up capability disable
01	I/O-0 driver disable, Wake-up capability enable.
10	I/O-0 Low Side driver enable.
11	I/O-0 High Side driver enable.

Table 34. INT Register, INT

MOSI First byte [15-8] [b_15 b_14] 10_010 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 10_ 010P	CAN failure	MCU req	LIN2 fail	LIN1fail	I/O	SAFE	-	Vmon
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Bits	Description
b7	**CAN failure** - control bit for CAN failure INT (CANH/L to GND, VDD or VSUP, CAN over-current, Driver Over Temp, TxD-PD, RxD-PR, RX2HIGH, and CANBUS Dominate clamp)
0	INT disable
1	INT enable.
b6	**MCU req -** Control bit to request an INT. INT will occur once when the bit is enable
0	INT disable
1	INT enable.
b5	**LIN2 fail** - Control bit to enable INT in case of failure on LIN2 interface
0	INT disable
1	INT enable.
b4	**LIN1 fail** - Control bit to enable INT in case of failure on LIN1 interface
0	INT disable
1	INT enable.
b3	**I/O** - Bit to control I/O interruption: I/O failure
0	INT disable
1	INT enable.
b2	**SAFE** - Bit to enable INT in case of: Vaux over-voltage, VDD over-voltage, VDD Temp pre warning, VDD under-voltage(29), SAFE resistor mismatch, RST terminal short to VDD, MCU request INT.(30)
0	INT disable
1	INT enable.
b0	**V_{MON}** - enable interruption by voltage monitoring of one of the voltage regulator: V_{AUX}, 5 V-CAN, V_{DD} (I_{DD} Over-current, V_{SUV}, V_{SOV}, $V_{SENSELOW}$, 5V-CAN low or thermal shutdown, V_{AUX} low or V_{AUX} over-current
0	INT disable
1	INT enable.

Notes
29. If VDD under-voltage is set to 70% of VDD, see bits b6 and b5 in Table 15 on page 63.
30. Bit 2 is used in conjunction with bit 6. Both bit 6 and bit 2 must be set to 1 to activate the MCU INT request.

Table 35. LIN 1 Register, LIN1[32]

MOSI First byte [15-8] [b_15 b_14] 10_010 [P/N]	MOSI Second Byte, bits 7-0							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01 10_ 011P	LIN mode[1]	LIN mode[0]	Slew rate[1]	Slew rate[0]	-	LIN T1 on	-	Vsup ext
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Bits	Description
b7 b6	LIN mode [1], LIN mode [0] - LIN 1 interface mode control, wake-up enable / disable
00	LIN1 disable, wake-up capability disable
01	not used
10	LIN1 disable, wake-up capability enable
11	LIN1 Transmit Receive mode[31]

b5 b4	Slew rate[1], Slew rate[0] LIN 1 slew rate selection
00	Slew rate for 20 kbit/s baud rate
01	Slew rate for 10 kbit/s baud rate
10	Slew rate for fast baud rate
11	Slew rate for fast baud rate

b2	LIN T1 on
0	LIN 1 termination OFF
1	LIN 1 termination ON

b0	V_{SUP} ext
0	LIN goes recessive when device V_{SUP2} is below typ 6.0 V. This is to meet J2602 specification
1	LIN continues operation below V_{SUP2} 6.0 V, until 5 V-CAN is disabled.

Notes

31. The LIN interface can be set in TxD/RxD mode only when the TXDL input signal is in recessive state. An attempt to set TxD/RxD mode, while TXDL is low, will be ignored and the LIN interface remains disabled.
32. In order to use LIN interface, the 5V-CAN regulator must be ON.

Table 36. LIN 2 Register, LIN2(34)

MOSI First byte [15-8] [b_15 b_14] 10_010 [P/N]	**MOSI Second Byte, bits 7-0**							
	bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
01 10_ 100P	LIN mode[1]	LIN mode[0]	Slew rate[1]	Slew rate[0]	-	LIN T2 on	-	Vsup ext
Default state	0	0	0	0	0	0	0	0
Condition for default	POR							

Bits	**Description**
b7 b6	LIN mode [1], LIN mode [0] - LIN 2 interface mode control, wake-up enable / disable
00	LIN2 disable, wake-up capability disable
01	not used
10	LIN2 disable, wake-up capability enable
11	LIN2 Transmit Receive mode(33)

b5 b4	Slew rate[1], Slew rate[0] LIN 2slew rate selection
00	Slew rate for 20 kbit/s baud rate
01	Slew rate for 10 kbit/s baud rate
10	Slew rate for fast baud rate
11	Slew rate for fast baud rate
b2	LIN T2 on
0	LIN 2 temination OFF
1	LIN 2 temination ON
b0	V_{SUP} ext
0	LIN goes recessive when device V_{SUP2} is below typ 6.0 V. This is to meet J2602 specification
1	LIN continues operation below V_{SUP2} 6.0 V, until 5 V-CAN is disabled.

Notes

33. The LIN interface can be set in TxD/RxD mode only when the TXDL input signal is in recessive state. An attempt to set TxD/RxD mode, while TXDL is low, will be ignored and the LIN interface remains disabled.
34. In order to use LIN interface, the 5V-CAN regulator must be ON.

FLAGS AND DEVICE STATUS

DESCRIPTION

The table below is a summary of the device flags, I/O real time level, device Identification and includes examples of SPI commands (SPI command do not use parity functions). They are obtained using the following commands.

This command is composed of the following:

bits 15 and 14:

- [1 1] for failure flags
  - - [0 0] for I/O real time status, device identification and CAN LIN driver receiver real time state.
- bit 13 to 9 are the register address from which the flags is to be read.
- bit 8 = 1 (this is not parity bit function, as this is a read command).

When a failure event occurs, the respective flag is set and remains latched until it is cleared by a read command (provided the failure event has recovered).

Table 37. Device Flag, I/O Real Time and Device Identification

Bits	15-14	13-9	8	7		6	5	4	3	2	1	0
MOSI	MOSI bits 15-7				Next 7 MOSI bits (bits 6.0) should be “000_0000”							
	bits [15, 14]	Address [13-9]	bit 8	bit 7								
MISO	8 Bits Device Fixed Status (bits 15...8)				MISO bits [7-0], device response on MISO pin							
					bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REG	11	0_1111 REG	1	0	V_{AUX_LOW}	$V_{AUX\_OVER-CURRENT}$	5V-CAN_ THERMAL SHUTDOWN	5V-CAN_ UV	5V-CAN_ OVER-CURRENT	V_{SENSE_LOW}	$V_{SUP\_}$ UNDER-VOLTAGE	$I_{DD-OC-NORMAL\ MODE}$
	11			1	-	-	-	$V_{DD\_}$ THERMAL SHUTDOWN		R_{ST_LOW} (<100 ms)	$V_{SUP\_}$ BATFAIL	$I_{DD-OC-LP}$ V_{DD}ON MODE
	Hexa SPI commands to get Vreg Flags: MOSI 0x DF 00, and MOSI Ox DF 80											
CAN	11	1_0000 CAN	1	0	CAN wake-up	-	CAN Over-temp	RxD low	Rxd high	TxD dom	Bus Dom clamp	CAN Over-current
				1	CAN_UF	CAN_F	CANL to V_{BAT}	CANL to V_{DD}	CANL to GND	CANH to V_{BAT}	CANH to V_{DD}	CANH to GND
	Hexa SPI commands to get CAN Flags: MOSI 0x E1 00, and MOSI 0x E1 80											
	00	1_0000 CAN	1	1	CAN Driver State	CAN Receiver State	CAN WU en/dis	-	-	-	-	-
	Hexa SPI commands to get CAN real time status: MOSI 0x 21 80											
I/O	11	1_0001 I/O	1	0	HS3 short to GND	HS2 short to GND	SPI parity error	CSB low >2ms	$V_{SUP2-UV}$	$V_{SUP1-OV}$	I/O_O thermal	W/D flash mode 50%
				1	I/O_1-3 wake-up	I/O_0-2 wake-up	SPI wake-up	FWU	INT service Timeout	Low Power V_{DD} OFF	Reset request	Hardware Leave Debug
	Hexa SPI commands to get I/O Flags and I/O wake-up: MOSI 0x E3 00, and MOSI 0x E3 80											
	00	1_0001 I/O	1	1		I/O_3 state		I/O_2 state		I/O_1 state		I/O_0 state
	Hexa SPI commands to get I/O real time level: MOSI 0x 23 80											
INT	11	1_0010 Interrupt	1	0	INT request	RST high	DBG resistor	V_{DD} temp Prewarning	V_{DD} UV	V_{DD} Over-voltage	$V_{AUX\_OVER-VOLTAGE}$	-
				1	-	-	-	V_{DD} low >100 ms	V_{DD} low RST	RST low >100 ms	multiple Resets	W/D refresh failure
	Hexa SPI commands to get INT Flags: MOSI 0x E5 00, and MOSI 0x E5 80											
	00	1_0010 Interrupt	1	1	V_{DD} (5.0 V or 3.3 V)	device p/n 1	device p/n 0	id4	id3	id2	id1	id0
	Hexa SPI commands to get device Identification: MOSI 0x 25 10 example: MISO bit [7-0] = 1011 0010: MC33904, 5.0 V version, silicon pass 3.1											

Table 37. Device Flag, I/O Real Time and Device Identification

LIN1	11	1_0011 LIN 1	1	0	-	LIN1 wake-up	LIN1 Term short to gnd	LIN 1 Over-temp	RxD1 low	RxD1 high	TxD1 dom	LIN1 bus dom clamp
	Hexa SPI commands to get LIN 2 Flags: MOSI 0x E7 00											
	00	1_0011 LIN 1	1	1	LIN1 State	LIN1 WU en/dis	-	-	-	-	-	-
	Hexa SPI commands to get LIN1 real time status: MOSI 0x 27 80											
LIN2	11	1_0100 LIN 2	1	0	-	LIN2 wake-up	LIN2 Term short to gnd	LIN 2 Over-temp	RxD2 low	RxD2 high	TxD2 dom	LIN2 bus dom clamp
	Hexa SPI commands to get LIN 2 Flags: MOSI 0x E9 00											
	00	1_0100 LIN 2	1	1	LIN2 State	LIN2 WU en/dis	-	-	-	-	-	-
	Hexa SPI commands to get LIN2 real time status: MOSI 0x 29 80											

Table 38. Flag Descriptions

Flag		Description
REG		
V_{AUX_LOW}	Description	Reports that V_{AUX} regulator output voltage is lower than the V_{AUX_UV} threshold.
	Set / Reset condition	Set: V_{AUX} below threshold for t >100 µs typ. Reset: V_{AUX} above threshold and flag read (SPI)
$V_{AUX\_OVER-CURRENT}$	Description	Report that current out of V_{AUX} regulator is above V_{AUX_OC} threshold.
	Set / Reset condition	Set: Current above threshold for t >100 µs. Reset: Current below threshold and flag read by SPI.
5 $V_{-CAN\_}$ THERMAL SHUTDOWN	Description	Report that the 5 V-CAN regulator has reached over-temperature threshold.
	Set / Reset condition	Set: 5 V-CAN thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI)
$5V_{-CAN\_UV}$	Description	Reports that 5 V_CAN regulator output voltage is lower than the 5 $V_{-CAN\ UV}$ threshold.
	Set / Reset condition	Set: 5V-CAN below $5V_{-CAN\ UV}$ for t >100 µs typ. Reset: 5V-CAN > threshold and flag read (SPI)
5V-can_ over-current	Description	Report that the CAN driver output current is above threshold.
	Set / Reset condition	Set: 5V-CAN current above threshold for t>100 µs. Reset: 5V-CAN current below threshold and flag read (SPI)
$V_{SENSE\_}$ LOW	Description	Reports that VSENSE pin is lower than the $V_{SENSE\ LOW}$ threshold.
	Set / Reset condition	Set: VSENSE below threshold for t >100 µs typ. Reset: V_{SENSE} above threshold and flag read (SPI)
$V_{SUP\_}$ UNDER-VOLTAGE	Description	Reports that VSUP1 pin is lower than the $V_{SUP1\ LOW}$ threshold.
	Set / Reset condition	Set: V_{SUP1} below threshold for t >100 µs typ. Reset: V_{SUP1} above threshold and flag read (SPI)
I_{DD-OC-} NORMAL MODE	Description	Report that current out of VDD pin is higher that I_{DD-OC} threshold, while device is in Normal mode.
	Set / Reset condition	Set: current above threshold for t>100 µs typ. Reset; current below threshold and flag read (SPI)
$V_{DD\_}$ THERMAL SHUTDOWN	Description	Report that the V_{DD} has reached over-temperature threshold, and was turned off.
	Set / Reset condition	Set: V_{DD} OFF due to thermal condition. Reset: V_{DD} recover and flag read (SPI)
R_{ST_LOW} (<100 ms)	Description	Report that the RESET pin has detected a low level, shorter than 100 ms
	Set / Reset condition	Set: after detection of reset low pulse. Reset: Reset pulse terminated and flag read (SPI)
$V_{SUP\_}$ BATFAIL	Description	Report that the device voltage at VSUP1 pin was below BATFAIL threshold.
	Set / Reset condition	Set: V_{SUP1} below BATFAIL. Reset: V_{SUP1} above threshold, and flag read (SPI)
$I_{DD-OC-LP}$ V_{DD}ON mode	Description	Report that current out of VDD pin is higher that I_{DD-OC} threshold LP, while device is in Low Power V_{DD} ON mode.
	Set / Reset condition	Set: current above threshold for t>100 µs typ. Reset; current below threshold and flag read (SPI)

Table 38. Flag Descriptions

Flag		Description
CAN		
CAN driver state	Description	Report real time CAN bus driver state: 1 if Driver is enable, 0 if driver disable
	Set / Reset condition	Set: CAN driver is enable. Reset: CAN driver is disable. Driver can be disable by SPI command (ex CAN set in RxD only mode) or following a failure event (ex: TxD Dominant). Flag read SPI command (0x2180) do not clear the flag, as it is “real time” information.
CAN receiver state	Description	Report real time CAN bus receiver state: 1 if Enable, 0 if disable
	Set / Reset condition	Set: CAN bus receiver is enable. Reset: CAN bus receiver is disable. Receiver disable by SPI command (ex: CAN set in sleep mode). Flag read SPI command (0x2180) do not clear the flag, as it is “real time” information.
CAN WU enable	Description	Report real time CAN bus wake up receiver state: 1 if WU receiver is enable, 0 if disable
	Set / Reset condition	Set: CAN wake up receiver is enable. Reset: CAN wake up receiver is disable. Wake up receiver is controlled by SPI, and is active by default after device Power ON. SPI command (0x2180) do not change flag state.
CAN wake-up	Description	Report that wake-up source is CAN
	Set / Reset condition	Set: after CAN wake detected. Reset: Flag read (SPI)
CAN Over-temp	Description	Report that the CAN interface has reach over-temperature threshold.
	Set / Reset condition	Set: CAN thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI)
RxD low	Description	Report that RxD pin is shorted to GND.
	Set / Reset condition	Set: RxD low failure detected. Reset: failure recovered and flag read (SPI)
Rxd high	Description	Report that RxD pin is shorted to recessive voltage.
	Set / Reset condition	Set: RxD high failure detected. Reset: failure recovered and flag read (SPI)
TxD dom	Description	Report that TxD pin is shorted to GND.
	Set / Reset condition	Set: TxD low failure detected. Reset: failure recovered and flag read (SPI)
Bus Dom clamp	Description	Report that the CAN bus is dominant for a time longer than t_{DOM}
	Set / Reset condition	Set: Bus dominant clamp failure detected. Reset: failure recovered and flag read (SPI)
CAN Over-current	Description	Report that the CAN current is above CAN over-current threshold.
	Set / Reset condition	Set: CAN current above threshold. Reset: current below threshold and flag read (SPI)
CAN_UF	Description	Report that the CAN failure detection has not yet identified the bus failure
	Set / Reset condition	Set: bus failure pre detection. Reset: CAN bus failure recovered and flag read
CAN_F	Description	Report that the CAN failure detection has identified the bus failure
	Set / Reset condition	Set: bus failure complete detetction.Reset: CAN bus failure recovered and flag read
CANL to V_{BAT}	Description	Report CAN L short to V_{BAT} failure
	Set / Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
CANL to VDD	Description	Report CANL short to VDD
	Set / Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
CANL to GND	Description	Report CAN L short to GND failure
	Set / Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
CANH to V_{BAT}	Description	Report CAN H short to V_{BAT} failure
	Set / Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
CANH to VDD	Description	Report CANH short to VDD
	Set / Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
CANH to GND	Description	Report CAN H short to GND failure
	Set / Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)

Table 38. Flag Descriptions

Flag		Description
I/O		
HS3 short to GND	Description	Report I/O-3 high side switch short to GND failure
	Set / Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
HS2 short to GND	Description	Report I/O-2 high side switch short to GND failure
	Set / Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
SPI parity error	Description	Report SPI parity error was detected.
	Set / Reset condition	Set: failure detected. Reset: flag read (SPI)
CSB low >2.0 ms	Description	Report SPI CSB was low for a time longer than typ 2.0 ms
	Set / Reset condition	Set: failure detected. Reset: flag read (SPI)
$V_{SUP2-UV}$	Description	Report that V_{SUP2} is below $V_{SUP2-UV}$ threshold.
	Set / Reset condition	Set V_{SUP2} below $V_{SUP2-UV}$ thresh. Reset V_{SUP2} > V_{SUPUV} thresh and flag read (SPI)
$V_{SUP1-OV}$	Description	Report that V_{SUP1} is above $V_{SUP1-OV}$ threshold.
	Set / Reset condition	Set V_{SUP1} above $V_{SUP1-OV}$ threshold. Reset V_{SUP1} < V_{SUPOV} thresh and flag read (SPI)
I/O-0 thermal	Description	Report that the I/O-0 high side switch has reach over-temperature threshold.
	Set / Reset condition	Set: I/O-0 high side switch thermal sensor above threshold. Reset: thermal sensor below threshold and flag read (SPI)
W/D flash mode 50%	Description	Report that the W/D period has reach 50% of its value, while device is in Flash mode.
	Set / Reset condition	Set: W/D period > 50%. Reset: flag read
I/O-1-3 wake-up	Description	Report that wake-up source is I/O-1 or I/O-3
	Set / Reset condition	Set: after I/O-1 or I/O-3 wake detected. Reset: Flag read (SPI)
I/O-0-2 wake-up	Description	Report that wake-up source is I/O-0 or I/O-2
	Set / Reset condition	Set: after I/O-0 or I/O-2 wake detected. Reset: Flag read (SPI)
SPI wake-up	Description	Report that wake-up source is SPI command, in Low Power V_{DD} ON mode.
	Set / Reset condition	Set: after SPI wake-up detected. Reset: Flag read (SPI)
FWU	Description	Report that wake-up source is forced wake-up
	Set / Reset condition	Set: after Forced wake-up detected. Reset: Flag read (SPI)
INT service Timeout	Description	Report that INT timeout error detected.
	Set / Reset condition	Set: INT service timeout expired. Reset: flag read.
Low Power V_{DD} OFF	Description	Report that Low Power V_{DD} OFF mode was selected, prior wake-up occurred.
	Set / Reset condition	Set: Low Power V_{DD} OFF selected. Reset: Flag read (SPI)
Reset request	Description	Report that RST source is an request from a SPI command (go to RST mode).
	Set / Reset condition	Set: After reset occurred due to SPI request. Reset: flag read (SPI)
Hardware Leave Debug	Description	Report that the device left the Debug mode due to hardware cause (voltage at DBG pin lower than typ 8.0 V).
	Set / Reset condition	Set: device leave debug mode due to hardware cause. Reset: flag read.

Table 38. Flag Descriptions

Flag		Description
INT		
INT request	Description	Report that INT source is an INT request from a SPI command.
	Set / Reset condition	Set: INT occurred. Reset: flag read (SPI)
RST high	Description	Report that $\overline{RST}$ pin is shorted to high voltage.
	Set / Reset condition	Set: RST failure detection. Reset: flag read.
DBG resistor	Description	Report that the resistor at DBG pin is different from expected (different from SPI register content).
	Set / Reset condition	Set: failure detected. Reset: correct resistor and flag read (SPI).
$V_{DD\ TEMP\ PREWARNING}$	Description	Report that the V_{DD} has reached over-temperature prewarning threshold.
	Set / Reset condition	Set: V_{DD} thermal sensor above threshold. Reset: V_{DD} thermal sensor below threshold and flag read (SPI)
$V_{DD\ UV}$	Description	Reports that VDD pin is lower than the V_{DDUV} threshold.
	Set / Reset condition	Set: VDD below threshold for t >100 µs typ. Reset: V_{DD} above threshold and flag read (SPI)
$V_{DD\ OVER\text{-}VOLTAGE}$	Description	Reports that VDD pin is higher than the typ V_{DD} + 0.6 V threshold. I/O-1 can be turned OFF if this function is selected in INIT register.
	Set / Reset condition	Set: VDD above threshold for t >100 µs typ. Reset: V_{DD} below threshold and flag read (SPI)
$V_{AUX\_OVER\text{-}VOLTAGE}$	Description	Reports that VAUX pin is higher than the typ V_{AUX} + 0.6 V threshold. I/O-1 can be turned OFF if this function is selected in INIT register.
	Set / Reset condition	Set: V_{AUX} above threshold for t >100 µs typ. Reset: V_{AUX} below threshold and flag read (SPI)
$V_{DD\ LOW}$ >100 ms	Description	Reports that VDD pin is lower than the VDD_{UV} threshold for a time longer than 100 ms
	Set / Reset condition	Set: VDD below threshold for t >100 ms typ. Reset: V_{DD} above threshold and flag read (SPI)
$V_{DD\ LOW}$	Description	Report that V_{DD} is below V_{DD} under-voltage threshold.
	Set / Reset condition	Set: V_{DD} below threshold. Reset: fag read (SPI)
V_{DD} (5.0 V or 3.3 V)	Description	0: mean 3.3V V_{DD} version 1: mean 5V V_DD version
	Set / Reset condition	N/A
Device P/N1 and 0	Description	Describe the device part number: 00: MC33903 01: MC33904 10: MC33905S 11: MC333905D
	Set / Reset condition	N/A
Device id 4 to 0	Description	Describe the silicon revision number 10001: silicon revision 3.0 10010: silicon revision 3.1 10011: silicon revision 3.2
	Set / Reset condition	N/A
RST low >100 ms	Description	Report that the RESET pin has detected a low level, longer than 100 ms (Reset permanent low)
	Set / Reset condition	Set: after detection of reset low pulse. Reset: Reset pulse terminated and flag read (SPI)
Multiple Resets	Description	Report that the more than 8 consecutive reset pulses occurred, due to missing or wrong W/D refresh.
	Set / Reset condition	Set: after detection of multiple reset pulses. Reset: flag read (SPI)
W/D refresh failure	Description	Report that a wrong or missing W/D failure occurred.
	Set / Reset condition	Set: failure detected. reset: flag read (SPI)

Table 38. Flag Descriptions

Flag		Description
LIN1/2		
LIN1/2 bus dom clamp	Description	Report that the LIN1/2 bus is dominant for a time longer than t_{DOM}
	Set / Reset condition	Set: Bus dominant clamp failure detected. Reset: failure recovered and flag read (SPI)
LIN 1/2 State	Description	Report real time LIN interface TxD/RxD mode. 1 if LIN is in TxD/RxD mode. 0 is LIN is not in TxD/RxD mode.
	Set / Reset condition	Set: LIN in TxD RxD mode. Reset: LIN not in TxD/RxD mode. LIN not in TxD/RxD mode by SPI command (ex LIN set in Sleep mode) or following a failure event (ex: TxL Dominant). Flag read SPI command (0x2780 or 0x2980) do not clear it, as it is “real time” flag.
LIN 1/2 WU	Description	Report real time LIN wake up receiver state. 1 if LIN wake up is enable, 0 if LIN wake up is disable (means LIN signal will not be detected and will not wake up the device).
	Set / Reset condition	Set: LIN WU enable (LIN interface set in Sleep mode wake up enable). Reset: LIN wake up disable (LIN interface set in Sleep mode wake up disable). Flag read SPI command (0x2780 or 0x2980) do not clear the flag, as it is “real time” information.
LIN1/2 wake-up	Description	Report that wake-up source is LIN1 or LIN2
	Set / Reset condition	Set: after LIN1 or LIN 2 wake detected. Reset: Flag read (SPI)
LIN1/2 Term short to GND	Description	Report LIN term 1 or LIN term 2 short to GND failure
	Set / Reset condition	Set: failure detected. Reset failure recovered and flag read (SPI)
LIN 1/2 Over-temp	Description	Report that the LIN1 or LIN 2 interface has reach over-temperature threshold.
	Set / Reset condition	Set: LIN1/2 thermal sensor above threshold. Reset: sensor below threshold and flag read (SPI)
RxD1/2 low	Description	Report that RxD1/2 pin is shorted to GND.
	Set / Reset condition	Set: RxD low failure detected. Reset: failure recovered and flag read (SPI)
RxD1/2 high	Description	Report that RxD1/2pin is shorted to recessive voltage.
	Set / Reset condition	Set: RxD high failure detected. Reset: failure recovered and flag read (SPI)
TxD1/2 dom	Description	Report that TxD1/2 pin is shorted to GND.
	Set / Reset condition	Set: TxD low failure detected. Reset: failure recovered and flag read (SPI)

FIX AND EXTENDED DEVICE STATUS

For every SPi command the device response on MISO is a fix status information. This information is either:

Two Bytes

Fix Status + Extended Status: when a device write command is used (MOSI bits 15-14, bits C1 C0 = 01)

One Byte

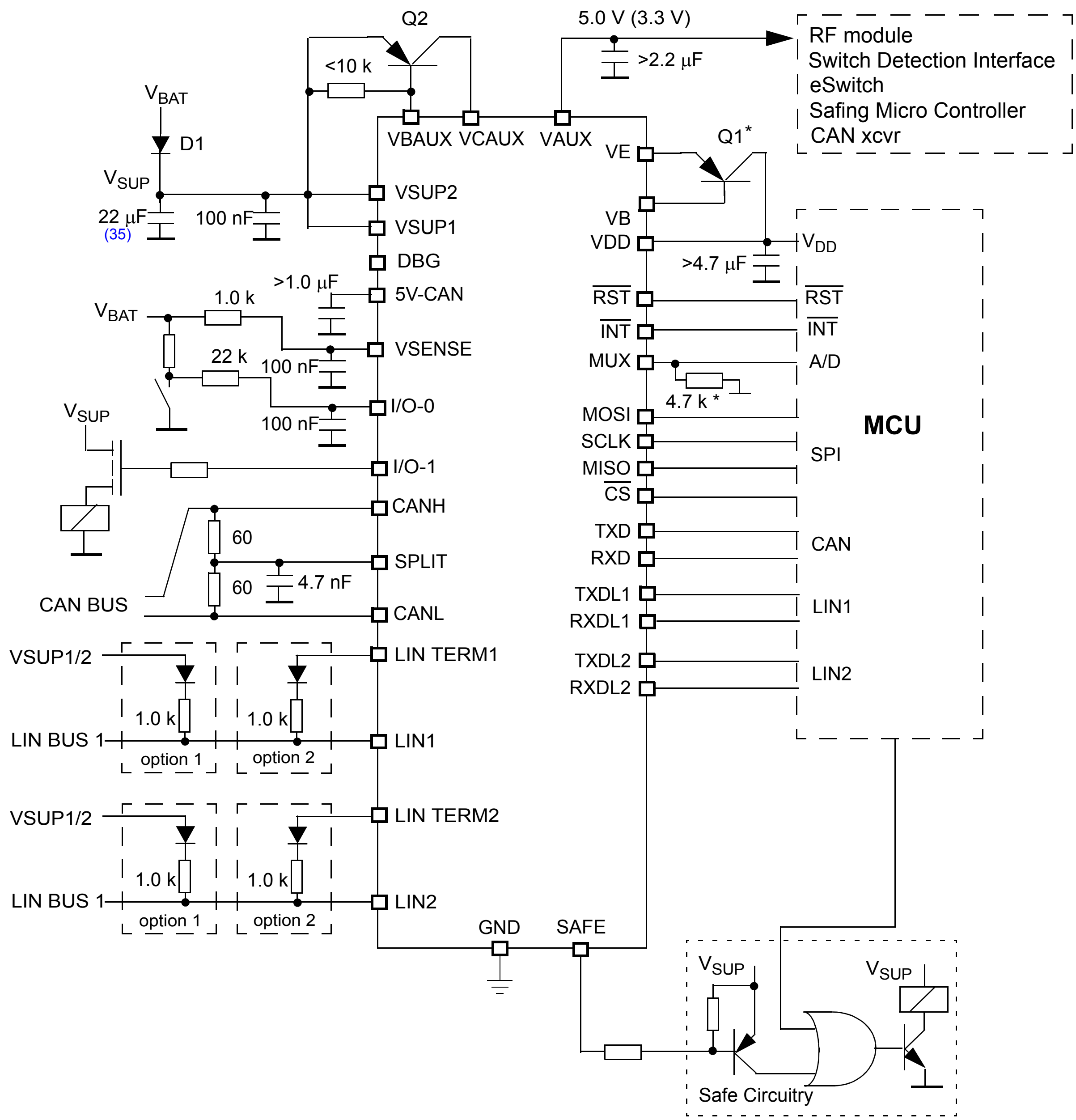
Fix Status: when a device read operation is performed (MOSI bits 15-14, bits C1 C0 = 00 or 11).

Table 39. Status Bits Description

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	INT	WU	RST	CAN-G	LIN-G	I/O-G	SAFE-G	VREG-G	CAN-BUS	CAN-LOC	LIN2	LIN1	I/O-1	I/O-0	VREG-1	VREG-0

Bits	Description
INT	Indicate that an INT has occurred and that INT flags are pending to be read.
WU	Indicate that a wake-up has occurred and that wake-up flags are pending to be read.
RST	Indicate that a reset has occurred and that the flags that report the reset source are pending to be read.
CAN-G	The INT, WU or RST source is CAN interface. CAN local or CAN bus source.
LIN-G	The INT, WU or RST source is LIN2 or LIN1 interface
I/O-G	The INT, WU or RST source is I/O interfaces.
SAFE-G	The INT, WU or RST source is from a SAFE condition
VREG-G	The INT, WU or RST source is from a Regulator event, or voltage monitoring event
CAN-LOC	The INT, WU or RST source is CAN interface. CAN local source.
CAN-BUS	The INT, WU or RST source is CAN interface. CAN bus source.
LIN2	The INT, WU or RST source is LIN2 interface
LIN1	The INT, WU or RST source is LIN1 interface
I/O-1	The INT, WU or RST source is I/O interface, flag from I/O sub adress Low (bit 7 = 0)
I/O-0	The INT, WU or RST source is I/O interface, flag from I/O sub adress High (bit 7 = 1)
VREG-1	The INT, WU or RST source is from a Regulator event, flag from REG register sub adress high (bit 7 = 1)
VREG-0	The INT, WU or RST source is from a Regulator event, flag from REG register sub adress low (bit 7 = 0)

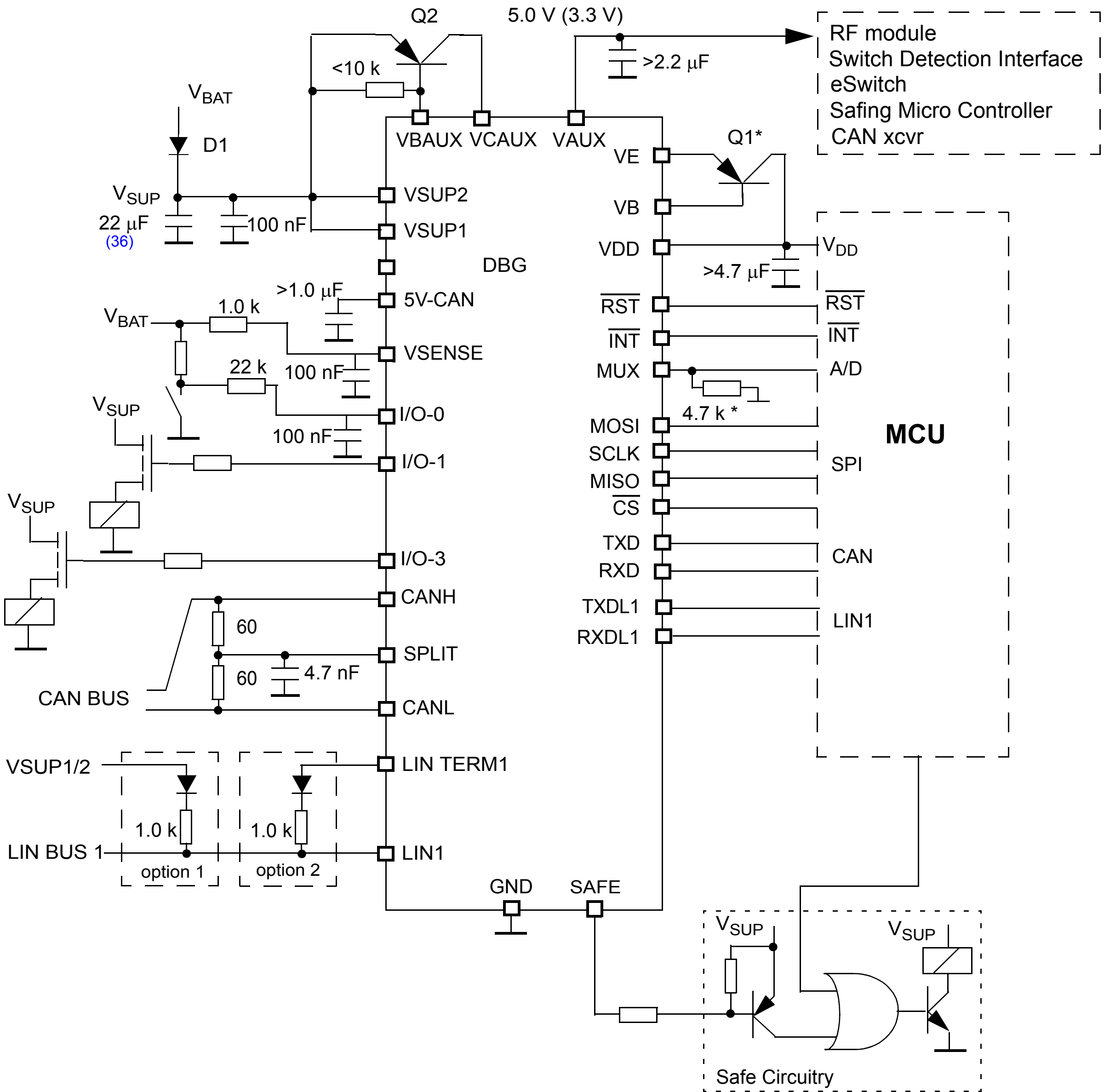
TYPICAL APPLICATIONS



Notes

35. Tested per specific OEM EMC requirements for CAN and LIN with additional capacitor > 10 µF on VSUP1/VSUP2 pins

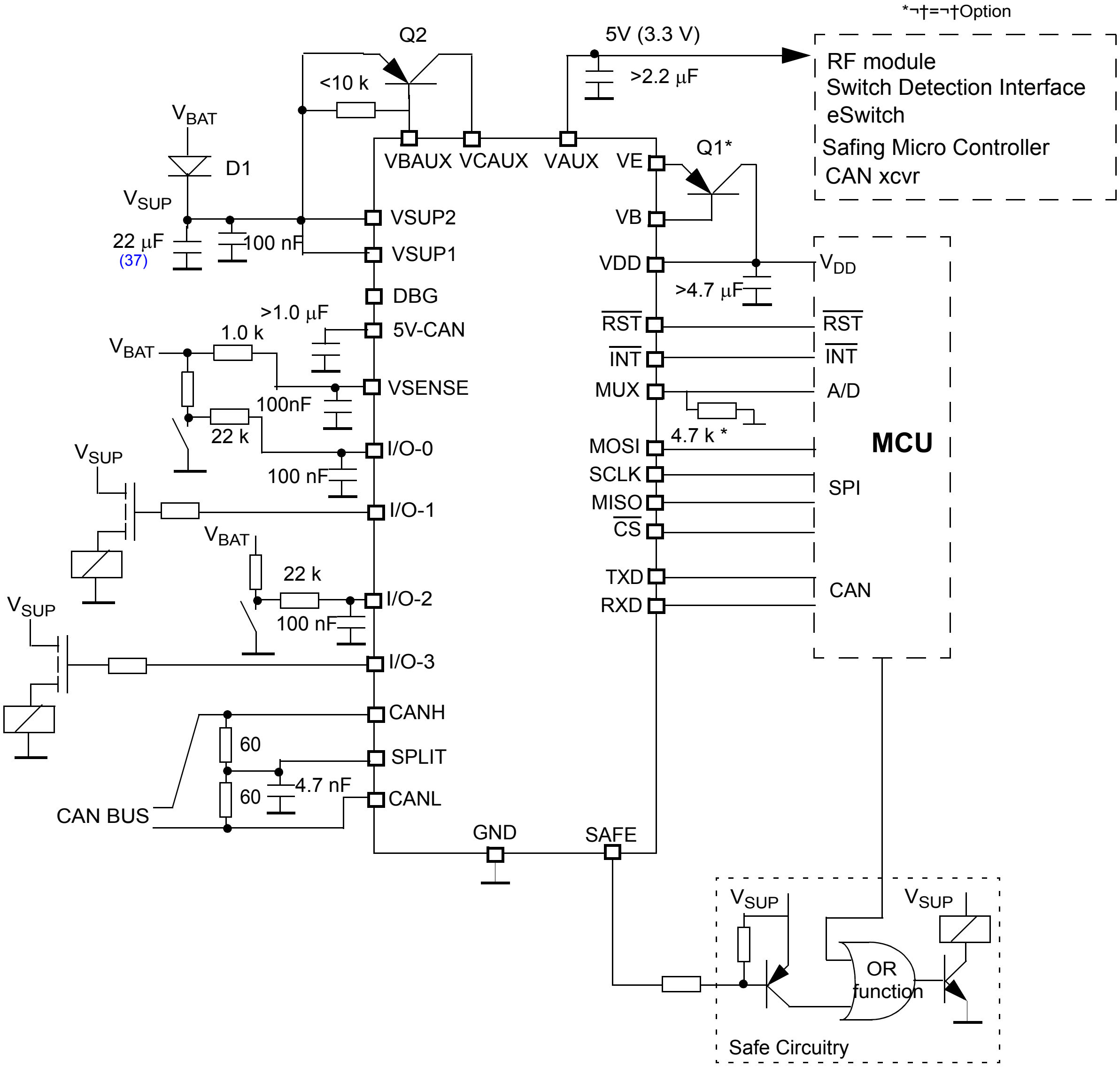
Figure 39. 33905D Typical Application Schematic



Notes

36. Tested per specific OEM EMC requirements for CAN and LIN with additional capacitor > 10 µF on VSUP1/VSUP2 pins

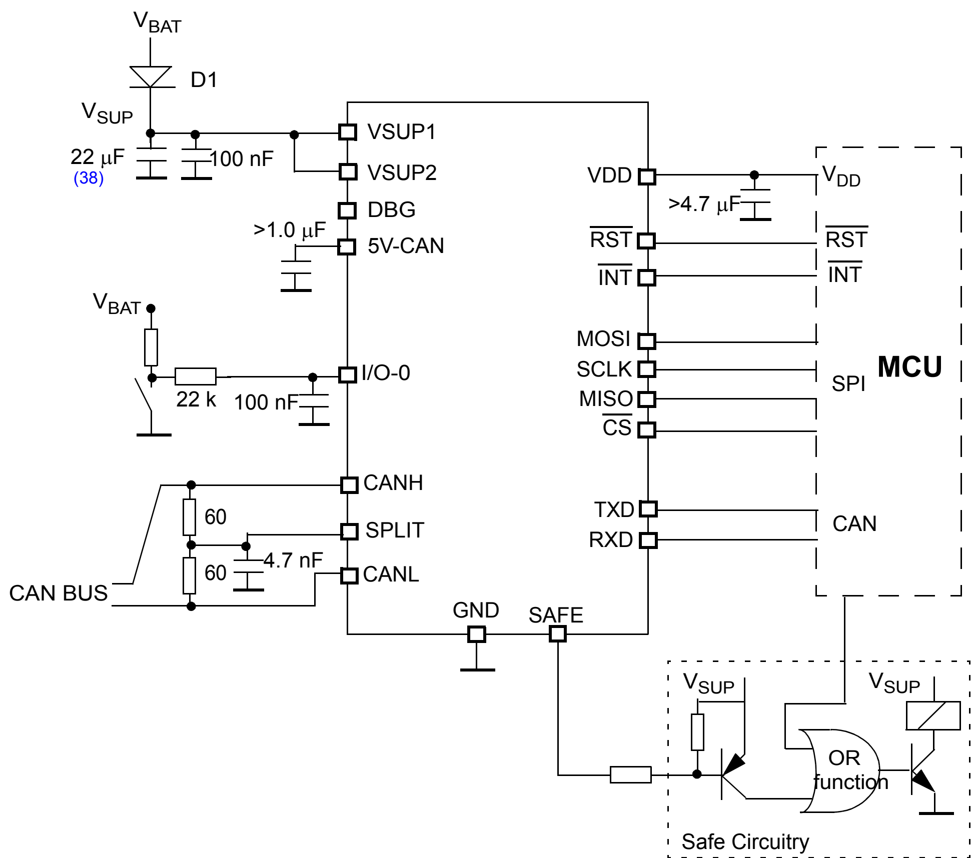
Figure 40. 33905S Typical Application Schematic



Notes

37. Tested per specific OEM EMC requirements for CAN and LIN with additional capacitor > 10 µF on VSUP1/VSUP2 pins

Figure 41. 33904 Typical Application Schematic



Notes
38. Tested per specific OEM EMC requirements for CAN and LIN with additional capacitor > 10 µF on VSUP1/VSUP2 pins

Figure 42. 33903 Typical Application Schematic

The following figure illustrates the application case where 2 reverse battery diodes can be used for optimization of the filtering and buffering capacitor at the VDD pin. This allows using a minimum value capacitor at the VDD pin to guarantee reset free operation of the MCU during the cranking pulse, and temporary (50 ms) loss of the V_{BAT} supply.

Applications without an external ballast on V_{DD} and without using the VAUX regulator are illustrated as well.

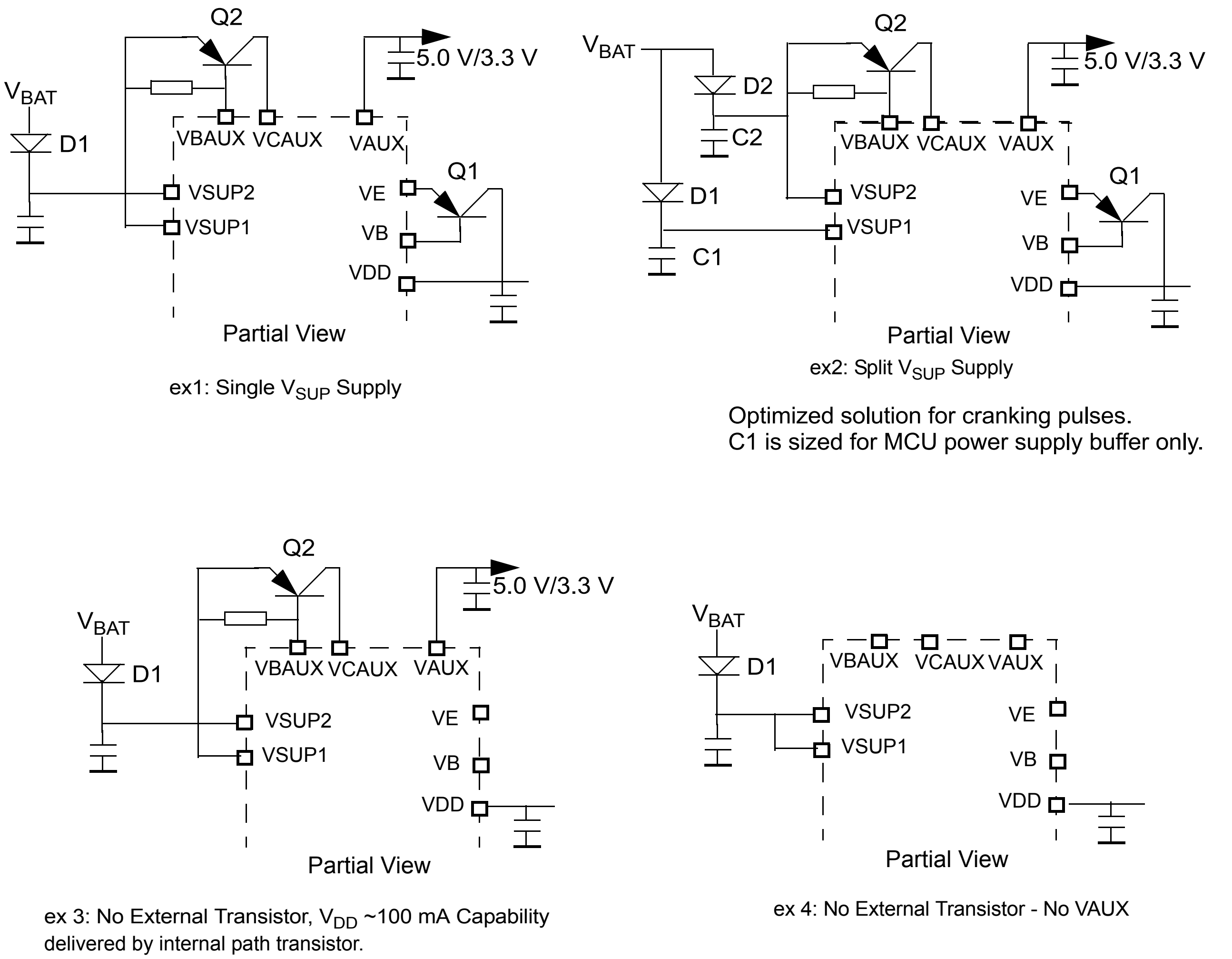
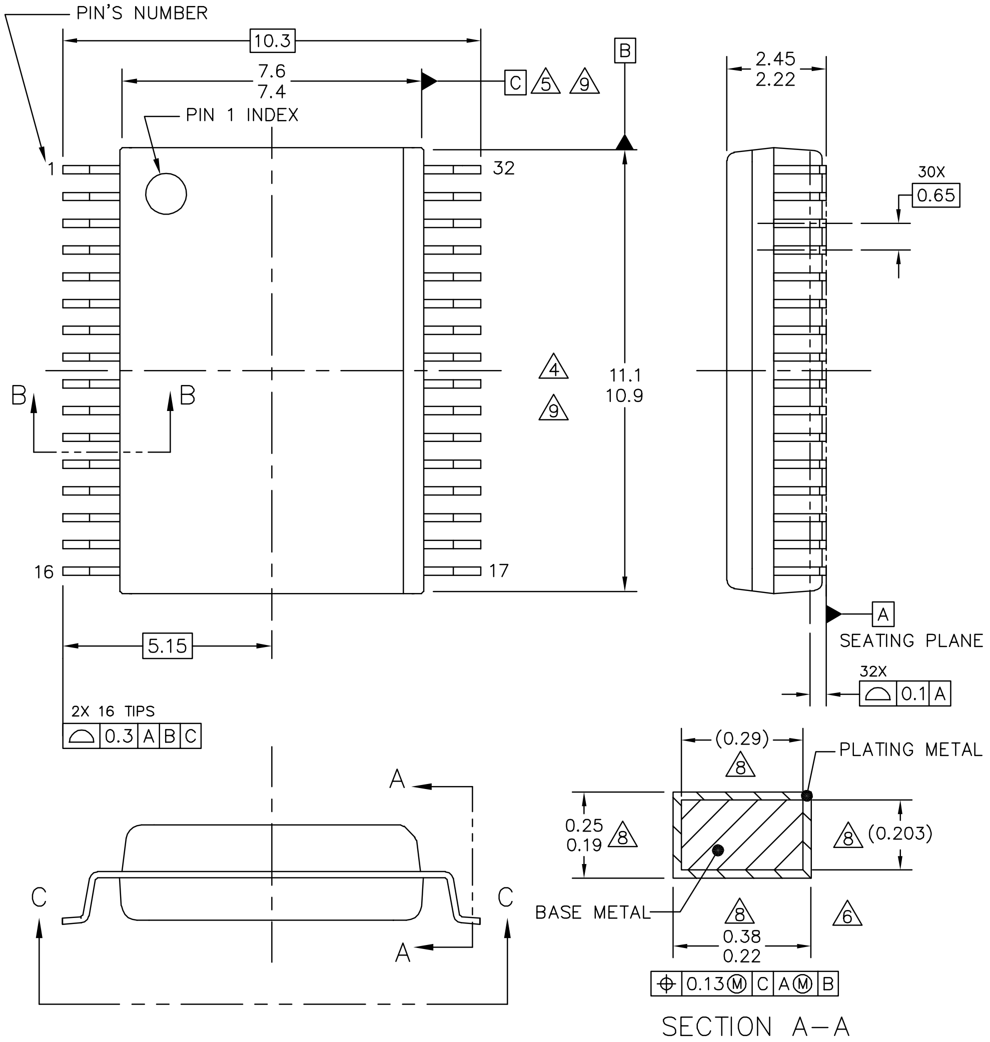


Figure 43. Application Options

PACKAGING

SOIC 32 PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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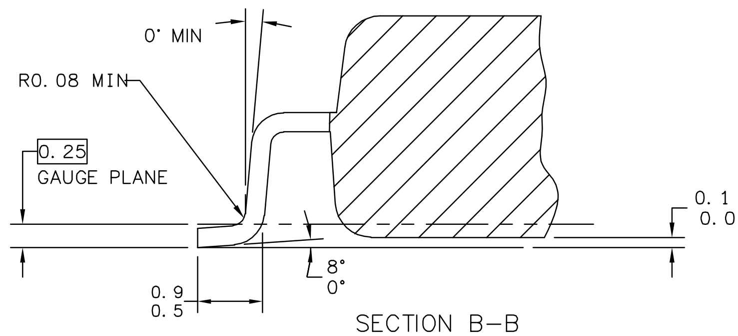
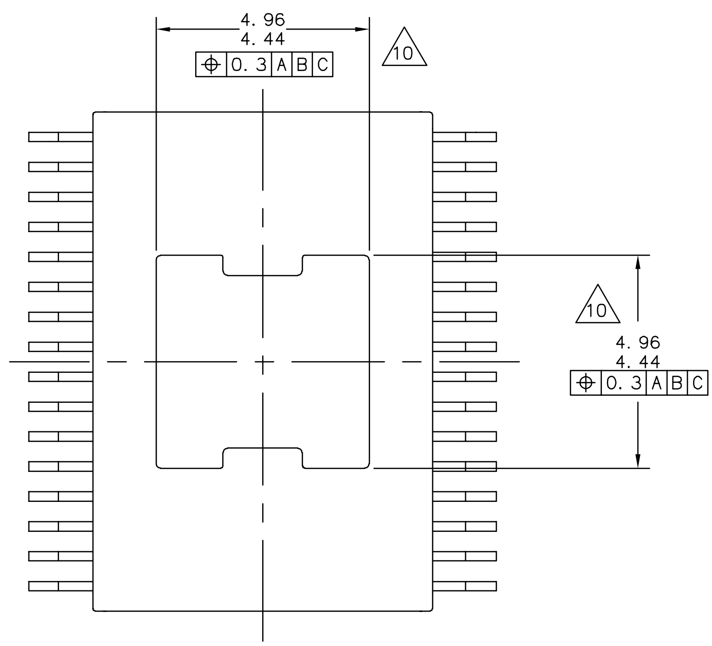
TITLE: 32LD SOIC W/B, 0.65 PITCH 4.7 X 4.7 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10556D	REV: D
	CASE NUMBER: 1454–04	20 JUN 2008
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
32-PIN SOIC WIDE BODY
EXPOSED PAD
98ASA10556D
REVISION D



SECTION B–B



VIEW C–C

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	CASE NUMBER: 1454–04	20 JUN 2008
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
32-PIN SOIC WIDE BODY
EXPOSED PAD
98ASA10556D
REVISION D

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. THIS DIMENSION DOES NOT INCLUDE INTER−LEAD FLASH OR PROTRUSIONS. INTER−LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.

9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER−LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

10. THESE DIMENSION RANGES DEFINE THE PRIMARY KEEP−OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.34mm FROM MAXIMUM EXPOSED PAD SIZE

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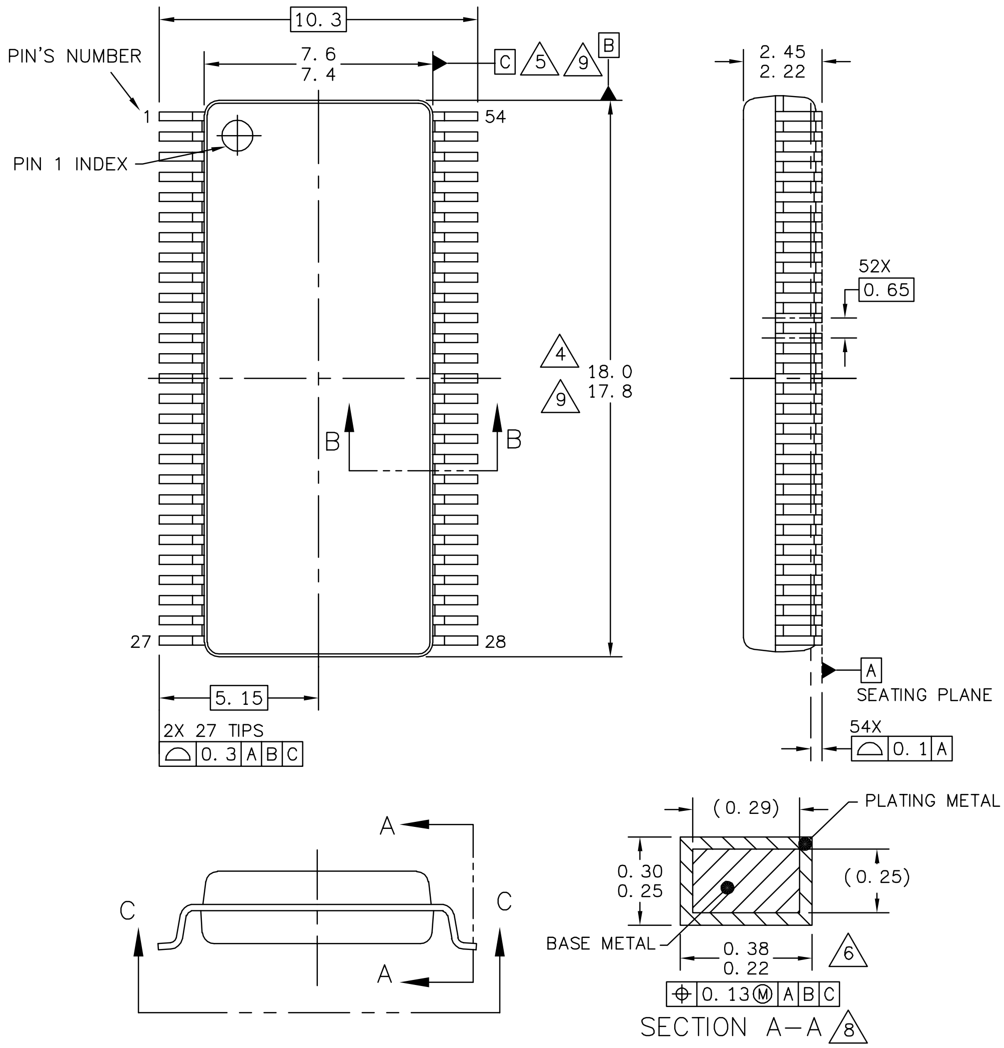
		CASE NUMBER: 1454−04	20 JUN 2008
		STANDARD: NON−JEDEC	

EK SUFFIX (PB-FREE)
32-PIN SOIC WIDE BODY
EXPOSED PAD
98ASA10556D
REVISION D

SOIC 54 PACKAGE DIMENSIONS



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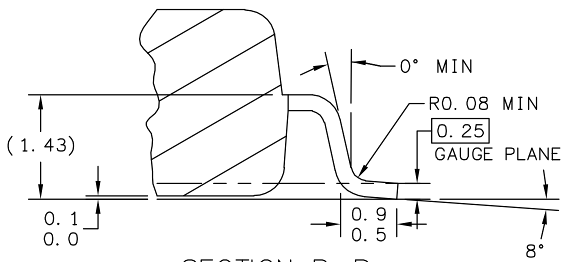
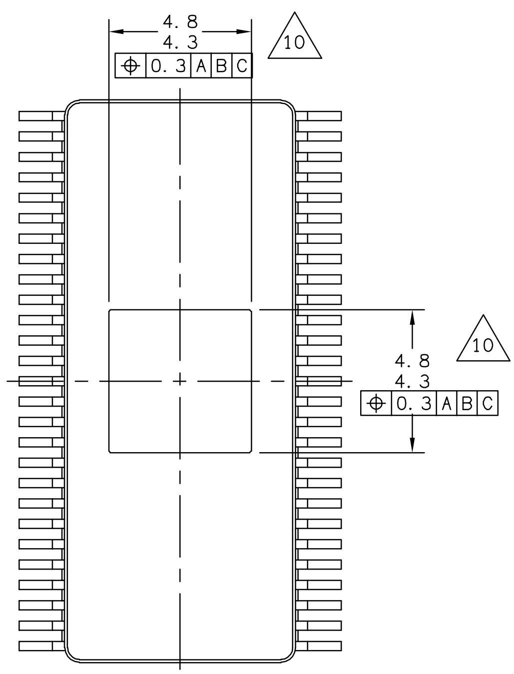
TITLE: 54LD SOIC W/B, 0. 65 PITCH 4. 6 X 4. 6 EXPOSED PAD, CASE-OUTLINE	DOCUMENT NO: 98ASA10506D		REV: D
	CASE NUMBER: 1390-03		02 MAY 2008
	STANDARD: NON-JEDEC		

EK SUFFIX (PB-FREE)
54-PIN SOIC WIDE BODY
EXPOSED PAD
98ASA10506D
REVISION D



SECTION B–B



VIEW C–C

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		CASE NUMBER: 1390–03	02 MAY 2008
		STANDARD: NON-JEDEC	

EK SUFFIX (PB-FREE)
54-PIN SOIC WIDE BODY
EXPOSED PAD
98ASA10506D
REVISION D

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

4. (△) THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. (△) THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. (△) THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.

7. (△) EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. (△) THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.

9. (△) THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

10. (△) THESE DIMENSIONS RANGES DEFINE THE PRIMARY KEEP-OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 1.5mm FROM MAXIMUM EXPOSED PAD SIZE

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	CASE NUMBER: 1390-03		02 MAY 2008
	STANDARD: NON-JEDEC		

EK SUFFIX (PB-FREE)
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EXPOSED PAD
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REVISION D

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
4.0	9/2010	• Initial Release - This document supersedes document MC33904_5. • Initial release of document includes the MC33903 part number, the VDD 3.3 V version description, and the silicon revision rev. 3.2. Change details available upon request.
5.0	12/2010	• Added Cyclic INT Operation During Low Power VDD ON Mode on page 42 • Changed VSUP pin to VSUP1 and pin 2 (NC) to VSUP2 for the 33903 device • Removed Drop voltage without external PNP pass transistor[9] on page 16 for V_{DD}=3.3 V devices • Added $V_{SUP1-3.3}$ to VDD Voltage regulator, VDD pin on page 16. • Added Pull-up Current, TxD, VIN = 0 V on page 20 for V_{DD}=3.3 V devices • Revised MUX and RAM registers on page 61 • Revised Status Bits Description on page 85 • Added Entering into LP Mode using Random Code on page 71.

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