

## 4K x 4 Static RAM with Separate I/O

### Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  - $t_{AA} = 15$  ns
- Transparent write (7C171A)
- Low active power
  - 375 mW
- Low standby power
  - 93 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

### Functional Description

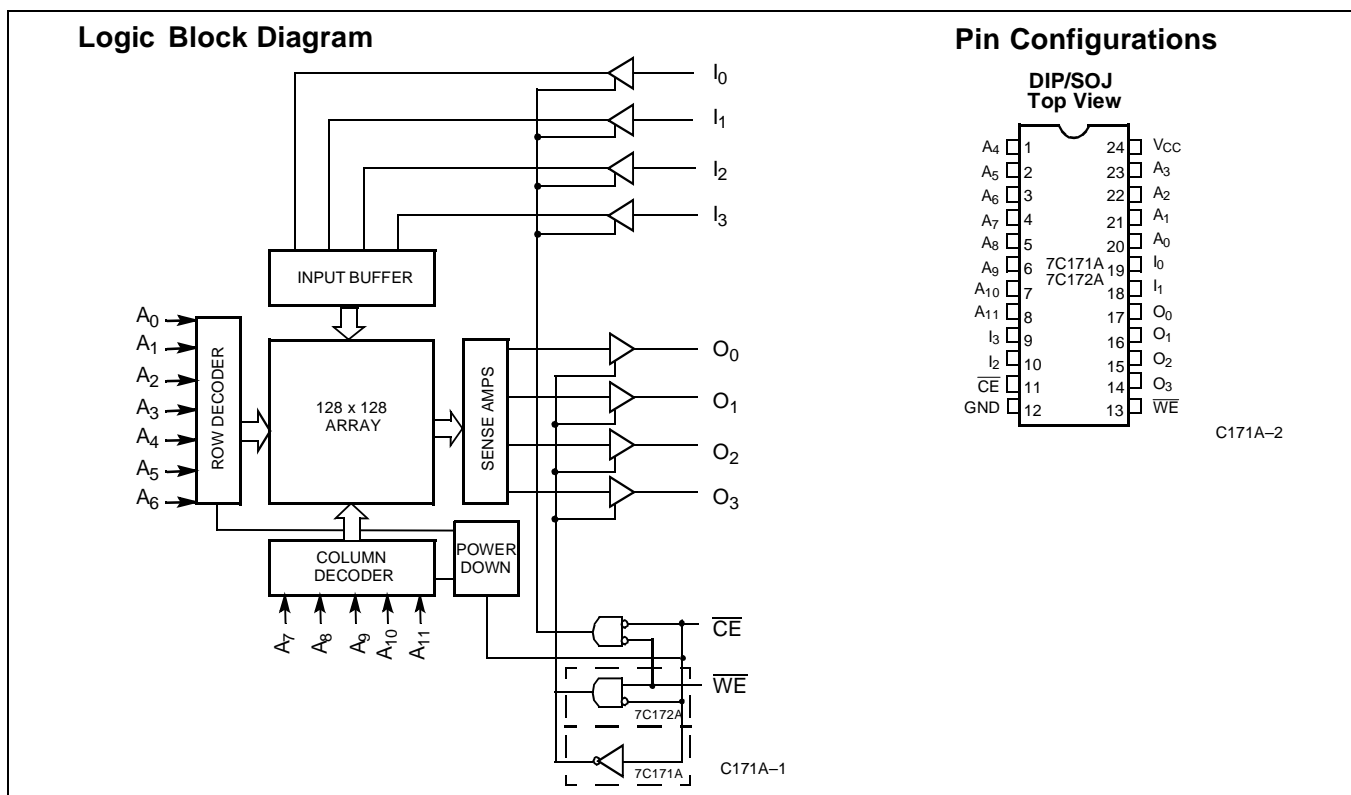
The CY7C171A and CY7C172A are high-performance CMOS static RAMs organized as 4096 by 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

Writing to the device is accomplished when the chip enable ( $\overline{CE}$ ) and write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the four input/output pins ( $I_0$  through  $I_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{11}$ ).

Reading the device is accomplished by taking chip enable ( $\overline{CE}$ ) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins remain in a high-impedance state when write enable ( $\overline{WE}$ ) is LOW (7C172A only), or chip enable is HIGH.

A die coat is used to insure alpha immunity.



### Selection Guide

		7C171A-15 7C172A-15	7C171A-20 7C172A-20	7C171A-25 7C172A-25	7C171A-35 7C172A-35	7C171A-45 7C172A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	80	70	70	
	Military		90	80	70	70

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential.....	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State .....	-0.5V to +7.0V
DC Input Voltage .....	-3.0V to +7.0V
Output Current into Outputs (LOW) .....	20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Military <sup>[1]</sup>	-55°C to +125°C	5V ± 10%

**Note:**

1. T<sub>A</sub> is the "instant on" case temperature.

### Electrical Characteristics Over the Operating Range<sup>[2]</sup>

Parameter	Description	Test Conditions	7C171A-15 7C172A-15		7C171A-20 7C172A-20		7C171A-25 7C172A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage		-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-10	+10	-10	+10	-10	+10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-350		-350		-350	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max. I <sub>OUT</sub> = 0 mA	Com'l	115		80		70	mA
			Mil			90		80	
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%	Com'l	40		40		20	mA
			Mil			40		20	
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	Com'l	20		20		20	mA
			Mil			20		20	



**CY7C171A**  
**CY7C172A**

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**Electrical Characteristics** Over the Operating Range<sup>[2]</sup> (continued)

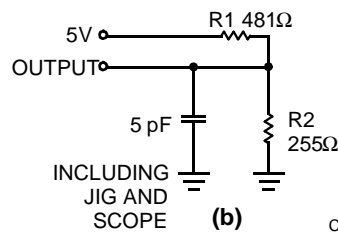
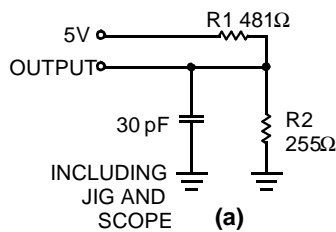
Parameter	Description	Test Conditions	7C171A-35 7C172A-35		7C171A-45 7C172A-45		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage		-3.0	0.8	-3.0	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-10	+10	-10	+10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-350		-350	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max. I <sub>OUT</sub> = 0 mA	Com'l		70		mA
			Mil		70	70	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%	Com'l		20		mA
			Mil		20	20	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	Com'l		20		mA
			Mil		20	20	mA

**Capacitance<sup>[4]</sup>**

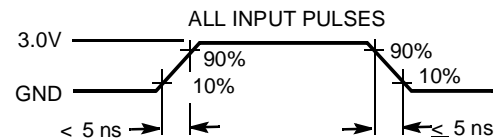
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Notes:**

- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters

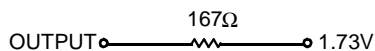
**AC Test Loads and Waveform**


C171A-3



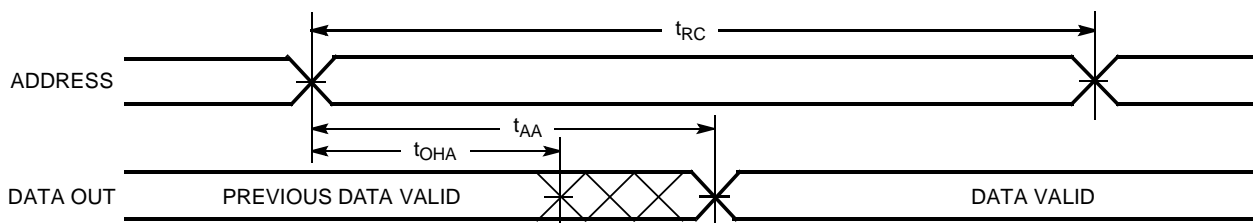
C171A-4

Equivalent to: THÉVENIN EQUIVALENT



**Switching Characteristics Over the Operating Range**<sup>[2,5]</sup>

Parameter	Description	7C171A-15 7C172A-15		7C171A-20 7C172A-20		7C171A-25 7C172A-25		7C171A-35 7C172A-35		7C171A-45 7C172A-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>												
$t_{RC}$	Read Cycle Time	15		20		25		35		45		ns
$t_{AA}$	Address to Data Valid		15		20		25		35		45	ns
$t_{OHA}$	Output Hold from Address Change	5		5		5		5		5		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
$t_{LZCE}$	$\overline{CE}$ LOW to LOW Z <sup>[6]</sup>	5		5		5		5		5		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to HIGH Z <sup>[6, 7]</sup>		8		8		10		15		15	ns
$t_{PU}$	$\overline{CE}$ LOW to Power Up	0		0		0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power Down		15		20		20		20		25	ns
$t_{RCS}$	Read Command Set-Up	0		0		0		0		0		ns
$t_{RCH}$	Read Command Hold	0		0		0		0		0		ns
<b>WRITE CYCLE</b> <sup>[8]</sup>												
$t_{WC}$	Write Cycle Time	15		20		20		25		40		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
$t_{AW}$	Address Set-Up to Write End	12		15		20		25		30		ns
$t_{HA}$	Address Hold from Write End	0		0		0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
$t_{SD}$	Data Set-Up to Write End	10		10		10		15		15		ns
$t_{HD}$	Data Hold from Write End	0		0		0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup> (7C172A)	5		5		5		5		5		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6,7]</sup> (7C172A)		7		7		7		10		15	ns
$t_{AWE}$	$\overline{WE}$ LOW to Data Valid (7C171A)		15		20		25		30		35	ns
$t_{ADV}$	Data Valid to Output Valid (7C171A)		15		20		25		30		35	ns

**Switching Waveforms**
**Read Cycle No. 1**<sup>[9,10]</sup>


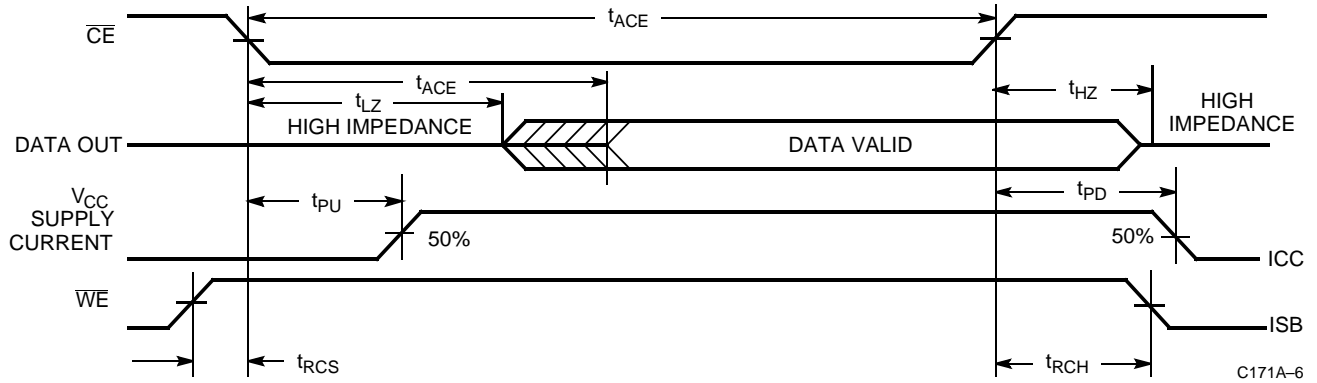
C171A-5

**Notes:**

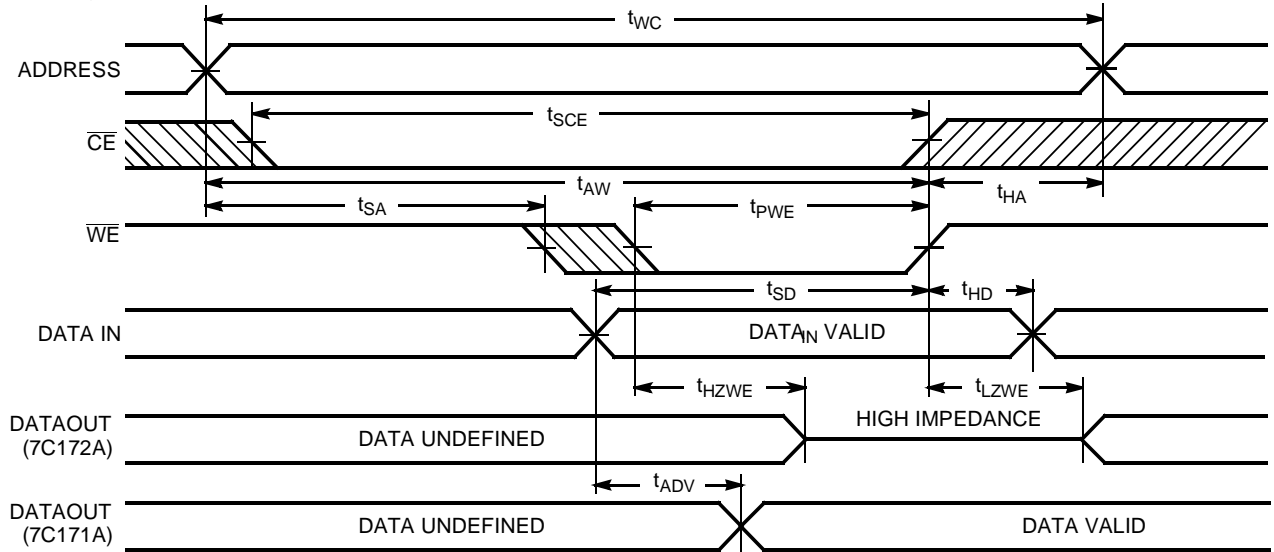
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified  $I_{OI}/I_{OH}$  and 30-pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZ}$  is less than  $t_{LZ}$  for any given device.
- $t_{HZCE}$  and  $t_{HZWE}$  are tested with  $C_L = 5\text{pF}$  as in part (b) of AC Test Loads. Transition is measured  $\pm 500\text{ mV}$  from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$  is HIGH for read cycle.
- Device is continuously selected,  $\overline{CE} = V_{IL}$ .

**Switching Waveforms (continued)**

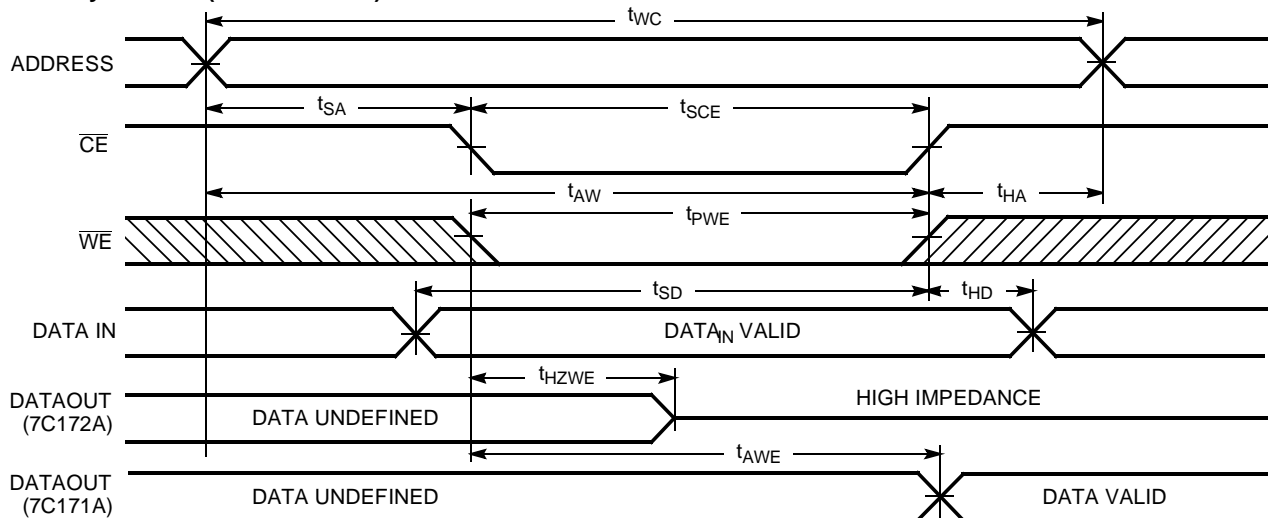
**Read Cycle No. 2<sup>[9,11]</sup>**



**Write Cycle No. 1 (WE Controlled)<sup>[8]</sup>**

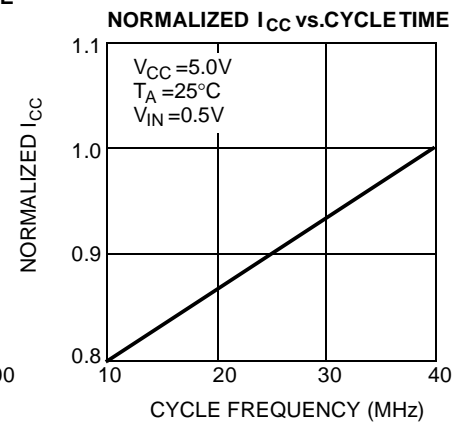
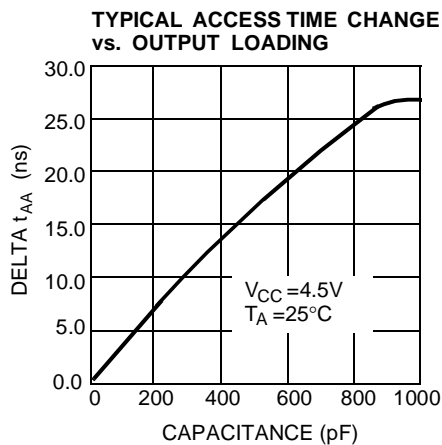
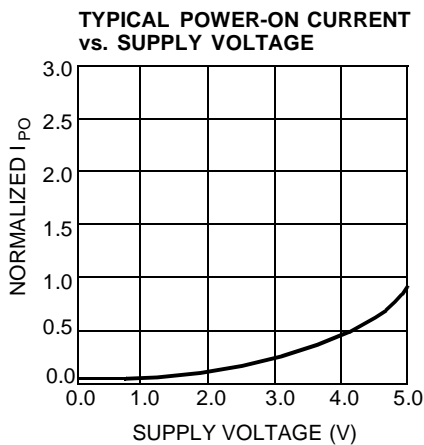
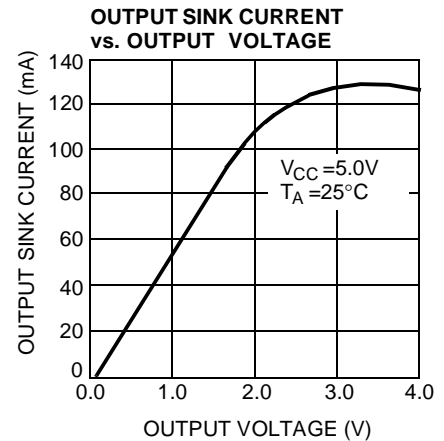
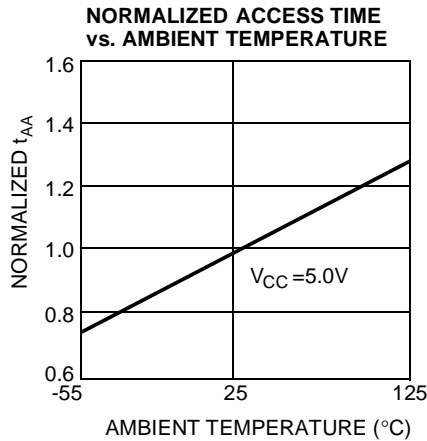
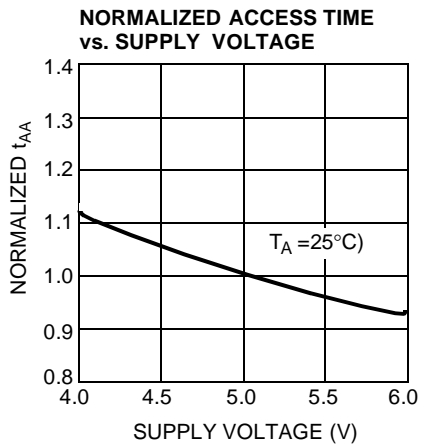
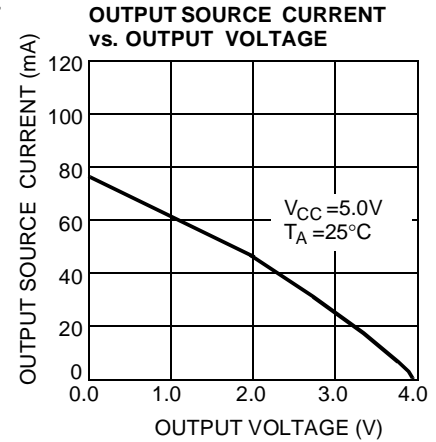
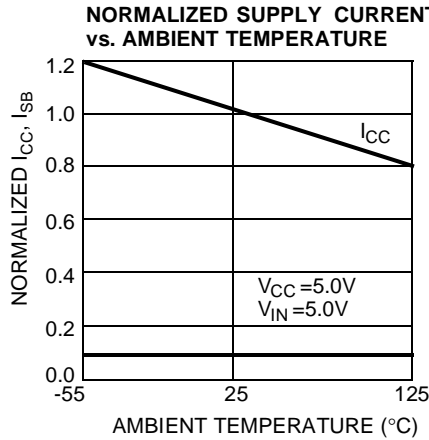
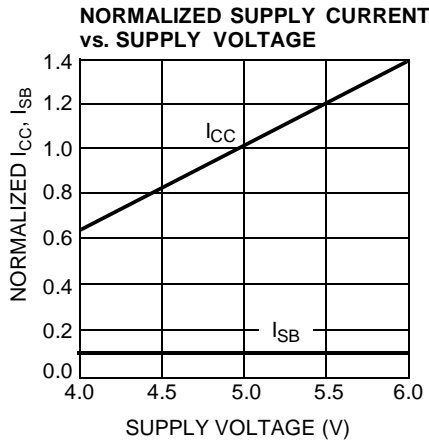


**Write Cycle No. 2 (CE Controlled)<sup>[8,12]</sup>**



**Notes:**

11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
12. If  $\overline{CE}$  goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state (7C172A).

**Typical DC and AC Characteristics**


**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C171A-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
20	CY7C171A-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
25	CY7C171A-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
35	CY7C171A-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C172A-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-15VC	V13	24-Lead Molded SOJ	
20	CY7C172A-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-20VC	V13	24-Lead Molded SOJ	
	CY7C172A-20DMB	D14	24-Lead (300-Mil) CerDIP	
25	CY7C172A-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-25VC	V13	24-Lead Molded SOJ	
	CY7C172A-25DMB	D14	24-Lead (300-Mil) CerDIP	
35	CY7C172A-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-35DMB	D14	24-Lead (300-Mil) CerDIP	
45	CY7C172A-45DMB	D14	24-Lead (300-Mil) CerDIP	Military

**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**
**DC Characteristics**

Parameter	Subgroups
$V_{OH}$	1, 2, 3
$V_{OL}$	1, 2, 3
$V_{IH}$	1, 2, 3
$V_{IL}$ Max.	1, 2, 3
$I_{IX}$	1, 2, 3
$I_{OZ}$	1, 2, 3
$I_{OS}$	1, 2, 3
$I_{CC}$	1, 2, 3
$I_{SB1}$	1, 2, 3
$I_{SB1}$	1, 2, 3

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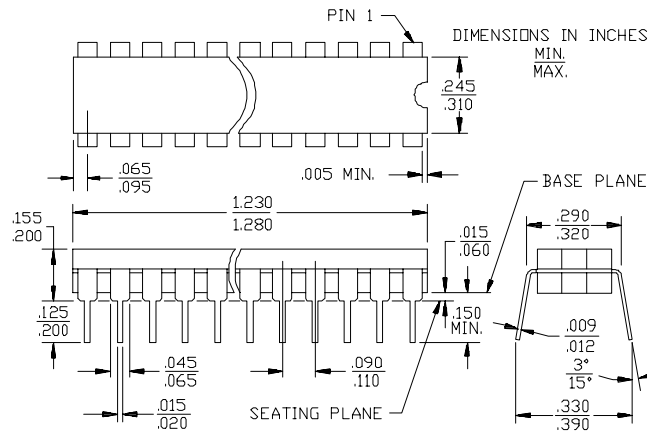
**Switching Characteristics**

Parameter	Subgroups
<b>READ CYCLE</b>	
$t_{RC}$	7, 8, 9, 10, 11
$t_{AA}$	7, 8, 9, 10, 11
$t_{OHA}$	7, 8, 9, 10, 11
$t_{ACE}$	7, 8, 9, 10, 11
$t_{RCS}$	7, 8, 9, 10, 11
$t_{RCH}$	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
$t_{WC}$	7, 8, 9, 10, 11
$t_{SCE}$	7, 8, 9, 10, 11
$t_{AW}$	7, 8, 9, 10, 11
$t_{HA}$	7, 8, 9, 10, 11
$t_{SA}$	7, 8, 9, 10, 11
$t_{PWE}$	7, 8, 9, 10, 11
$t_{SD}$	7, 8, 9, 10, 11
$t_{HD}$	7, 8, 9, 10, 11
$t_{AWE}^{[13]}$	7, 8, 9, 10, 11
$t_{ADV}^{[13]}$	7, 8, 9, 10, 11

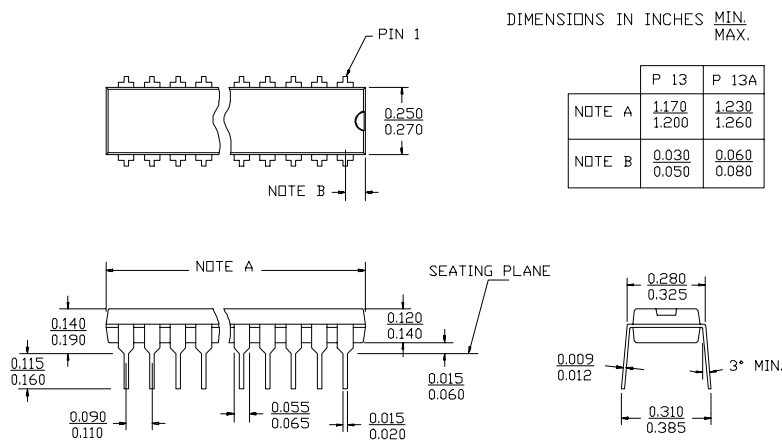


**Note:**  
13. 7C171A only.  
**Package Diagrams**

**24-Lead (300-Mil) CerDIP D14**  
MIL-STD-1835 D-9 Config.A



**24-Lead (300-Mil) Molded DIP P13/P13A**



**24-Lead Molded SOJ V13**

