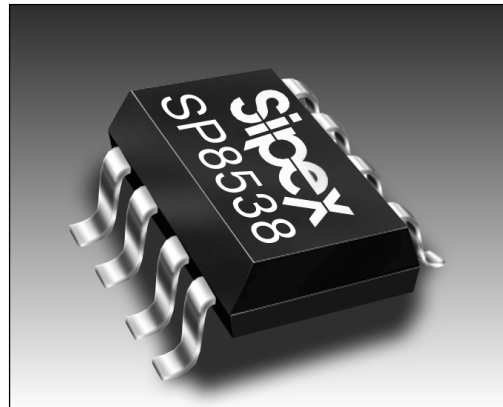


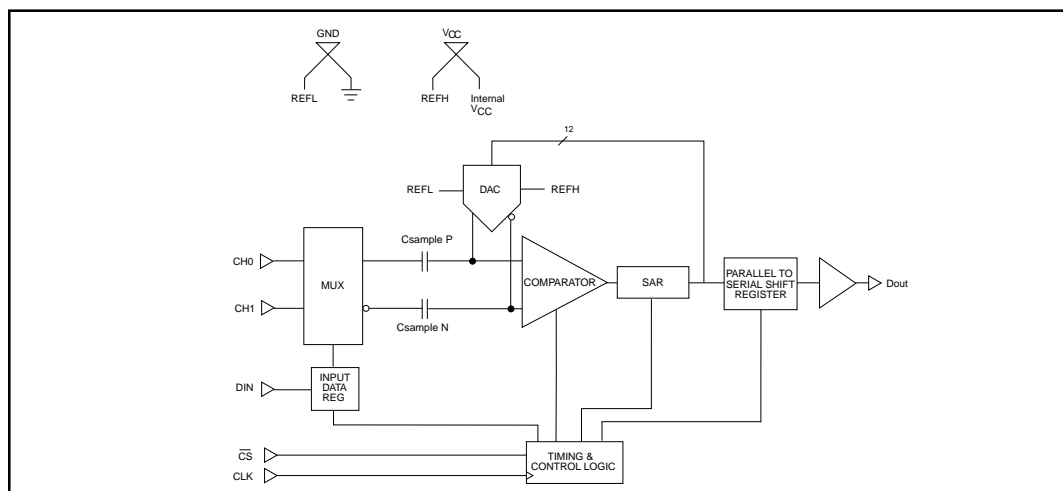
## Micropower Sampling 12-Bit A/D Converter

- Low Cost
- 12-Bit Serial Sampling ADC
- Guaranteed  $\pm 1.0$  LSB Max INL
- Guaranteed No Missing Codes
- 8-Pin NSOIC Plastic Package
- Low Power @ 250 $\mu$ A including Automatic Shutdown: 1nA(typ)
- Programmable Input Configuration:  
Full differential or 2 channel single-ended
- Single Supply 3.0V to 5.5V operation
- Half Duplex Digital Serial Interface
- Sample Rate: 40 $\mu$ S
- Pin Compatible Upgrade to LTC 1298



### DESCRIPTION

The **SP8538** is a very low power 12-Bit data acquisition chip. The **SP8538** typically draws 250 $\mu$ A of supply current when sampling at 25 kHz. Supply current drops linearly as the sample rate is reduced. The ADC automatically powers down when not performing conversions, drawing only leakage current. The **SP8538** is available in 8-Pin NSOIC packages, specified over Commercial and Industrial temperature ranges. The **SP8538** is best suited for Battery-Operated Systems, Portable Data Acquisition Instrumentation, Battery Monitoring, and Remote Sensing applications. The serial port allows efficient data transfer to a wide range of microprocessors and microcontrollers over 3 or 4 wires.



**SP8538 Block Diagram**

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

(TA=+25°C unless otherwise noted) .....	
VCC to GND .....	7.0V
Vin to GND .....	-0.3 to VCC +0.3V
Digital input to GND .....	-0.3 to VCC +0.3V
Digital output to GND .....	-0.3 to VCC +0.3V
Operating Temperature Range	
Commercial (J, K Version) .....	0°C to 70°C
Industrial (A, B Version) .....	-40°C to +85°C
Lead Temperature (Solder 10Sec) .....	+300°C
Storage Temperature .....	-65°C to +150°C
Power Dissipation to 70°C .....	500mW



**CAUTION:**  
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

## SPECIFICATIONS

Unless otherwise noted the following specifications apply for VCC=5V or 3.3V with limits applicable for Tmin to Tmax. Typical applies for Ta=25°C.

PARAMETERS	VCC=5.0V			VCC=3.3V			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
<b>DC ACCURACY</b>								
Resolution		12			12		Bits	
Integral Linearity								
J,A		+0.6	+2.0		+0.6	+2.0	LSB	No Missing Codes
K,B		+0.6	+1.0		+0.6	+1.0	LSB	
Differential Linearity Error								
J,A		+0.75	+2.0		+0.75	+2.0	LSB	
K,B		+0.75	+1.0		+0.75	+1.0	LSB	
Gain Error								
J,A		+2.0	+10		+2.0	+10	LSB	
K,B		+2.0	+8		+2.0	+8	LSB	
Offset Error								
J,A		+1.5	+5		+3.0	+8	LSB	
K,B		+1.5	+3		+3.0	+5	LSB	
<b>ANALOG INPUT</b>								
Input Signal FS Range	0		V <sub>CC</sub>	0		V <sub>CC</sub>		
Input Impedance								
On Channel		20			20		pF	In Parallel with 100mΩ
		100			100		MΩ	
Off Channel		3			3		pF	In Parallel with 100mΩ
		100			100		MΩ	
Input Bias Current		.001	1		.001	1	μA	
Analog Input Range	-0.05		V <sub>CC</sub> +0.05	-0.05		V <sub>CC</sub> +0.05	Volts	
<b>MULTIPLEXER</b>								
Crosstalk (f <sub>D</sub> = Nyquist)		-90			-90		dB	Off to On Channel
Feedthrough (f <sub>D</sub> = Nyquist)		-90			-90		dB	Off to On Channel f <sub>D</sub> = Disturbance
<b>CONVERSION SPEED</b>								
Sample Time		1.5			1.5		clock cycles	See Timing Diagrams
Conversion Time		12			12		clock cycles	See Timing Diagrams
Complete Cycle			25		5.85		kHz	See Timing Diagrams
Clock Period	2.25			10.0			μS	See Timing Diagrams
Clock High Time	1.0			4.5			μS	See Timing Diagrams
Clock Low Time	1.0			4.5			μS	See Timing Diagrams

## SPECIFICATIONS (cont.)

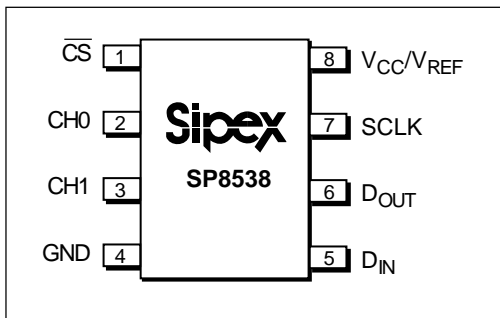
Unless otherwise noted the following specifications apply for VCC=5V or 3.3V with limits applicable for Tmin to Tmax. Typical applies for Ta=25°C.

PARAMETERS	VCC=5.0V			VCC=3.3V			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
<b>DIGITAL INPUTS</b> Input Low Voltage, VIL Input High Voltage, VIH Input Current IIN Input Capacitance	2.0		0.8 ±2.0	2.0		0.8 ±2.0	Volts Volts µA pF	V <sub>DD</sub> =5V ±5% V <sub>DD</sub> =5V ±5%
<b>DIGITAL OUTPUTS</b> Data Format Data Coding VOH VOL	4.0		0.4	2.0		0.4	Volts Volts	See Timing Diagram V <sub>DD</sub> =5V ±5%, IOH=-0.4mA V <sub>DD</sub> =5V ±5%, IOH=+1.6mA
<b>AC ACCURACY</b> Spurious free Dynamic Range (SFDR)  Total Harmonic Distortion (THD)  Signal to Noise & Distortion (SINAD)  Signal to Noise (SNR)		86		86			dB  dB  dB  dB	For all FFT's (Full Differential Mode) If V <sub>CC</sub> = 5V fsample = 25kHz fin = 12kHz  If V <sub>CC</sub> = 3.3V fsample = 5.8kHz fin = 2.8kHz
<b>SAMPLING DYNAMICS</b> Acquisition Time to 0.01%  -3dB Small Signal BW Aperture Delay Aperture Jitter Common-Mode Rejection Ratio		2 5 20 150 70	3.38	3 4 30 150 70	15.0		µs MHz nS pS dB	f <sub>CM</sub> = 12.5kHz @ 5 volts 2.8kHz @ 3.3 volts
<b>POWER SUPPLIES</b> V <sub>CC</sub> Supply Current Operation Mode  Shutdown Mode  Power Dissipation Operating Mode Shutdown Mode	+3.0	+5.0 250 0.001 1.25	+5.5 400 0.5 2	+3.0 150 0.001 0.5	+3.3 300 0.5 0.99	+5.5	Volts µA µA mW µW	(CS=0) 25kHz, 5 volt conversion rate. 5.8kHz 3.3 volts  (CS=1)
<b>TEMPERATURE RANGE</b> Commercial Industrial Storage		0° to +70°C -40° to +85°C -65° to +150°C		0° to +70°C -40° to +85°C -65° to +150°C			°C °C °C	

**SPECIFICATIONS (cont.)**  
**Recommended Operating Conditions**

SYMBOL	PARAMETERS	VCC=5.0V			VCC=3.3V			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	Supply Voltage	+3.0	+5.0	+5.5	+3.0	+3.3	+5.5	Volts
$f_{CLK}$	Clock Frequency			444			100	kHz
$t_{CVC}$	Total Cycle Time	40			170			$\mu$ S
$t_{hDI}$	Hold Time $D_{IN}$ After $CLK^{\wedge}$	50	0		50	0		nS
$t_{suCS}$	Setup Time $\overline{CS}$ Before $CLK^{\wedge}$	100			150			nS
$t_{suDI}$	Setup Time, $D_{IN}$ Stable Before $CLK^{\wedge}$	100	10		150			nS
$t_{WHCLK}$	CLK High Time	1			4.5			$\mu$ S
$T_{WHCLK}$	CLK Low Time	1			4.5			$\mu$ S
$T_{WHCS}$	$\overline{CS}$ High Time between Data Transfers Cycles	100			150			nS

**PIN DESCRIPTION**



**PIN ASSIGNMENTS**

- Pin 1-  $\overline{CS}$  - Chip Select.
- Pin 2- CH0 - Channel 0
- Pin 3- CH1 - Channel 1
- Pin 4- GND - Ground
- Pin 5-  $D_{IN}$  - Data In
- Pin 6 -  $D_{OUT}$  - Data Out
- Pin 7- SCLK - Serial Clock
- Pin 8-  $V_{CC}/V_{REF}$  - Supply & Reference Voltage

## DESCRIPTION

The **SP8538** is a 12 bit sampling ADC with a programmable two channel multiplexer and serial data interface. The ADC samples and converts 12 bits of data in 40  $\mu$ S with a 5V supply voltage applied. The **SP8538** will also operate at a 3.3V supply at 170 $\mu$ S throughput. The device automatically shuts down to a  $\pm 0.5 \mu$ A (MAX) level as soon as the chip is deselected ( $\overline{CS}=1$ ). Serial data output is available in an MSB first or LSB first format.

## FEATURES

Two program bits, which are shifted into the device prior to conversion, determine the input configuration. In the single ended MUX configuration the input signal will be applied to either channel 0 or channel 1 and will be ground referenced. The maximum full scale range is VCC. In the full differential mode, the signal will be applied between channel 0 and channel 1. The signals applied at each input may both be dynamic. This is in contrast with pseudo differential devices which must have input low held at a constant level during conversion. The converter will provide significant common mode rejection when used in full differential manner. Both inputs must remain between ground and VCC for proper conversion.

The device uses a capacitive DAC architecture which provides the sampling behavior. This results in full Nyquist performance at the fastest throughput rate (25 KHz) the device is capable of.

The power supply voltage is variable from 3.0V to 5.5V which provides supply flexibility. At the 5.0V supply level, conversion plus sampling time is 40 $\mu$ S and supply current is 250 $\mu$ A (1.25 mW). With a 3.3V supply the conversion plus sampling time is 170 $\mu$ S and current is reduced to 150 $\mu$ A (0.5 mW).

The device features automatic shutdown and will shutdown to a  $\pm 0.5 \mu$ A power level as  $\overline{CS}$  is brought high (de-selected). Power is proportional to conversion duty cycle and varies from 250  $\mu$ A at 40 $\mu$ S (Duty cycle = 100%) to 6.25 $\mu$ A at 1.6 ms (Duty cycle = 2.5%).

### Examples:

<u>Conversion rate</u>	<u>I<sub>CC</sub>@ 5V</u>	<u>Duty Cycle</u>
40 $\mu$ S	250 $\mu$ A	100%
80 $\mu$ S	125 $\mu$ A	50%
160 $\mu$ S	62.5 $\mu$ A	25%

## ADDRESSING

Mux Addressing		Channel #		GND	Comments
SGL/DIFF	ODD/SIGN	0	1		
0	0	V <sub>INH</sub>	V <sub>INL</sub>		Full Differential Mode
0	1	V <sub>INL</sub>	V <sub>INH</sub>		
1	0	V <sub>INH</sub>		V <sub>INL</sub>	Single Ended Mux Mode
1	1		V <sub>INH</sub>	V <sub>INL</sub>	

## ADC TRANSFER FUNCTION

INPUT VOLTAGE (V <sub>INH</sub> -V <sub>INL</sub> )*	INPUT VOLTAGE AT V <sub>CC</sub> /V <sub>REF</sub> = 5V	OUTPUT CODE
0 LSB	0V	000000000000
1 LSB	0.00122V	000000000001
2048 LSB	2.5000V	100000000000
4094 LSB	4.9976V	111111111110
4095 LSB	4.9988V	111111111111

\* See Mux Addressing Table for a definition of V<sub>INH</sub> - V<sub>INL</sub>.

1.6 mS      6.25  $\mu$ A      2.5%

The device can be configured such that it delivers serial data MSB first requiring 17 clock periods for a full conversion. Alternately, the device can be programmed to deliver 12 bits of data MSB first, followed by the same 12 bits of data LSB first. This sequence will require 28 clock periods to complete. Please refer to the timing diagram.

### Circuit Operation

The device will ignore any leading zeros applied to the  $\overline{\text{DIN}}$  pin even if CS is low. After Chip Select Bar (CS) is brought low and the START bit is clocked in to the converter, the conversion sequence is initiated. Three additional bits are clocked in immediately following the START bit: SGL/DIFF, ODD/SIGN & MSBF. The second and third bits clocked in determine the MUX configuration (see MUX addressing table). The fourth bit determines the data output format (MSB first or LSB first). Please refer to the timing diagram.

The SGL/DIFF bit when zero sets the input MUX for full differential mode and when one, sets the input MUX for single ended mode. The ODD/SIGN bit when zero sets channel zero as the positive input (ground referred for single ended operation and referred to channel one in differential mode). With the ODD/SIGN bit one, channel one will be the positive input (ground referred for single ended operation and referred to channel zero in differential mode).

With MSBF set to one, the output data stream will be MSB through LSB, with MSBF set to zero the output data stream will be MSB through LSB followed by the same data in LSB through MSB format.

The **SP8538** is a SAR converter with full differential multiplexed front end, capacitive DAC, precision comparator, Successive Approximations Register, control logic and data output register. After the input is sampled and held the conversion process begins. The DAC MSB is set and its output is compared with the signal input, if the DAC output is less than the input, the comparator outputs a one which is latched into the SAR and simultaneously made available at the ADC serial output pin. Each bit

is tested in a similar manner until the SAR contains a code which represents the signal input to within  $\pm 1/2$  LSB. During this process the SAR content has been shifted out of the ADC serially. If the MSB first format was chosen, the data will appear at the DOUT pin MSB through LSB in 17 clock periods. If the LSB first format was chosen then during conversion the data will appear at the DOUT pin just as before (MSB through LSB) but the LSB will be followed by D1, D2 through the MSB. This sequence will require 28 clock periods. Note that the Chip Select Bar pin must be toggled high between conversions. The DOUT pin will be in a high impedance state whenever Chip Select Bar is high. After Chip Select Bar has been toggled and brought low again, the converter is ready to accept another START bit and begin a new conversion.

### Full Differential Sampling

The **SP8538** can be configured for single-ended sampling (i.e. CH0-ground or CH1-ground) or full differential sampling (CH0-CH1 or CH1-CH0). In the full differential sampling configuration, both inputs are sampled and held simultaneously. Because of the balanced differential sampling, dynamic common mode noise riding along the input signal is cancelled above and beyond DC noise. This is a significant improvement over pseudo-differential sampling schemes, where the low side of the input must remain constant during the conversion, and therefore only DC noise (i.e. signal offset) is cancelled. If AC common mode noise is left to be converted along with the differential component, the output signal will be degraded.

Full differential sampling allows flexibility in converting the input signal. If the signal low-side is already tied to a ground elsewhere in the system, it can be hardwired to the low side channel (i.e. CH0 or CH1) which acts as a signal ground sense, breaking a potential ground loop. It is also possible to drive the inputs balanced differential, as long as both inputs are within the power rails. In this configuration, both the high and low signals have the same impedance looking back to ground, and therefore pick up the same noise along the physical path from signal source (i.e. sensor, transducer, battery) to converter. This noise becomes common mode, and is cancelled out

by the differential sampling of the **SP8538**.  
**Layout Considerations**

To preserve the high resolution and linearity of the **SP8538** attention must be given to circuit board layout, ground impedance and bypassing.

A circuit board layout which includes separate analog and digital ground planes will prevent the coupling of noise into sensitive converter circuits and will help to preserve the dynamic performance of the device. In single ended mode, the analog input signal should be referenced to the ground pin of the converter. This prevents any voltage drops that occur in the power supply's common return from appearing in series with the input signal.

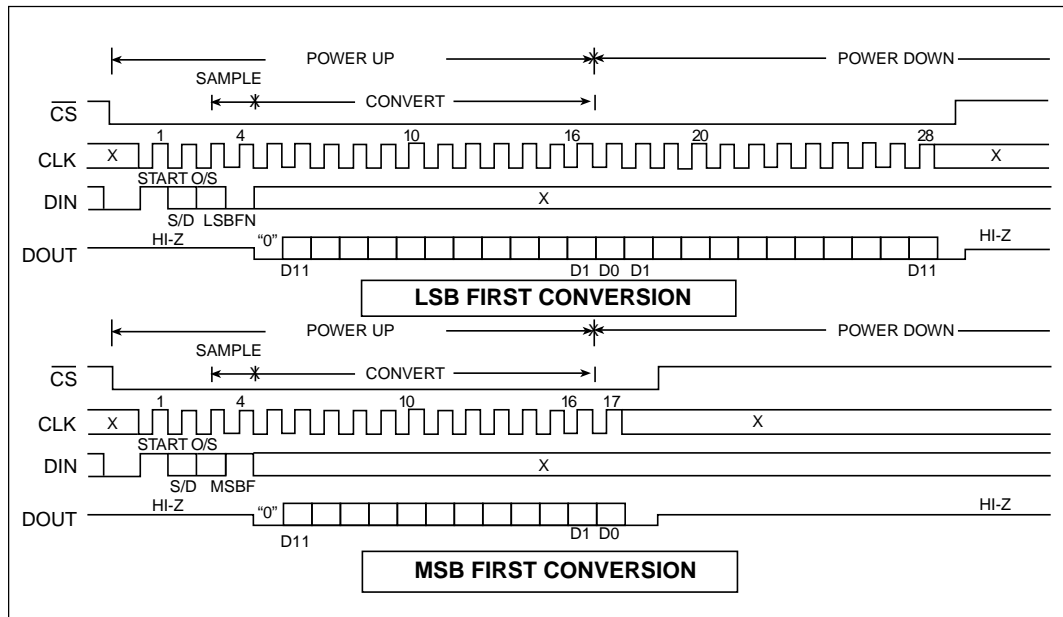
In full differential mode, the high and low side board traces should run close to each other, with the same layout. This will insure that any noise coupling will be common mode, and cancelled by the converters (patent pending) full differential architecture.

If separate analog and digital ground planes are not possible, care should be used to prevent coupling between analog and digital signals. If analog and digital lines must cross, they should

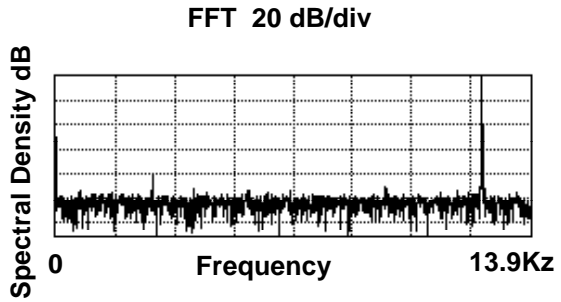
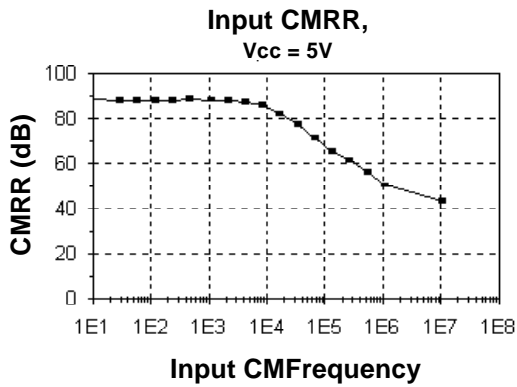
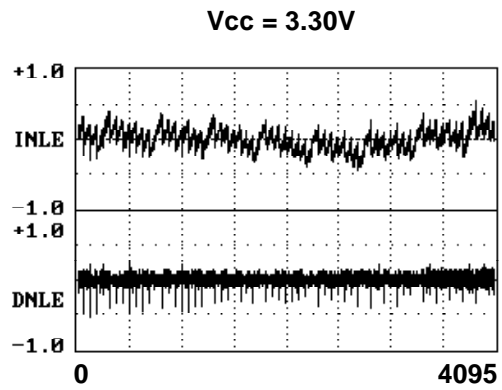
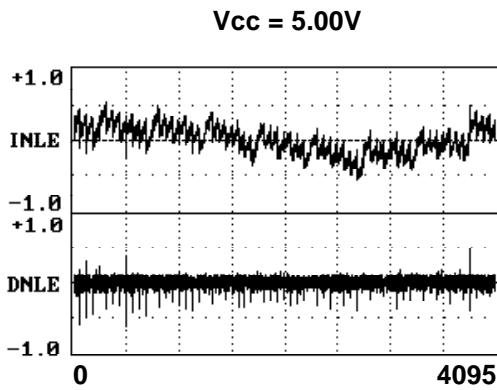
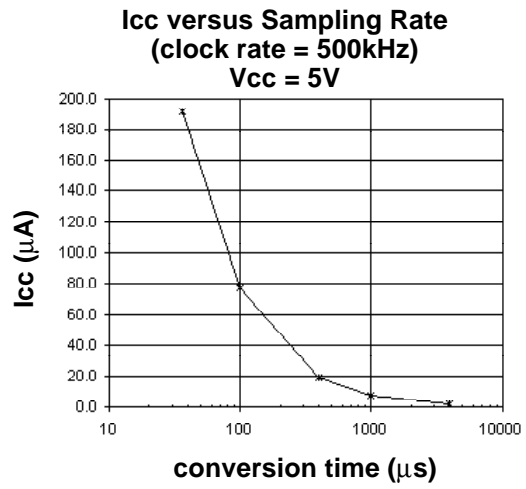
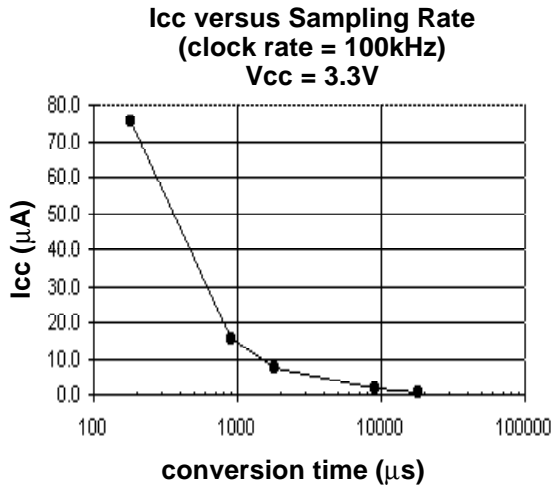
do so at right angles. Parallel analog and digital lines should be separated by a circuit board trace which is connected to common.

The **SP8538** VCC pin is also the reference pin for the device. This means that noise on the VCC pin will be proportionally represented as noise in the converters output data. A noise signal of 1.22mV (at a 5V supply) will produce 1 LSB of error in the output data. The VCC pin should be bypassed to the ground pin with a parallel combination of a 6.8 $\mu$ F tantalum and a 0.1 $\mu$ F ceramic capacitor. To maintain maximum system accuracy, the supply connected to the VCC pin should be well isolated from digital supplies and wide load variations. A separate conductor from the supply regulator to the A/D converter will limit the effects of digital switching elsewhere in the system. Power supply noise can degrade the converters performance. Especially corrupting are noise and spikes from a switching power supply.

To avoid introducing distortion when driving the A/D converter input, the input signal source should be able to charge the **SP8538's** equivalent 20 pF of input capacitance from zero volts to the signal level in 1.5 clock periods.



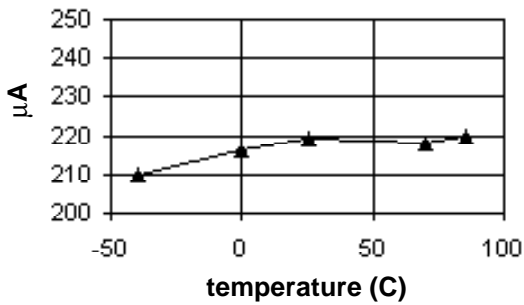
**SP8538 Timing Diagram**



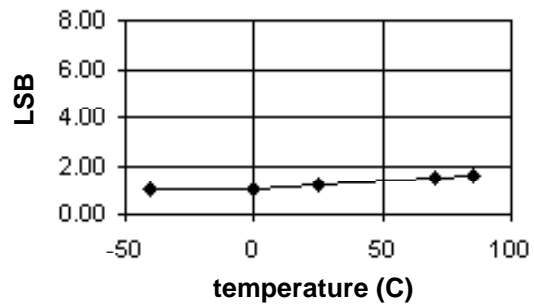
SNR = -73.31 dB  
 THD = -78.53 dB  
 SINAD = -72.17 dB  
 SFDR = -80.15 dB  
 Vin amp = -0.02 dB



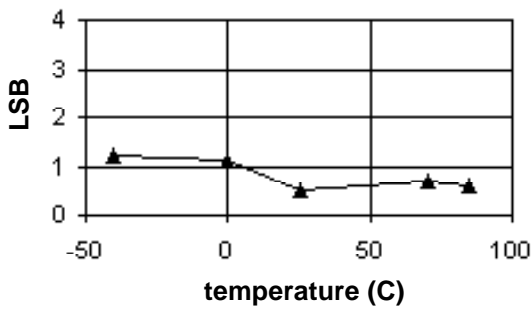
Icc vs. Temperature



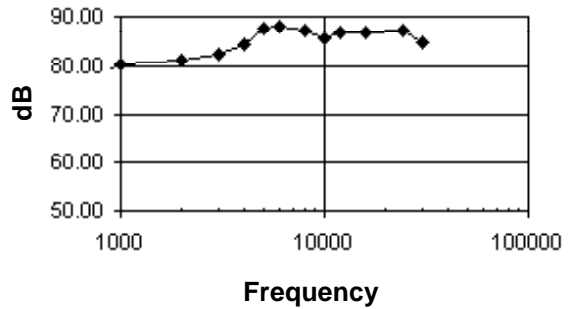
Gain Error vs. Temperature



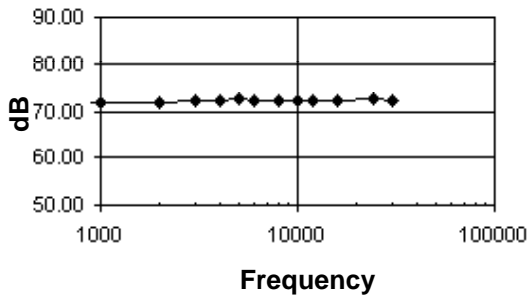
Offset vs. Temperature



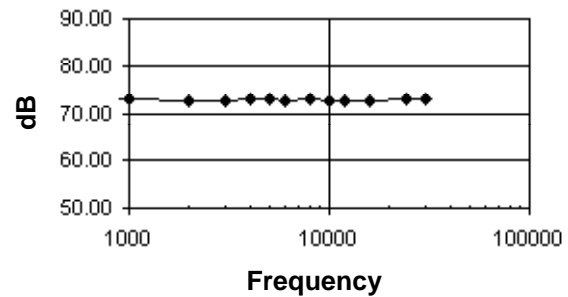
Spurious Free Dynamic Range



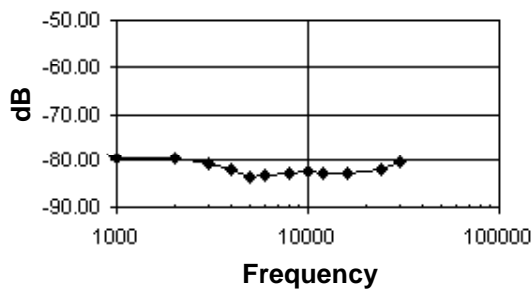
SINAD



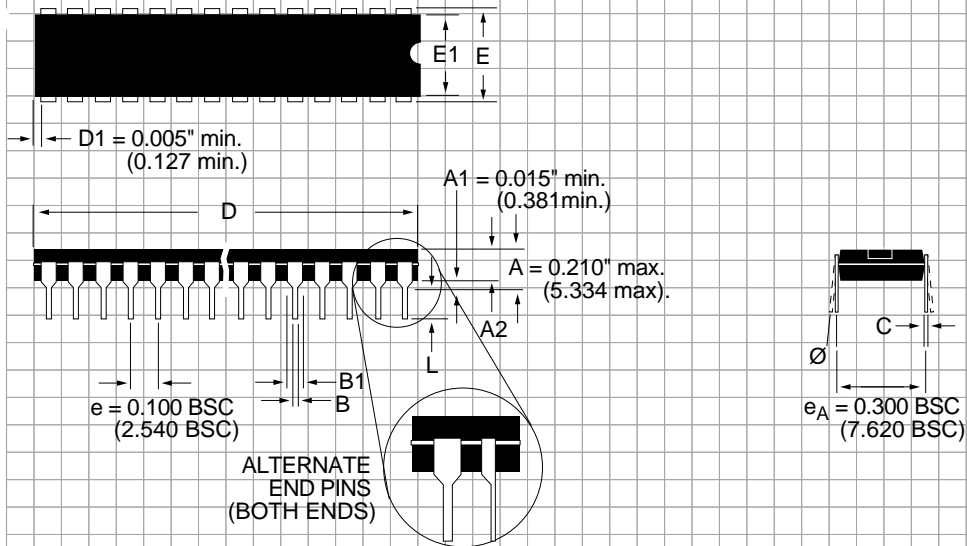
Signal to Noise Ratio



Total Harmonic Distortion

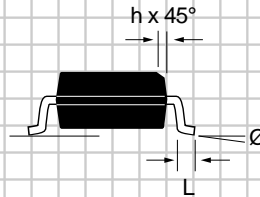
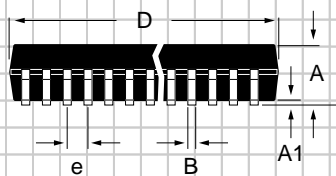
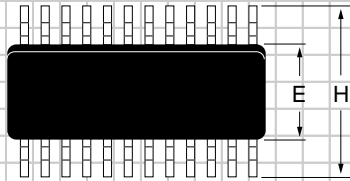


**PACKAGE: PLASTIC  
DUAL-IN-LINE  
(NARROW)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	8-PIN	14-PIN	16-PIN	18-PIN	20-PIN	22-PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.355/0.400 (9.017/10.160)	0.735/0.775 (18.669/19.685)	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)	0.980/1.060 (24.892/26.924)	1.145/1.155 (29.083/29.337)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
$\text{Ø}$	0°/15° (0°/15°)	0°/15° (0°/15°)	0°/15° (0°/15°)	0°/15° (0°/15°)	0°/15° (0°/15°)	0°/15° (0°/15°)

**PACKAGE: PLASTIC  
SMALL OUTLINE (SOIC)  
(NARROW)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	8-PIN	14-PIN	16-PIN
A	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)	0.053/0.069 (1.346/1.748)
A1	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)	0.004/0.010 (0.102/0.249)
B	0.014/0.019 (0.35/0.49)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.189/0.197 (4.80/5.00)	0.337/0.344 (8.552/8.748)	0.386/0.394 (9.802/10.000)
E	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)	0.150/0.157 (3.802/3.988)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)	0.228/0.244 (5.801/6.198)
h	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)	0.010/0.020 (0.254/0.498)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

## ORDERING INFORMATION

Model .....	Linearity (LSB) .....	Temperature Range .....	Package .....
SP8538BN .....	±1.0 .....	-40°C to +85°C .....	8-pin, 0.3" Plastic DIP
SP8538KN .....	±1.0 .....	-0°C to +70°C .....	8-pin, 0.3" Plastic DIP
SP8538BS .....	±1.0 .....	-40°C to +85°C .....	8-pin, 0.15" Plastic SOIC
SP8538KS .....	±1.0 .....	-0°C to +70°C .....	8-pin, 0.15" Plastic SOIC
SP8538AN .....	±2.0 .....	-40°C to +85°C .....	8-pin, 0.3" Plastic DIP
SP8538JN .....	±2.0 .....	-0°C to +70°C .....	8-pin, 0.3" Plastic DIP
SP8538AS .....	±2.0 .....	-40°C to +85°C .....	8-pin, 0.15" Plastic SOIC
SP8538JS .....	±2.0 .....	-0°C to +70°C .....	8-pin, 0.15" Plastic SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.



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