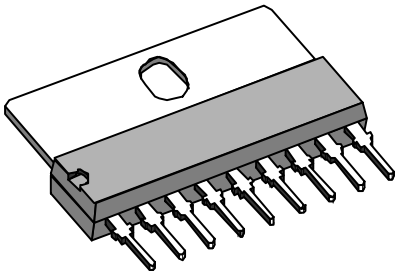
STV8130AD

ADJUSTABLE AND +3.3 V DUAL VOLTAGE REGULATOR WITH DISABLE AND RESET FUNCTIONS

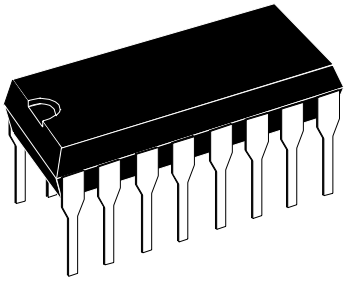
PRELIMINARY DATA

FEATURES

- **Input Voltage Range: 5 V to 18 V**
- **Output Currents up to 750 mA**
- **Fixed Precision Output 1 Voltage: 3.3 V ±2%**
- **Adjustable Output 2 Voltage: 2.8 to 16 V**
- **Output 1 with Reset Function**
- **Output 2 with Disable Function by TTL Input**
- **Short-circuit Protection at both Outputs**
- **Thermal Protection**
- **Low Dropout Voltage**



SIP9 (Plastic Package)
ORDER CODE: STV8130A#



DIP16 (8 + 8)
ORDER CODE: STV8130D#

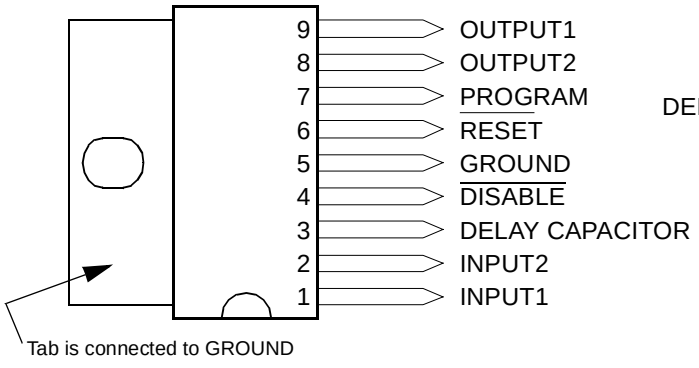
DESCRIPTION

The STV8130A# and STV8130D# are monolithic dual positive voltage regulators designed to provide a fixed precision output voltage of 3.3 V and an adjustable voltage between 2.8 and 16 V for currents up to 750 mA.

An internal reset circuit generates a reset pulse when the voltage of Output 1 drops below the regulated voltage value.

Output 2 can be disabled via the TTL input.

Short-circuit and thermal protections are included.



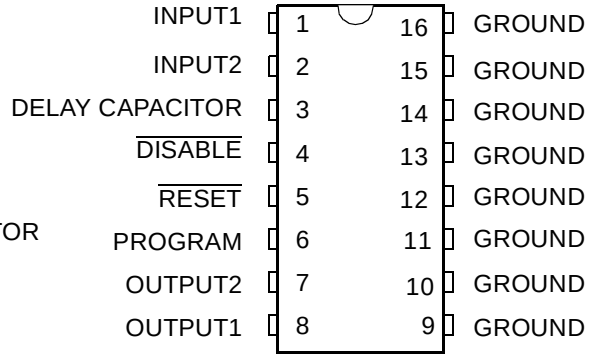


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Figure 1: STV8130A# Block Diagram

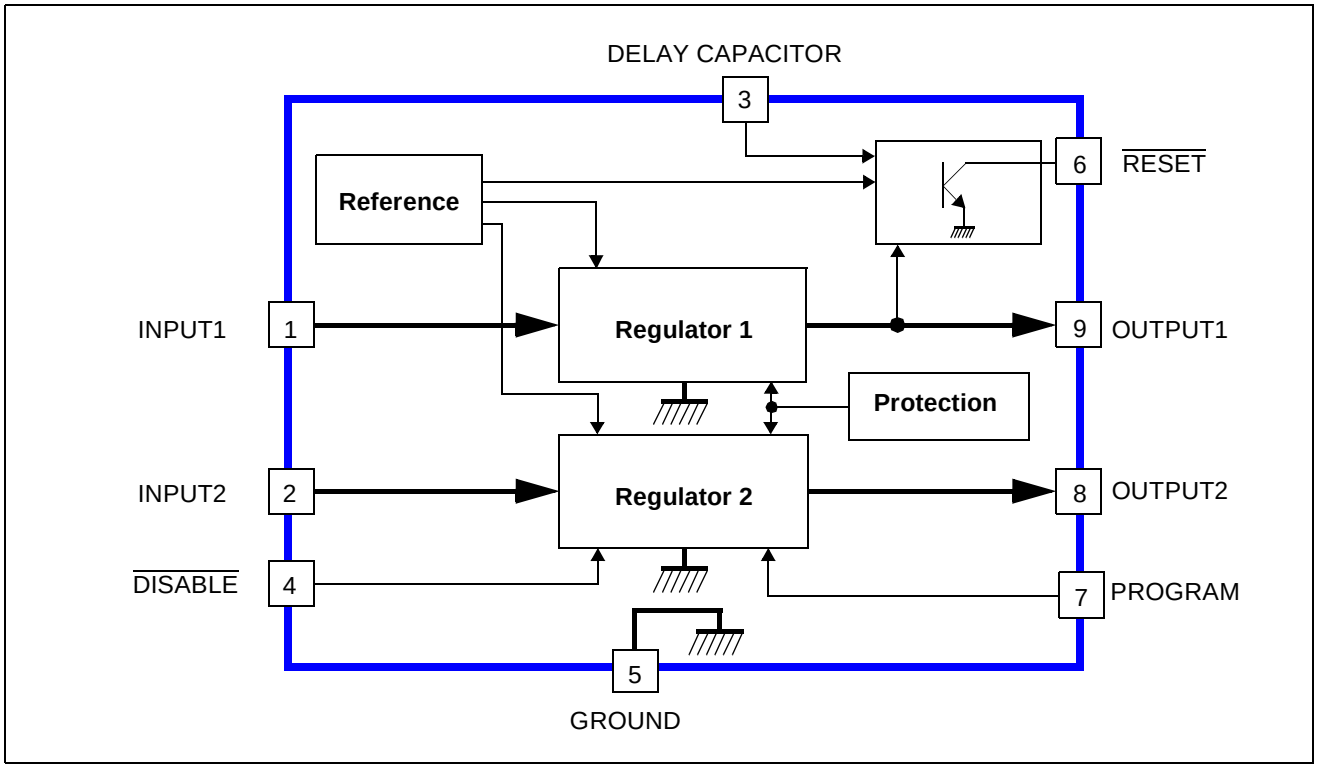
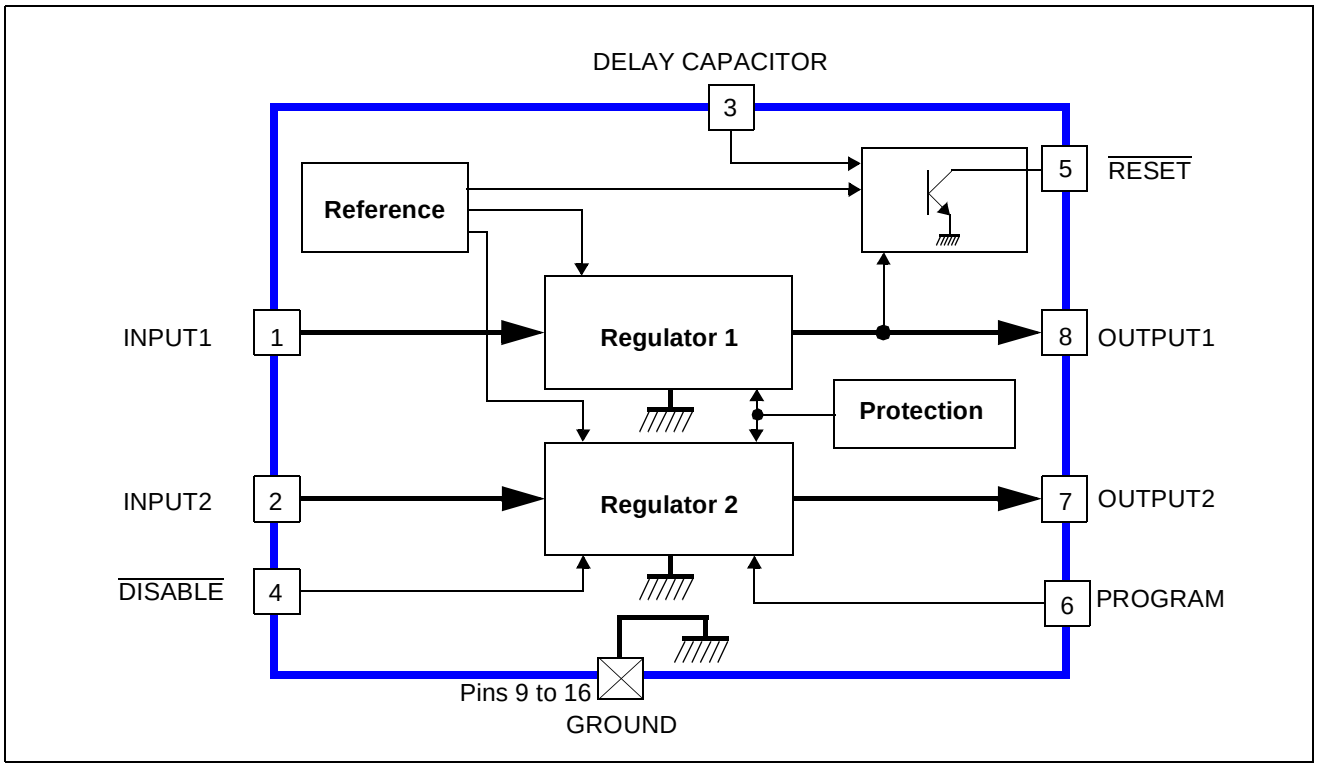


Figure 2: STV8130D# Block Diagram



2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage at pins INPUT1 and INPUT2	20	V
V_{DIS}	Disable Input Voltage at pin $\overline{DISABLE}$	20	V
V_{RST}	Output Voltage at pin $\overline{RESET}$	20	V
$I_{OUT1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	0 to +150	°C

2.2 Thermal Data

Symbol	Parameter		Value	Unit
R_{thJC}	Thermal Resistance (Junction-to-Case)	STV8130A# STV8130D#	9 15	°C/W
R_{thJA}	Thermal Resistance [1] (Junction-to-Ambient)	STV8130A# STV8130D#	50 56	°C/W
T_J	Maximum Recommended Junction Temperature		140	°C
T_{OPER}	Operating Free Air Temperature Range		0 to +70	°C

1. Mounted on board. For more information, refer to Section 5.

2.3 Electrical Characteristics

T_{AMB} = 25° C, V_{IN1} = 7 V, V_{IN2} = 10 V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OUT1}	Output Voltage	I_{OUT1} = 10 mA	3.23	3.30	3.37	V
V_{OUT2}	Output Voltage	I_{OUT2} = 10 mA	2.8		16.0	V
$V_{IO1,2}$	Dropout Voltage	$I_{OUT1,2}$ = 750 mA			1.4	V
$V_{O1,2LI}$	Line Regulation	6 V < V_{IN1} < 12 V 12 V < V_{IN2} < 18 V $I_{OUT1,2}$ = 200 mA			50 100	mV
$V_{O1,2LO}$	Load Regulation	5 mA < I_{OUT1} < 600 mA 5 mA < I_{OUT2} < 600 mA			100 200	mV

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	I_{OUT1} = 10 mA, OUTPUT2 Disabled			2	mA
V_{O1RST}	Reset Threshold Voltage[1]	K = V_{OUT1}, $I_{OUT1} \geq$ 50 mA	K - 0.4	K - 0.25	K - 0.1	V
V_{RTH}	Reset Threshold Hysteresis	See circuit description.	20	50	75	mV
t_{RD}	Reset Pulse Delay	C_e = 100 nF See circuit description.		25		ms
V_{RL}	Saturation Voltage in Reset Condition	$I_{\overline{RESET}}$ = 5 mA			0.4	V
I_{RH}	Leakage Current in Normal Condition	$V_{\overline{RESET}}$ = 10 V			10	µA
$K_{OUT1, 2}$	Output Voltage Thermal Drift	$K_0 = \frac{\Delta V_0 \cdot 10^6}{\Delta T \cdot V_0}$ T_J = 0 to + 125°C		100		ppm/°C
$I_{OUT1,2SC}$	Short Circuit Output Current	V_{IN1} = 7 V, V_{IN2} = 10 V $V_{IN1,2}$ = 16 V[2]			1.6 1.0	A
V_{DISH}	Disable Voltage when pin $\overline{\text{DISABLE}}$ is High (OUTPUT2 active)		2			V
V_{DISL}	Disable Voltage when pin $\overline{\text{DISABLE}}$ is Low (OUTPUT2 disabled)				0.8	V
I_{DIS}	Disable Bias Current	0 V < V_{DIS} < 7 V	-100		2	µA
V_{REF}	Reference Voltage at PROGRAM Pin			2.44		V
T_{JSD}	Junction Temperature for Thermal Shutdown			145		°C

1. This reset signal is activated by a decrease of V_{OUT1} voltage which can be due to an overload of pin OUT1 or by a lack of Input Voltage (V_{IN1}).
2. The output short-circuit currents are tested one channel at time. During a short-circuit, a large consumption of power occurs, but the thermal protection circuit prevents any excessive temperatures. A safe permanent short-circuit protection is only guaranteed for input voltages up to 16 V.

3 CIRCUIT DESCRIPTION

The STV8130A# and STV8130D# are dual-voltage regulators with Reset and Disable functions.

The two regulation parts are supplied from a single voltage reference circuit trimmed by zener zapping during EWS testing. Since the supply voltage of this voltage reference is connected to pin INPUT1 (V_{IN1}), the second regulator will not work if pin INPUT1 is not supplied.

The adjustable voltage of pin OUTPUT2 (V_{OUT2}) is defined by output bridge resistors (R1, R2): the values of these resistors are calculated to obtain, with the targetted value for V_{OUT2}, the reference voltage (V_{REF} = 2.44 V) on the median point connected to pin PROGRAM.

The output stages are designed using a Darlington configuration with a typical dropout voltage of 1.2 V.

The Disable circuit will switch off pin OUTPUT2 if a voltage less than 0.8 V is applied to pin $\overline{\text{DISABLE}}$.

The Reset circuit checks the voltage at pin OUTPUT1. If this voltage drops below V_{OUT1} - 0.25 V (3.05 V Typ.), the "a" comparator (Figure 3) rapidly discharges the external capacitor (Ce) and the reset output immediately switches to low. This drop can be caused by a parasitic loading condition on pin OUTPUT1 or by a too low value of V_{IN} (short powering off). When the voltage at pin OUTPUT1 exceeds V_{OUT1} - 0.2 V (3.1 V Typ.), the V_{Ce} voltage increases linearly to the reference voltage (V_{REF} = 2.44 V) corresponding to a Reset Pulse Delay (t_{RD}) as shown in Figure 4.

$$t_{RD} = \frac{C_e \times 2.44V}{10\mu A}$$

Afterwards, the reset output returns to high. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.84 V).

Figure 3: Reset Diagram

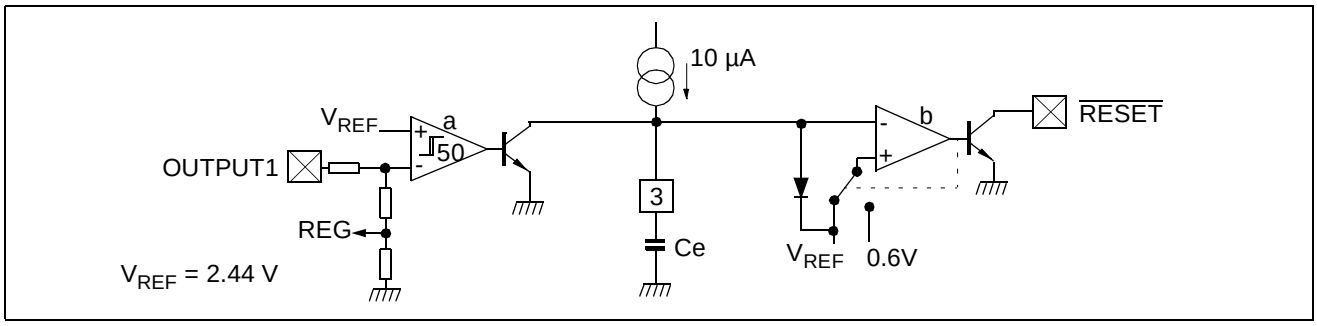
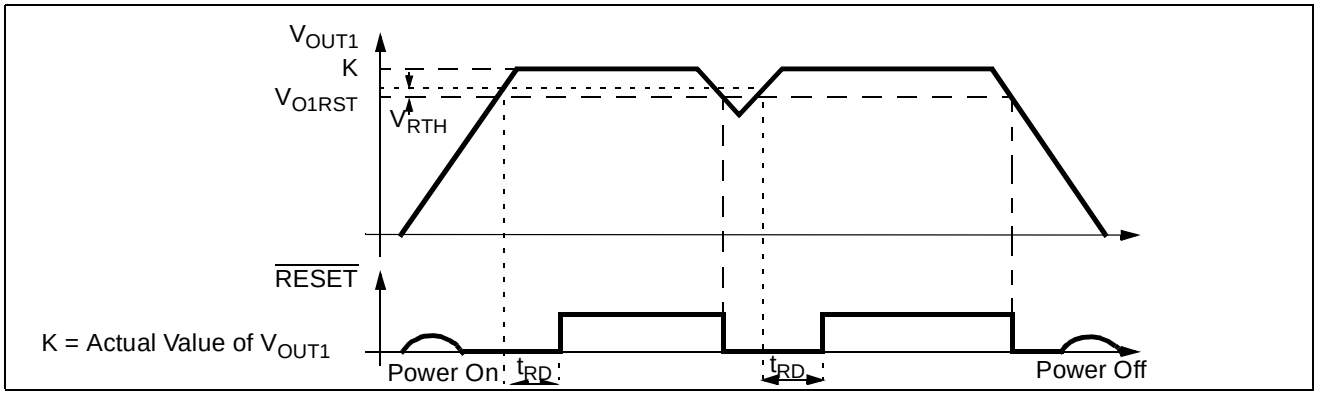


Figure 4: Internal Reset Voltages



4 APPLICATION DIAGRAMS

Figure 5: STV8130A# Typical Application

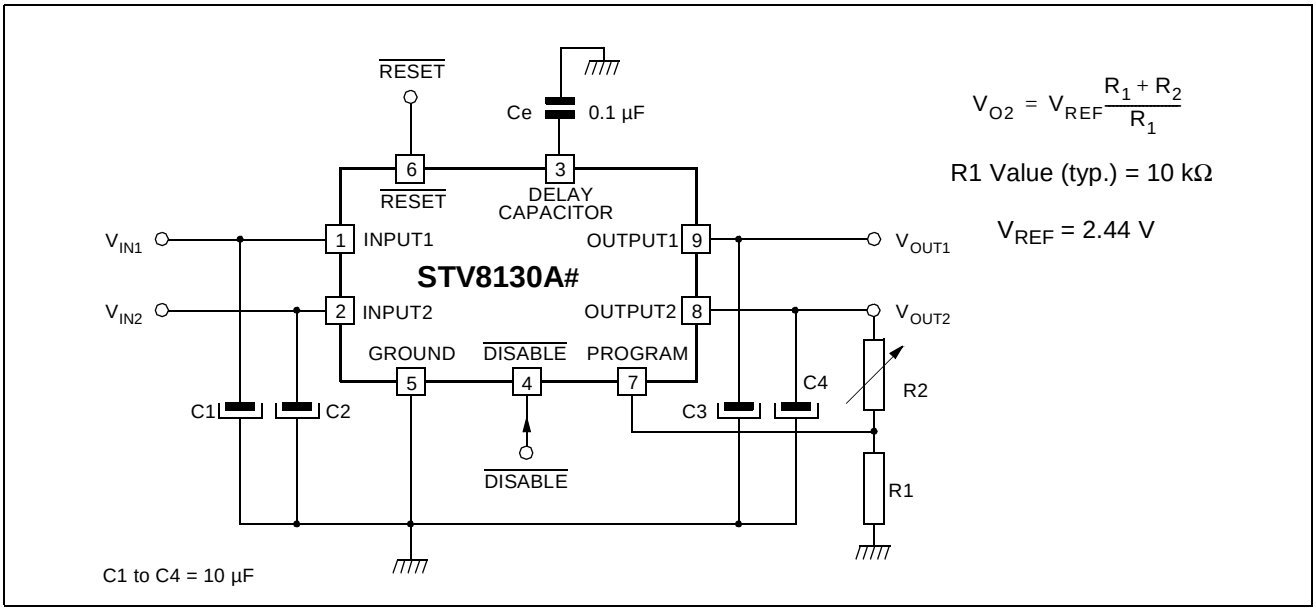
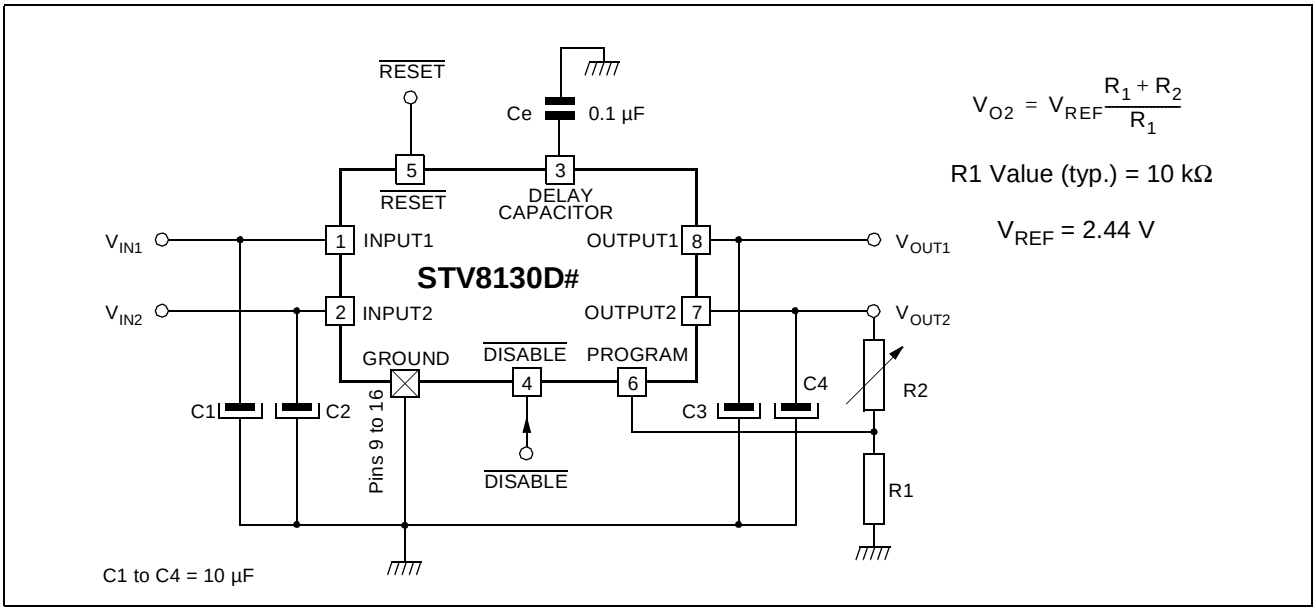


Figure 6: STV8130D# Typical Application



5 POWER DISSIPATION AND LAYOUT INDICATIONS

The power is mainly dissipated by the two device buffers. It can be calculated by the equation:

$$P = (V_{IN1}-V_{OUT1}) \times I_{OUT1} + (V_{IN2}-V_{OUT2}) \times I_{OUT2}$$

The following table lists the different R_{thJA} values of these packages with or without a heat sink and the corresponding maximum power dissipation assuming:

- Maximum Ambient Temperature = 70° C
- Maximum Junction Temperature = 140° C

Device	Heat Sink	R_{thJA} in °C/W	P_{MAX} in W
STV8130A#	No	50	1.4
	Yes	20	3.5
STV8130D#	No	56 to 40	1.25 to 1.75
	Yes	32	2.2

Figure 7: Thermal Resistance (Junction-to-Ambient) of DIP16 Package without Heat Sink

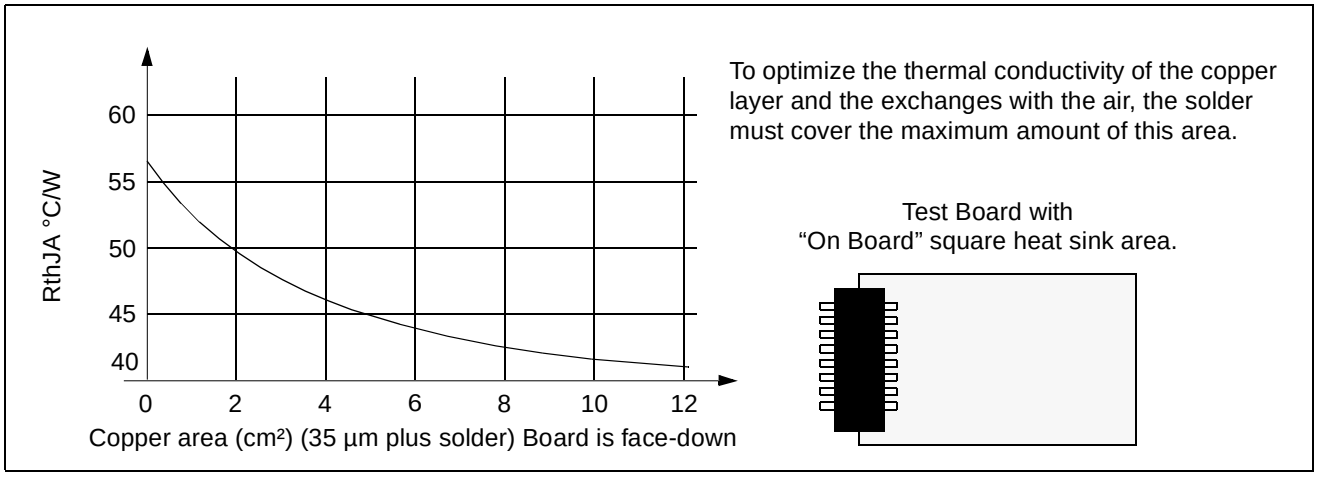
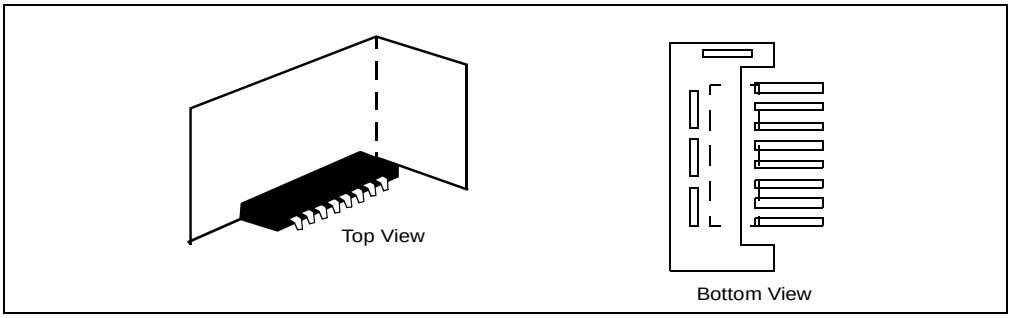
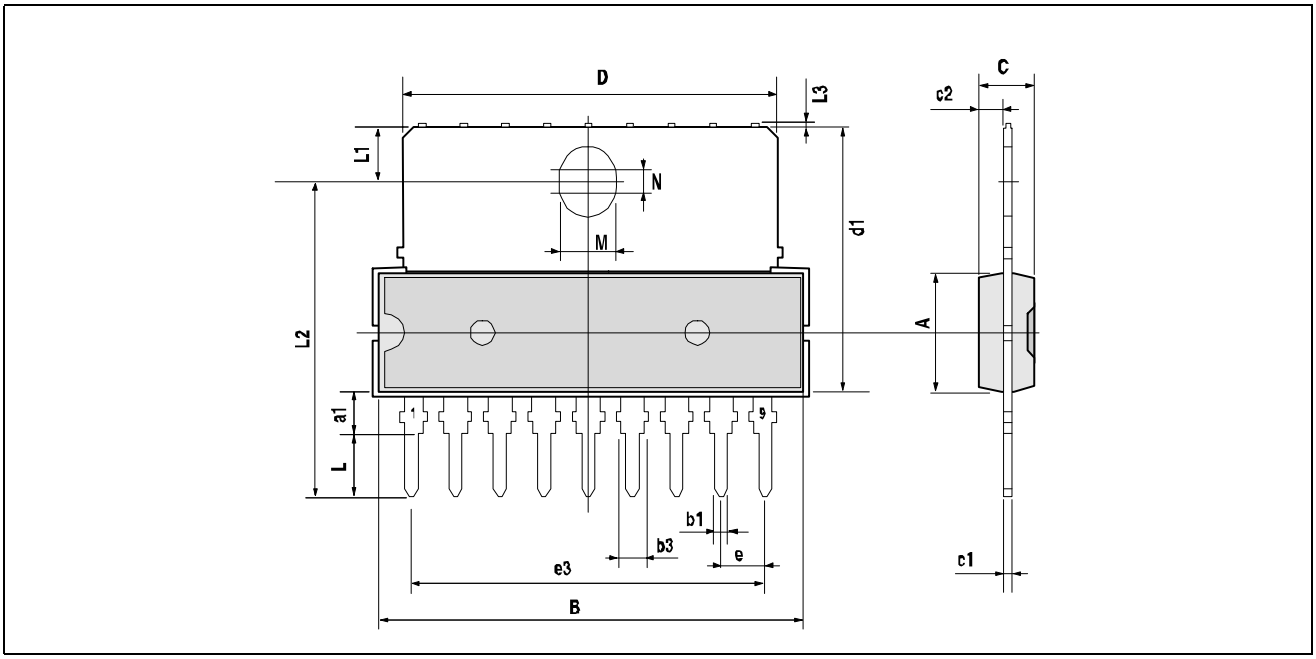


Figure 8: Metal plate mounted near the STV8130D# for heat sinking



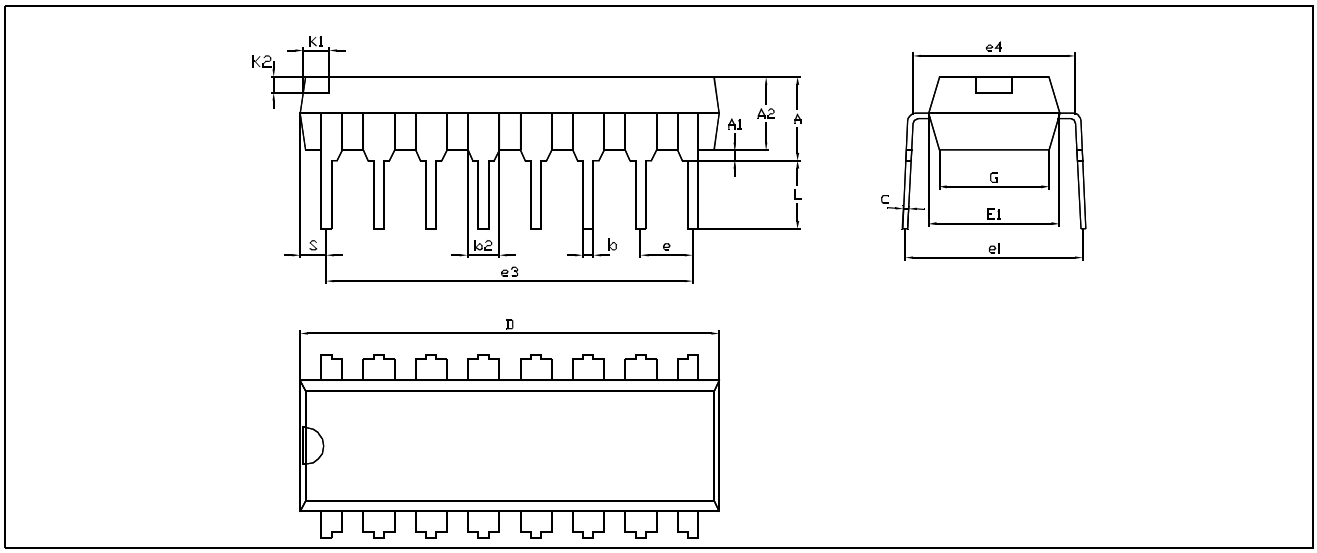
6 PACKAGE MECHANICAL DATA

Figure 9: 9-Pin Plastic Single In Line Package



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			1.122		
L1		3			0.116	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

Figure 10: 16-Pin Plastic Dual In-Line Package, 300-mil Width



Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36		0.56	0.014		0.022
b2		1.52	1.78		0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	18.67	19.18	19.69	0.735	0.755	0.775
e		2.54			0.100	
E1	6.10	6.35	7.11	0.240	0.250	0.280
L	2.92	3.30	3.81	0.115	0.130	0.150

7 REVISION HISTORY

Revision	Main Changes	Date
1.8	General Update; DISABLE pin renamed $\overline{\text{DISABLE}}$ (function remains unchanged).	August 2001
1.9	Thermal Data updated.	September 2001
2.0	Addition of DIP16 package.	September 2001
2.1	Thermal Data updated. Figure 1 and Figure 2 updated.	October 2001
2.2	Order code changed from STV8130A and STV8130D to STV8130A# and STV8130D#. Update of V_{O1RST} values in Chapter 2.3: Electrical Characteristics on page 4.	31 January 2002