IEEE 1284 ECP/EPP Termination Network

Features

- Single chip IEEE 1284 parallel port termination
- 28-pin QSOP package, smallest physical solution
- 17 terminating lines in a single package
- In-system ESD protection to ±8KV, HBM
- In-system ESD protection to ±4KV per IEC 61000-4-2
- Protects downstream devices to 30V
- Lead-free version available

Applications

- ECP/EPP Parallel Port termination
- PC Peripherals
- Notebook and Desktop computers
- Engineering Workstations and Servers

Product Description

California Micro Devices' PACS1284 Parallel Port Termination Network provides a complete integrated solution for the entire IEEE 1284 interface in a single QSOP package.

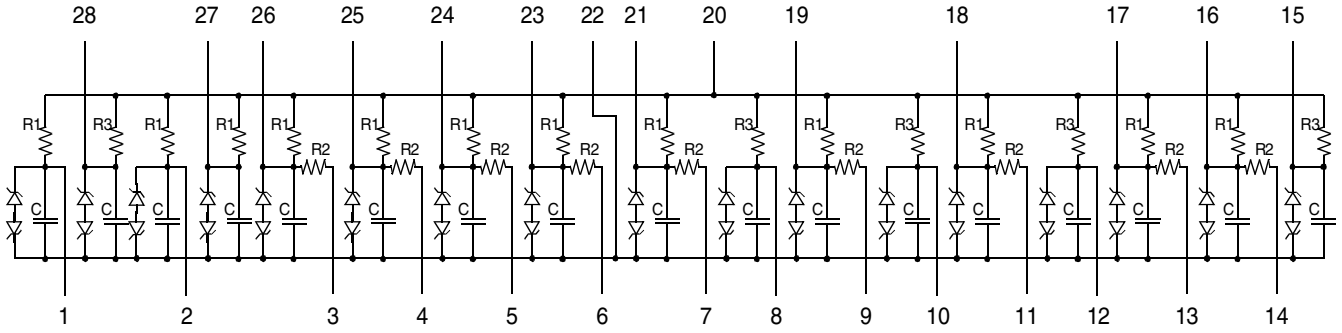
To support the bi-directional transfer data rates of enhanced high-speed parallel ports, the IEEE 1284 Standard recommends a combined termination/pull-up filter network between the driver/receiver and the cable at both ends of the parallel port interface. In addition, government EMC compatibility requirements impose strict filtering requirements on the parallel port. The California Micro Devices PACS1284 addresses all these requirements by providing a seventeen-line IEEE 1284-compliant network in a thin film integrated circuit. The device provides a complete parallel port termination solution for space critical applications by integrating a total of 60 discrete components. In addition, all the I/O pins are ESD protected for contact discharges up to ±4KV per the Human Body Model (HBM), with the output pins having the highest probability of ESD pulse exposure protected to ±8KV (HBM), thereby providing the necessary robustness for the port's application environment.

The PACS1284 is manufactured in a 28-pin QSOP package and is available with optional lead-free finishing.

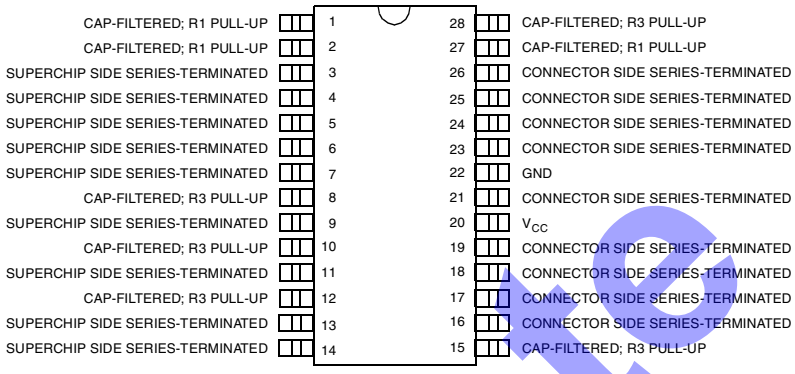
Electrical Schematic

PACS1284-02:	R1 = 2.2kΩ R2 = 33Ω R3 = 2.2kΩ C = 220pF

PACS1284-04:	R1 = 4.7kΩ R2 = 33Ω R3 = 4.7kΩ C = 180pF



PACKAGE / PINOUT DIAGRAM



Note: This drawing is not to scale. 28-pin QSOP

PIN DESCRIPTIONS

PINS	PIN NAME	DESCRIPTION
1, 2, 27	Cap-filtered; R1 Pull-up	IEEE 1284 signals which require no series termination; pull-up is R1 value.
8, 10, 12, 15, 28	Cap-filtered; R3 Pull-up	IEEE 1284 signals which require no series termination; pull-up is R3 value.
3-7, 9,11, 13,14	SuperChip Side Series-terminated	IEEE 1284 signals on the Super I/O Chip side which require series termination.
16-19, 21, 23-26	Connector Side Series-terminated	IEEE 1284 signals on the Parallel Port Connector side which require series termination.
20	V_{CC}	Supply rail for the device
22	GND	Ground reference for the device

Ordering Information

STANDARD VALUES

Product	R1 (Ω)	R2 (Ω)	R3 (Ω)	C (pF)
PACS1284-02	2.2k	33	2.2k	220
PACS1284-04	4.7k	33	4.7k	180

PART NUMBERING INFORMATION

Pins	Package	Standard FInish		Lead-free Finish	
		Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
28	QSOP	PACS1284-02Q	PACS128402Q	PACS1284-02QR	PACS128402QR
28	QSOP	PACS1284-04Q	PACS128404Q	PACS1284-04QR	PACS128404QR

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
V_{CC} Voltage	6.0	V
Input Voltage Range, no clamping	-6.0 to 6.0	V
Storage Temperature Range	-65 to +150	°C
Power Dissipation per Resistor	100	mW
Package Power Dissipation	1.00	W

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
V_{CC} Voltage	5.0	V
Operating Temperature	0 to +70	°C

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
TOL_R	Absolute Resistance Tolerance (R1, R2, R3)	Measured at T_A=25°C			±10	%
TOL_C	Absolute Capacitance Tolerance	Measured at 1MHz, 2.5VDC, T_A=25°C			±20	%
I_{LEAK}	Leakage current to GND	Measured at 5.0VDC, T_A=25°C			1	µA
V_{ESD}	Peak Discharge Voltage at any I/O	Per MIL-STD-883, Method 3015 (HBM); $C_{Discharge}$=100pF; $R_{Discharge}$=1.5KΩ; Notes 2,3	±4			kV
V_{ESD}	In-System ESD Protection	Per MIL-STD-883, Method 3015 (HBM); $C_{Discharge}$=100pF; $R_{Discharge}$=1.5KΩ; Notes 2,3	±8			kV
V_{ESD}	In-System ESD Protection	Per IEC 61000-4-2 Level 2; $C_{Discharge}$=150pF; $R_{Discharge}$=330Ω; Notes 2,3	±4			kV
V_{CL}	Clamping voltage under ESD discharge	ESD applied to connector pin, measured at corresponding input pin; ±8kV discharge, Human Body Model Note 2			±30	V

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.
Note 2: Guaranteed by design.
Note 3: ESD contact discharge between pin 22 (GND) and pins 1, 2, 8, 10, 12, 15, 16, 17, 18, 19, 21, 23, 24, 25, 26, 27, & 28 (one at a time, all other I/O pins open), pin 20=5V; pin 22=GND

Performance Information

Filter Capacitors

Figure 1 shows typical insertion loss graphs for the PACS1284, for Data and Strobe signals. The curves are dependent on the physical location of the filter elements with respect to the ground and V_{CC} terminals of the device.

These graphs are measured in a 50 Ohm environment. The signal is introduced at the series resistor input and the output is measured at the corresponding filter capacitor.

The three plotted lines in Figure 1 depict the following measurements:

- Line labeled "A" is measured between pin 14 (input) and pin 16 (output).
- Line labeled "B" is measured between pin 3 (input) and pin 26 (output).
- Line labeled "C" is measured between pin 6 (input) and pin 23 (output).

The "A" graph depicts “worst case” filter performance, while "C" represents a “best case” situation. Graphs of all other filter elements will fall between these two. (The filter insertion loss was measured using a Hewlett Packard HP8753C Analyzer.)

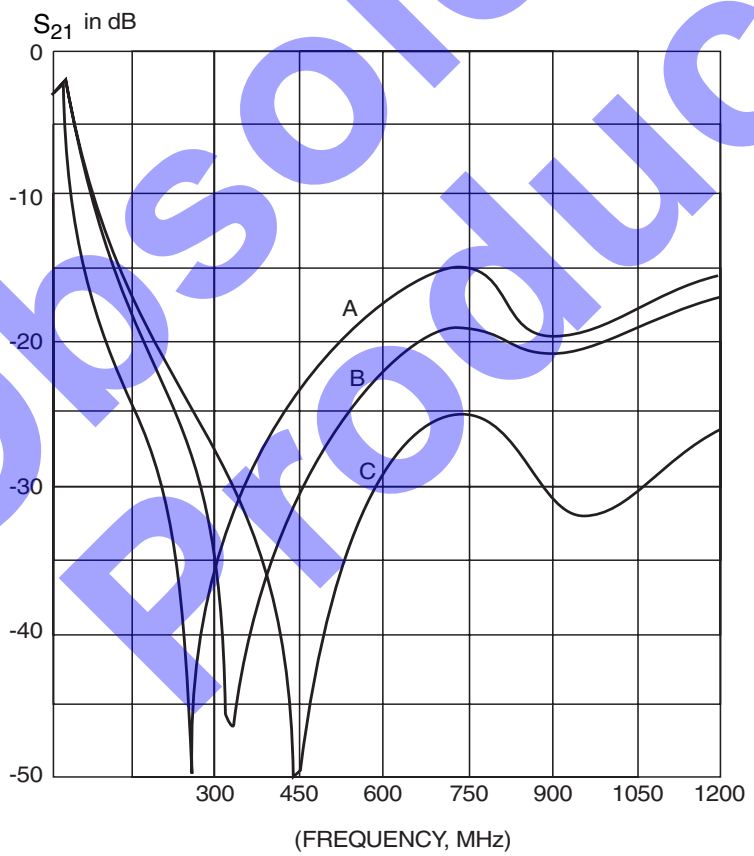


Figure 1. Typical Filter Insertion Loss for PACS1284 (S_{21} in dB, T_A=25°C)

Application Information

Termination Considerations

The IEEE 1284 specification requires both termination and EMI filtering on a total of 17 signal lines. Control and Status lines (8 in total) only require a pull-up resistor and a filter capacitor. The Data lines and Strobe also require a series termination resistor in addition to the pull-up resistors and filter capacitors. See Table 1, in conjunction with the schematic diagram on page 1.

Table 1: IEEE 1284 Termination Requirements

SIGNAL TERMINATION REQUIREMENTS	
Signal Name	**Series Termination**
Data1 - Data8	Yes
Strobe	Yes
Init	Not Required
AutoFeedXT	Not Required
Selectin	Not Required
ACK	Not Required
Busy	Not Required
Paper Empty	Not Required
Select	Not Required
Fault	Not Required

Interfacing to IEEE 1284 Connectors

IEEE 1284 defines three interface connectors:

- 1284 A is a 25-pin DB series connector which is the de facto PC standard for the host connection.
- 1284 B is a 36-pin, 0.085 inch centerline connector used on the peripheral device.
- 1284 C is a new 36-pin, 0.050 inch centerline connector which can be used for both host and peripheral.

Figure 2A shows a possible hook-up between the 1284-A connector on a PC motherboard and the PACS1284, illustrating how the pin configuration of the PACS1284 allows for easy interconnect between the two. The dotted I/O signals of the PACS1284 will typically be connected to a Super I/O chip on the motherboard.

Figure 2B shows a possible hook-up between the 1284-B connector on a peripheral and the PACS1284.

Figure 2C shows a possible hook-up between the 1284-C connector and the PACS1284.

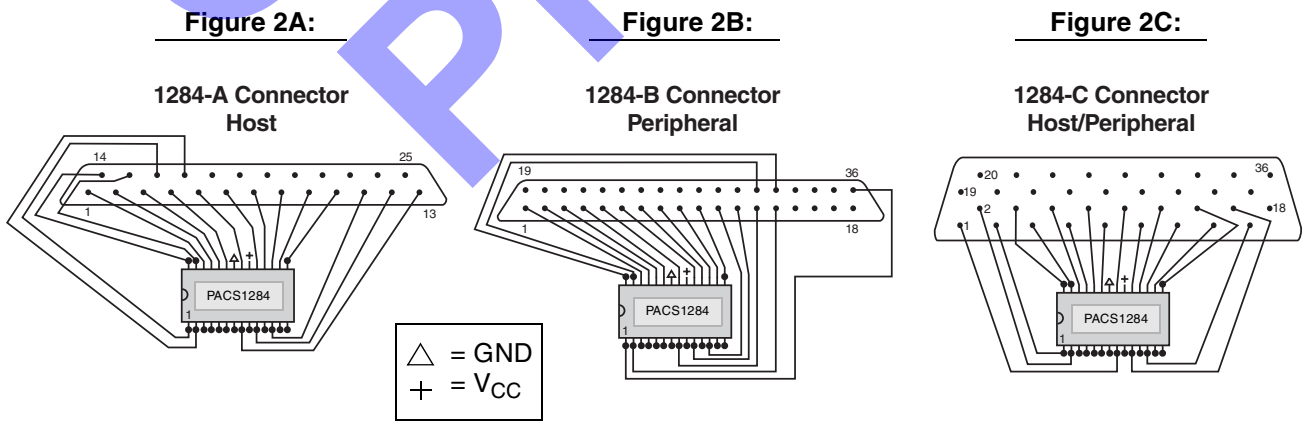


Figure 2. Example Connections of IEEE 1284 Connectors with PACS1284

Application Information (continued)

Table 2 provides the IEEE 1284 signal assignments for the three connectors, and example PACS1284 pin connections.

When connecting a 1284-A host to a 1284-B peripheral, the "Peripheral Logic High" signal is not used. Similarly, when a 1284-A host is connected to a 1284-C peripheral, the "Peripheral Logic High" and "Host Logic High" are not used. These two signals are optionally used to detect a "Power Off" or "Cable Disconnect" state for host and peripheral, respectively.

Table 2: IEEE 1284 Connector Pinouts and PACS1284 Connection Guidelines

PACS1284 PIN TYPE	1284-A 25-PIN DSUB		1284-B 36-PIN CHAMP		1284-C 36-PIN HIGH DENSITY	
	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	STROBE	1	STROBE	1	STROBE	15
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 1	2	Data 1	2	Data 1	6
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 2	3	Data 2	3	Data 2	7
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 3	4	Data 3	4	Data 3	8
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 4	5	Data 4	5	Data 4	9
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 5	6	Data 5	6	Data 5	10
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 6	7	Data 6	7	Data 6	11
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 7	8	Data 7	8	Data 7	12
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 8	9	Data 8	9	Data 8	13
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	ACK	10	ACK	10	ACK	3
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	BUSY	11	BUSY	11	BUSY	1
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	PError	12	PError	12	PError	5
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	Select	13	Select	13	Select	2
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	AUTOFD	14	AUTOFD	14	AUTOFD	17
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	FAULT	15	FAULT	32	FAULT	4
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	INIT	16	INIT	31	INIT	14
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	Selectin	17	Selectin	36	Selectin	16
	Ground	18	Ground	19	Ground	19
	Ground	19	Ground	20	Ground	20
	Ground	20	Ground	21	Ground	21
	Ground	21	Ground	22	Ground	22
	Ground	22	Ground	23	Ground	23
	Ground	23	Ground	24	Ground	24
	Ground	24	Ground	25	Ground	25
	Ground	25	Ground	26	Ground	26
			Ground	27	Ground	27
			Ground	28	Ground	28
			Ground	29	Ground	29
			Ground	30	Ground	30
			Not Defined	33	Ground	31
			Not Defined	34	Ground	32
			Not Defined	35	Ground	33
			Not Defined	15	Ground	34
			Logic Ground	16	Ground	35
			Chassis GND	17	Not Required	36
			Peripheral Logic	18	Host Logic High	18

Mechanical Details

QSOP Mechanical Specifications:

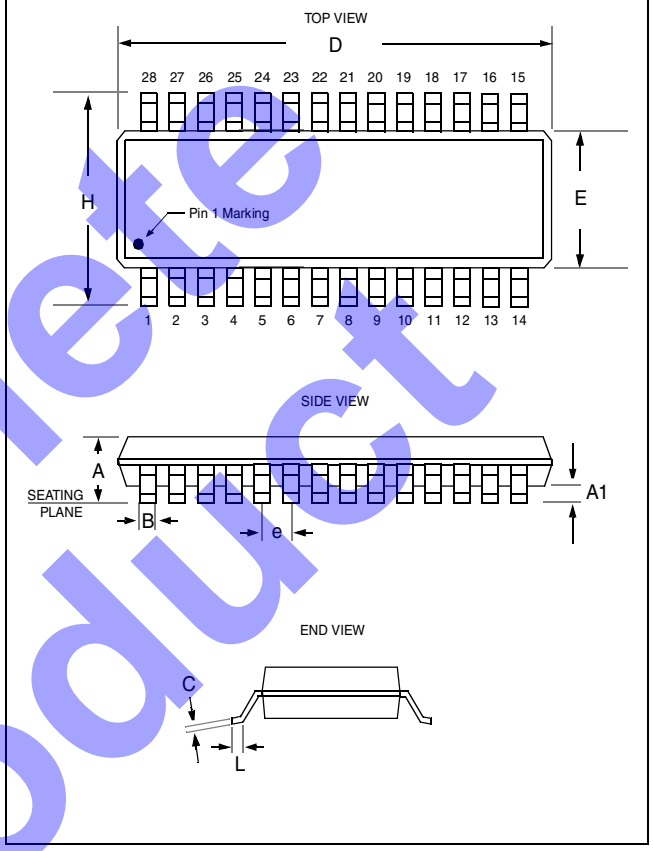
PACS1284 devices are packaged in 28-pin QSOP packages. Dimensions are presented below.

For complete information on the QSOP-28 package, see the California Micro Devices QSOP Package Information document.

PACKAGE DIMENSIONS				
Package	QSOP (JEDEC name is SSOP)			
Pins	28			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.20	0.30	0.008	0.012
C	0.18	0.25	0.007	0.010
D	9.80	9.98	0.386	0.393
E	3.81	3.98	0.150	0.157
e	0.64 BSC		0.025 BSC	
H	5.79	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	50 pieces*			
# per tape and reel	2500 pieces			
Controlling Dimensions: inches				

* This is an approximate amount which may vary.

Mechanical Package Diagrams



Package Dimensions for QSOP-28