

## FlipKY<sup>®</sup>, 1 A


 FlipKY<sup>®</sup>

### FEATURES

- Ultra low  $V_F$  to foot print area
- Low leakage
- Low thermal resistance
- One-fifth footprint of SMA
- Super low profile (< 0.7 mm)
- Available tested on tape and reel
- Small foot print, surface mountable
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Lead (Pb)-free
- Designed and qualified for consumer level


**RoHS**  
COMPLIANT

### PRODUCT SUMMARY

$I_{F(AV)}$	1 A
$V_R$	40 V

### DESCRIPTION

True chip-scale packaging is available from Vishay HPP. The FCSP1H40TR surface mount Schottky rectifier has been designed for applications requiring low forward drop and very small foot prints on PC boards. Typical applications are in disk drives, switching power supplies, converters, freewheeling diodes, battery charging, and reverse battery protection.

The FlipKY<sup>®</sup> package, is one-fifth the footprint of a comparable SMA package and has a profile of less than 0.7 mm. Combined with the low thermal resistance of the die level device, this makes the FlipKY the best device for applications where printed circuit board space is at a premium and in extremely thin application environments such as battery packs, cell phones and PCMCIA cards.

### MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	1.0	A
$V_{RRM}$		40	V
$I_{FSM}$	$t_p = 5 \mu s$ sine	250	A
$V_F$	1.0 Apk, $T_J = 125^\circ C$	0.42	V
$T_J$	Range	- 55 to 150	$^\circ C$

### VOLTAGE RATINGS

PARAMETER	SYMBOL	FCSP1H40TR	UNITS
Maximum DC reverse voltage	$V_R$	40	V
Maximum working peak reverse voltage	$V_{RWM}$		



ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current	$I_{F(AV)}$	50 % duty cycle at $T_{PCB} = 117\text{ °C}$ , rectangular waveform		1.0	A
Maximum peak one cycle non-repetitive surge current at 25 °C	$I_{FSM}$	5 $\mu$ s sine or 3 $\mu$ s rect. pulse	Following any rated load condition and with rated $V_{RRM}$ applied	250	
		10 ms sine or 6 ms rect. pulse		21	
Non-repetitive avalanche energy	$E_{AS}$	$T_J = 25\text{ °C}$ , $I_{AS} = 2.0\text{ A}$ , $L = 5.0\text{ mH}$		10	mJ
Repetitive avalanche current	$I_{AR}$	Current decaying linearly to zero in 1 $\mu$ s Frequency limited by $T_J$ maximum $V_A = 1.5 \times V_R$ typical		2.0	A

ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Maximum forward voltage drop See fig. 1	$V_{FM}^{(1)}$	1 A	$T_J = 25\text{ °C}$	0.48	0.52	V
		2 A		0.54	0.59	
		1 A	$T_J = 125\text{ °C}$	0.38	0.42	
		2 A		0.48	0.52	
Maximum reverse leakage current See fig. 2	$I_{RM}^{(1)}$	$V_R = \text{Rated } V_R$	$T_J = 25\text{ °C}$	3	15	$\mu$ A
		$V_R = 20\text{ V}$		0.5	1	
		$V_R = 10\text{ V}$		0.2	0.5	
		$V_R = 5\text{ V}$		0.15	0.3	
		$V_R = \text{Rated } V_R$	$T_J = 125\text{ °C}$	2.5	4	mA
		$V_R = 20\text{ V}$		0.9	2	
		$V_R = 10\text{ V}$		0.6	1.5	
		$V_R = 5\text{ V}$		0.5	1	
Maximum junction capacitance	$C_T$	$V_R = 5\text{ V}_{DC}$ (test signal range 100 kHz to 1 MHz) 25 °C		-	160	pF
Maximum voltage rate of change	dV/dt	Rated $V_R$		-	10 000	V/ $\mu$ s

**Note**

(1) Pulse width < 300  $\mu$ s, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum junction and storage temperature range	$T_J^{(1)}, T_{Stg}$			- 55 to 150	°C
Typical thermal resistance, junction to PCB	$R_{thJL}^{(2)}$	DC operation		40	°C/W
Maximum thermal resistance, junction to ambient	$R_{thJA}$			62	

**Notes**

(1)  $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$  thermal runaway condition for a diode on its own heatsink

(2) Mounted on 1" square PCB

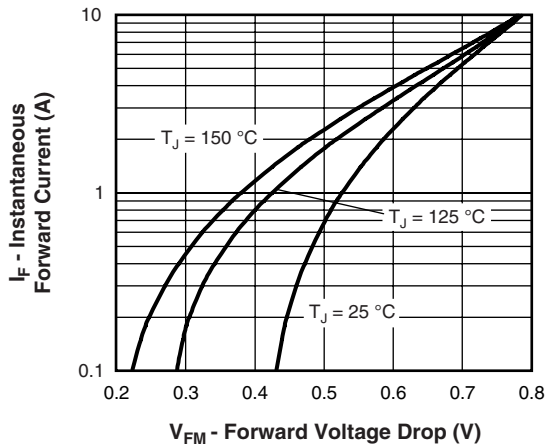


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

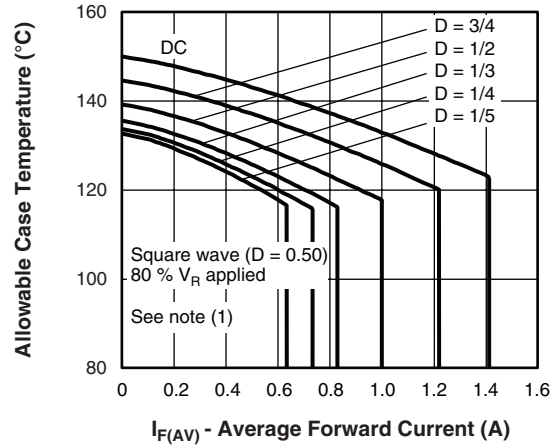


Fig. 4 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

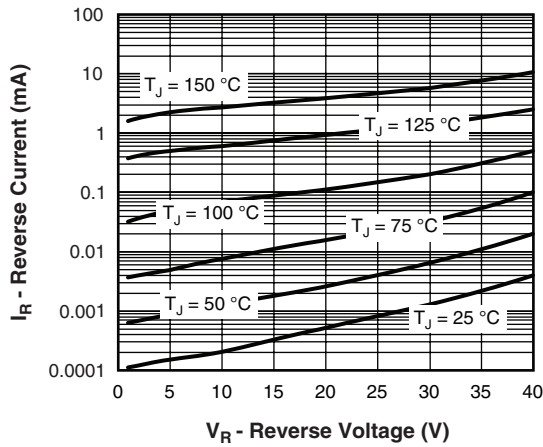


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

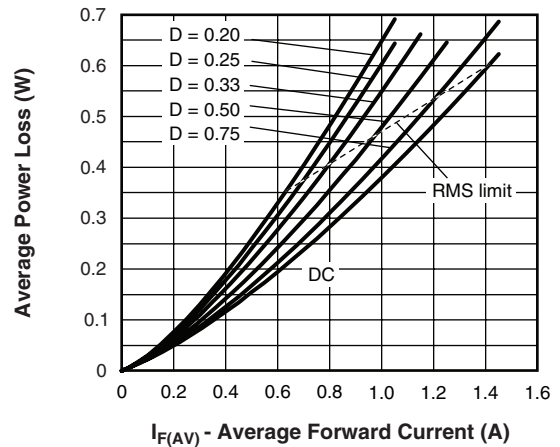


Fig. 5 - Forward Power Loss Characteristics (Per Leg)

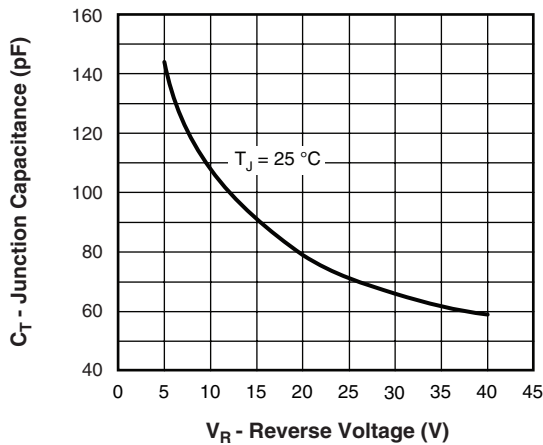


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

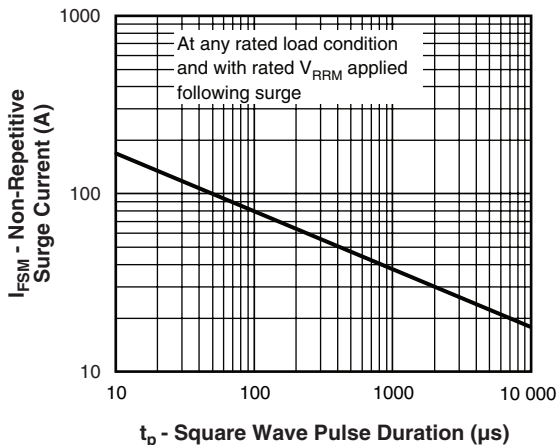


Fig. 6 - Maximum Non-Repulsive Surge Current (Per Leg)

**Note**

(1) Formula used:  $T_C = T_J - (P_d + P_{d_{REV}}) \times R_{thJC}$ ;

$P_d$  = Forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 6);  $P_{d_{REV}}$  = Inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R$  at 80%  $V_R$  applied

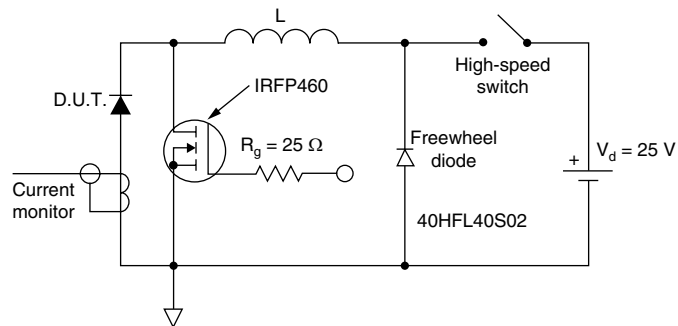


Fig. 7 - Unclamped Inductive Test Circuit

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95052">http://www.vishay.com/doc?95052</a>
Part marking information	<a href="http://www.vishay.com/doc?95281">http://www.vishay.com/doc?95281</a>
Packaging information	<a href="http://www.vishay.com/doc?95062">http://www.vishay.com/doc?95062</a>
SPICE model	<a href="http://www.vishay.com/doc?95292">http://www.vishay.com/doc?95292</a>



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