

November 1996

### Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair For Low-Power Applications from DC to 120MHz
- General-Purpose Use in Signal Processing Systems Operating in the DC to 190MHz Range
- Temperature Compensated Amplifiers
- See Application Note, AN5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

### Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3086	-55 to 125	14 Ld PDIP	E14.3
CA3086M (3086)	-55 to 125	14 Ld SOIC	M14.15
CA3086M96 (3086)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15
CA3086F	-55 to 125	14 Ld CERDIP	F14.3

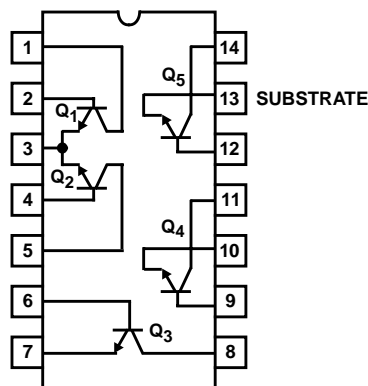
### Description

The CA3086 consists of five general-purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching

### Pinout

CA3086  
(PDIP, CERDIP, SOIC)  
TOP VIEW



# CA3086

## Absolute Maximum Ratings

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, $V_{CEO}$ .....	15V
Collector-to-Base Voltage, $V_{CBO}$ .....	20V
Collector-to-Substrate Voltage, $V_{CIO}$ (Note 1) .....	20V
Emitter-to-Base Voltage, $V_{EBO}$ .....	5V
Collector Current, $I_C$ .....	50mA

## Operating Conditions

Temperature Range .....

-55°C to 125°C

## Thermal Information

Thermal Resistance (Typical, Note 2)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
CERDIP Package .....	150	75
PDIP Package .....	180	N/A
SOIC Package .....	220	N/A
Maximum Power Dissipation (Any one transistor) .....	300mW	
Maximum Junction Temperature (Hermetic Packages) .....	175°C	
Maximum Junction Temperature (Plastic Package) .....	150°C	
Maximum Storage Temperature Range .....	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s) .....	300°C (SOIC - Lead Tips Only)	

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## NOTES:

- The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (Terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications $T_A = 25^\circ\text{C}$ , For Equipment Design

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu\text{A}$ , $I_E = 0$	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\text{mA}$ , $I_B = 0$	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu\text{A}$ , $I_{CI} = 0$	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu\text{A}$ , $I_C = 0$	5	7	-	V
Collector-Cutoff Current (Figure 1)	$I_{CBO}$	$V_{CB} = 10\text{V}$ , $I_E = 0$ ,	-	0.002	100	nA
Collector-Cutoff Current (Figure 2)	$I_{CEO}$	$V_{CE} = 10\text{V}$ , $I_B = 0$ ,	-	(Figure 2)	5	$\mu\text{A}$
DC Forward-Current Transfer Ratio (Figure 3)	$h_{FE}$	$V_{CE} = 3\text{V}$ , $I_C = 1\text{mA}$	40	100	-	

## Electrical Specifications $T_A = 25^\circ\text{C}$ , Typical Values Intended Only for Design Guidance

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS	
DC Forward-Current Transfer Ratio (Figure 3)	$h_{FE}$	$V_{CE} = 3\text{V}$	$I_C = 10\text{mA}$	100	
			$I_C = 10\mu\text{A}$	54	
Base-to-Emitter Voltage (Figure 4)	$V_{BE}$	$V_{CE} = 3\text{V}$	$I_E = 1\text{mA}$	0.715	V
			$I_E = 10\text{mA}$	0.800	V
$V_{BE}$ Temperature Coefficient (Figure 5)	$\Delta V_{BE}/\Delta T$	$V_{CE} = 3\text{V}$ , $I_C = 1\text{mA}$	-1.9	mV/°C	
Collector-to-Emitter Saturation Voltage	$V_{CE\text{ SAT}}$	$I_B = 1\text{mA}$ , $I_C = 10\text{mA}$	0.23	V	
Noise Figure (Low Frequency)	NF	$f = 1\text{kHz}$ , $V_{CE} = 3\text{V}$ , $I_C = 100\mu\text{A}$ , $R_S = 1\text{k}\Omega$	3.25	dB	

**Electrical Specifications**  $T_A = 25^{\circ}\text{C}$ , Typical Values Intended Only for Design Guidance (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:				
Forward Current-Transfer Ratio (Figure 6)	$h_{FE}$	$f = 1\text{kHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$	100	-
Short-Circuit Input Impedance (Figure 6)	$h_{iE}$		3.5	$\text{k}\Omega$
Open-Circuit Output Impedance (Figure 6)	$h_{oE}$		15.6	$\mu\text{S}$
Open-Circuit Reverse-Voltage Transfer Ratio (Figure 6)	$h_{rE}$		$1.8 \times 10^{-4}$	-
Admittance Characteristics:				
Forward Transfer Admittance (Figure 7)	$Y_{FE}$	$f = 1\text{MHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$	$31 - j1.5$	mS
Input Admittance (Figure 8)	$Y_{iE}$		$0.3 + j0.04$	mS
Output Admittance (Figure 9)	$Y_{oE}$		$0.001 + j0.03$	mS
Reverse Transfer Admittance (Figure 10)	$Y_{rE}$		See Figure 10	-
Gain-Bandwidth Product (Figure 11)	$f_T$	$V_{CE} = 3\text{V}, I_C = 3\text{mA}$	550	MHz
Emitter-to-Base Capacitance	$C_{EBO}$	$V_{EB} = 3\text{V}, I_E = 0$	0.6	pF
Collector-to-Base Capacitance	$C_{CBO}$	$V_{CB} = 3\text{V}, I_C = 0$	0.58	pF
Collector-to-Substrate Capacitance	$C_{CIO}$	$V_{CI} = 3\text{V}, I_C = 0$	2.8	pF

**Typical Performance Curves**

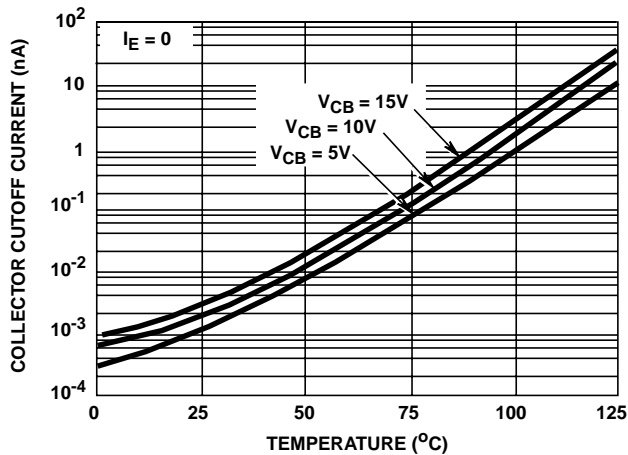


FIGURE 1.  $I_{CBO}$  vs TEMPERATURE

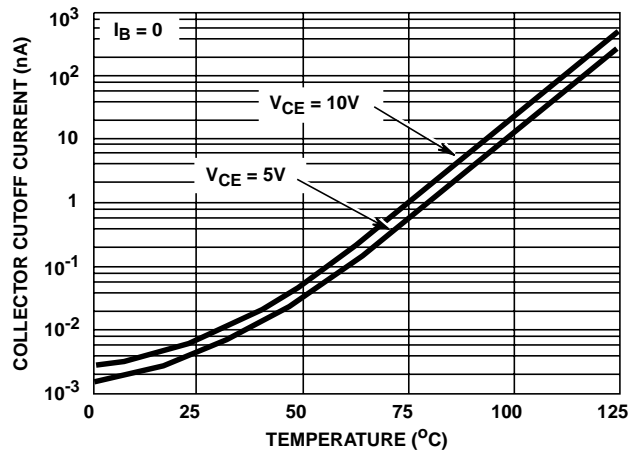


FIGURE 2.  $I_{CEO}$  vs TEMPERATURE

Typical Performance Curves (Continued)

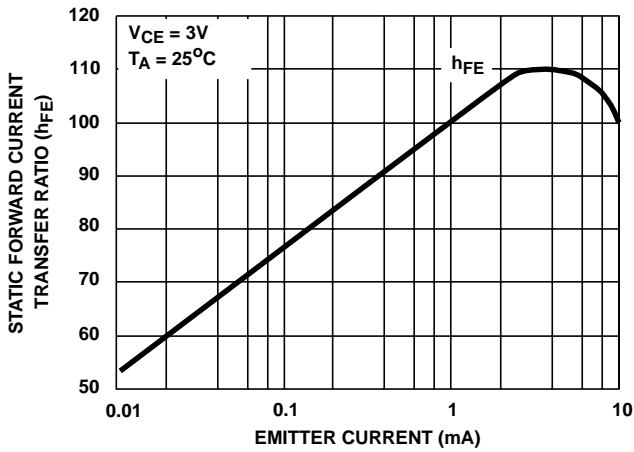


FIGURE 3.  $h_{FE}$  vs  $I_E$

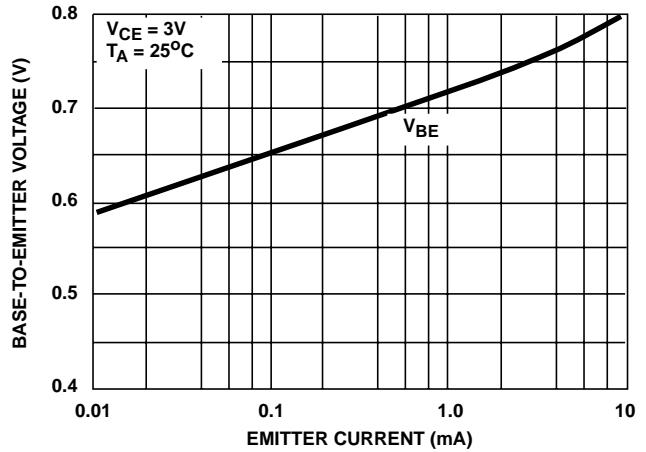


FIGURE 4.  $V_{BE}$  vs  $I_E$

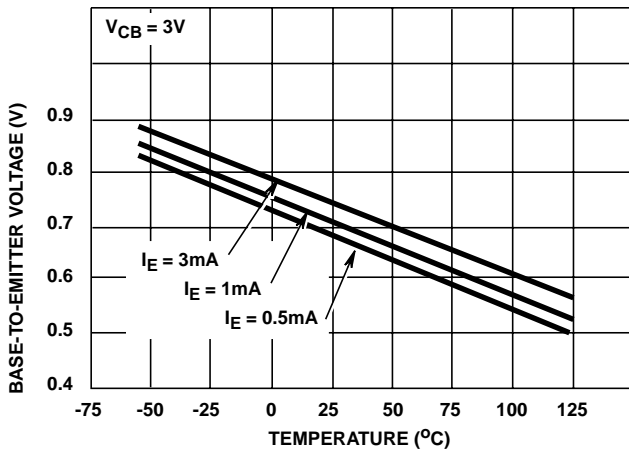


FIGURE 5.  $V_{BE}$  vs TEMPERATURE

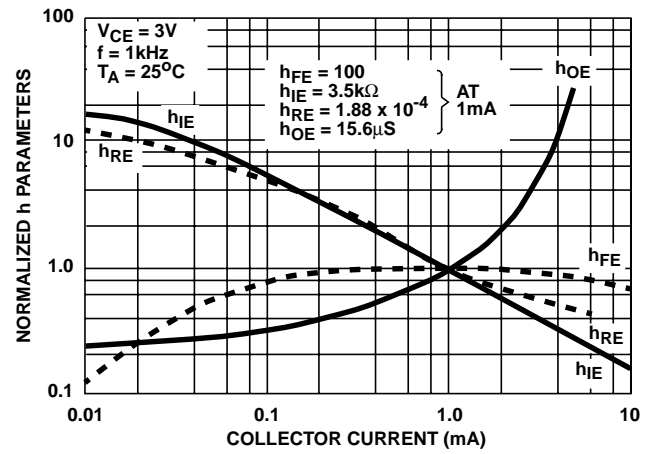


FIGURE 6. NORMALIZED  $h_{FE}$ ,  $h_{IE}$ ,  $h_{RE}$ ,  $h_{OE}$  vs  $I_C$

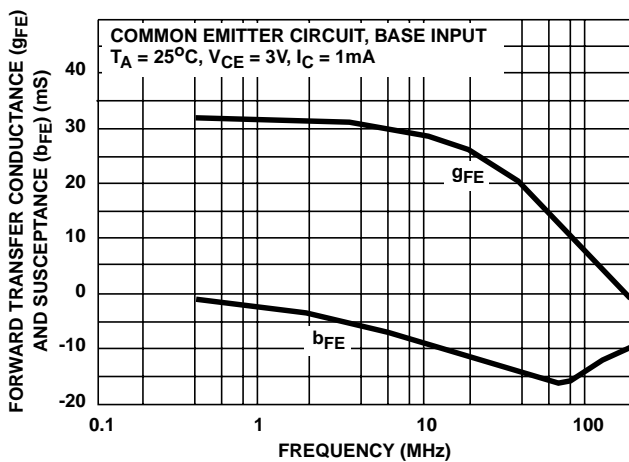


FIGURE 7.  $y_{FE}$  vs FREQUENCY

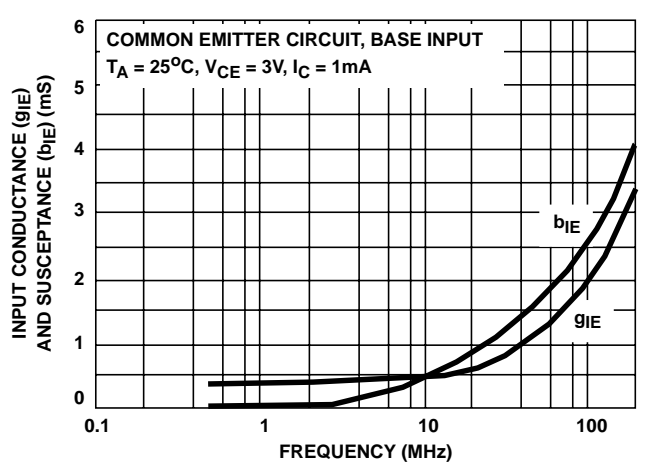
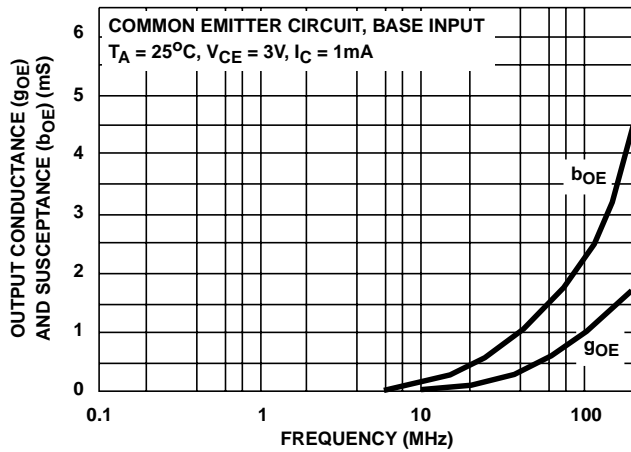
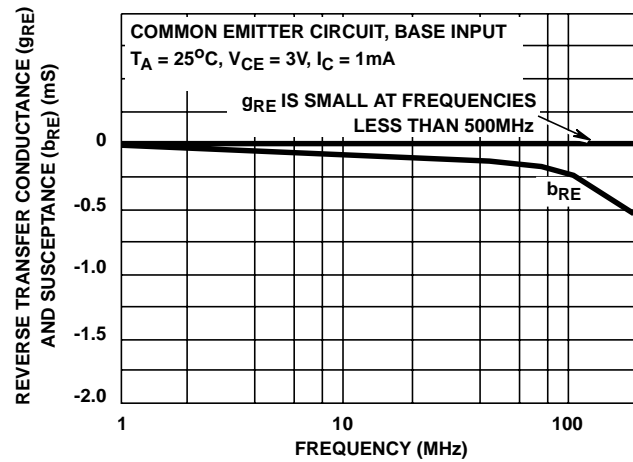
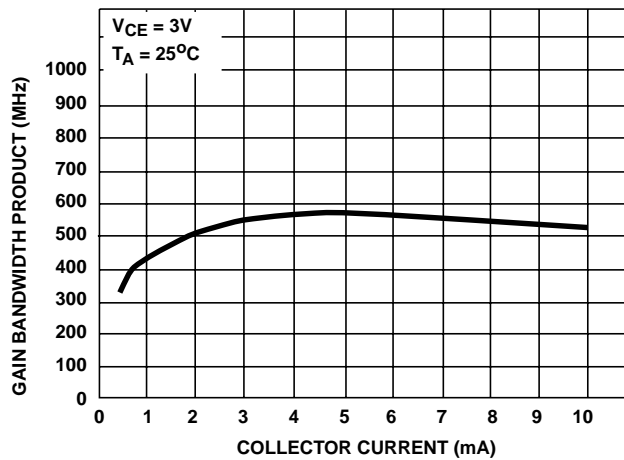


FIGURE 8.  $y_{IE}$  vs FREQUENCY

## Typical Performance Curves (Continued)

FIGURE 9.  $y_{OE}$  vs FREQUENCYFIGURE 10.  $y_{RE}$  vs FREQUENCYFIGURE 11.  $f_T$  vs  $I_C$ 

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