XC61C Series

ETR0201_006

Low Voltage Detectors (V_{DF}= 0.8V～1.5V)
Standard Voltage Detectors (V_{DF} 1.6V～6.0V)

■GENERAL DESCRIPTION

The XC61C series are highly precise, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies.
Detect voltage is extremely accurate with minimal temperature drift.
Both CMOS and N-channel open drain output configurations are available.

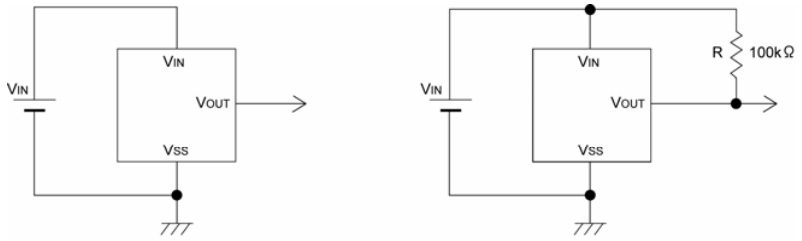
■APPLICATIONS

- ●Microprocessor reset circuitry
- ●Memory battery back-up circuits
- ●Power-on reset circuits
- ●Power failure detection
- ●System battery life and charge voltage monitors

■FEATURES

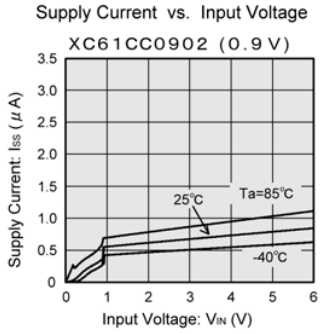
Highly Accurate : ± 2%
(Low Voltage VD: 0.8V~1.5V)
(Standard Voltage VD: 1.6V~6.0V)
± 1%
(Standard Voltage VD: 2.6V~5.0V)
Low Power Consumption : 0.7μA (TYP.) [VIN=1.5V]
Detect Voltage Range : 0.8V ~ 6.0V in 100mV increments
Operating Voltage Range : 0.7V ~ 6.0V (Low Voltage)
0.7V～10.0V (Standard Voltage)
Detect Voltage Temperature Characteristics
: ±100ppm/℃ (TYP.) @Ta=25℃
Output Configuration : N-channel open drain or CMOS
CMOS
Ultra Small Packages : SSOT-24 (150mW)
SOT-23 (150mW)
SOT-89 (500mW)
TO-92 (300mW)

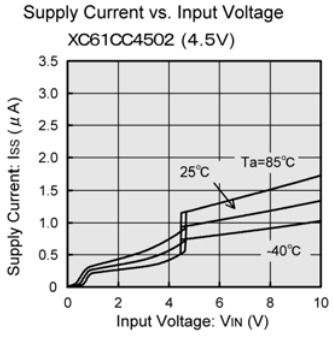
■TYPICAL APPLICATION CIRCUITS



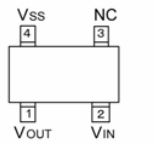
CMOS Output　　N-ch Open Drain Output

■TYPICAL PERFORMANCE CHARACTERISTICS

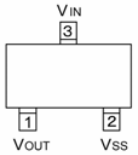




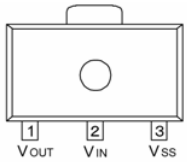
■PIN CONFIGURATION



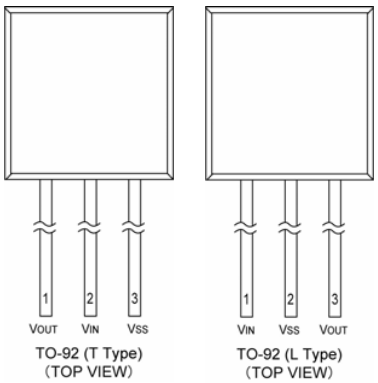
SSOT-24(SC-82)
(TOP VIEW)



SOT-23
(TOP VIEW)



SOT-89
(TOP VIEW)



TO-92 (T Type)
(TOP VIEW)

TO-92 (L Type)
(TOP VIEW)

■PIN ASSIGNMENT

PIN NUMBER					PIN NAME	FUNCTION
SSOT-24	SOT-23	SOT-89	TO-92 (T)	TO-92 (L)		
2	3	2	2	1	VIN	Supply Voltage
4	2	3	3	2	VSS	Ground
1	1	1	1	3	VOUT	Output
3	-	-	-	-	NC	No Connection

■PRODUCT CLASSIFICATION

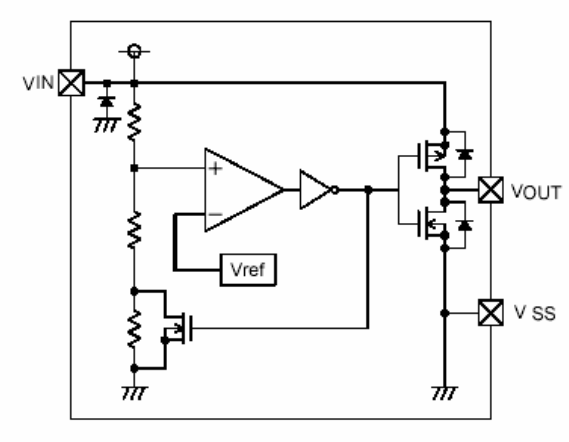
●Ordering Information

XC61C①②③④⑤⑥⑦

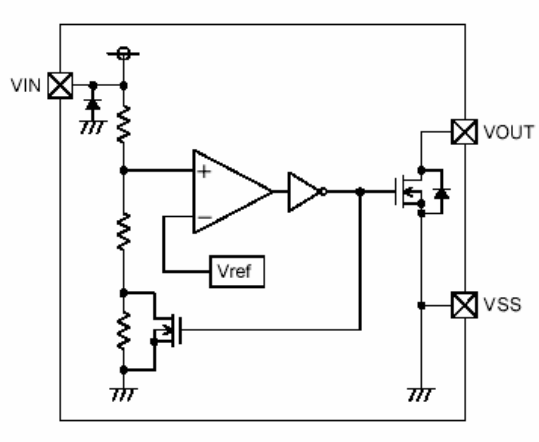
DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Output Configuration	C	: CMOS output
		N	: N-ch open drain output
② ③	Detect Voltage	08 ~ 60	: e.g.0.9V → ②0, ③9
			: e.g.1.5V → ②1, ③5
④	Output Delay	0	: No delay
⑤	Detect Accuracy	1	: Within ±1%
		2	: Within ±2%
⑥	Package	N	: SSOT-24 (SC-82)
		M	: SOT-23
		P	: SOT-89
		T	: TO-92 (Standard)
		L	: TO-92 (Custom pin configuration)
⑦	Device Orientation	R	: Embossed tape, standard feed
		L	: Embossed tape, reverse feed
		H	: Paper type (TO-92)
		B	: Bag (TO-92)

■BLOCK DIAGRAMS

(1) CMOS Output



(2) N-ch Open Drain Output



■ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage	*1	V_{IN}	9.0	V
	*2		12.0	
Output Current		I_{OUT}	50	mA
Output Voltage	CMOS	V_{OUT}	V_{SS} -0.3 ~ V_{IN} +0.3	V
	N-ch Open Drain Output *1		V_{SS} -0.3 ~ 9.0	
	N-ch Open Drain Output *2		V_{SS} -0.3 ~ 12.0	
Power Dissipation	SSOT-24	Pd	150	mW
	SOT-23		150	
	SOT-89		500	
	TO-92		300	
Operating Temperature Range		Topr	-40～+85	°C
Storage Temperature Range		Tstg	-40～+125	°C

*1: Low voltage: $V_{DF(T)}$=0.8V~1.5V
*2: Standard voltage: $V_{DF(T)}$=1.6V~6.0V

■ELECTRICAL CHARACTERISTICS

$V_{DF\ (T)}$ = 0.8V to 6.0V ± 2%

$V_{DF\ (T)}$ = 2.6V to 5.0V ± 1%

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS	CIRCUITS
Detect Voltage	V_{DF}	$V_{DF(T)}$=0.8V~1.5V *1 $V_{DF(T)}$=1.6V~6.0V *2		$V_{DF(T)}$ x 0.98	$V_{DF(T)}$	$V_{DF(T)}$ x 1.02	V	1
		$V_{DF(T)}$=2.6V~5.0V *2		$V_{DF(T)}$ x 0.99	$V_{DF(T)}$	$V_{DF(T)}$ x 1.01	V	1
Hysteresis Range	V_{HYS}			V_{DF} x 0.02	V_{DF} x 0.05	V_{DF} x 0.08	V	1
Supply Current	I_{SS}		V_{IN} = 1.5V	-	0.7	2.3	μA	2
			V_{IN} = 2.0V	-	0.8	2.7		
			V_{IN} = 3.0V	-	0.9	3.0		
			V_{IN} = 4.0V	-	1.0	3.2		
			V_{IN} = 5.0V	-	1.1	3.6		
Operating Voltage *1	V_{IN}	$V_{DF(T)}$ = 0.8V to 1.5V		0.7	-	6.0	V	1
Operating Voltage *2		$V_{DF(T)}$ = 1.6V to 6.0V		0.7	-	10.0		
Output Current *1	I_{OUT}	N-ch V_{DS} = 0.5V	V_{IN} = 0.7V	0.10	0.80	-	mA	3
			V_{IN} = 1.0V	0.85	2.70	-		
		CMOS, P-ch V_{DS} = 2.1V	V_{IN} = 6.0V	-	-7.5	-1.5		4
Output Current *2		N-ch V_{DS} = 0.5V	V_{IN} = 1.0V	1.0	2.2	-		3
			V_{IN} = 2.0V	3.0	7.7	-		
			V_{IN} = 3.0V	5.0	10.1	-		
			V_{IN} = 4.0V	6.0	11.5	-		
			V_{IN} = 5.0V	7.0	13.0	-		
		CMOS, P-ch V_{DS} = 2.1V	V_{IN} = 8.0V	-	-10.0	-2.0		4
Leak Current	I_{leak}	V_{IN}=6.0V, V_{OUT}=6.0V*1	CMOS	-	10	-	nA	3
		V_{IN}=10.0V, V_{OUT}=10.0V*2	N-ch Open Drain	-	10	100		
Temperature Characteristics	$\frac{\Delta V_{DF}}{\Delta Topr \cdot V_{DF}}$	-40℃ ≦ Topr ≦ 85℃		-	±100	-	ppm/℃	-
Delay Time (V_{DR}→V_{OUT} inversion)	tDLY	Inverts from V_{DR} to V_{OUT}		-	0.03	0.20	ms	5

NOTE:
*1: Low Voltage: $V_{DF(T)}$=0.8V~1.5V
*2: Standard Voltage: $V_{DF(T)}$=1.6V~6.0V
$V_{DF\ (T)}$: Setting detect voltage
Release Voltage: V_{DR} = V_{DF} + V_{HYS}

■OPERATIONAL EXPLANATION

(Especially prepared for CMOS output products)

① When input voltage (V_{IN}) rises above detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to V_{IN}.
(A condition of high impedance exists with N-ch open drain output configurations.)

② When input voltage (V_{IN}) falls below detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to the ground voltage (V_{SS}) level.

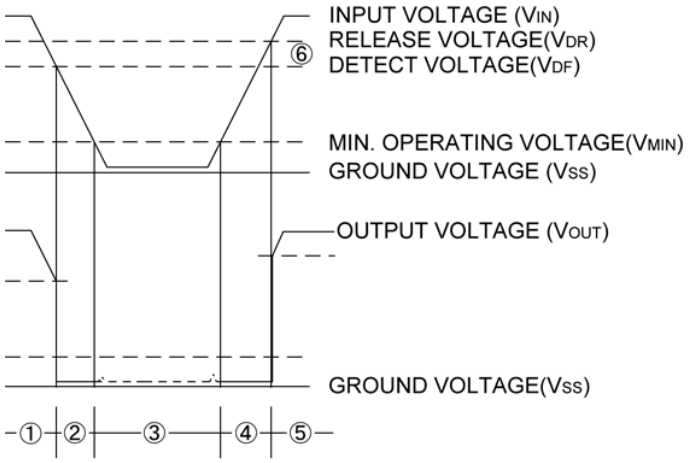
③ When input voltage (V_{IN}) falls to a level below that of the minimum operating voltage (V_{MIN}), output will become unstable. In this condition, V_{IN} will equal the pulled-up output (should output be pulled-up.)

④ When input voltage (V_{IN}) rises above the ground voltage (V_{SS}) level, output will be unstable at levels below the minimum operating voltage (V_{MIN}). Between the V_{MIN} and detect release voltage (V_{DR}) levels, the ground voltage (V_{SS}) level will be maintained.

⑤ When input voltage (V_{IN}) rises above detect release voltage (V_{DR}), output voltage (V_{OUT}) will be equal to V_{IN}.
(A condition of high impedance exists with N-ch open drain output configurations.)

⑥ The difference between V_{DR} and V_{DF} represents the hysteresis range.

●Timing Chart



■NOTES ON USE

1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.
2. When a resistor is connected between the VIN pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at RIN if load current (IOUT) exists. (refer to the Oscillation Description (1) below)
3. When a resistor is connected between the VIN pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (IOUT) does not exist. (refer to the Oscillation Description (2) below)
4. With a resistor connected between the VIN pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the VIN pin.
5. In order to stabilize the IC's operations, please ensure that VIN pin's input frequency's rise and fall times are more than several μ sec / V.
6. Please use N-ch open drains configuration, when a resistor RIN is connected between the VIN pin and power source. In such cases, please ensure that RIN is less than 10kΩ and that C is more than 0.1μF.

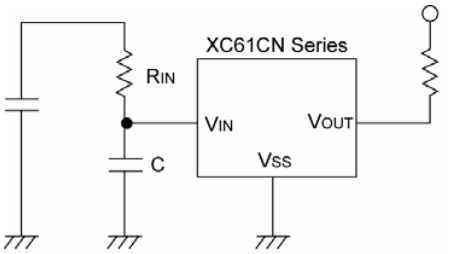


Figure 1: Circuit using an input resistor

●Oscillation Description

(1) Output current oscillation with the CMOS output configuration

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (IOUT) will flow at RL. Because a voltage drop (RIN x IOUT) is produced at the RIN resistor, located between the input (IN) and the VIN pin, the load current will flow via the IC's VIN pin. The voltage drop will also lead to a fall in the voltage level at the VIN pin. When the VIN pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at RIN will disappear, the voltage level at the VIN pin will rise and release operations will begin over again.

Oscillation may occur with this " release - detect - release " repetition.

Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Oscillation as a result of through current

Since the XC61C series are CMOS IC s, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (RIN) during release voltage operations. (refer to Figure 3)

Since hysteresis exists during detect operations, oscillation is unlikely to occur.

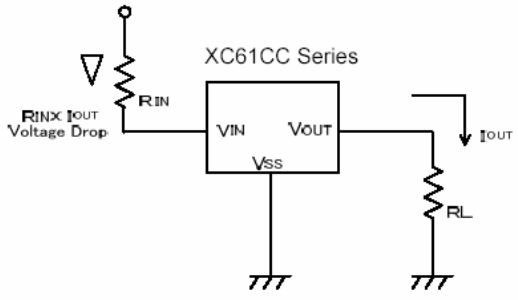


Figure 2: Oscillation in relation to output current

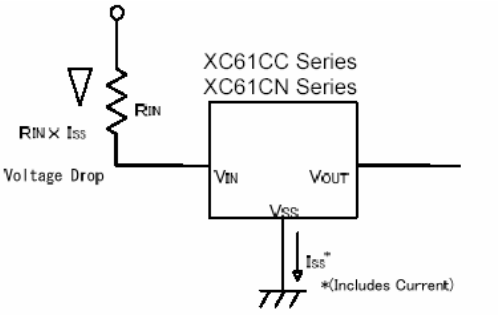
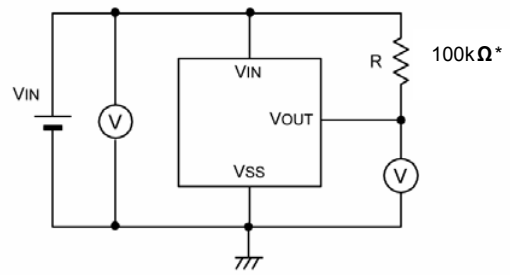


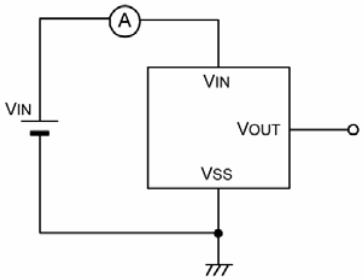
Figure 3: Oscillation in relation to through current

■ TEST CIRCUITS

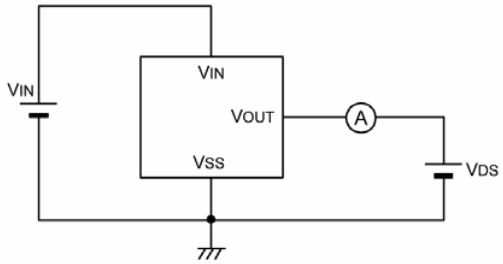
Circuit 1



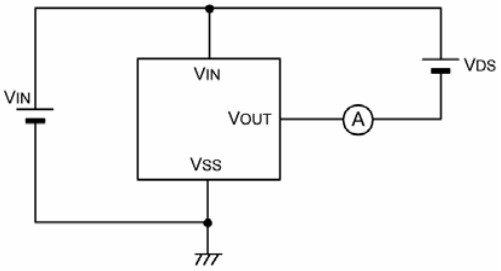
Circuit 2



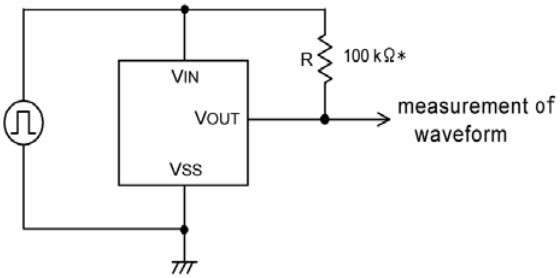
Circuit 3



Circuit 4



Circuit 5

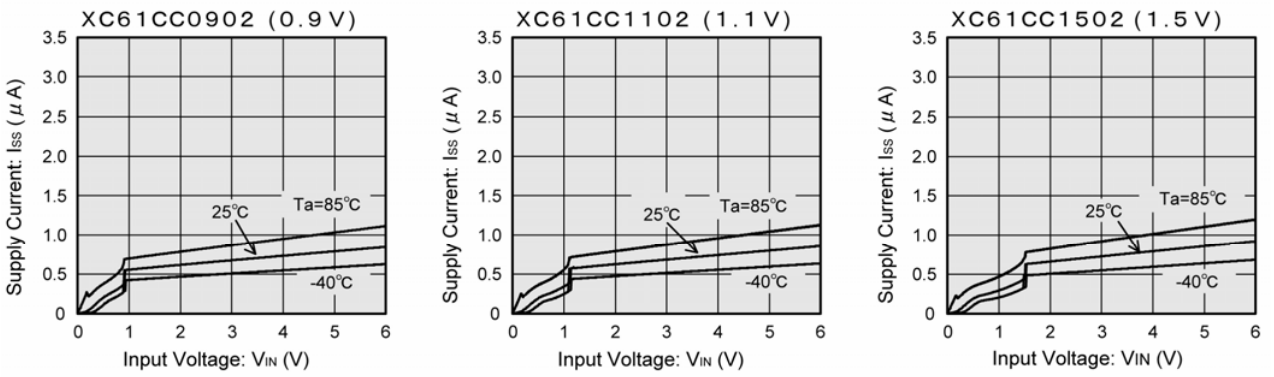


* : A resistor is not necessary with CMOS output products.

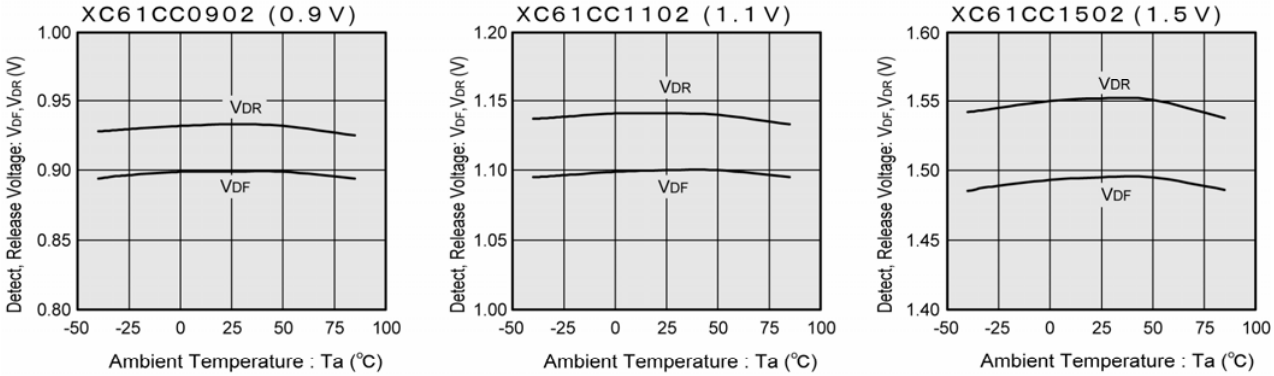
■TYPICAL PERFORMANCE CHARACTERISTICS

●Low Voltage

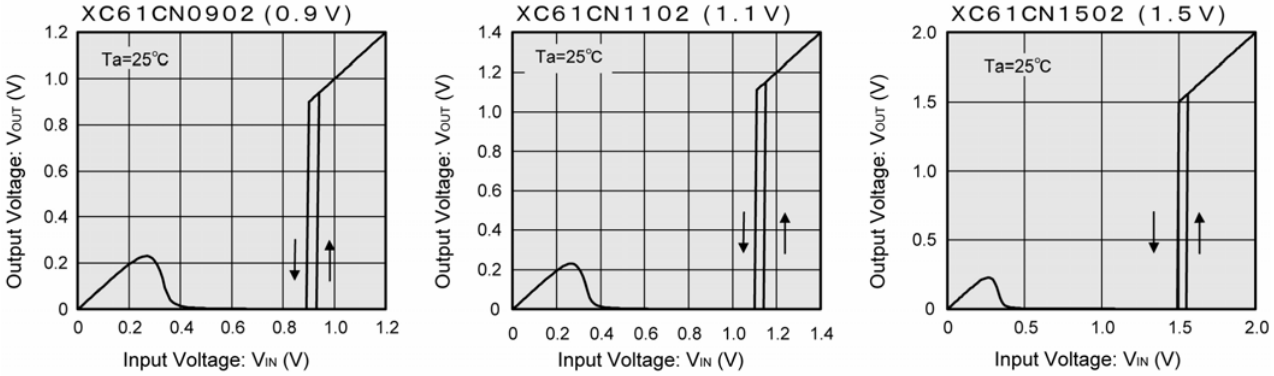
(1) Supply Current vs. Input Voltage



(2) Detect, Release Voltage vs. Ambient Temperature



(3) Output Voltage vs. Input Voltage



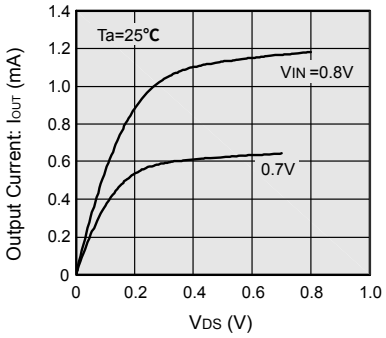
Note : Unless otherwise stated, the N-channel open drain pull-up resistance value is 100kΩ.

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

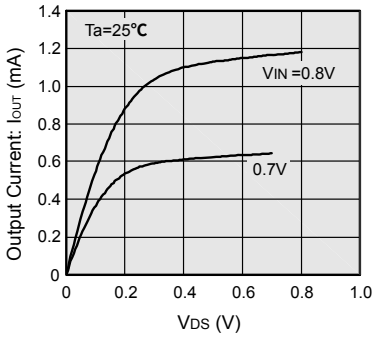
●Low Voltage (Continued)

(4) N-ch Driver Output Current vs. VDS

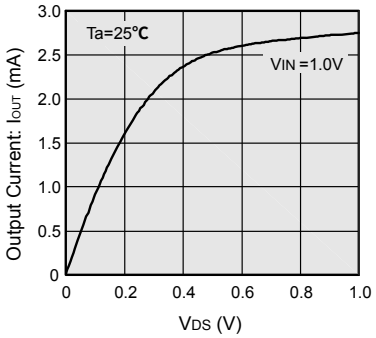
XC61CC0902 (0.9V)



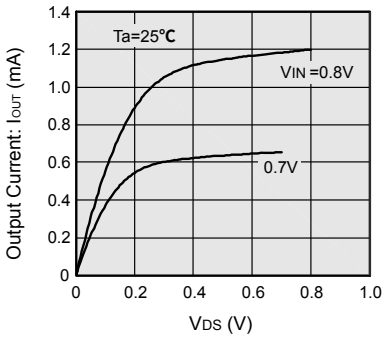
XC61CC1102(1.1V)



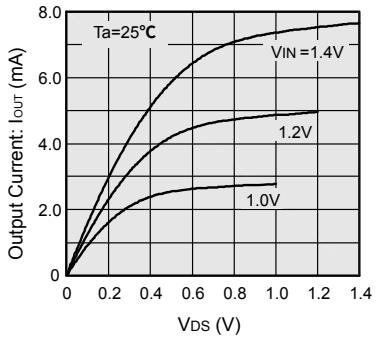
XC61CC1102(1.1V)



XC61CC1502(1.5V)

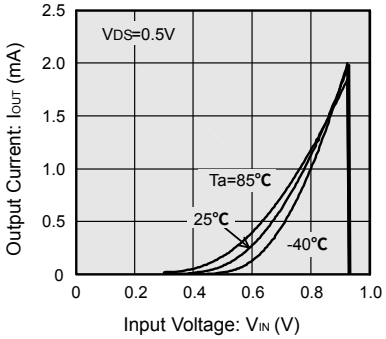


XC61CC1502(1.5V)

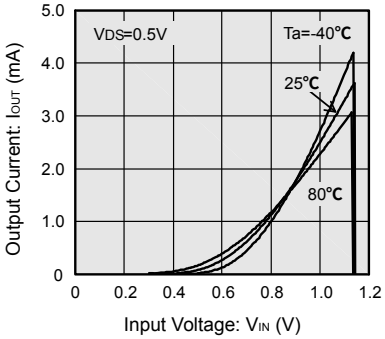


(5) N-ch Driver Output Current vs. Input Voltage

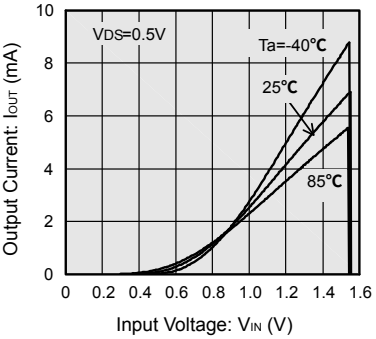
XC61CC0902 (0.9V)



XC61CC1102 (1.1V)

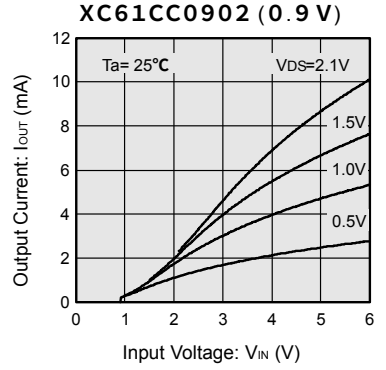


XC61CC1502(1.5V)

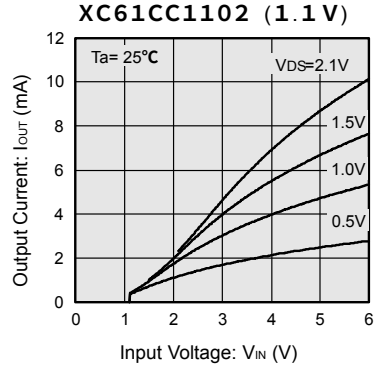


(6) P-ch Driver Output Current vs. Input Voltage

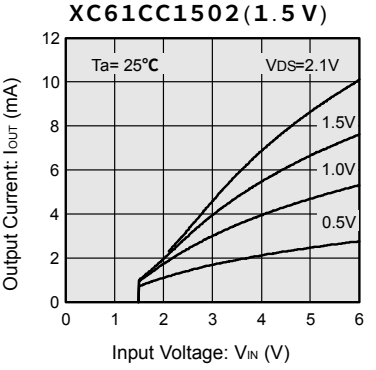
XC61CC0902 (0.9V)



XC61CC1102 (1.1V)



XC61CC1502(1.5V)

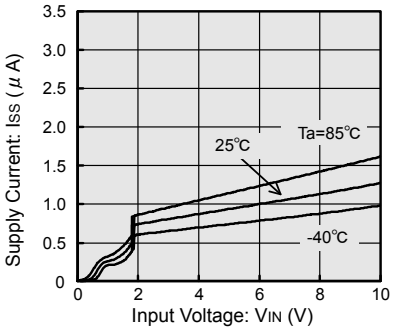


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

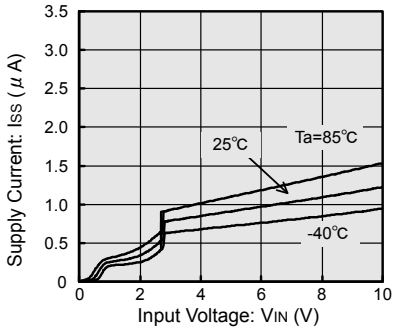
●Standard Voltage

(1) Supply Current vs. Input Voltage

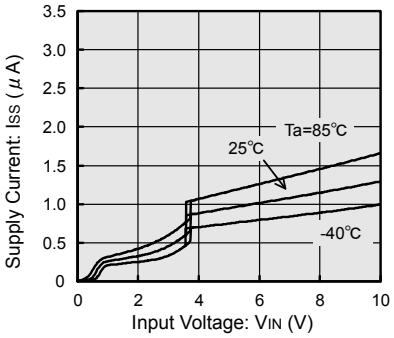
XC61CC1802 (1.8V)



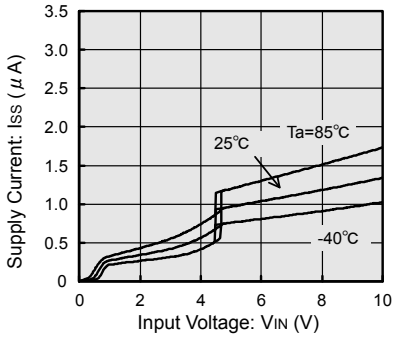
XC61CC2702 (2.7V)



XC61CC3602 (3.6V)

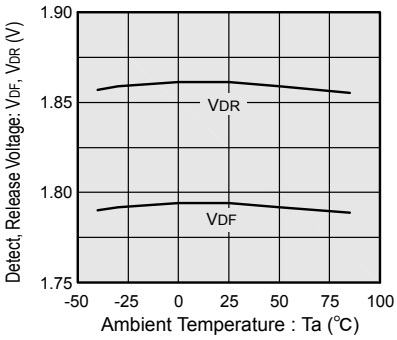


XC61CC4502 (4.5V)

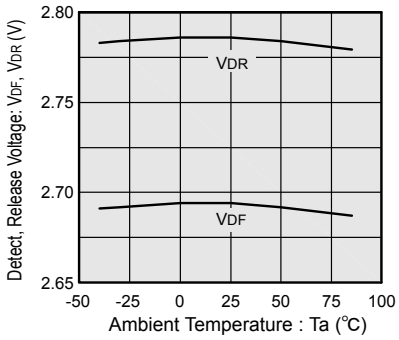


(2) Detect, Release Voltage vs. Ambient Temperature

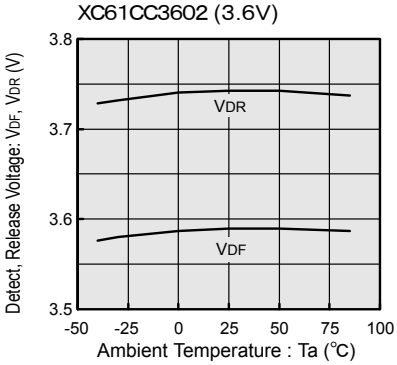
XC61CC1802 (1.8V)



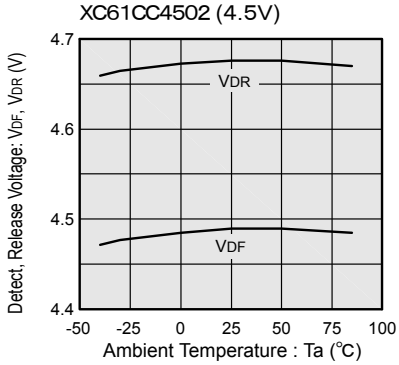
XC61CC2702 (2.7V)



XC61CC3602 (3.6V)



XC61CC4502 (4.5V)

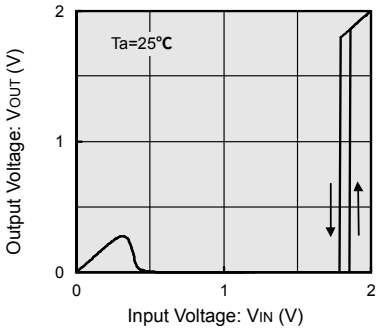


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

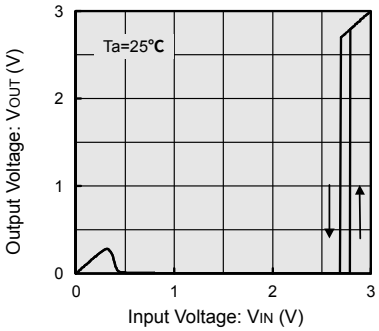
●Standard Voltage (Continued)

(3) Output Voltage vs. Input Voltage

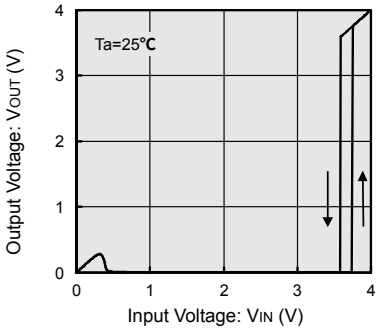
XC61CN1802 (1.8V)



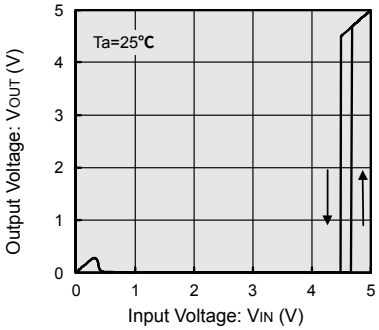
XC61CN2702 (2.7V)



XC61CN3602 (3.6V)



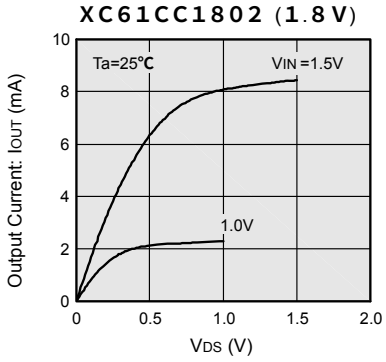
XC61CN4502 (4.5V)



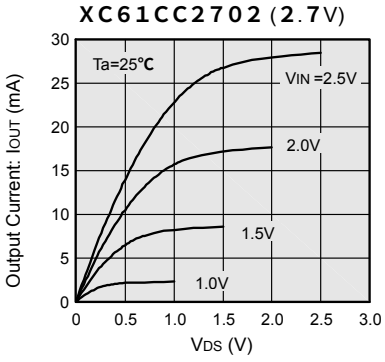
Note : The N-channel open drain pull up resistance value is 100kΩ.

(4) N-ch Driver Output Current vs. VDS

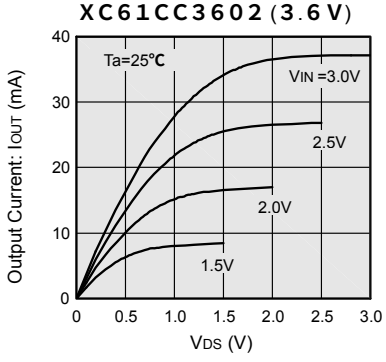
XC61CC1802 (1.8V)



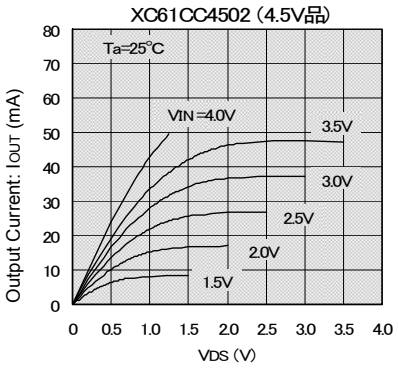
XC61CC2702 (2.7V)



XC61CC3602 (3.6V)



XC61CC4502 (4.5V品)

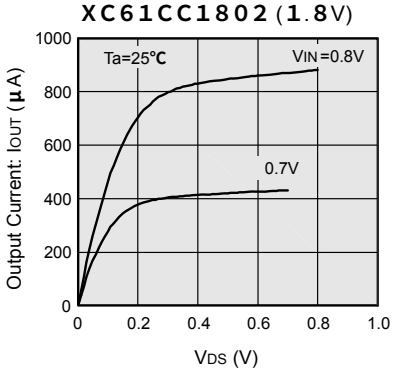


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

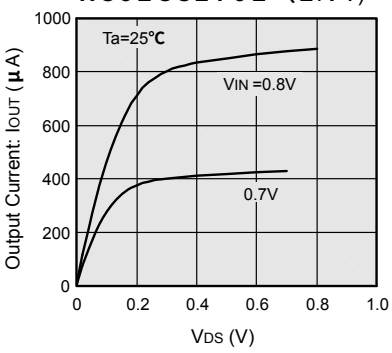
●Standard Voltage (Continued)

(4) N-ch Driver Output Current vs. V_{DS}

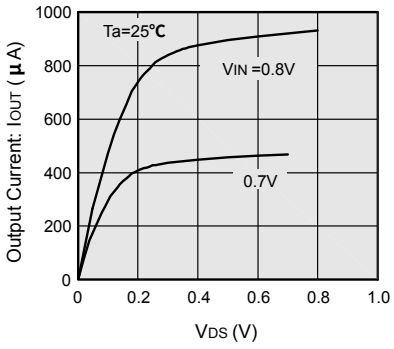
XC61CC1802 (1.8V)



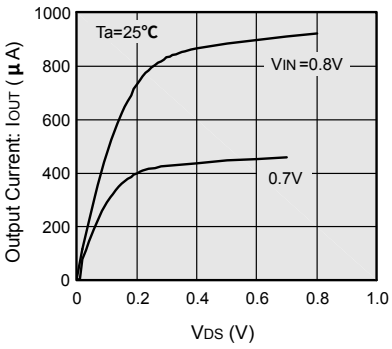
XC61CC2702 (2.7V)



XC61CC3602 (3.6V)

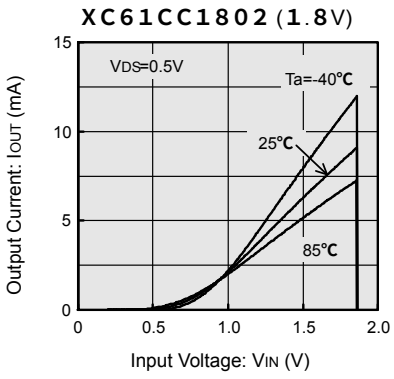


XC61CC4502 (4.5V)

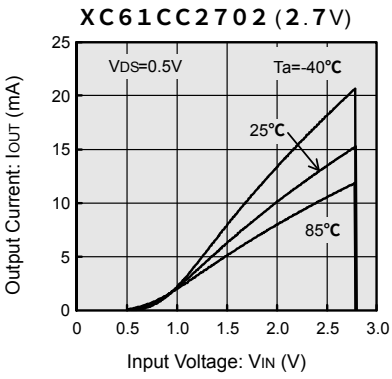


(5) N-ch Driver Output Current vs. Input Voltage

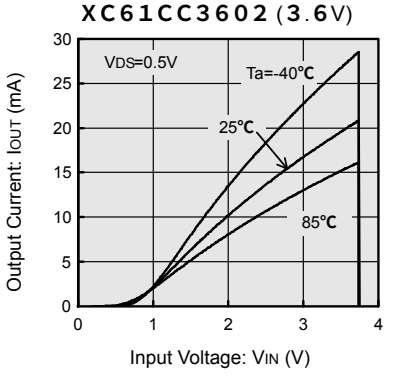
XC61CC1802 (1.8V)



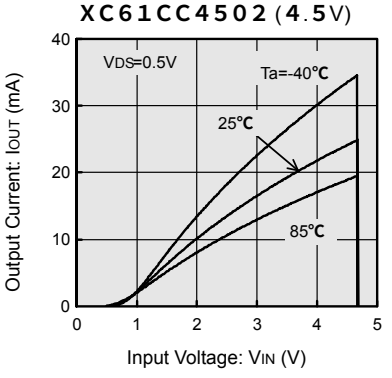
XC61CC2702 (2.7V)



XC61CC3602 (3.6V)



XC61CC4502 (4.5V)

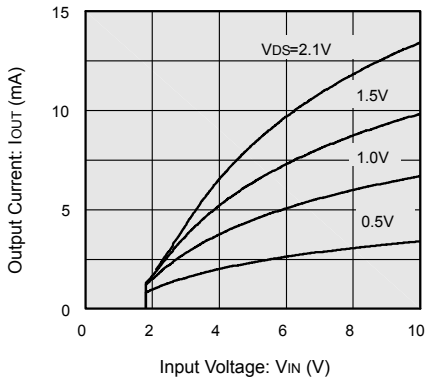


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

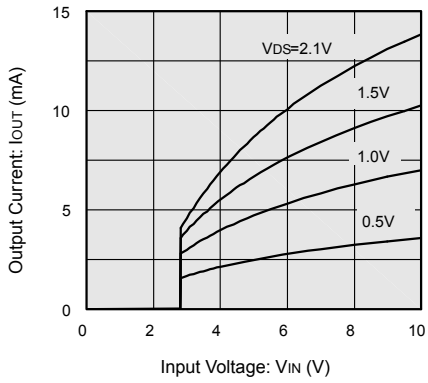
●Standard Voltage (Continued)

(6) P-ch Driver Output Current vs. Input Voltage

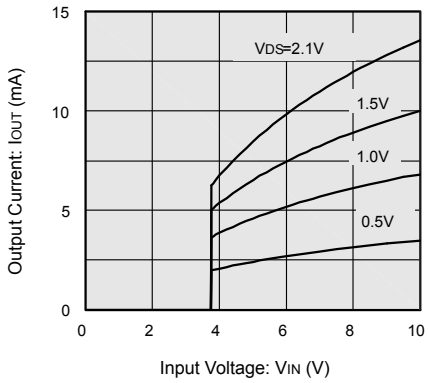
XC61CC1802 (1.8V)



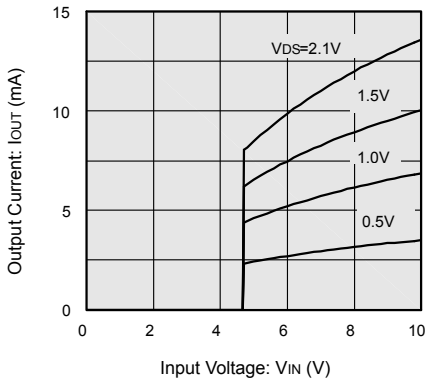
XC61CC2702 (2.7V)



XC61CC3602 (3.6V)

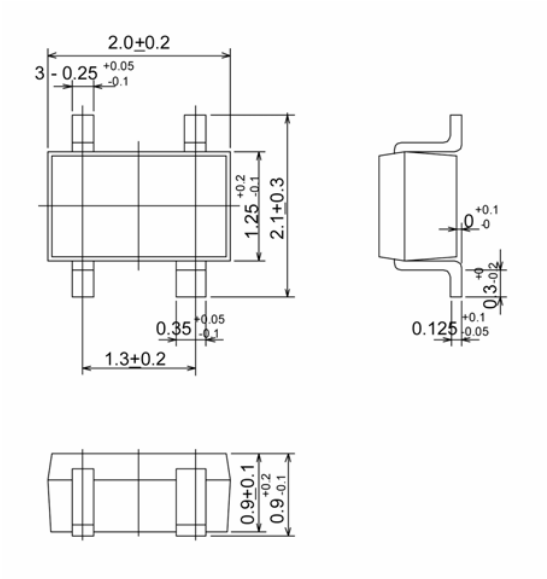


XC61CC4502 (4.5V)

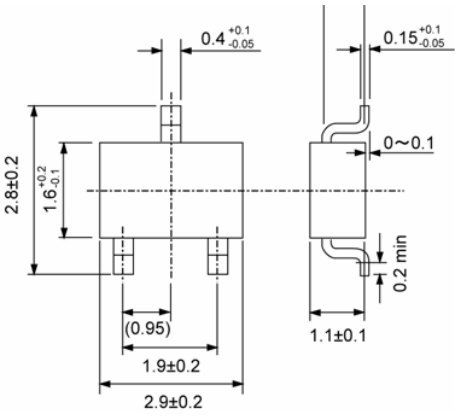


■PACKAGING INFORMATION

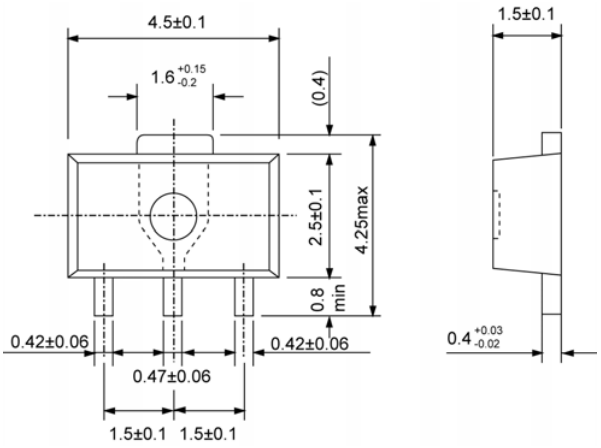
●SSOT-24 (SC-82)



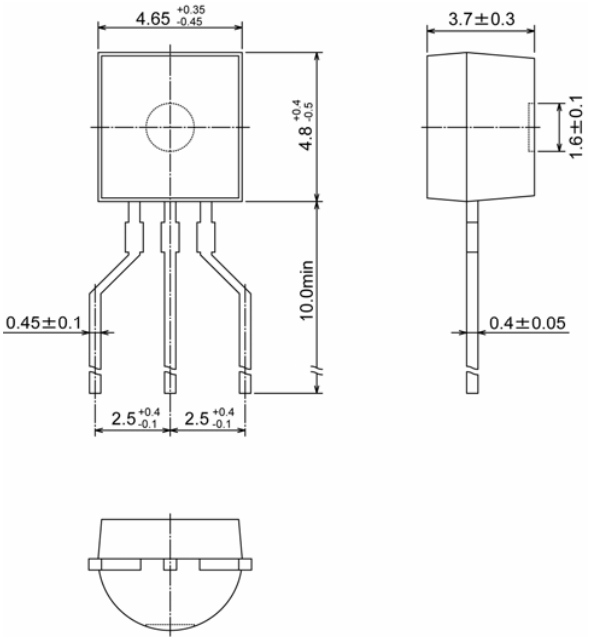
●SOT-23



●SOT-89

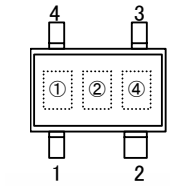


●TO-92

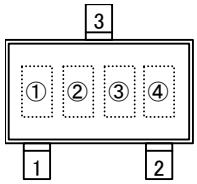


■MARKING RULE

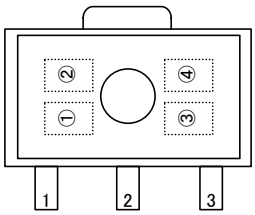
● SSOT-24, SOT-23, SOT-89



SSOT-24 (SC-82)
(TOP VIEW)



SOT - 23
(TOP VIEW)



SOT - 89
(TOP VIEW)

① Represents integer of detect voltage and CMOS Output (XC61CC series)

MARK	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.X
B	CMOS	1.X
C	CMOS	2.X
D	CMOS	3.X
E	CMOS	4.X
F	CMOS	5.X
H	CMOS	6.X

N-Channel Open Drain Output (XC61CN series)

MARK	CONFIGURATION	VOLTAGE (V)
K	N-ch	0.X
L	N-ch	1.X
M	N-ch	2.X
N	N-ch	3.X
P	N-ch	4.X
R	N-ch	5.X
S	N-ch	6.X

②Represents decimal number of detect voltage

MARK	VOLTAGE (V)	MARK	VOLTAGE (V)
0	X.0	5	X.5
1	X.1	6	X.6
2	X.2	7	X.7
3	X.3	8	X.8
4	X.4	9	X.9

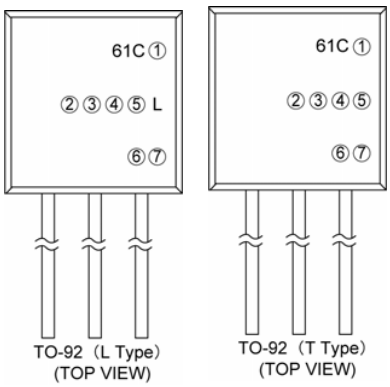
③Represents delay time
(Except for SSOT-24)

MARK	DELAY TIME	PRODUCT SERIES
3	No Delay Time	XC61Cxxx0xxx

④Represents production lot number
Based on the internal standard. (G, I, J, O, Q, W excepted)

■MARKING RULE (Continued)

●TO-92



①Represents output configuration

MARK	OUTPUT CONFIGURATION
C	CMOS
N	N-ch

②, ③Represents detect voltage (ex.)

MARK		VOLTAGE (V)
②	③	
3	3	3.3
5	0	5.0

④Represents delay time

MARK	DELAY TIME
0	No delay

⑤Represents detect voltage accuracy

MARK	DETECT VOLTAGE ACCURACY
1	Within ± 1% (Semi-custom)
2	Within ± 2%

⑥Represents a least significant digit of production year

MARK	PRODUCTION YEAR
5	2005
6	2006

⑦Represents production lot number
0 to 9, A to Z repeated. (G, I, J, O, Q, W excepted)
* No character inversion used.

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