

PROTECTION PRODUCTS

Description

The SFC05-5 is a five line flip chip TVS array. They are state-of-the-art devices that utilize solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. The SFC series TVS diodes are designed to protect sensitive semiconductor components from damage or latch-up due to electrostatic discharge (ESD) and other voltage induced transient events.

The SFC05-5 is a 6-bump, 0.5mm pitch flip chip array with a 3x2 bump grid. It measures 1.5 x 1.0 x 0.65mm. This small outline makes the SFC05-5 especially well suited for portable applications. CSP TVS devices are compatible with current pick and place equipment and assembly methods.

Each device will protect up to five data or I/O lines. The flip chip design results in lower inductance, virtually eliminating voltage overshoot due to leads and inter-connecting bond wires. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Features

- ◆ 200 Watts peak pulse power ($t_p = 8/20\mu\text{s}$)
- ◆ Transient protection for data lines to
IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
IEC 61000-4-4 (EFT) 40A (5/50ns)
IEC 61000-4-5 (Lightning) 20A (8/20 μs)
- ◆ Small chip scale package requires less board space
- ◆ Low profile ($< 0.65\text{mm}$)
- ◆ No need for underfill material
- ◆ Protects five I/O or data lines
- ◆ Low clamping voltage
- ◆ Working voltage: 5V
- ◆ Solid-state silicon-avalanche technology

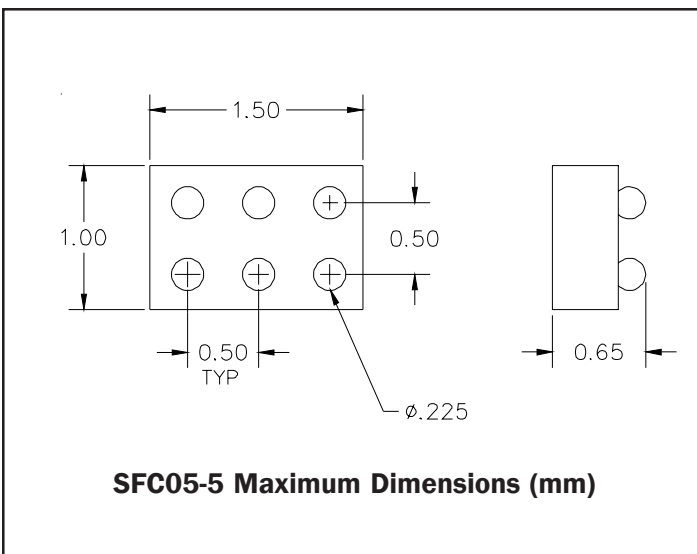
Mechanical Characteristics

- ◆ JEDEC MO-211, 0.50 mm Pitch Flip Chip Package
- ◆ Non-conductive top side coating
- ◆ Marking : Marking Code
- ◆ Packaging : Tape and Reel

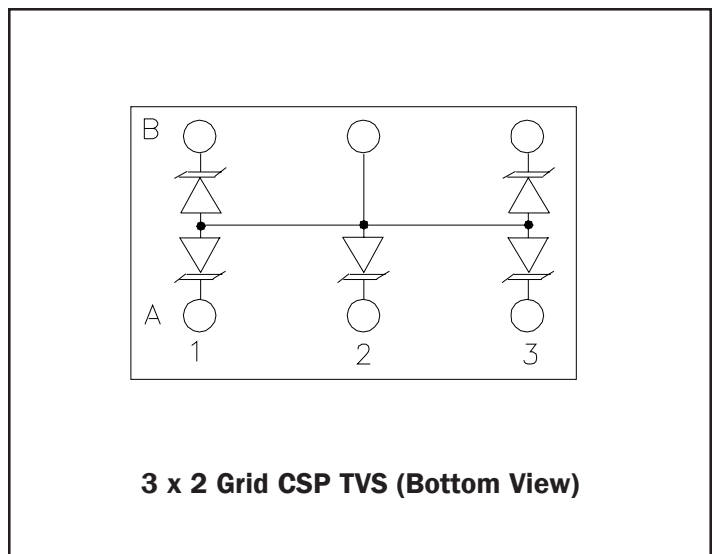
Applications

- ◆ Cell Phone Handsets and Accessories
- ◆ Personal Digital Assistants (PDA's)
- ◆ Notebook and Hand Held Computers
- ◆ Portable Instrumentation
- ◆ Smart Cards
- ◆ MP3 Players
- ◆ GPS

Device Dimensions



Schematic & PIN Configuration



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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	200	Watts
Peak Pulse Current (tp = 8/20μs)	I_{pp}	20	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	>25 >15	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

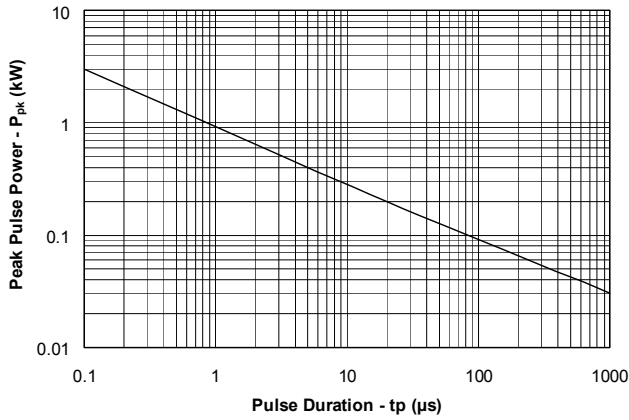
Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	6			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T=25°C$			10	μA
Clamping Voltage	V_C	$I_{pp} = 5A, tp = 8/20μs$ Any I/O to Ground			9.5	V
Clamping Voltage	V_C	$I_{pp} = 20A, tp = 8/20μs$ Any I/O to Ground			11	V
Junction Capacitance	C_J	$V_R = 0V, f = 1MHz$			350	pF

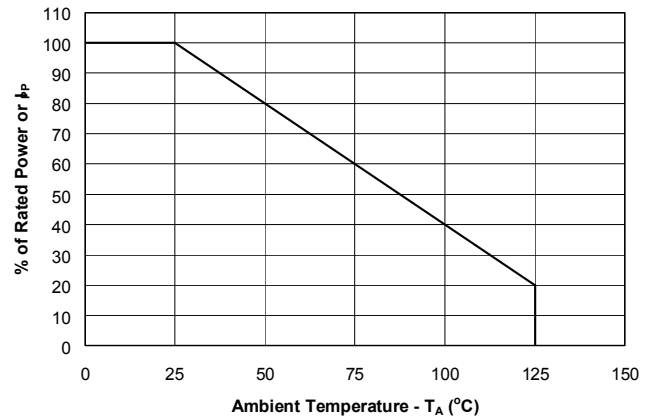
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Typical Characteristics

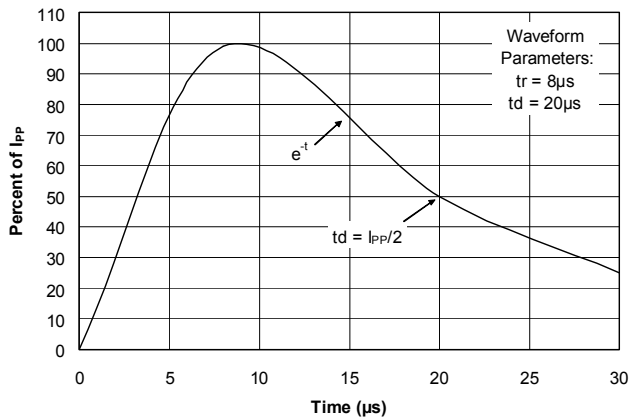
Non-Repetitive Peak Pulse Power vs. Pulse Time



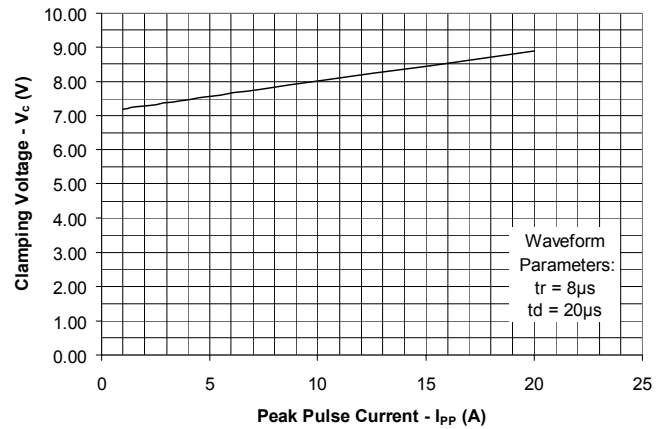
Power Derating Curve



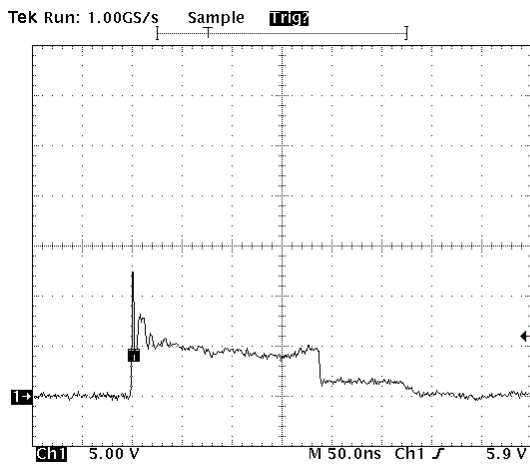
Pulse Waveform



Clamping Voltage vs. Peak Pulse Current



ESD Clamping (8kV Contact Discharge)



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Applications Information

Device Connection Options

The SFC05-5 has solder bumps located in a 3 x 2 matrix layout on the active side of the device. The bumps are designated by the numbers 1 - 3 along the horizontal axis and letters A - B along the vertical axis. The lines to be protected are connected at bumps A1, B1, A2, A3, and B3. Bump B2 is connected to ground. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces.

Flip Chip TVS

Flip chip TVS devices are wafer level chip scale packages. They eliminate external plastic packages and leads and thus result in a significant board space savings. Manufacturing costs are minimized since they do not require an intermediate level interconnect or interposer layer for reliable operation. They are compatible with current pick and place equipment further reducing manufacturing costs. Certain precautions and design considerations have to be observed however for maximum solder joint reliability. These include solder pad definition, board finish, and assembly parameters.

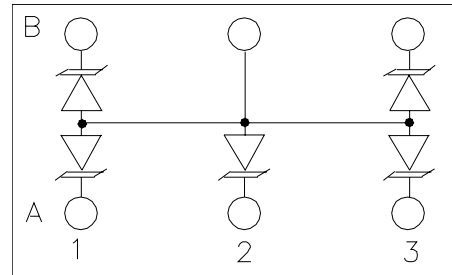
Printed Circuit Board Mounting

Non-solder mask defined (NSMD) land patterns are recommended for mounting the SFC05-5. Solder mask defined (SMD) pads produce stress points near the solder mask on the PCB side that can result in solder joint cracking when exposed to extreme fatigue conditions. The recommended pad size is 0.225 ± 0.010 mm with a solder mask opening of 0.350 ± 0.025 mm.

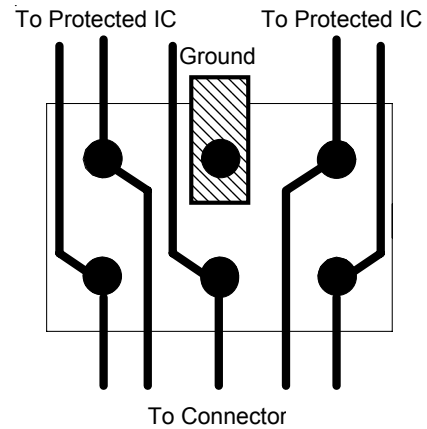
Grid Courtyard

The recommended grid placement courtyard is 1.3 x 1.8 mm. The grid courtyard is intended to encompass the land pattern and the component body that is centered in the land pattern. When placing parts on a PCB, the highest recommended density is when one courtyard touches another.

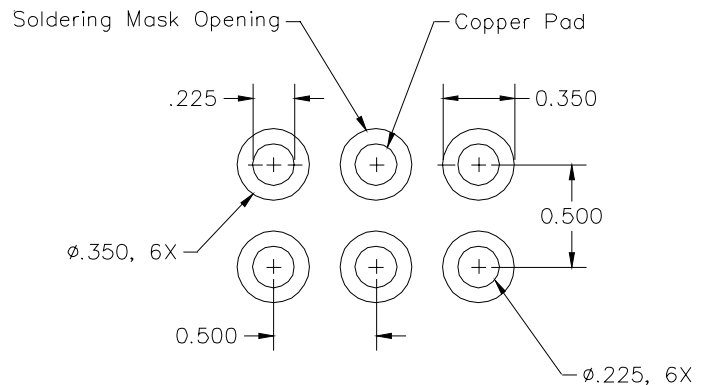
Device Schematic and Pin Configuration



Layout Example



NSMD Package Footprint



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Applications Information (Continued)

Printed Circuit Board Finish

A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems and should be avoided.

Stencil Design

A properly designed stencil is key to achieving adequate solder volume without compromising assembly yields. A 0.100mm thick, laser cut, electro-polished stencil with 0.275mm square apertures and rounded corners is recommended.

Reflow Profile

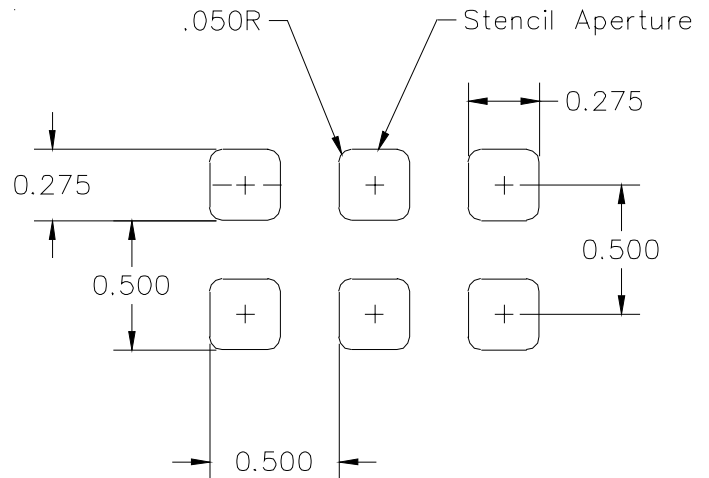
The flip chip TVS can be assembled using the reflow requirements for IPC/JEDEC standard J-STD-020 for assembly of small body components. During reflow, the component will self-align itself on the pad.

Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Stencil Design



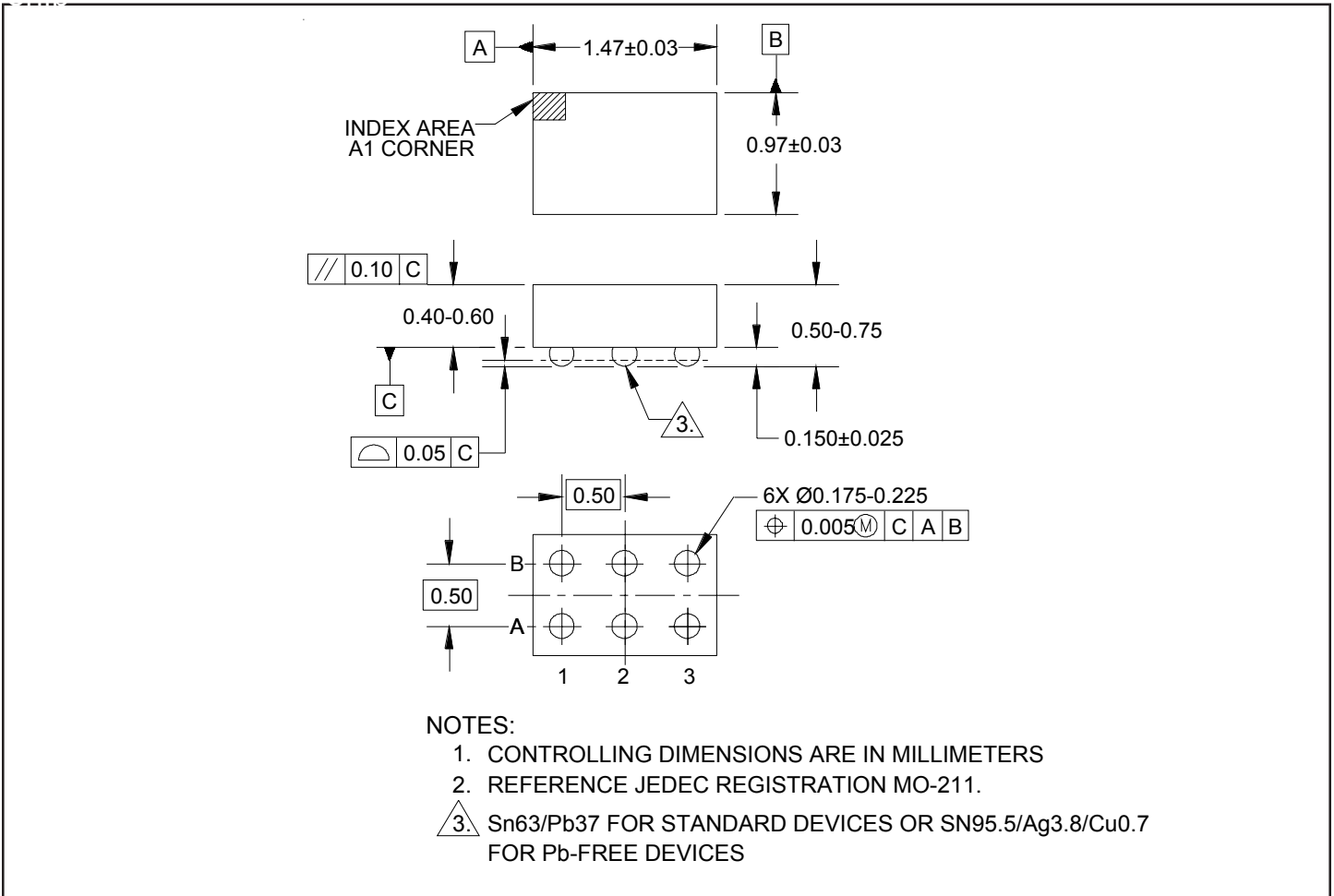
Assembly Guideline for Pb-Free Soldering

The following are recommendations for the assembly of this device:

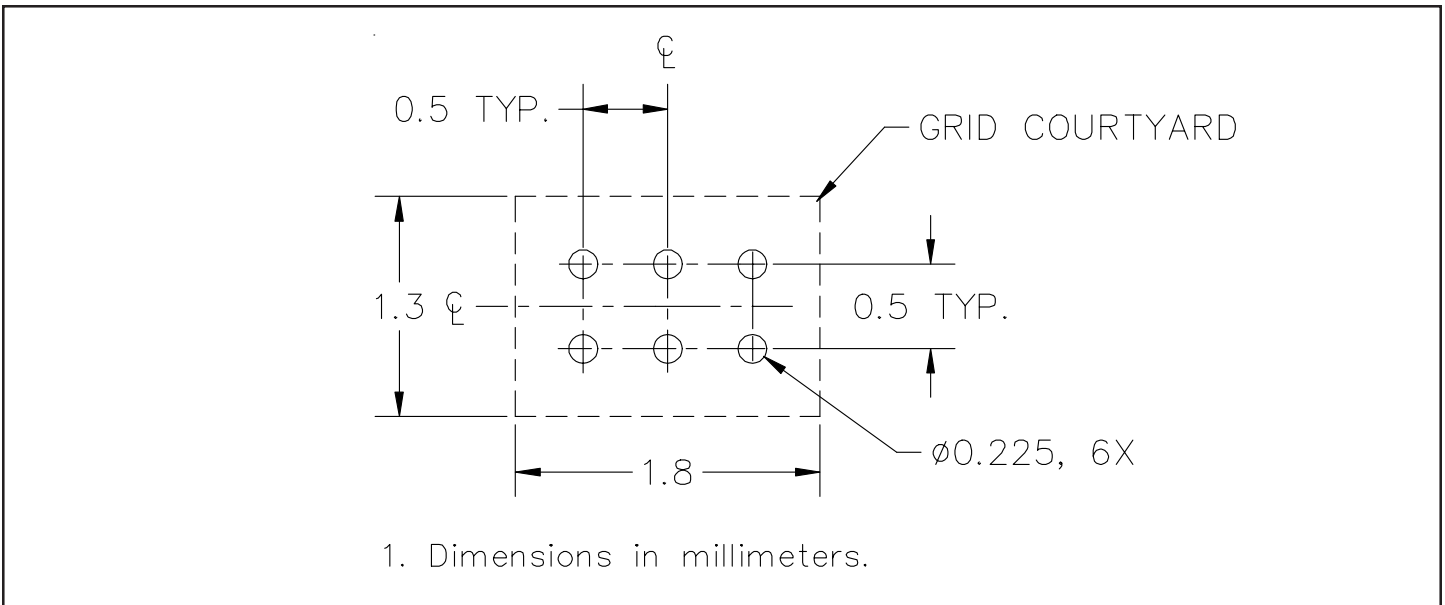
Assembly Parameter	Recommendation
Solder Ball Composition	95.5Sn/3.8Ag/0.7Cu
Solder Stencil Design	Same as the SnPb design
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Composition	Sn Ag (3-4) Cu (0.5-0.9)
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	per JEDEC J-STD-020
PCB Solder Pad Design	Same as the SnPb Design
PCB Pad Finish	OSP or AuNi

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Outline Drawing - 3x2 Grid Flip



Land Pattern - 3x2 Grid Flip Chip



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Marking Codes

Part Number	Marking Code
SFC05-5	F55U

Ordering Information

Part Number	Pitch Option	Qty per Reel	Reel Size
SFC05-5.WC	2mm	3,000	7 Inch
SFC05-5.WCT ⁽¹⁾	2mm	3,000	7 Inch

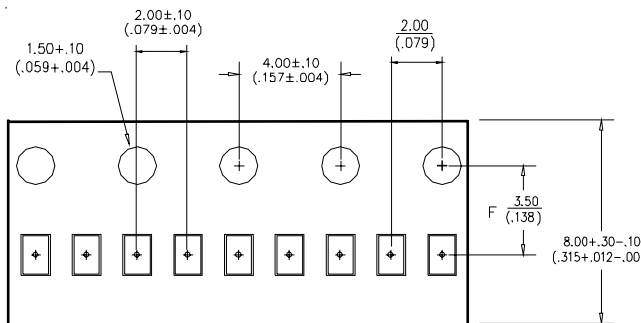
Top Coating: The top (non-bump side) of the device is a white non-conductive coating. The coating is laser markable and increases mechanical durability. This material is compliant with UL 94V-0 flammability requirements.

Notes

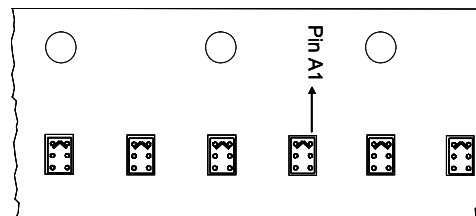
(1) Lead Free Solder Balls

ChipClamp is a mark of Semtech Corporation

Tape and Reel Specification



Tape Specifications



Device Orientation

Contact Information

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