
Low Voltage 3-Mode Dual 150mA LDO

NO.EA-139-071130

OUTLINE

The R5328K Series are dual 150mA voltage regulator ICs with 3-mode. The 3-mode describes that they are the inactive standby, the active fast mode, and the active low power mode. The two active modes can be switched over with ECO pin. With this function, the output voltage maintains the level, and the mode can be switched over.

The minimum operating voltage is 1.4V, and the output voltage range is from 0.8V to 4.0V.

Since the package for these ICs is DFN(PLP)2020-8, high density mounting of the ICs on boards is possible.

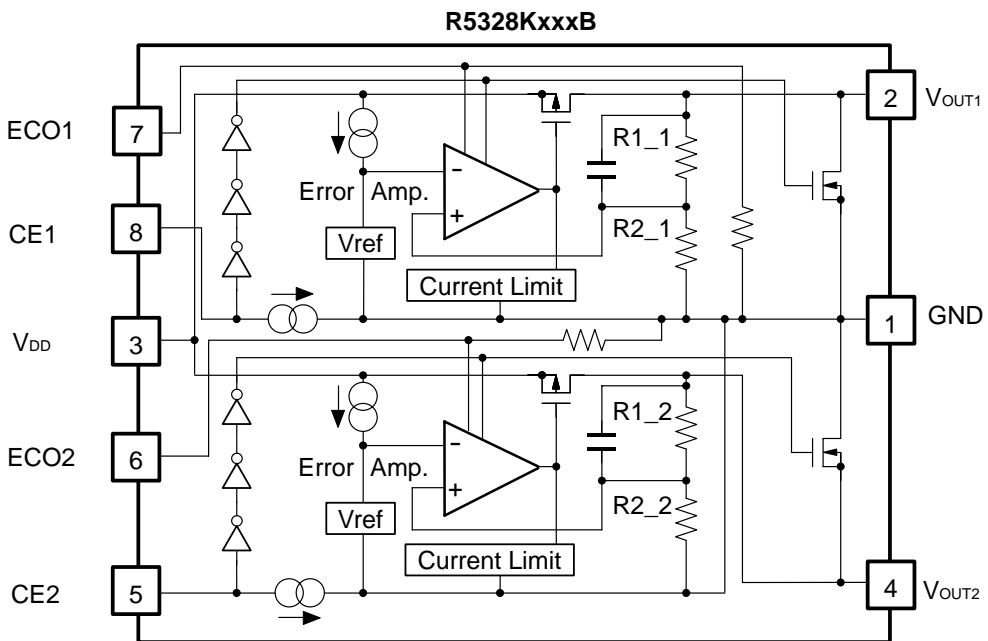
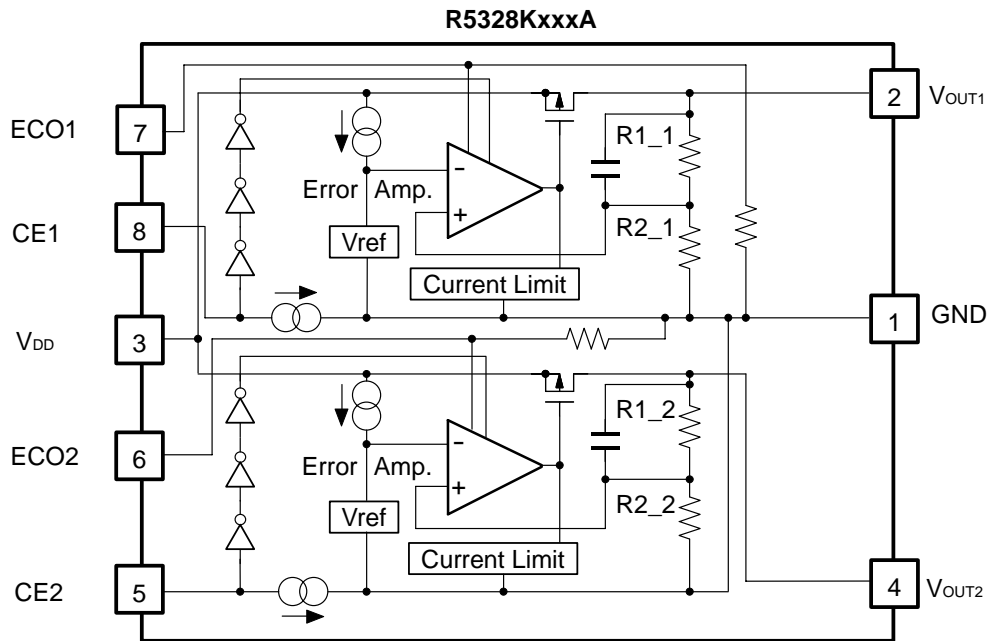
FEATURES

- Supply Current (Low Power Mode).....Typ. 2.0 μ A \times 2 (VR1&VR2) ($V_{OUT}<2.0V$)
Typ. 2.5 μ A \times 2 (VR1&VR2) ($V_{OUT} \geq 2.0V$)
- Supply Current (Fast Mode).....Typ. 75 μ A \times 2 (VR1&VR2) ($V_{OUT}<2.0V$)
Typ. 65 μ A \times 2 (VR1&VR2) ($V_{OUT} \geq 2.0V$)
- Standby ModeTyp. 0.1 μ A (VR1&VR2)
- Input Voltage1.4V to 6.0V
- Output Voltage0.8V to 4.0V
- Dropout VoltageTyp. 0.25V ($I_{OUT}=150mA$, $V_{OUT}=2.8V$)
- Ripple Rejection (Fast Mode)Typ. 70dB ($f=1kHz$)
- Line Regulation (Fast Mode).....Typ. 0.02%/V
- Output Voltage Accuracy (Fast Mode) $\pm 1.0\%$
- Output Voltage Accuracy (Low Power Mode) ... $\pm 1.2\%$
- Temperature-drift Coefficient of Output Voltage.. Typ. $\pm 100ppm/^{\circ}C$
- PackageDFN(PLP)2020-8
- Built-in fold-back protection circuitTyp. 50mA (Current at short mode)
- Ceramic Capacitor is recommended.1.0 μ F
- Built-in chip enable circuit (A/B: active high)
(Depending on V_{IN} and set V_{OUT} . Refer to the electrical characteristics table.)

APPLICATIONS

- Power source for handheld communication equipment.
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for battery-powered equipment.

BLOCK DIAGRAMS



SELECTION GUIDE

The output voltage, auto discharge function*, and the taping type for the ICs can be selected at the user's request.

The selection can be made with designating the part number as shown below;

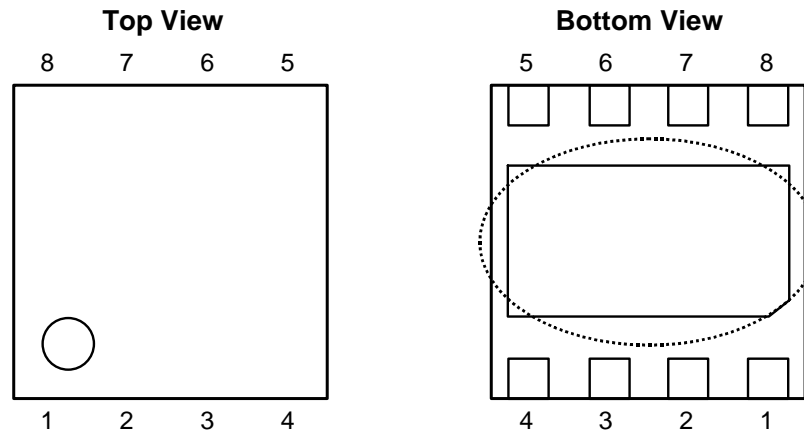
R5328K xxxx-xx-x ← Part Number
 ↑ ↑ ↑ ↑ ↑
 a b c d e

Code	Contents
a	Designation of Package Type: K: DFN(PLP)2020-8
b	Setting combination of dual Output Voltage (V_{OUT}): Serial Number for Voltage Setting, Stepwise setting with a step of 0.1V in the range of 0.8V to 4.0V is possible for each channel.
c	Designation of Mask Option: A: without auto discharge function* at OFF state. B: with auto discharge function* at OFF state.
d	Designation of Taping Type: Ex. TR (refer to Taping Specifications; TR type is the standard direction.)
e	Designation of composition of plating: None : Au plating

*) When the mode is into standby with CE signal, auto discharge transistor turns on, and it makes the turn-off speed faster than normal type.

PIN CONFIGURATION


- DFN(PLP)2020-8



PIN DESCRIPTIONS

- R5328K

Pin No.	Symbol	Description
1	GND	Ground Pin
2	V _{OUT1}	Output Pin 1
3	V _{DD}	Input Pin
4	V _{OUT2}	Output Pin 2
5	CE2	Chip Enable Pin 2
6	ECO2	Low Power/ Fast Mode Changer Pin2
7	ECO1	Low Power/ Fast Mode Changer Pin1
8	CE1	Chip Enable Pin 1

* Tab in the  parts have GND level. (They are connected to the back side of this IC.)
Do not connect to other wires or land patterns.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	6.0	V
V_{CE1}, V_{CE2} V_{ECO1}, V_{ECO2}	Input Voltage (CE/ECO Pin)	-0.3 to 6.5	V
V_{OUT1}, V_{OUT2}	Output Voltage	-0.3 to $V_{IN}+0.3$	V
I_{OUT1}, I_{OUT2}	Output Current	160	mA
P_D	Power Dissipation (DFN(PLP)2020-8)*	880	mW
T_{opt}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 125	°C

*) For Power Dissipation, please refer to PACKAGE INFORMATION to be described.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded ever for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

ELECTRICAL CHARACTERISTICS

• R5328KxxxA/B

VR1/VR2

T_{opt}=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit	
V _{OUT}	Output Voltage (Fast Mode)	V _{IN} -V _{OUT} =1.0V I _{OUT} =1mA V _{ECO} =V _{IN}	V _{OUT} > 1.5V	×0.99		×1.01	V
			V _{OUT} ≤ 1.5V	-15		+15	mV
	Output Voltage (Low Power Mode)	V _{IN} -V _{OUT} =1.0V I _{OUT} =1mA V _{ECO} =GND	V _{OUT} > 1.5V	×0.988		×1.012	V
			V _{OUT} ≤ 1.5V	-18		+18	mV
I _{OUT}	Output Current	V _{IN} -V _{OUT} =1.0V	150			mA	
ΔV _{OUT} / ΔI _{OUT}	Load Regulation (Fast Mode)	V _{IN} -V _{OUT} =1.0V, V _{ECO} =V _{IN} 1mA ≤ I _{OUT} ≤ 150mA		20	40	mV	
	Load Regulation (Low Power Mode)	V _{IN} -V _{OUT} =1.0V, V _{ECO} =GND 1mA ≤ I _{OUT} ≤ 150mA		25	45	mV	
V _{DIF}	Dropout Voltage	Refer to the following table					
I _{SS1}	Supply Current (Fast Mode)	V _{IN} -V _{OUT} =1.0V, V _{ECO} =V _{IN}	V _{OUT} < 2.0V		75	95	μA
			V _{OUT} ≥ 2.0V		65	95	
I _{SS2}	Supply Current (Low Power Mode)	V _{IN} -V _{OUT} =1.0V, V _{ECO} =GND, Except CE pull-down current	V _{OUT} < 2.0V		2	4	μA
			V _{OUT} ≥ 2.0V		2.5	4	
I _{standby}	Standby Current	V _{IN} =6.0V, V _{CE} =GND		0.1	1	μA	
ΔV _{OUT} / ΔV _{IN}	Line Regulation (Fast Mode)	I _{OUT} =1mA V _{OUT} +0.5V ≤ V _{IN} ≤ 6V	V _{ECO} =V _{IN}		0.02	0.1	%V
	Line Regulation (Low Power Mode)	If V _{OUT} ≤ 0.9V: 0.5V ≤ V _{IN} ≤ 6V	V _{ECO} =GND		0.1	0.2	
RR	Ripple Rejection (Fast Mode)	f=1kHz, Ripple 0.2Vp-p, V _{IN} -V _{OUT} =1.0V, I _{OUT} =30mA V _{ECO} =V _{IN}		70		dB	
V _{IN}	Input Voltage		1.4		6.0	V	
ΔV _{OUT} / ΔT _{opt}	Output Voltage Temperature Coefficient	I _{OUT} =1mA, -40°C ≤ T _{opt} ≤ 85°C		±100		ppm/ °C	
I _{lim}	Short Current Limit	V _{OUT} =0V		50		mA	
I _{PD}	CE Pull-down Constant Current			0.3	0.8	μA	
R _{PDE}	ECO Pull-down Resistance		2.4	5	15	MΩ	
V _{CEH} , V _{ECOH}	CE, ECO Input Voltage "H"		1		6	V	
V _{CEL} , V _{ECOL}	CE, ECO Input Voltage "L"		0		0.4	V	
en	Output Noise	BW=10Hz to 100kHz		30		μVrms	
R _{LOW}	Low Output Nch Tr. ON Resistance (of B version)	V _{CE} =0V		50		Ω	

• Dropout Voltage by Output Voltage

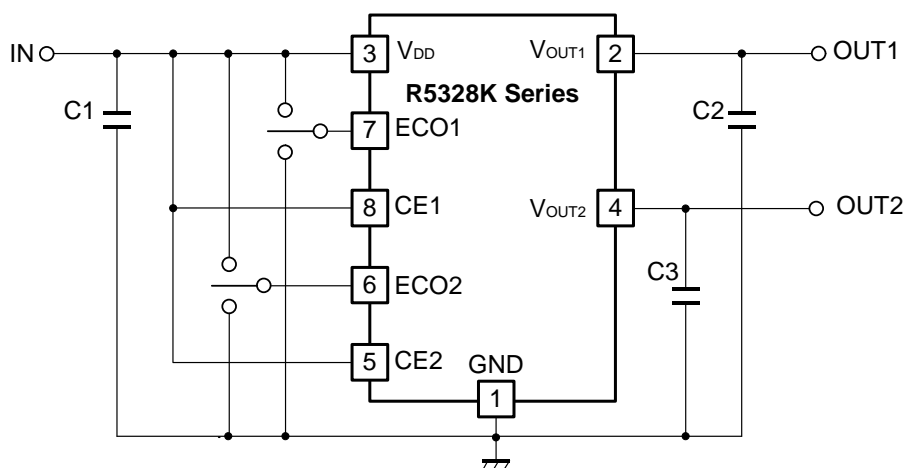
Output Voltage V_{OUT} (V)	Dropout Voltage V_{DIF} (mV)				
	Condition	ECO="H"		ECO="L"	
		Typ.	Max.	Typ.	Max.
$0.8V \leq V_{OUT} < 0.9V$	$I_{OUT}=150mA$	755	1100	795	1100
$0.9V \leq V_{OUT} < 1.0V$		675	950	715	960
$1.0V \leq V_{OUT} < 1.2V$		600	890	645	930
$1.2V \leq V_{OUT} < 1.5V$		490	730	520	770
$1.5V \leq V_{OUT} < 2.0V$		395	610	415	640
$2.0V \leq V_{OUT} < 2.8V$		310	440	315	445
$2.8V \leq V_{OUT} \leq 4.0V$		250	350	255	350

*Recommended Ceramic capacitor for Output:

General Example of External Components

Ceramic Capacitors:

TYPICAL APPLICATION



(External Components)

1.0 μ F	CM05X5R105K06AB	(Kyocera)
	C1005JB0J105K	(TDK)
	GRM155B30J105KE18B	(Murata)

TECHNICAL NOTES

When using these ICs, consider the following points:

Phase Compensation

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a capacitor C2 and C3 with good frequency characteristics and ESR (Equivalent Series Resistance).

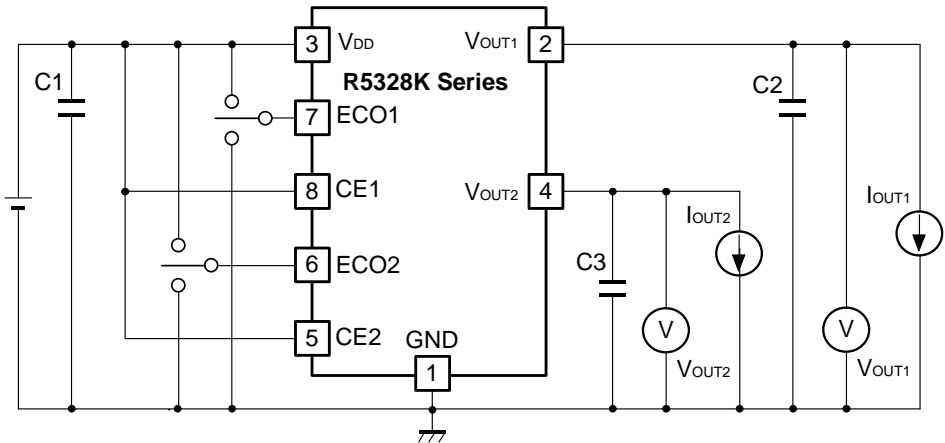
(Note: If additional ceramic capacitors are connected with parallel to the output pin with an output capacitor for phase compensation, the operation might be unstable. Because of this, test these ICs with as same external components as ones to be used on the PCB.)

PCB Layout

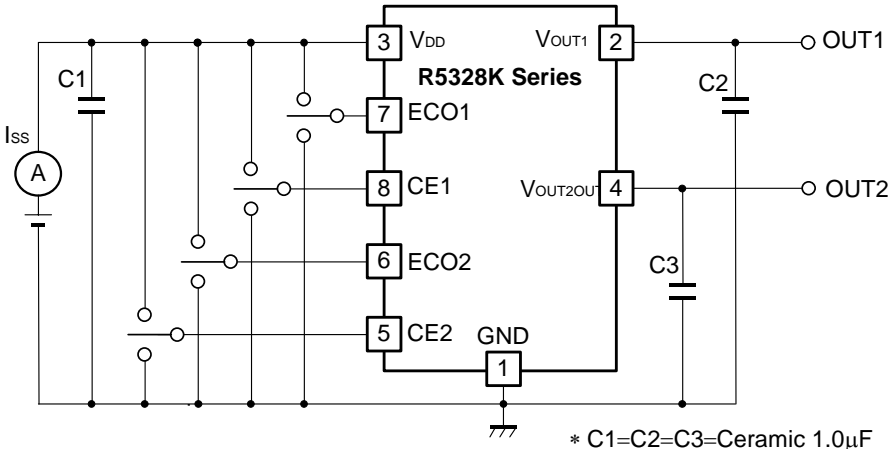
Make V_{DD} and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect a capacitor C1 with a capacitance value as much as 1.0 μ F or more between V_{DD} and GND pin, and as close as possible to the pins.

Set external components, especially the output capacitor C2 and C3, as close as possible to the ICs, and make wiring as short as possible.

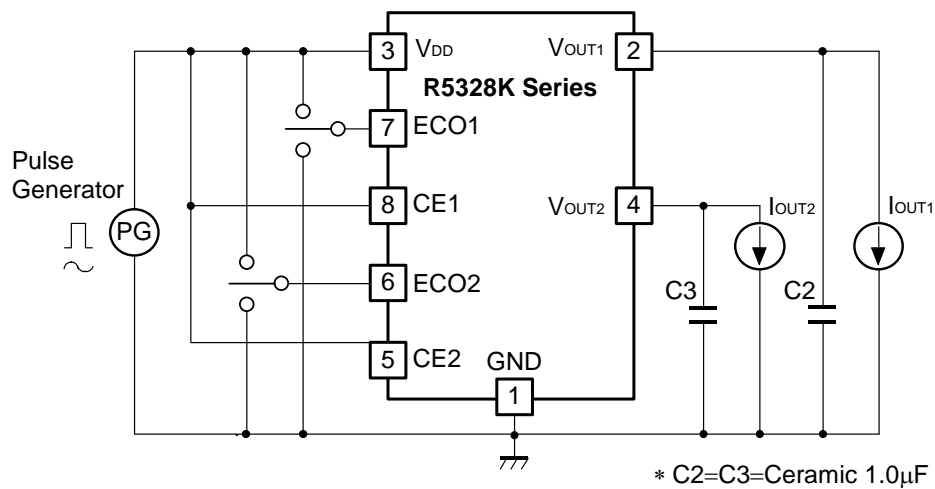
TEST CIRCUITS



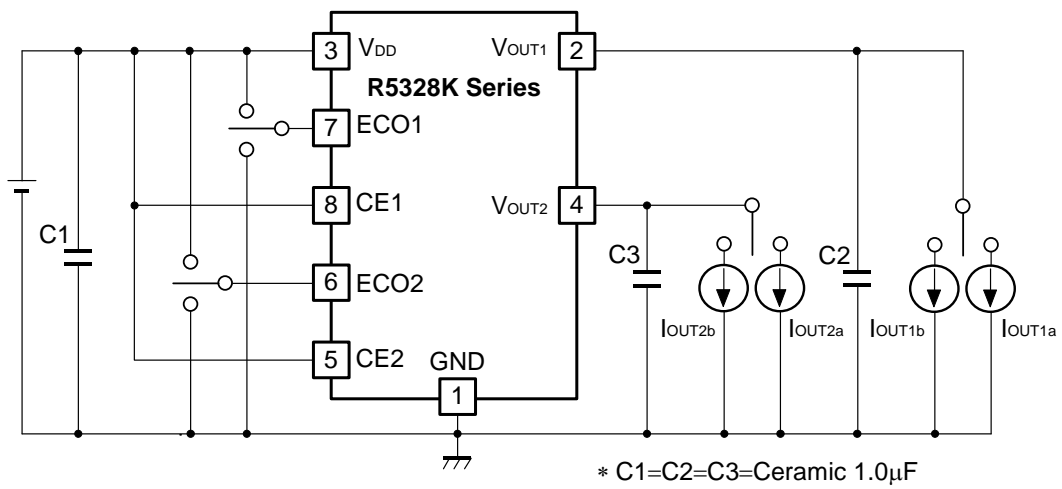
Standard test Circuit



Supply Current Test Circuit



Ripple Rejection, Line Transient Response Test Circuit

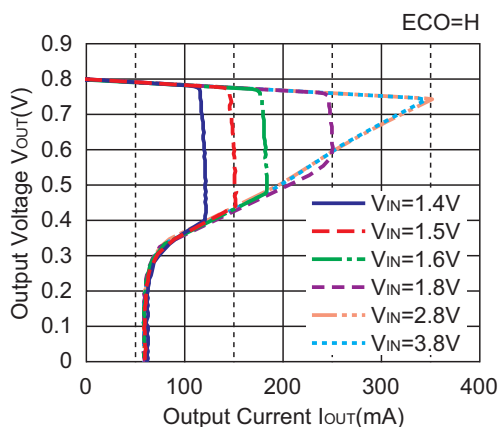


Load Transient Response Test Circuit

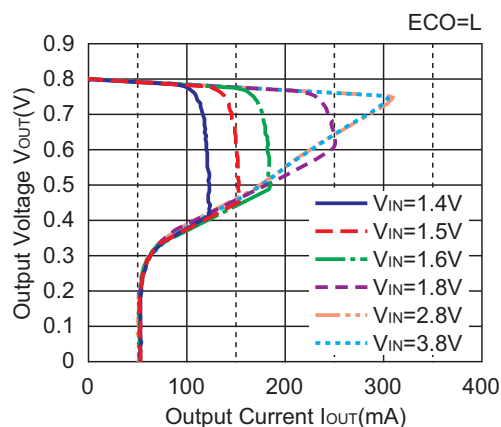
TYPICAL CHARACTERISTICS

1) Output Voltage vs. Output Current (T_{opt}=25°C)

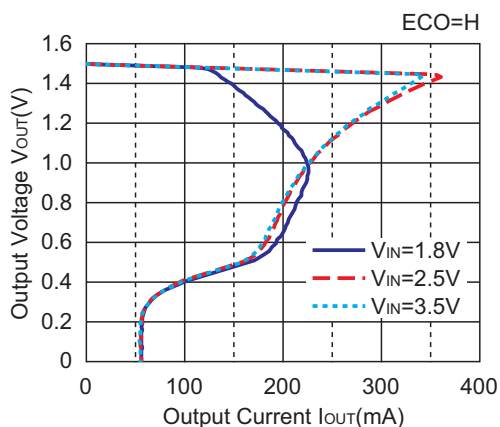
0.8 V (VR1/VR2)



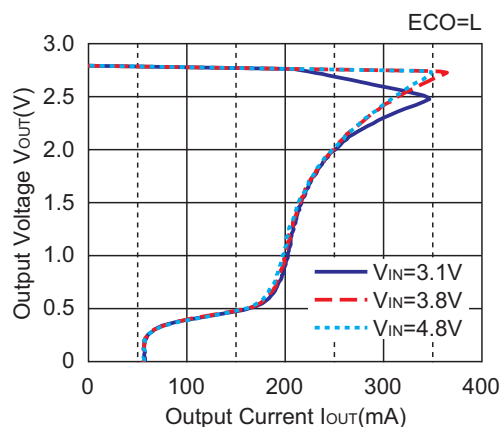
0.8V (VR1/VR2)



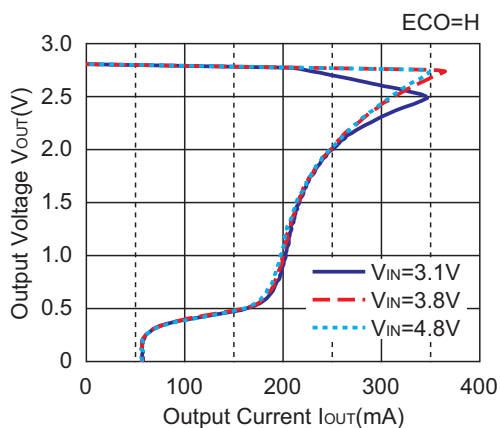
1.5V (VR1/VR2)



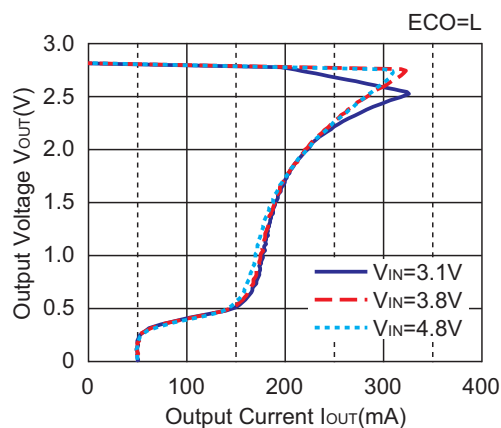
1.5V (VR1/VR2)



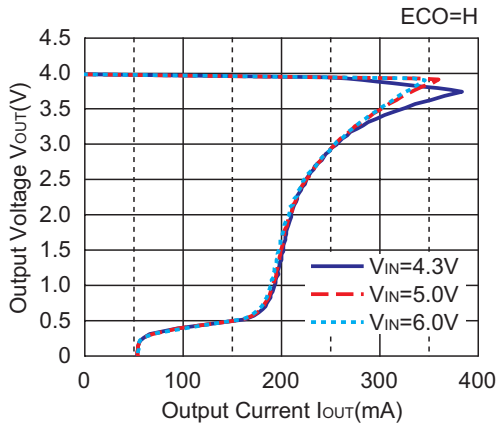
2.8V (VR1/VR2)



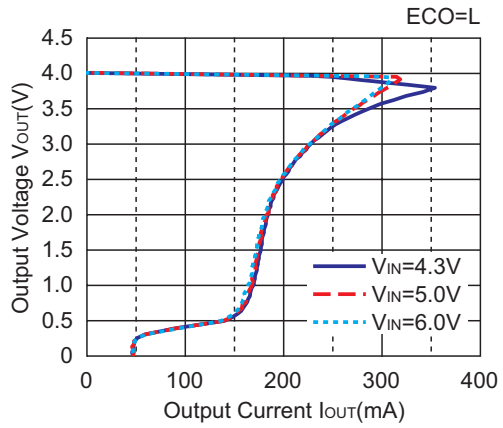
2.8V (VR1/VR2)



4.0V (VR1/VR2)

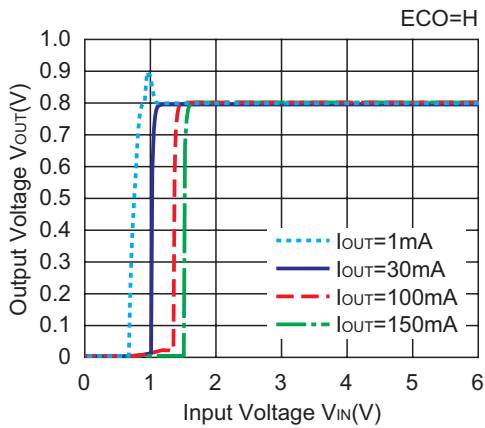


4.0V (VR1/VR2)

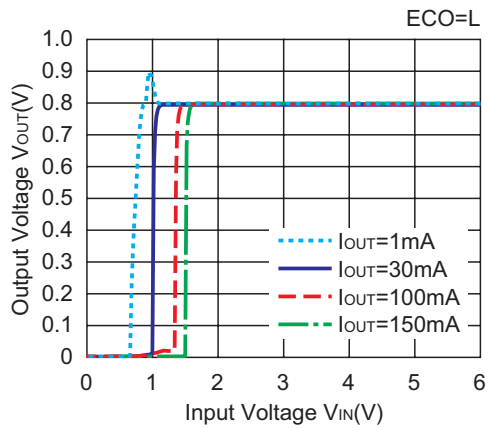


2) Output Voltage vs. Input Voltage (T_{opt}=25°C)

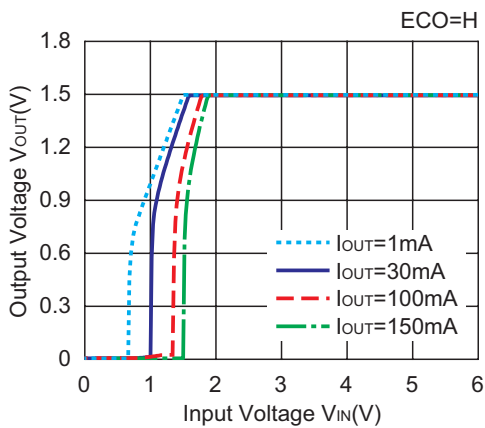
0.8V (VR1/VR2)



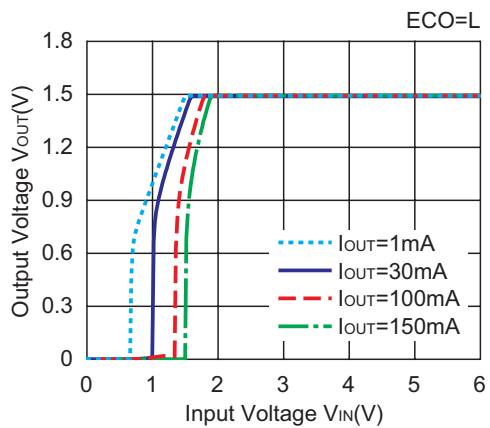
0.8V (VR1/VR2)

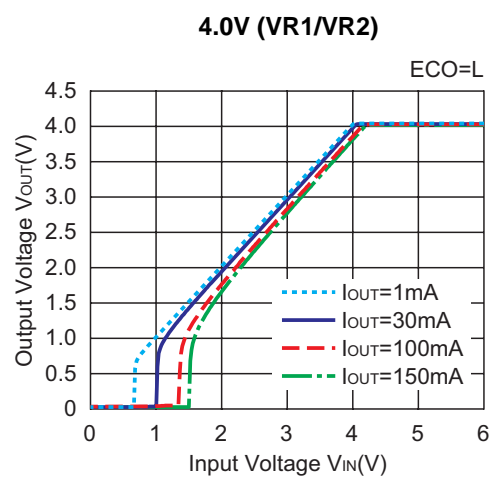
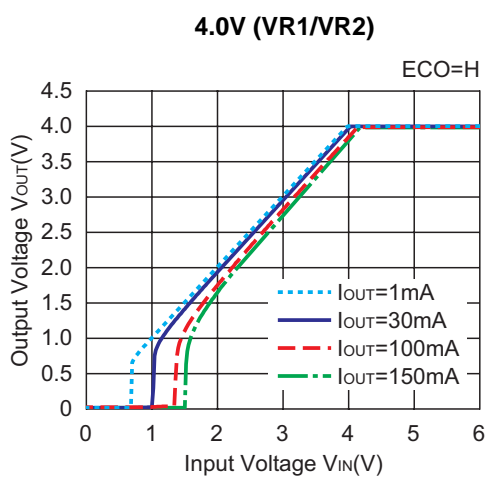
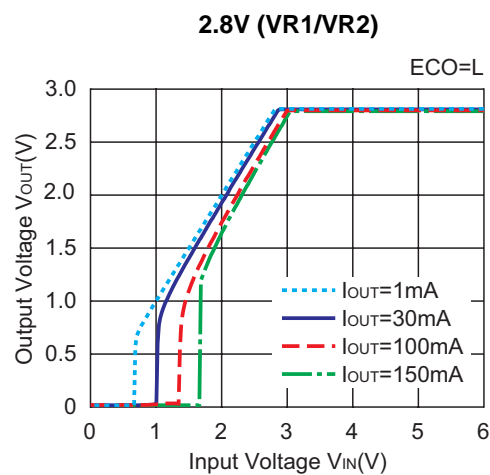
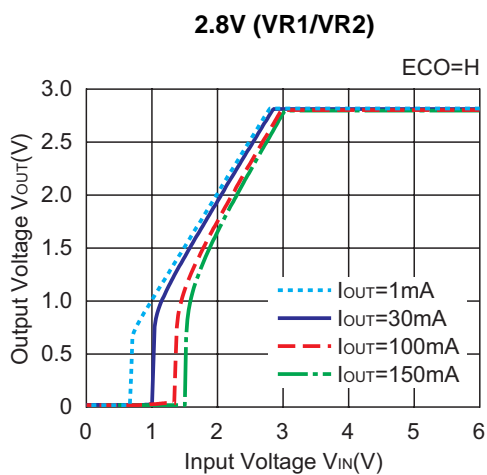


1.5V (VR1/VR2)

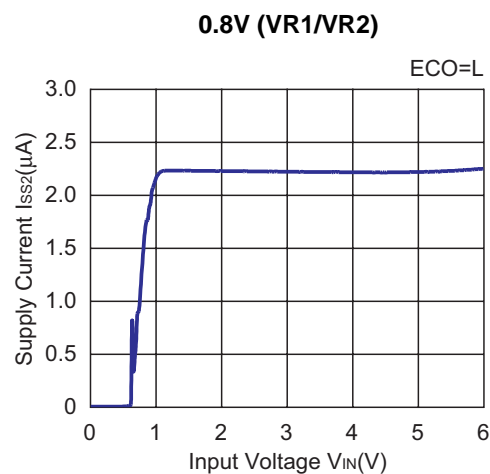
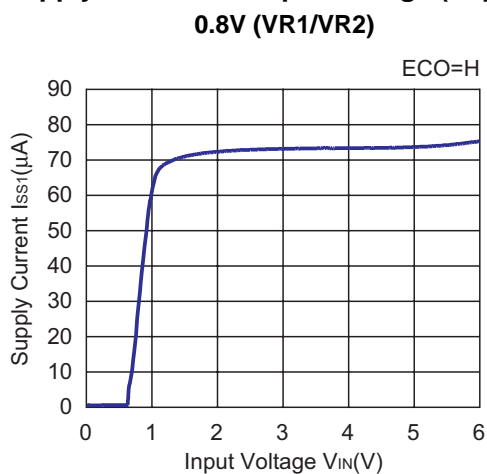


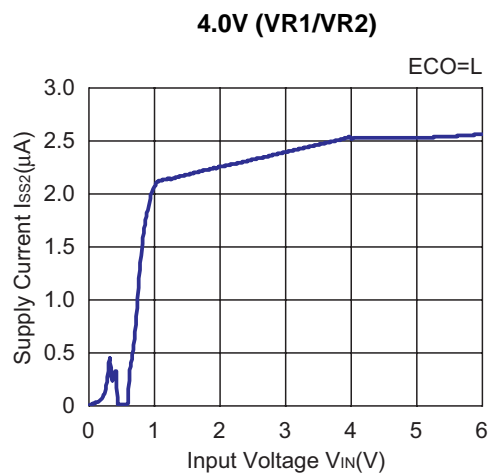
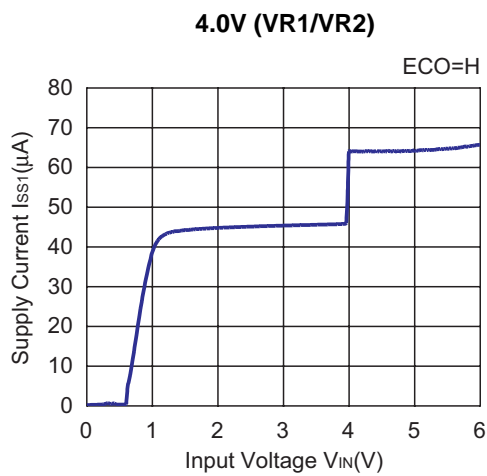
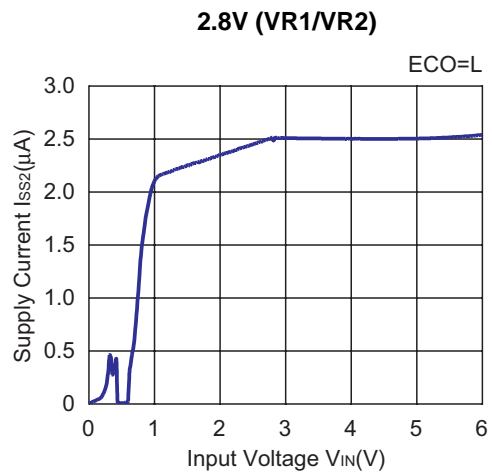
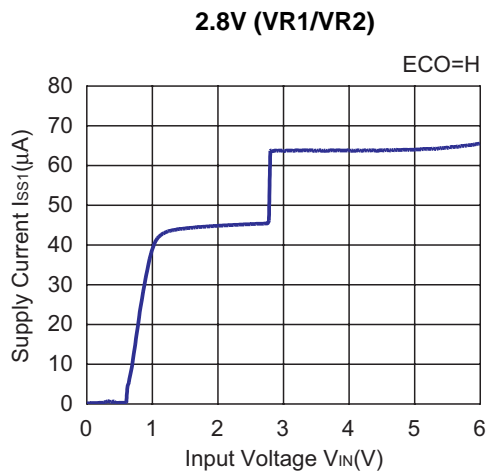
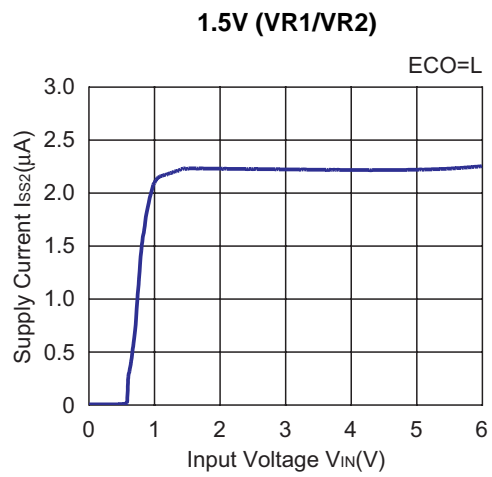
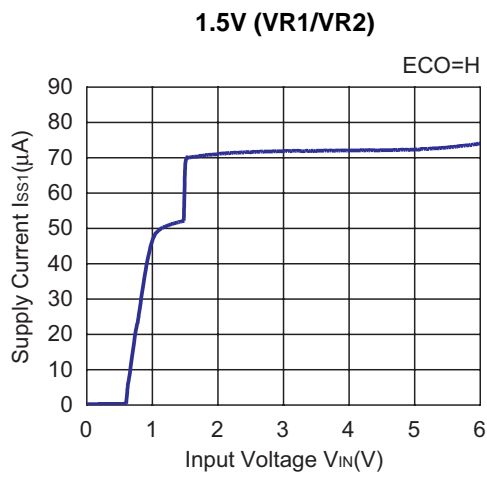
1.5V (VR1/VR2)





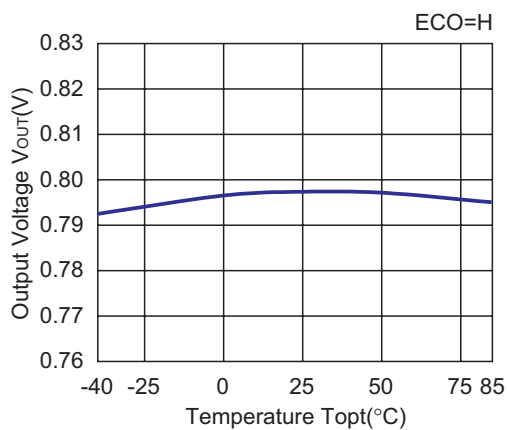
3) Supply Current vs. Input Voltage ($T_{opt}=25^{\circ}\text{C}$)



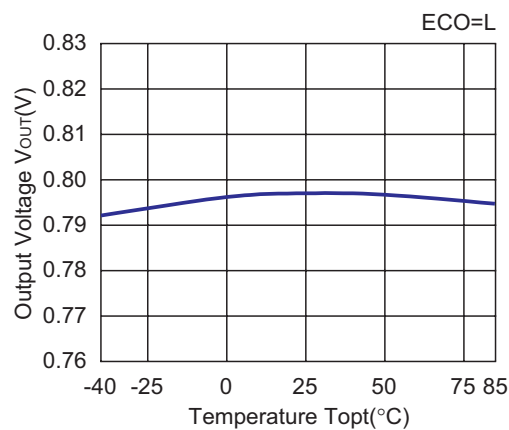


4) Output Voltage vs. Temperature

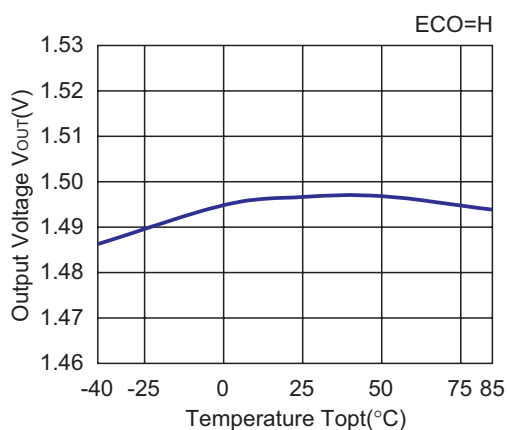
0.8V (VR1/VR2)



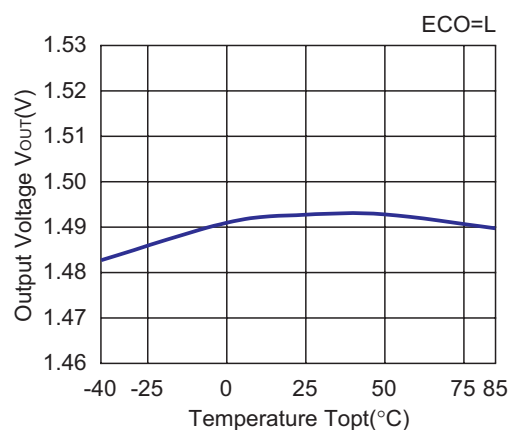
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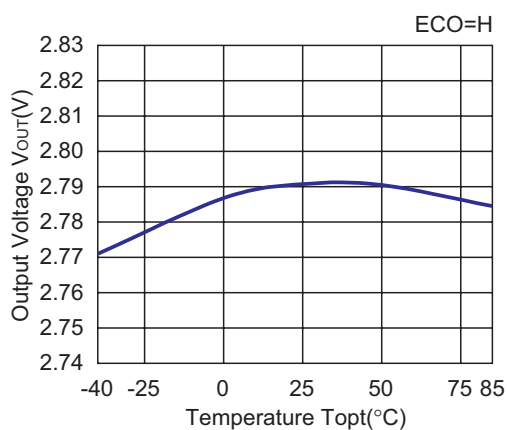
1.5V (VR1/VR2)



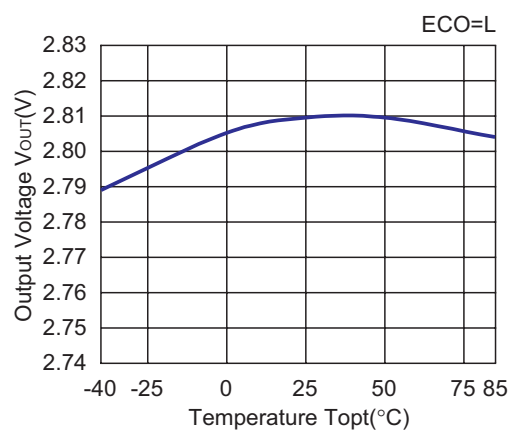
1.5V (VR1/VR2)



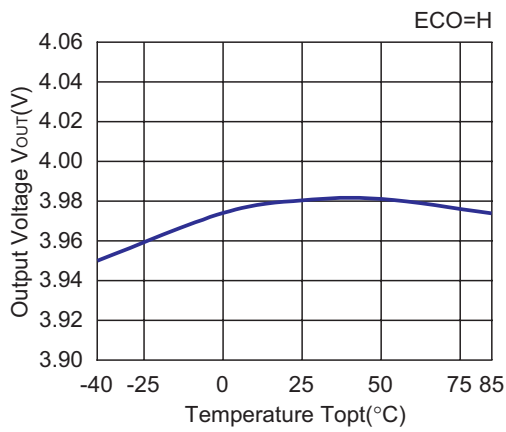
2.8V (VR1/VR2)



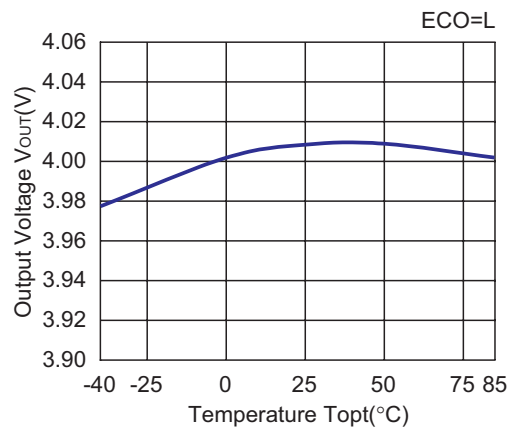
2.8V (VR1/VR2)



4.0V (VR1/VR2)

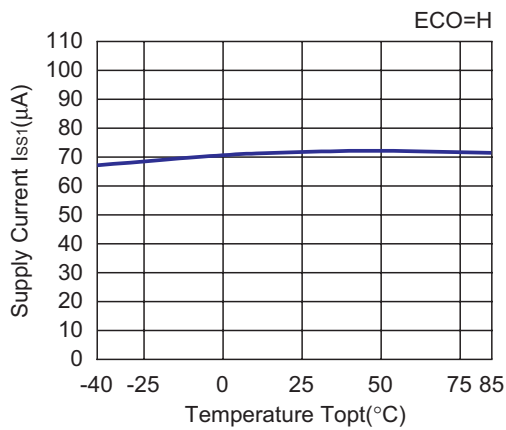


4.0V (VR1/VR2)

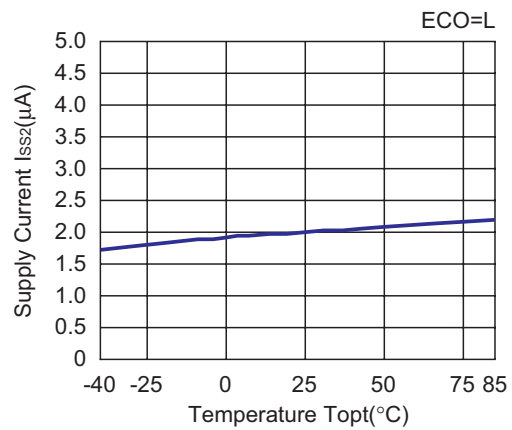


5) Supply Current vs. Temperature

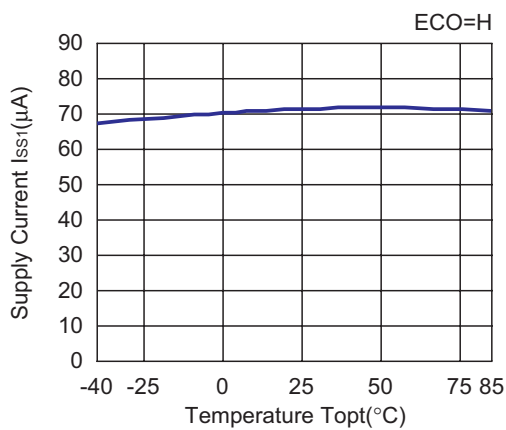
0.8V (VR1/VR2)



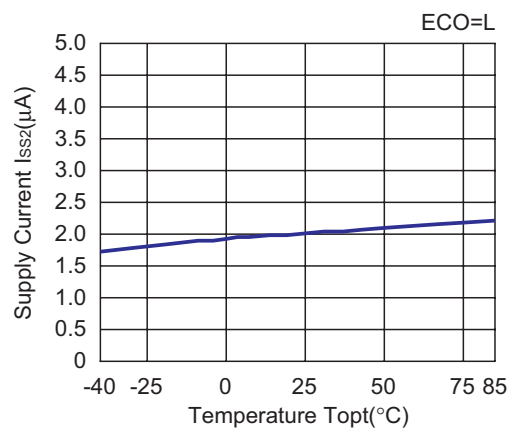
0.8V (VR1/VR2)



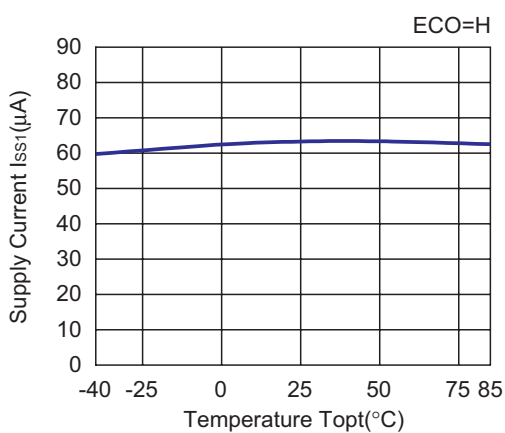
1.5V (VR1/VR2)



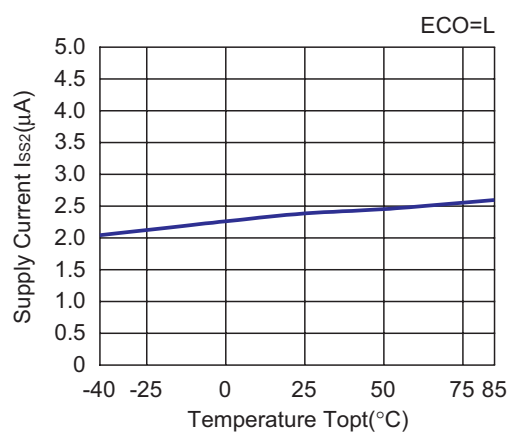
1.5V (VR1/VR2)



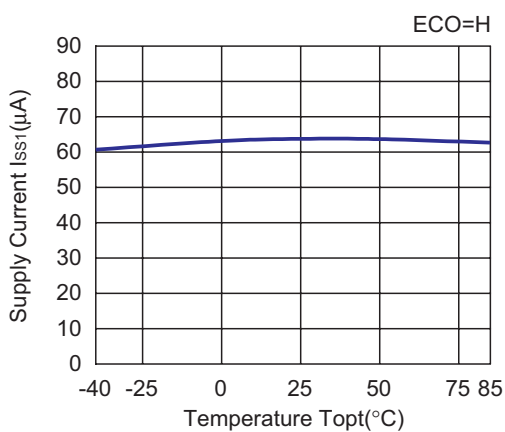
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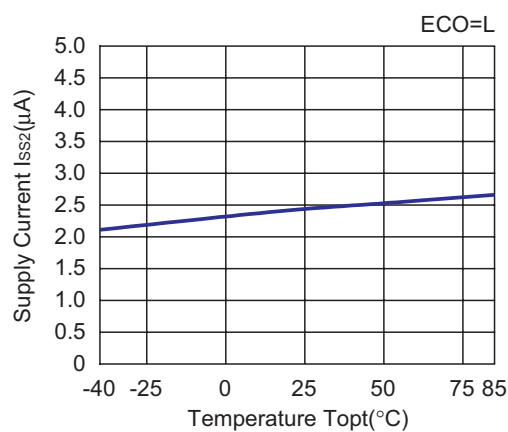
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4.0V (VR1/VR2)

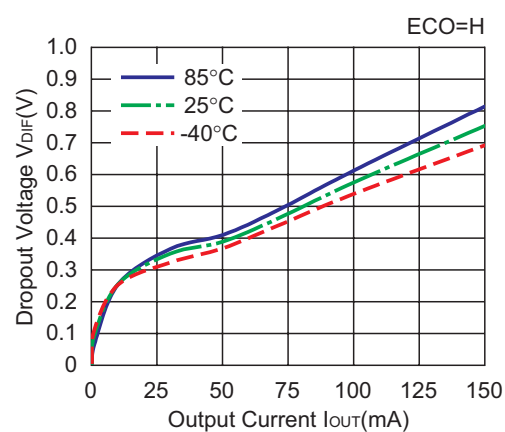


4.0V (VR1/VR2)

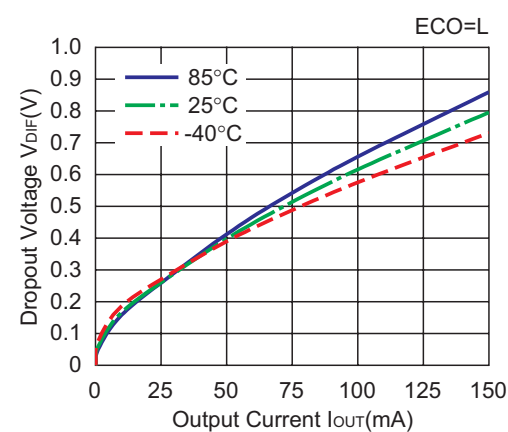


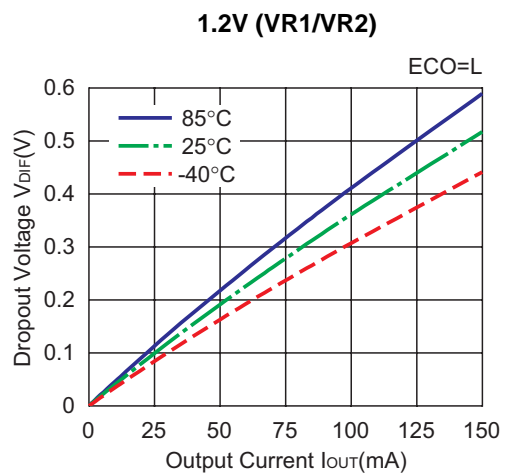
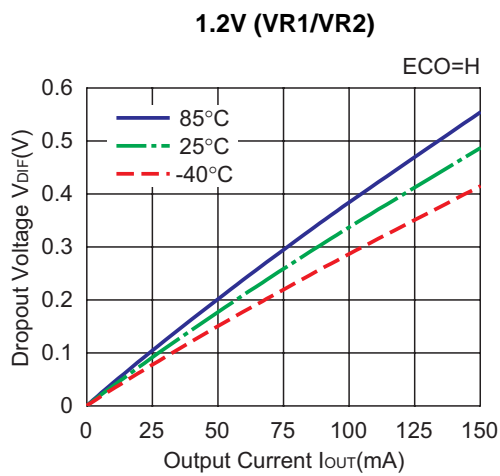
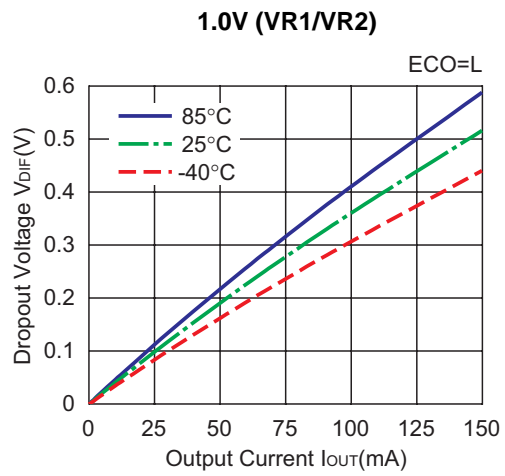
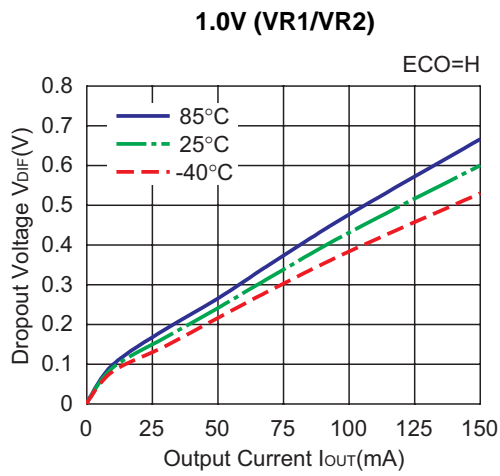
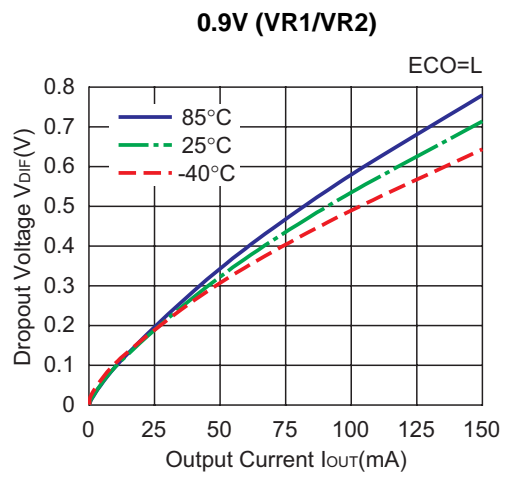
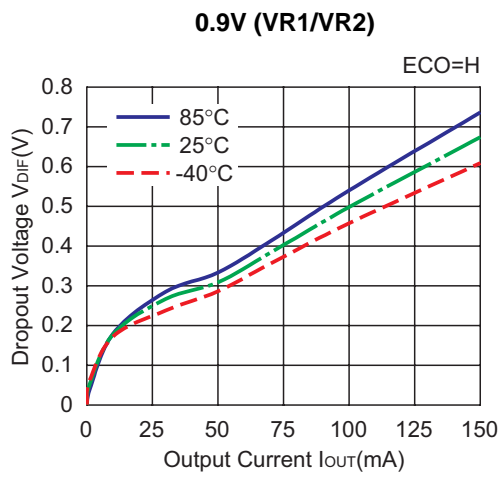
6) Dropout Voltage vs. Output Current

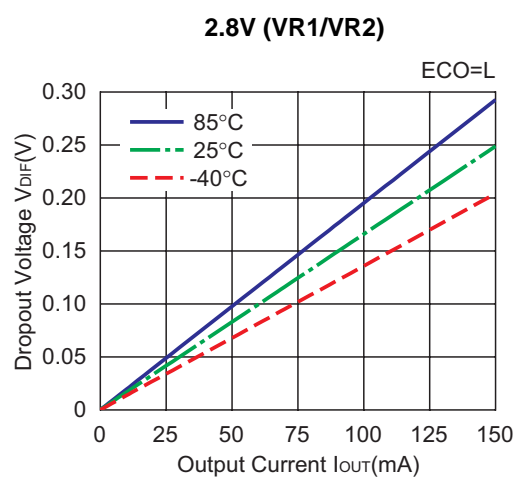
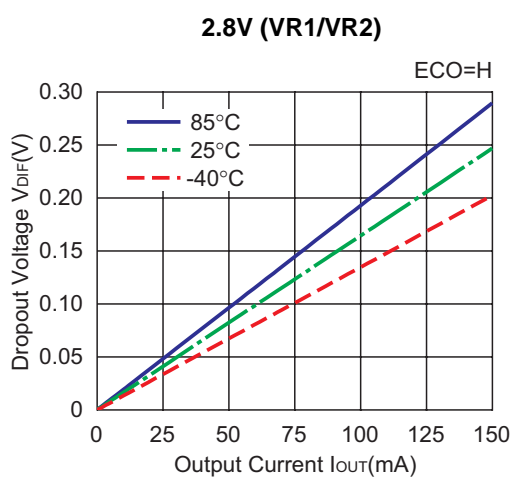
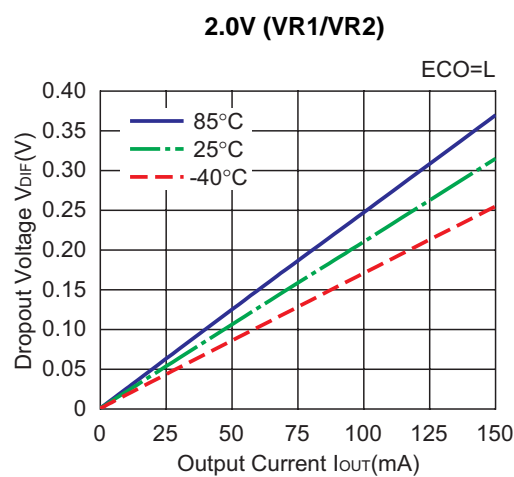
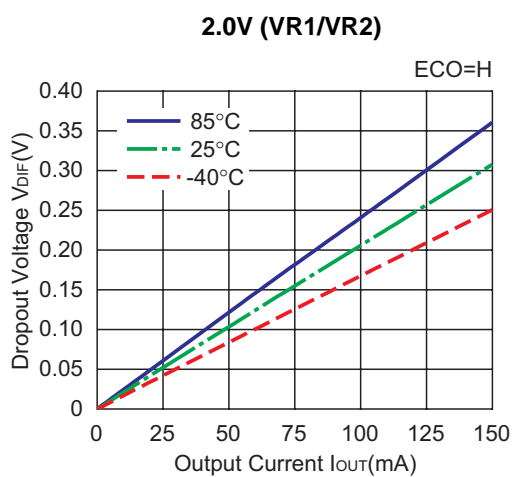
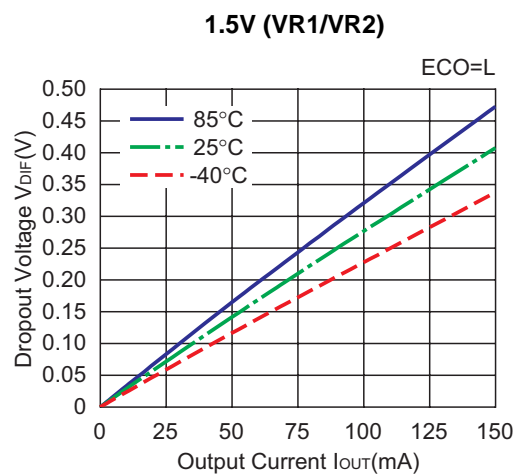
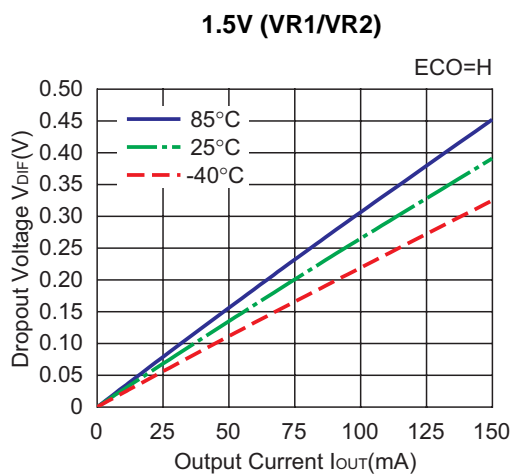
0.8V (VR1/VR2)



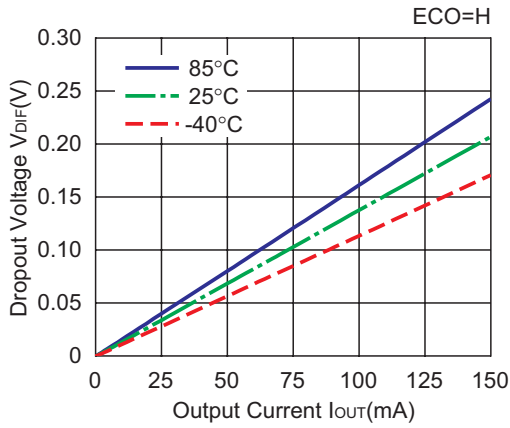
0.8V (VR1/VR2)



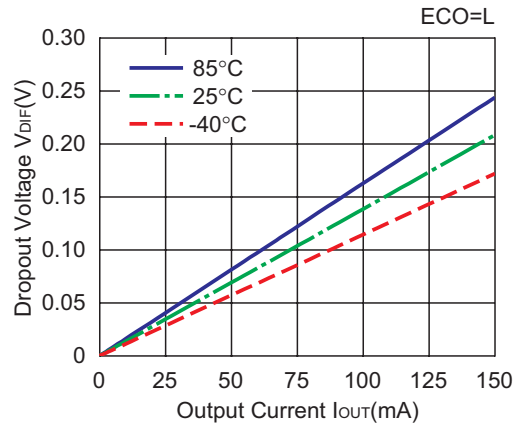




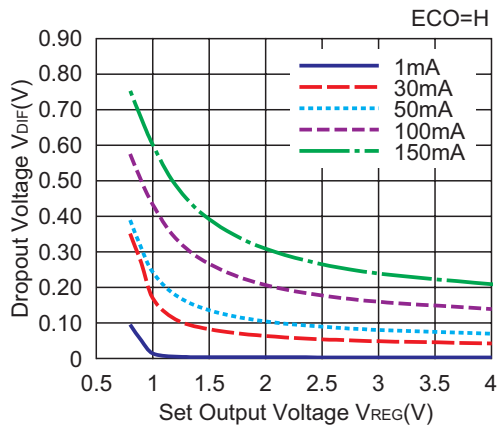
4.0V (VR1/VR2)



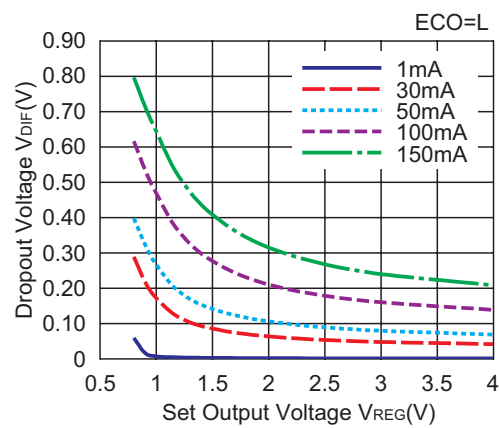
4.0V (VR1/VR2)



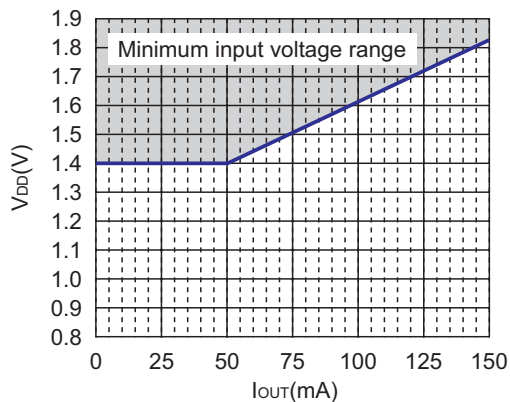
7) Dropout Voltage vs. Set Output Voltage (Topt=25°C)
R5328K (VR1/VR2)



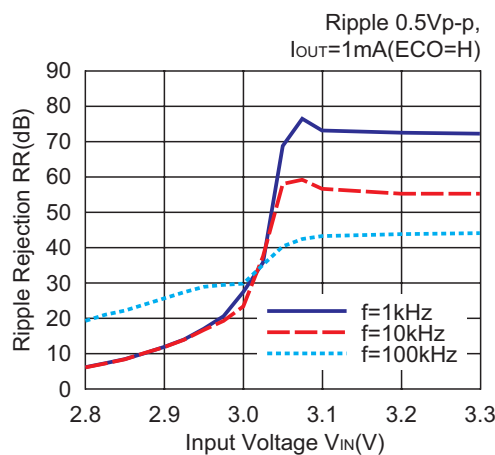
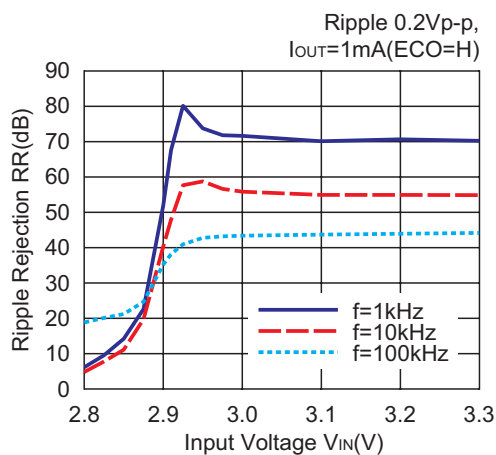
R5328K (VR1/VR2)



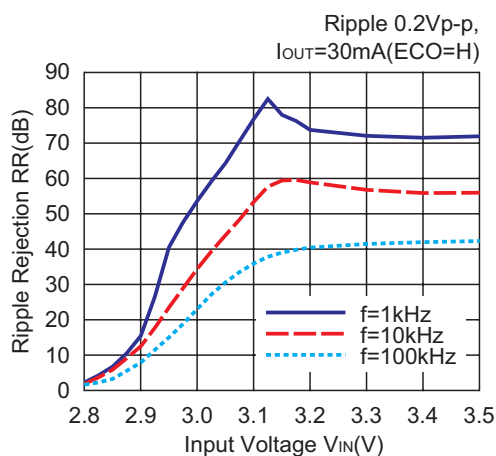
8) 0.8V (VR1/VR2) type minimum input voltage limit (Topt=25°C)



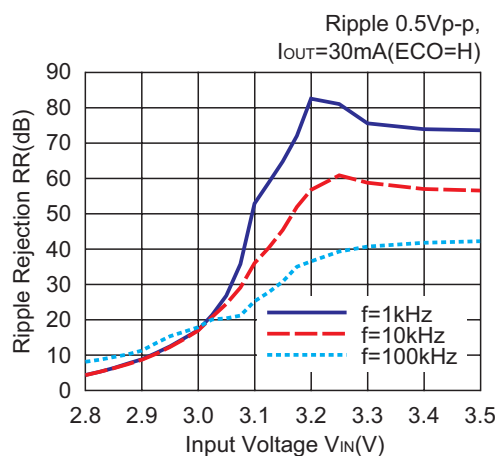
9) Ripple Rejection vs. Input Bias Voltage ($T_{opt}=25^{\circ}\text{C}$, $C_{IN}=\text{none}$, $C_{OUT}=\text{Ceramic } 1.0\mu\text{F}$, $\text{ECO}=\text{H}$)
2.8V (VR1/VR2)



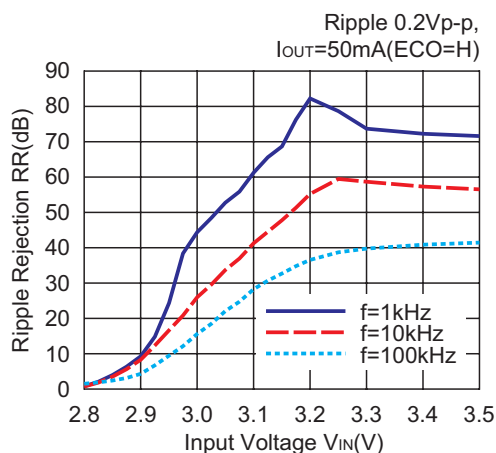
2.8V (VR1/VR2)



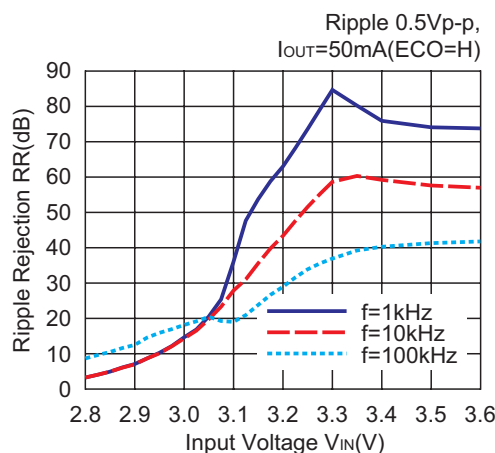
2.8V (VR1/VR2)



2.8V (VR1/VR2)

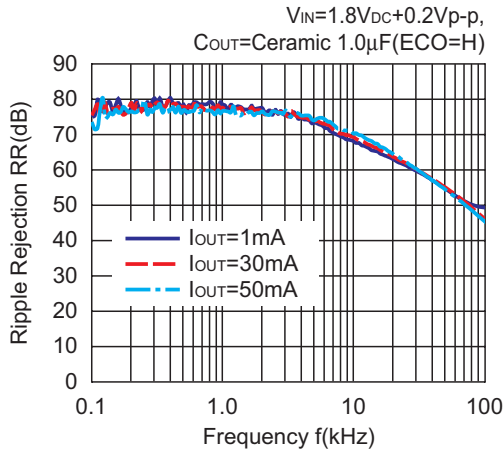


2.8V (VR1/VR2)

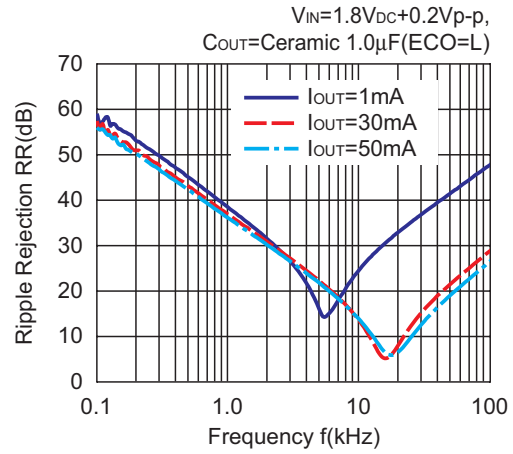


10) Ripple Rejection vs. Frequency (Topt=25°C, CIN=none)

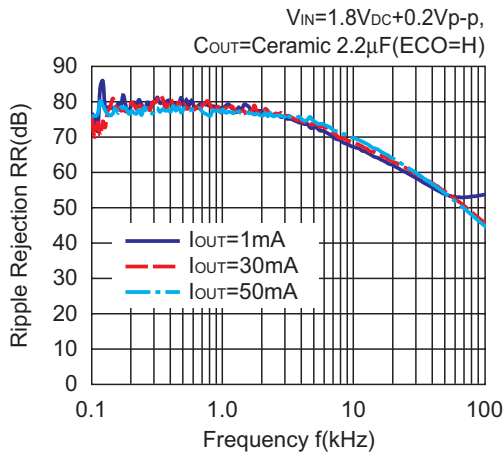
0.8V (VR1/VR2)



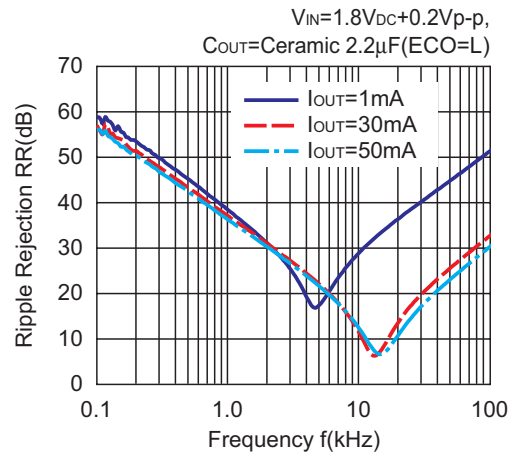
0.8V (VR1/VR2)



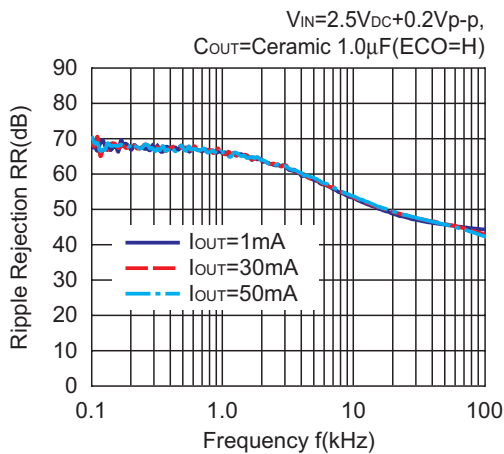
0.8V (VR1/VR2)



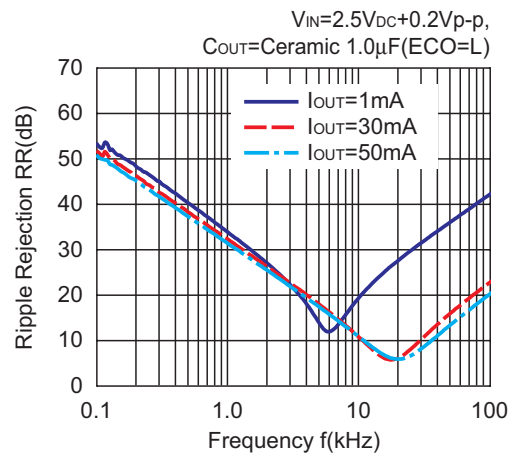
0.8V (VR1/VR2)



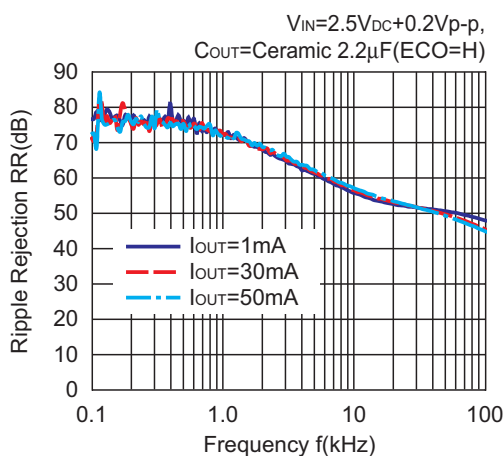
1.5V (VR1/VR2)



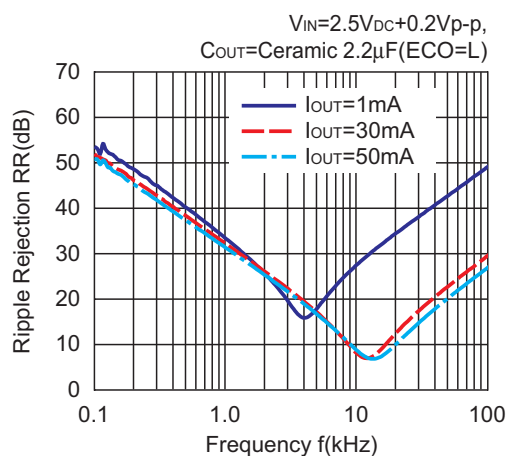
1.5V (VR1/VR2)



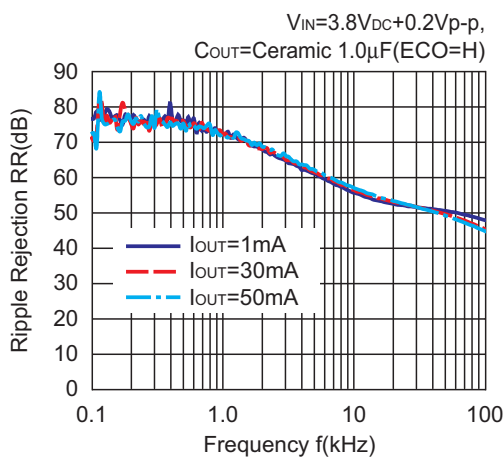
1.5V (VR1/VR2)



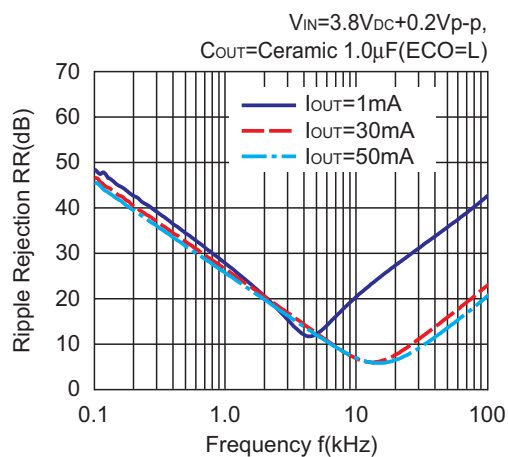
1.5V (VR1/VR2)



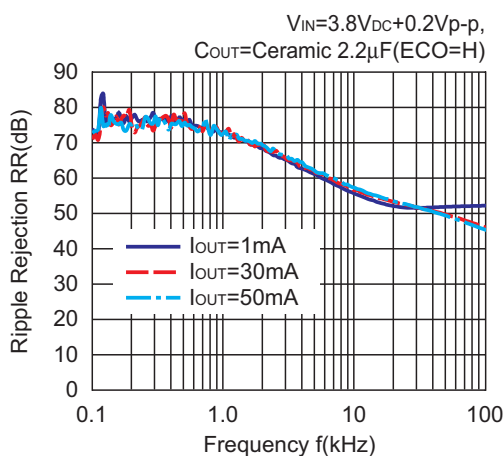
2.8V (VR1/VR2)



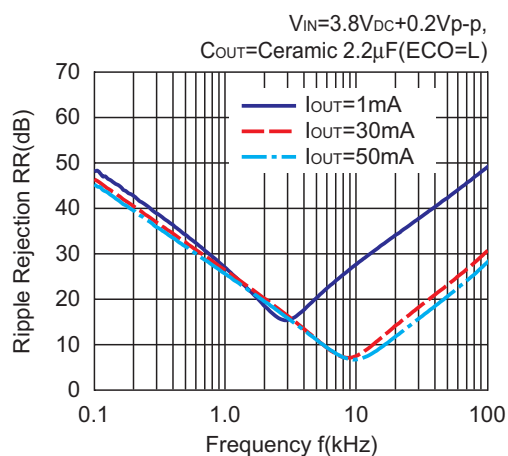
2.8V (VR1/VR2)



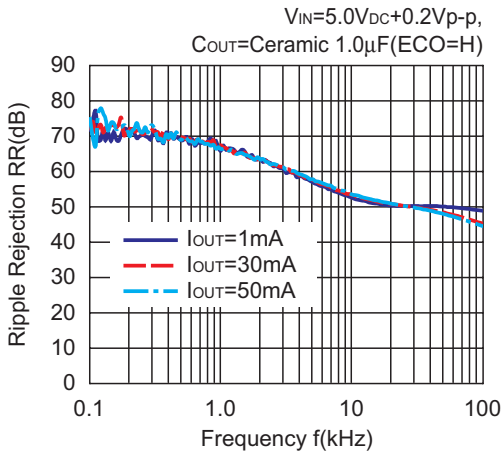
2.8V (VR1/VR2)



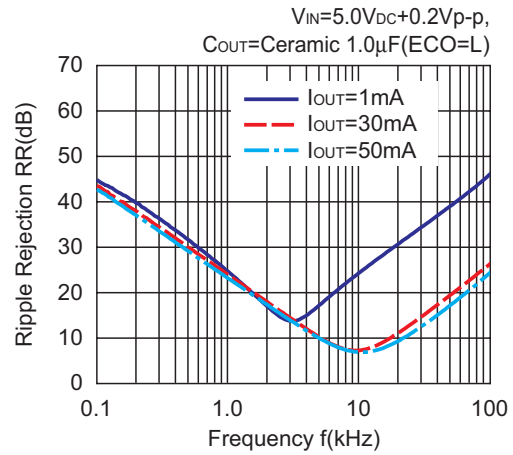
2.8V (VR1/VR2)



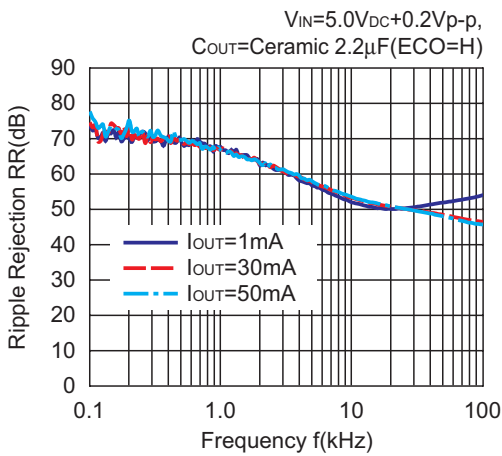
4.0V (VR1/VR2)



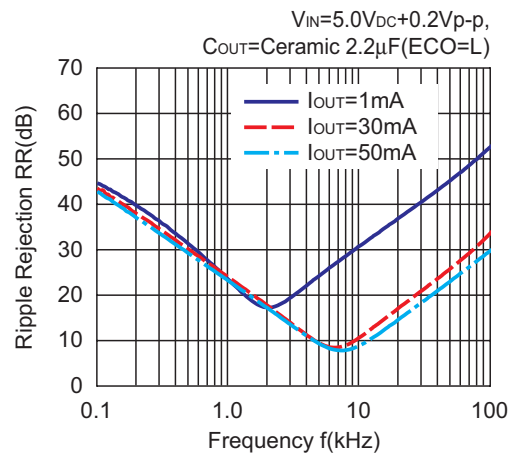
4.0V (VR1/VR2)



4.0V (VR1/VR2)

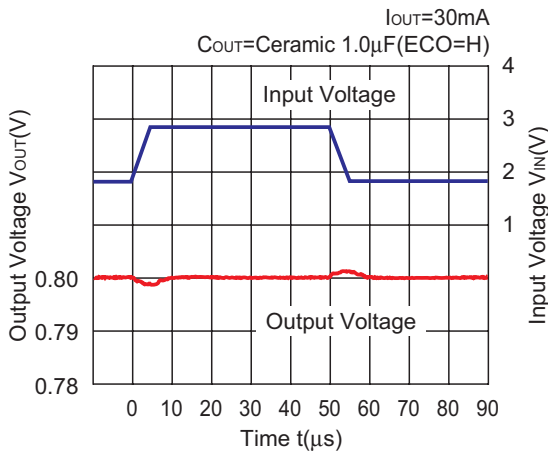


4.0V (VR1/VR2)

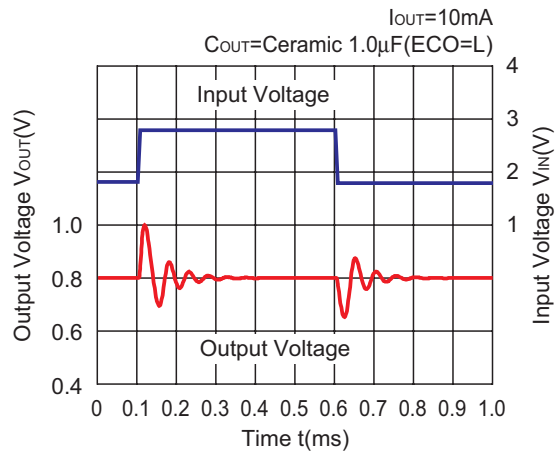


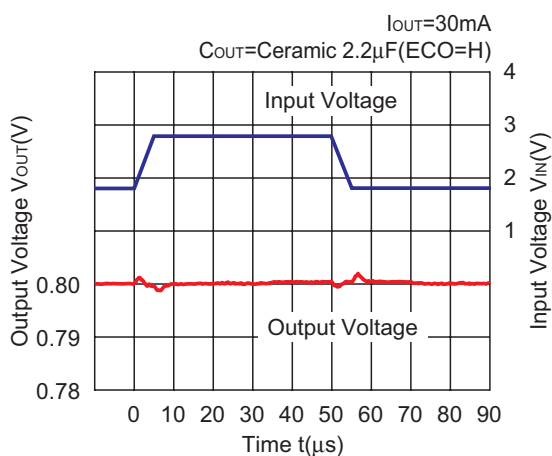
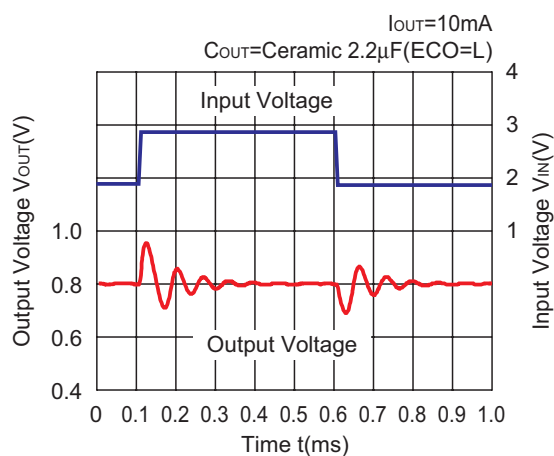
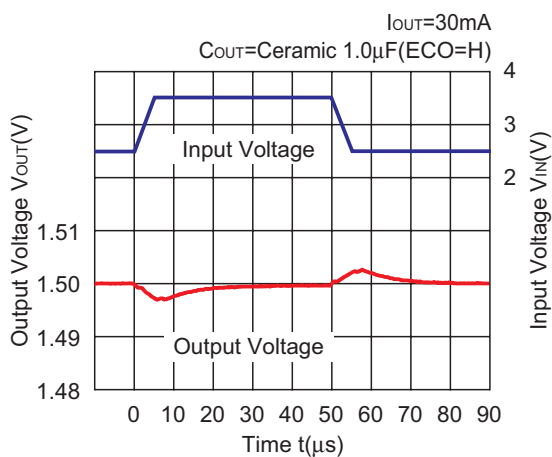
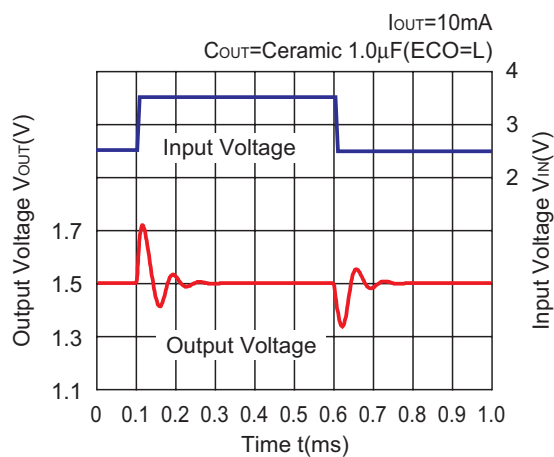
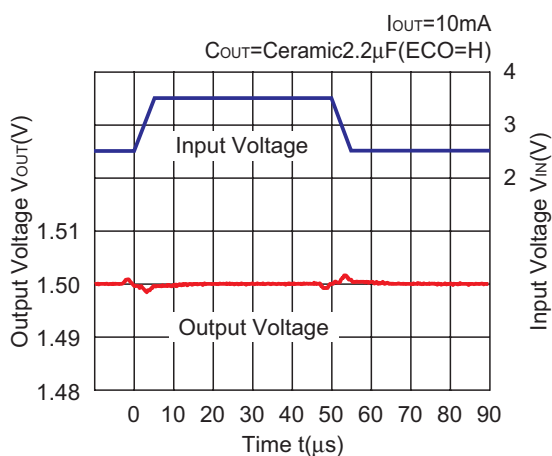
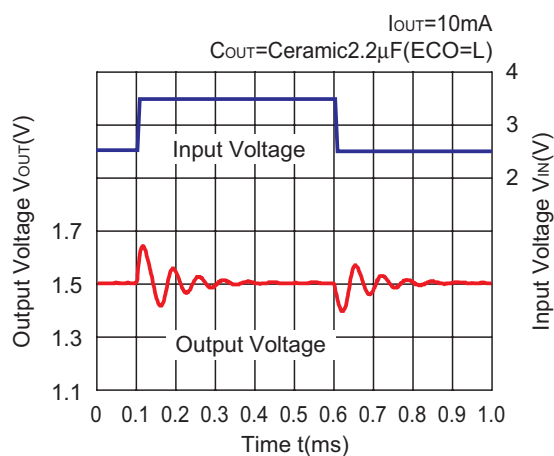
11) Input Transient Response ($C_{IN}=\text{none}$)

0.8V (VR1/VR2)

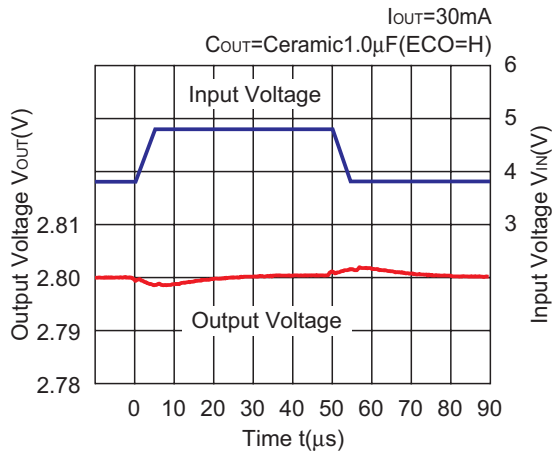


0.8V (VR1/VR2)

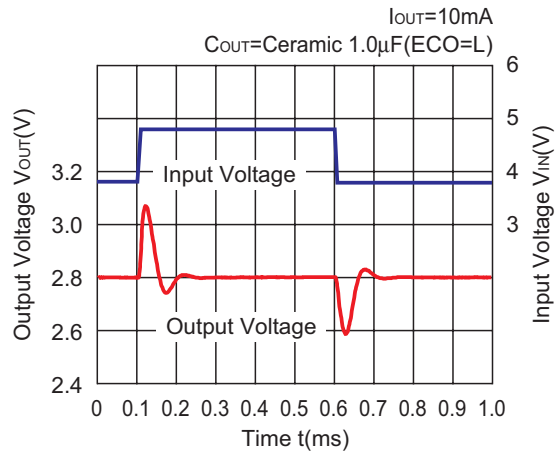


0.8V (VR1/VR2)**0.8V (VR1/VR2)****1.5V (VR1/VR2)****1.5V (VR1/VR2)****1.5V (VR1/VR2)****1.5V (VR1/VR2)**

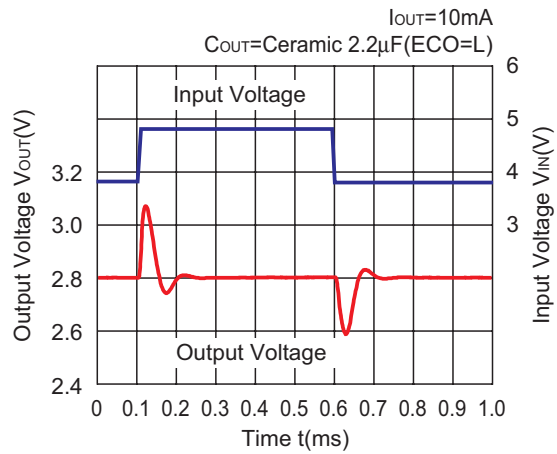
2.8V (VR1/VR2)



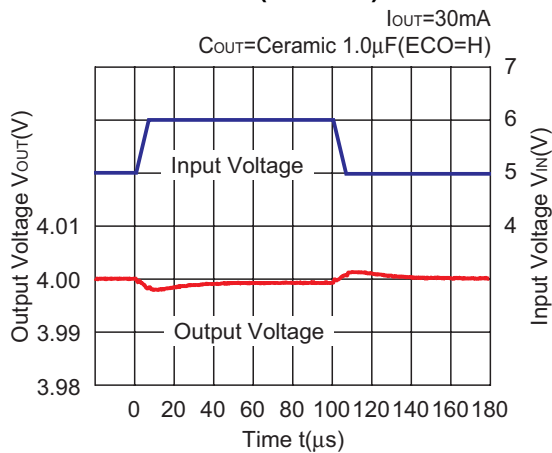
2.8V (VR1/VR2)



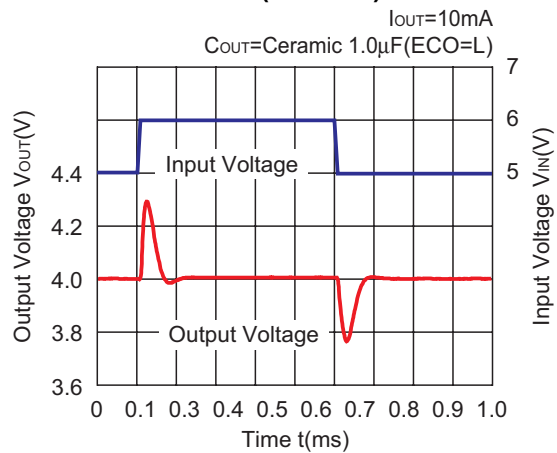
2.8V (VR1/VR2)



4.0V (VR1/VR2)

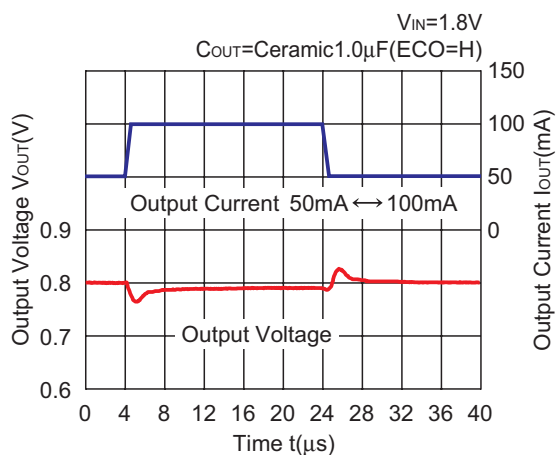


4.0V (VR1/VR2)

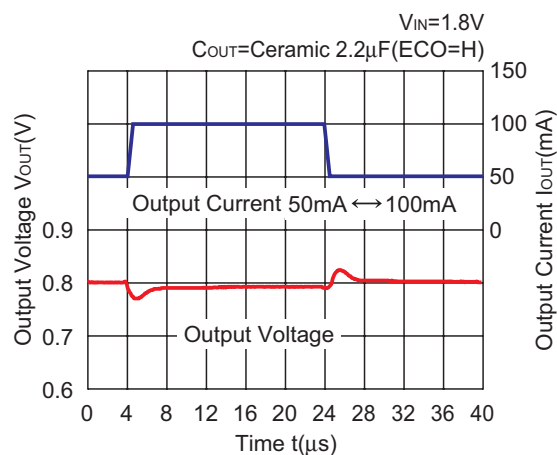


12) Load Transient Response (C_{IN} =Ceramic 1.0 μ F)

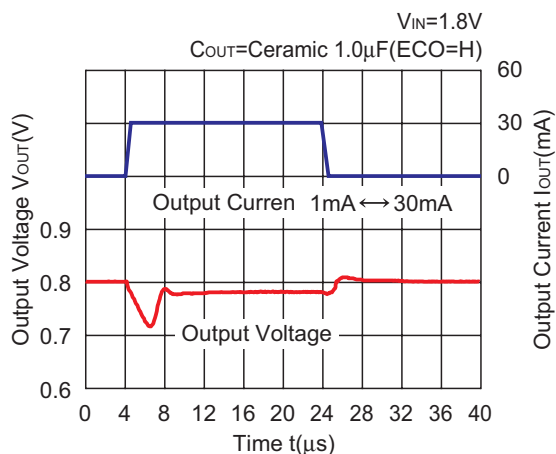
0.8V (VR1/VR2)



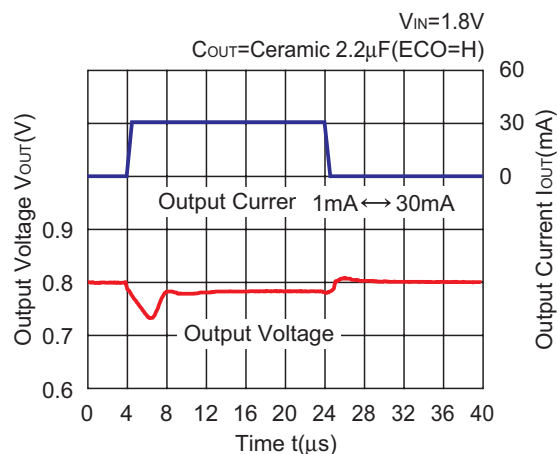
0.8V (VR1/VR2)



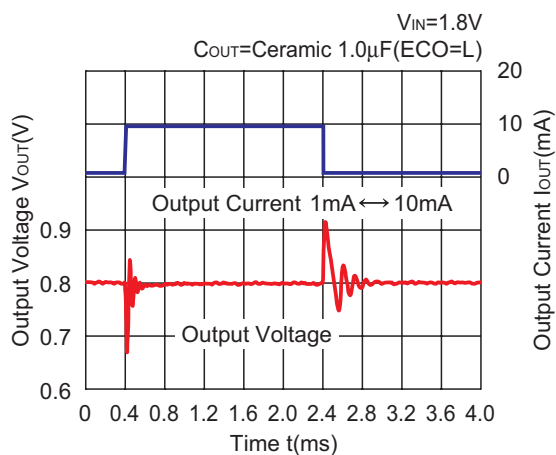
0.8V (VR1/VR2)



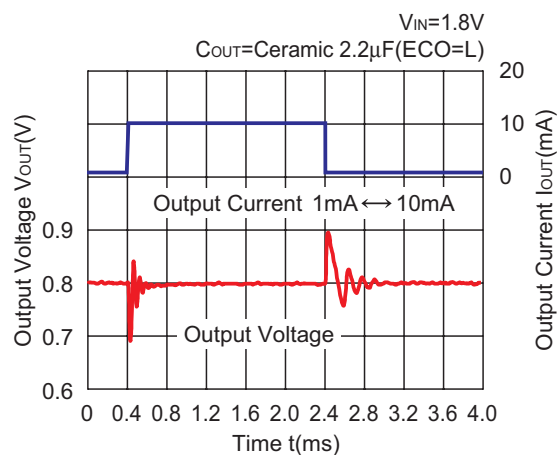
0.8V (VR1/VR2)



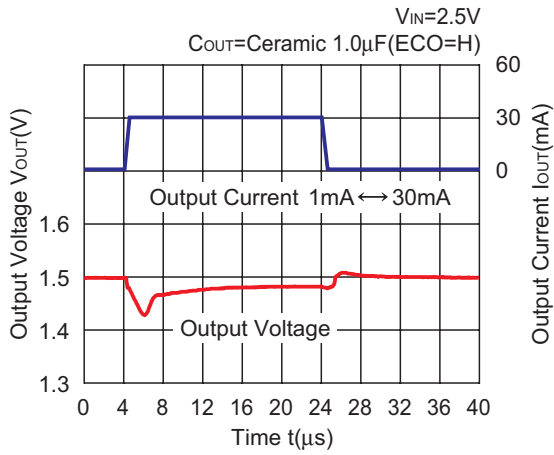
0.8V (VR1/VR2)



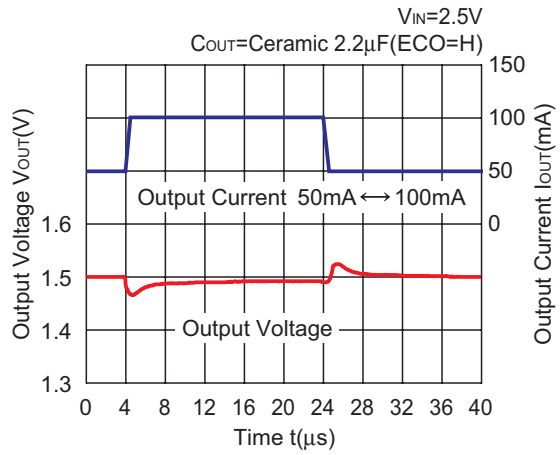
0.8V (VR1/VR2)



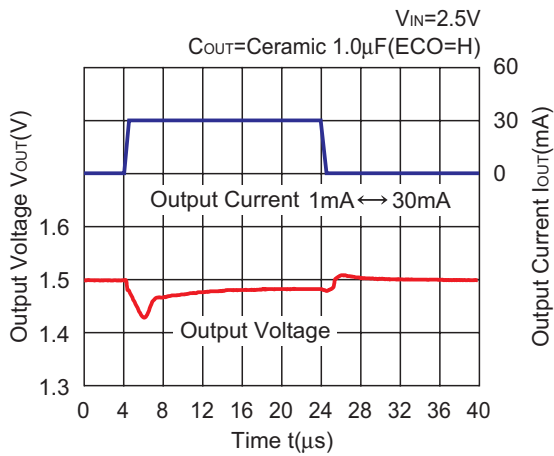
1.5V (VR1/VR2)



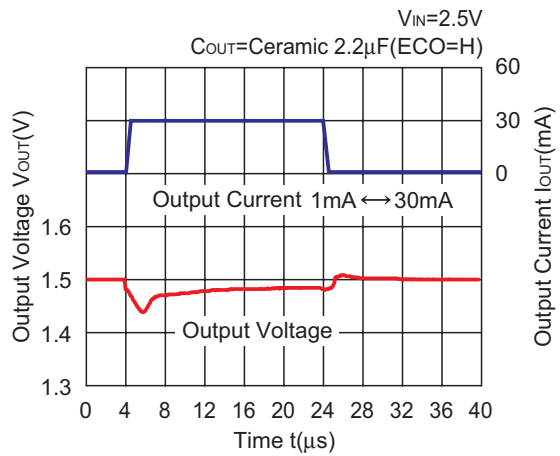
1.5V (VR1/VR2)



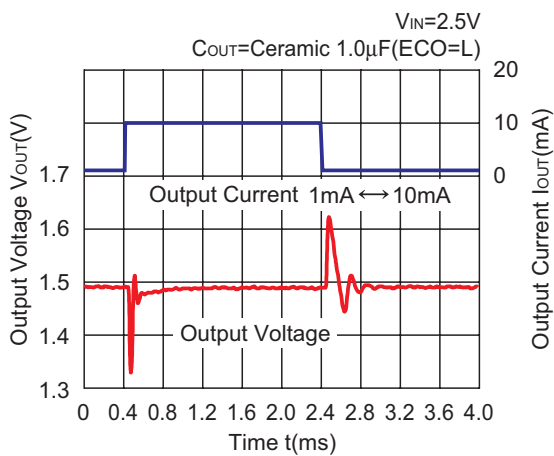
1.5V (VR1/VR2)



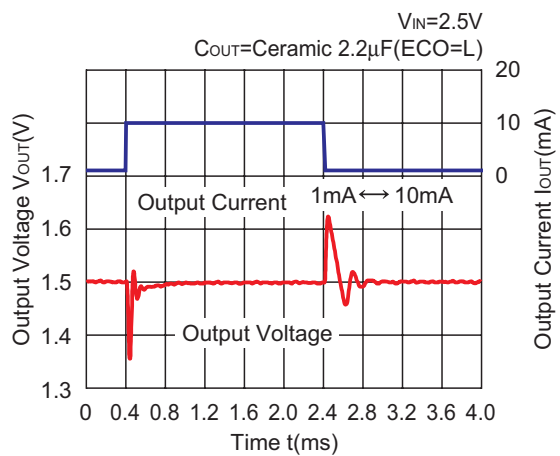
1.5V (VR1/VR2)

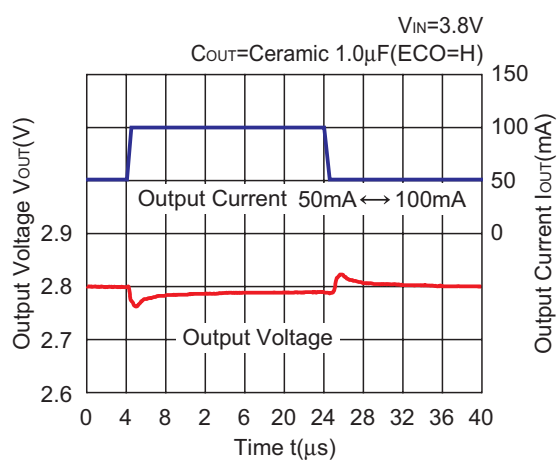
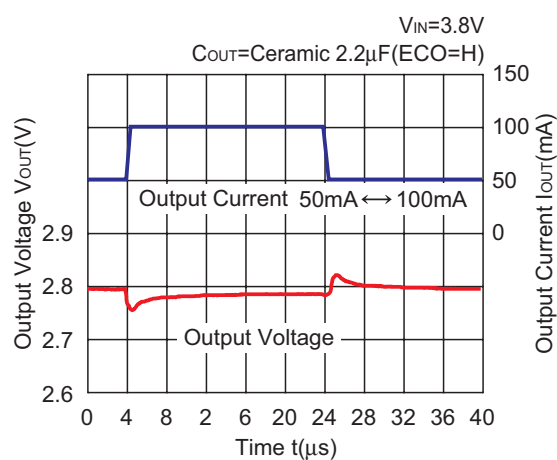
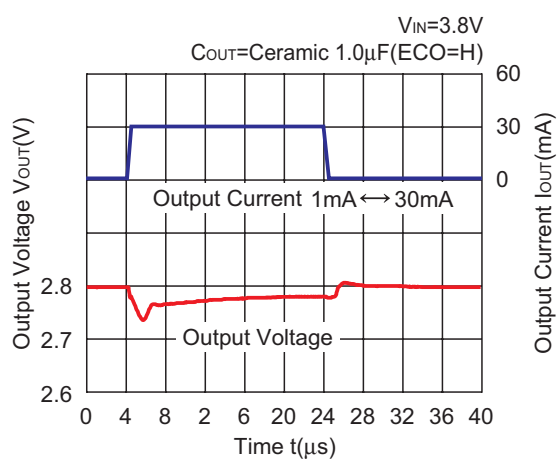
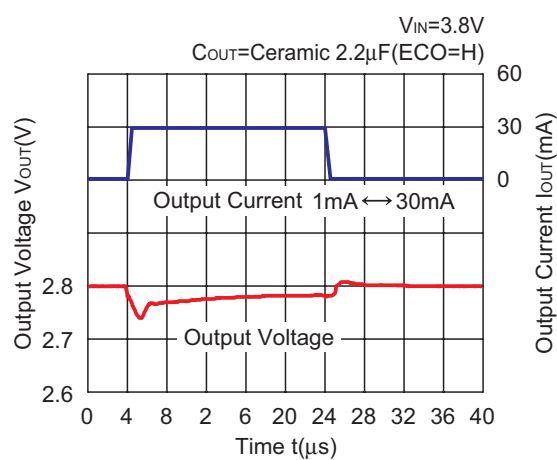
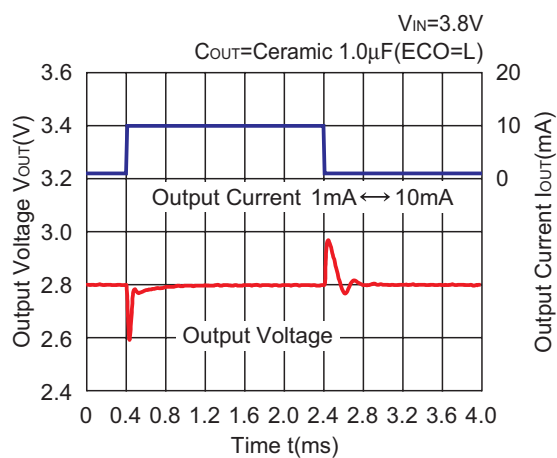
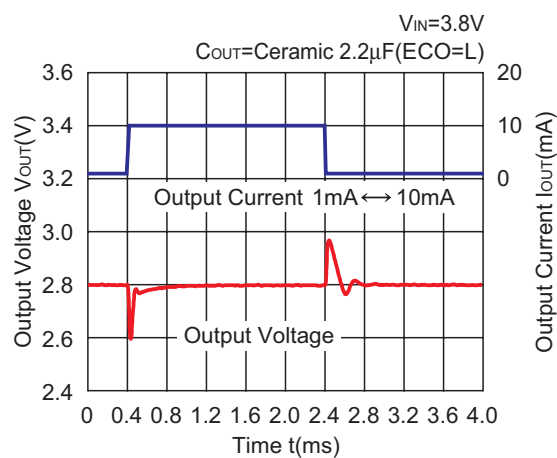


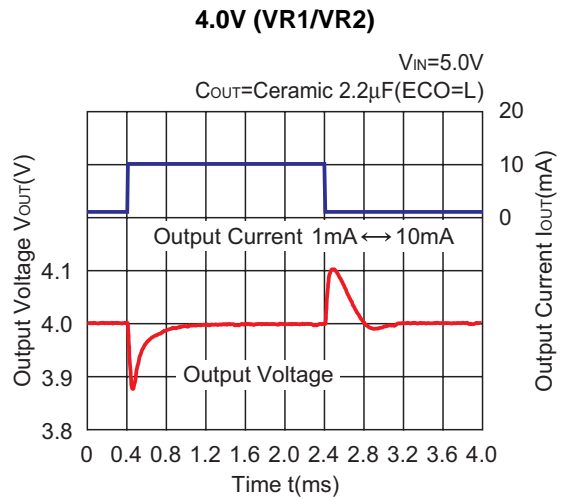
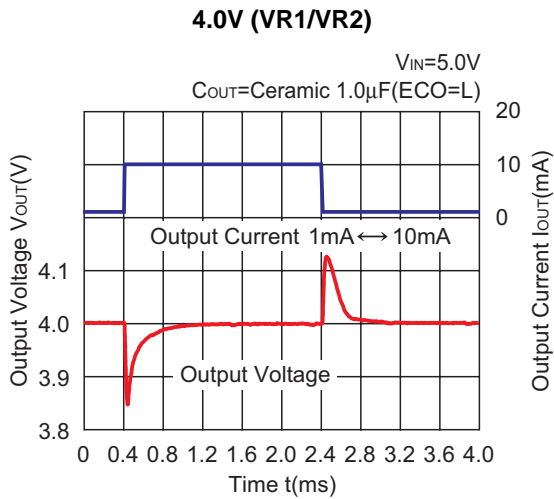
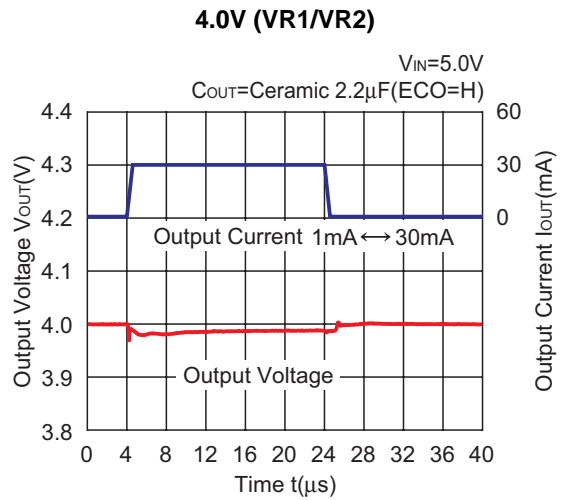
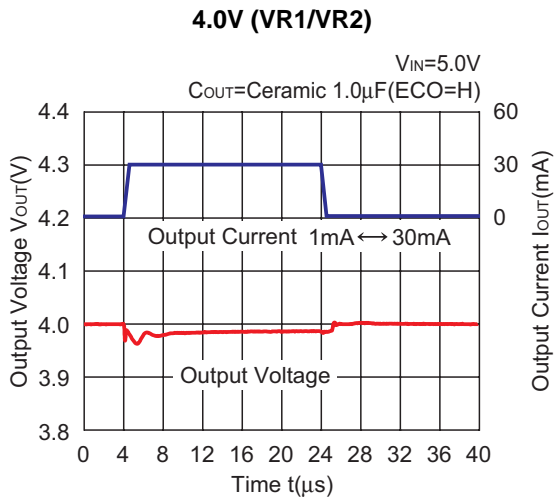
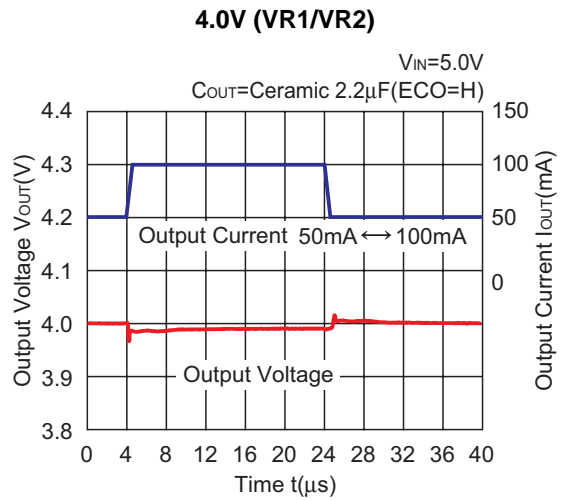
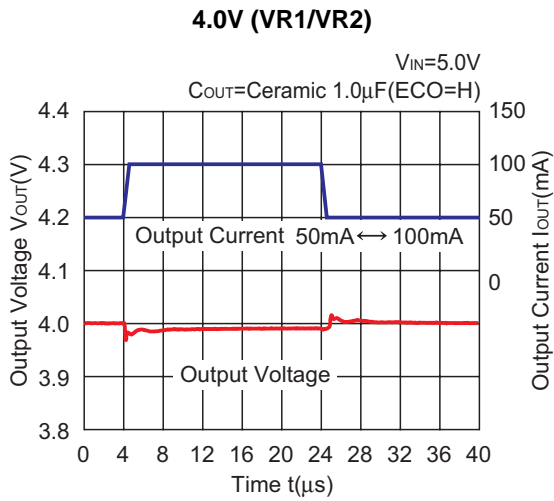
1.5V (VR1/VR2)



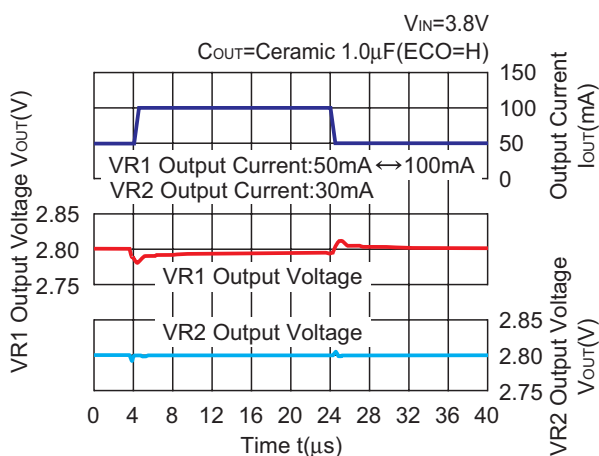
1.5V (VR1/VR2)



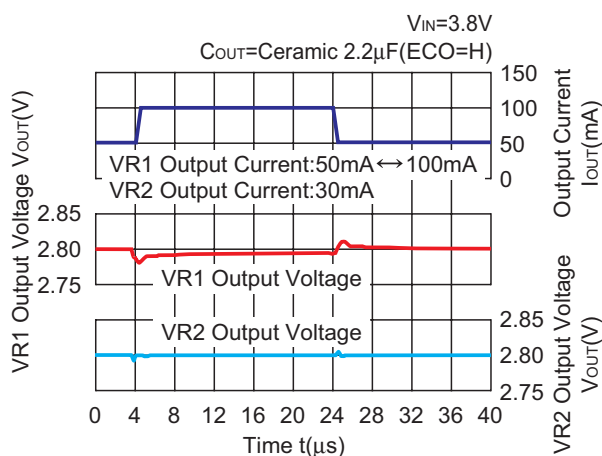
2.8V (VR1/VR2)**2.8V (VR1/VR2)****2.8V (VR1/VR2)****2.8V (VR1/VR2)****2.8V (VR1/VR2)****2.8V (VR1/VR2)**



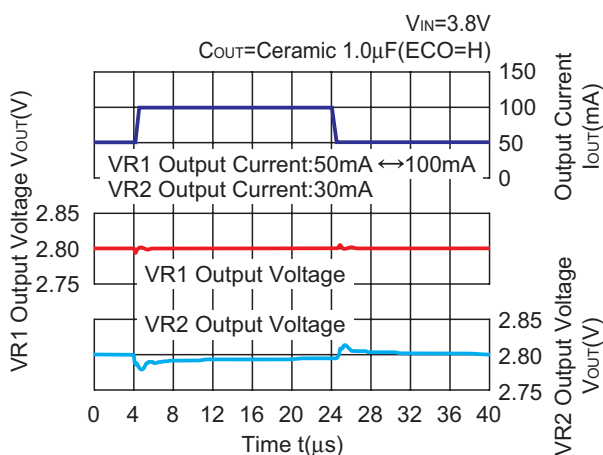
2.8V (VR1/VR2)



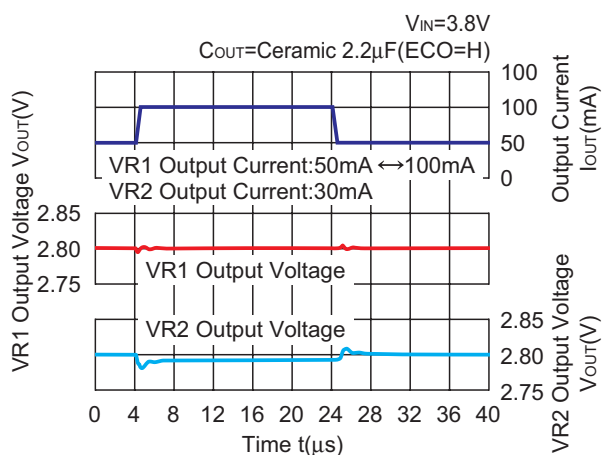
2.8V (VR1/VR2)



2.8V (VR1/VR2)

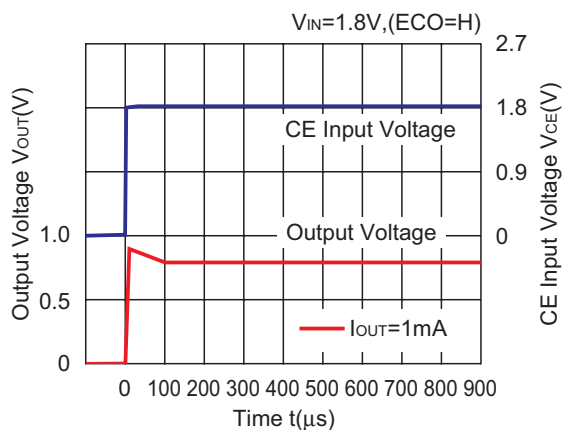


2.8V (VR1/VR2)

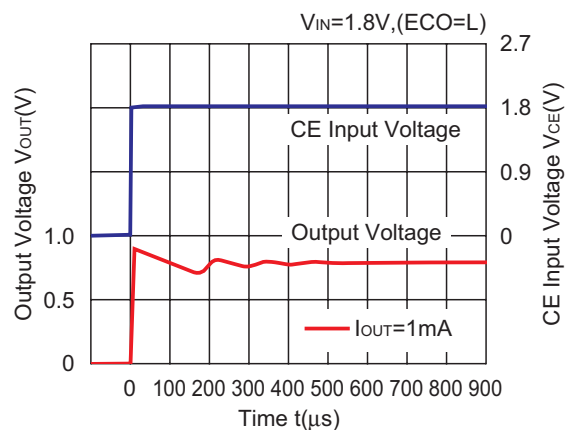


13) Turn on speed by CE pin control ($C_{IN} = 1.0\mu\text{F}$, $C_{OUT} = \text{Ceramic } 1.0\mu\text{F}$)

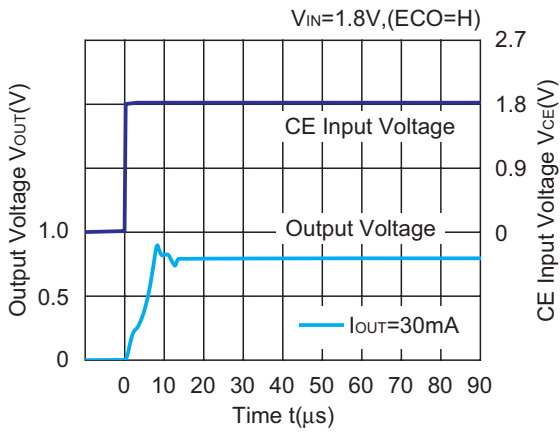
0.8V (VR1/VR2)



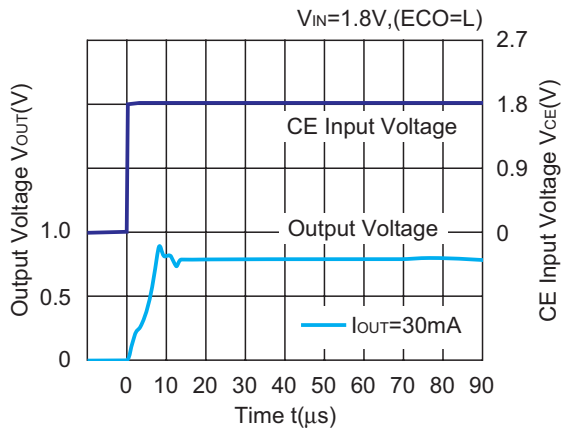
0.8V (VR1/VR2)



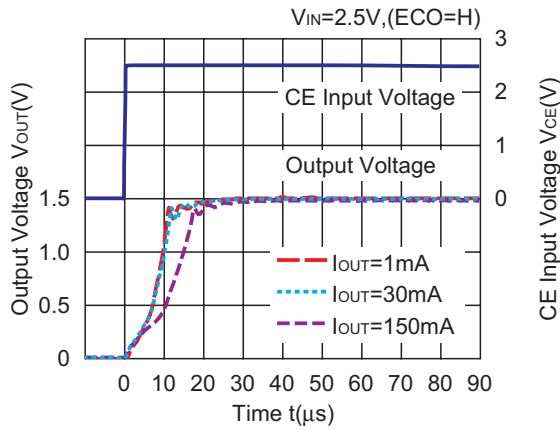
0.8V (VR1/VR2)



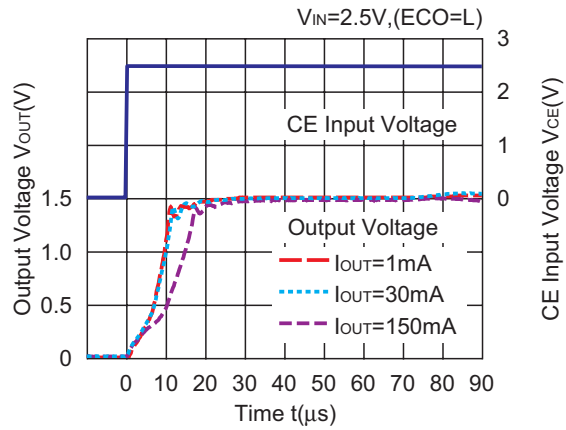
0.8V (VR1/VR2)



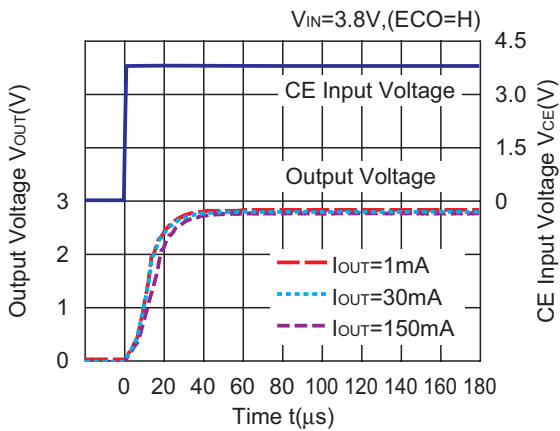
1.5V (VR1/VR2)



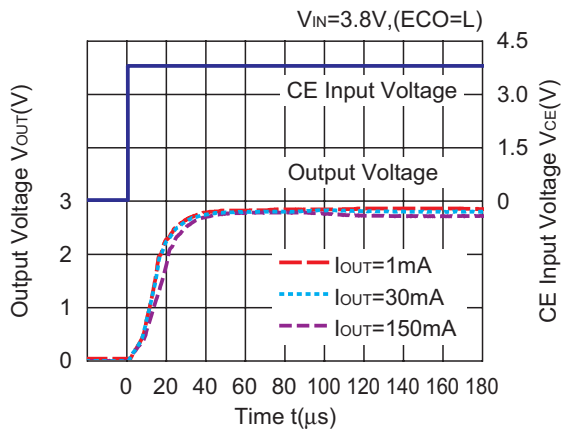
1.5V (VR1/VR2)

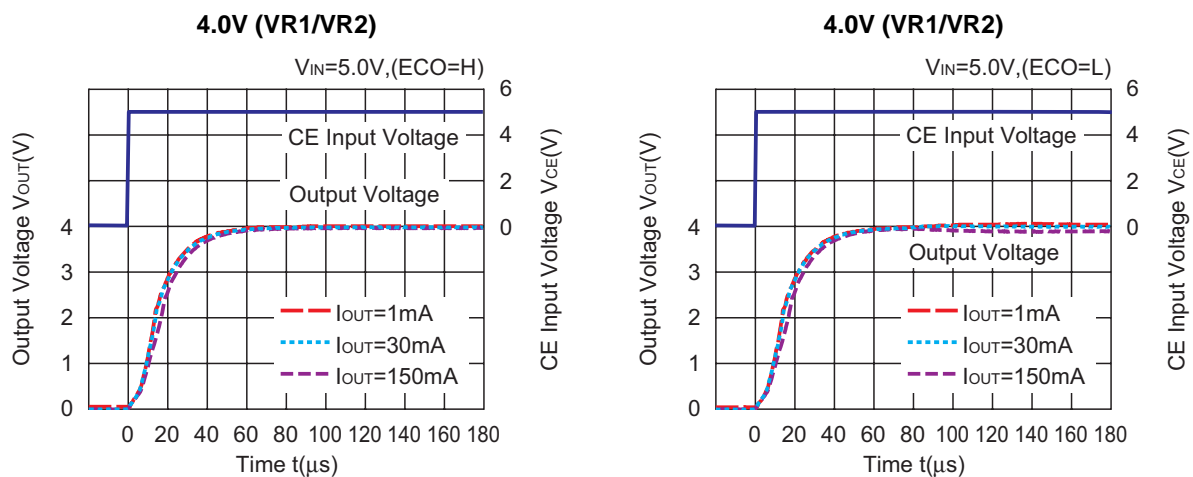


2.8V (VR1/VR2)

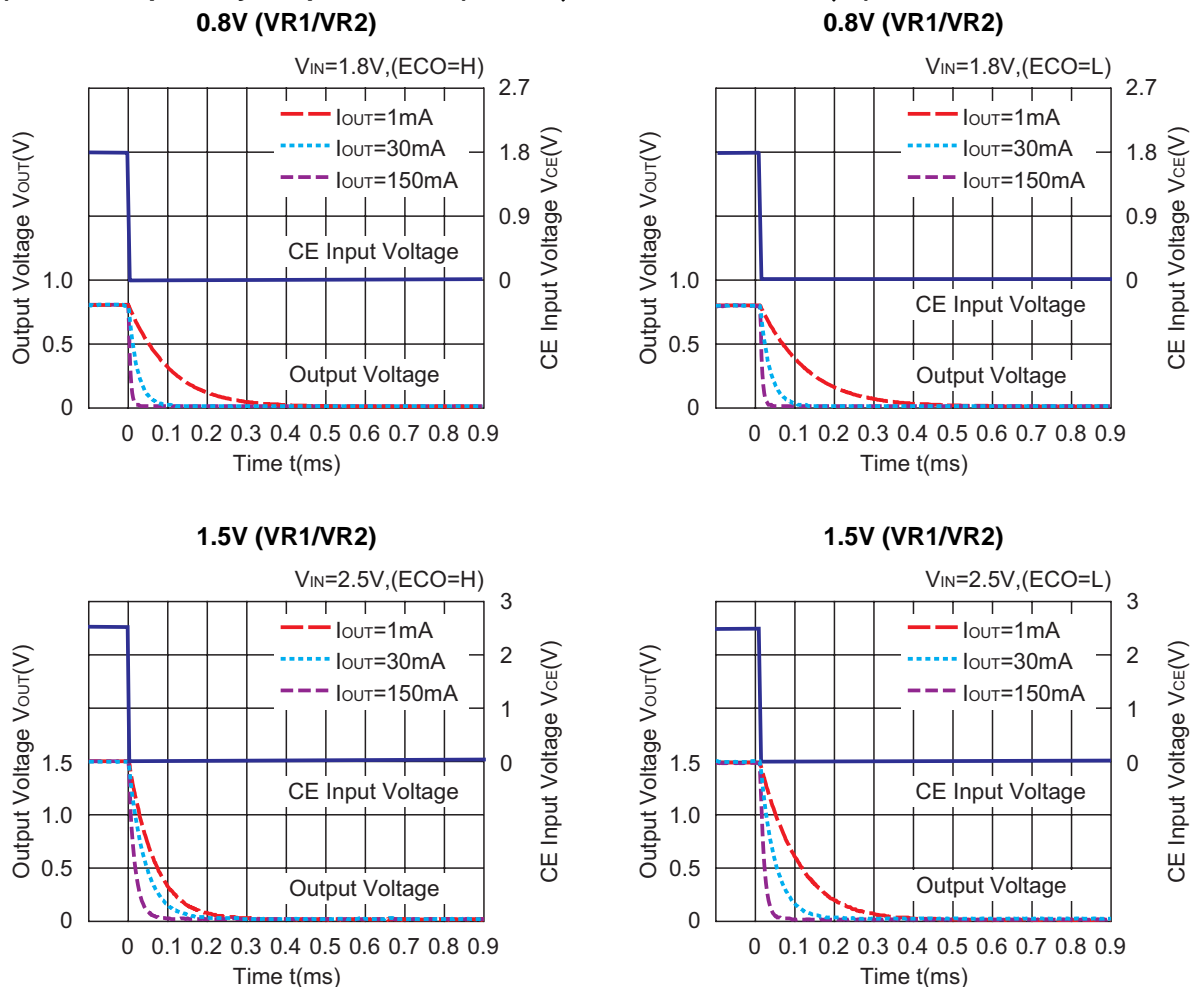


2.8V (VR1/VR2)

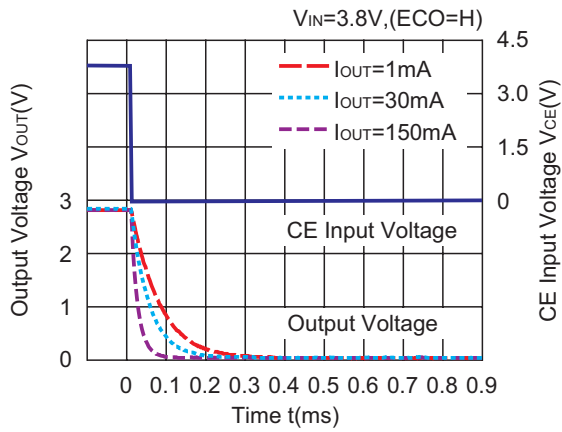




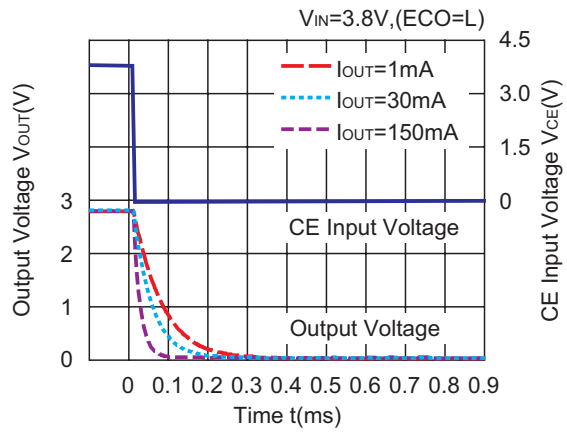
14) Turn off speed by CE pin control ($C_{IN}=1.0\mu F$, $C_{OUT}=\text{Ceramic } 1.0\mu F$)



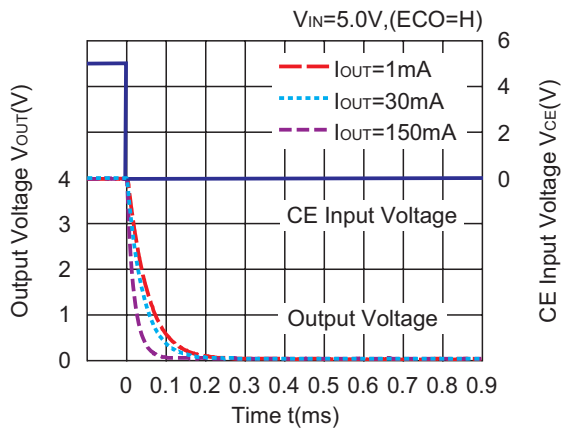
2.8V (VR1/VR2)



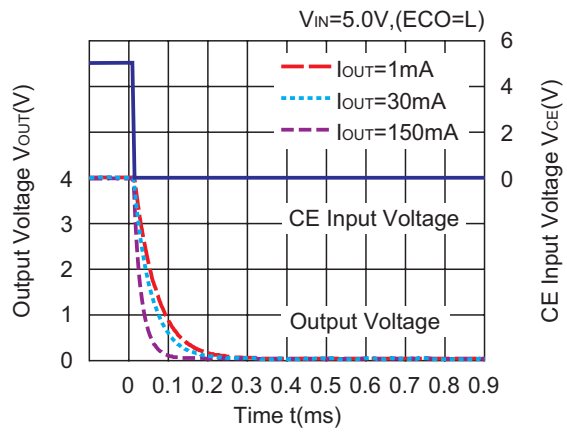
2.8V (VR1/VR2)



4.0V (VR1/VR2)

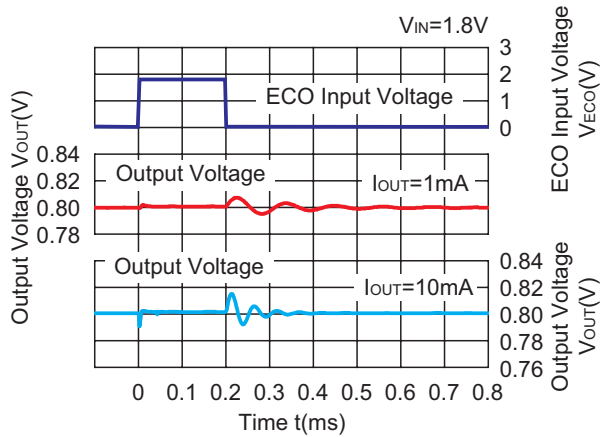


4.0V (VR1/VR2)

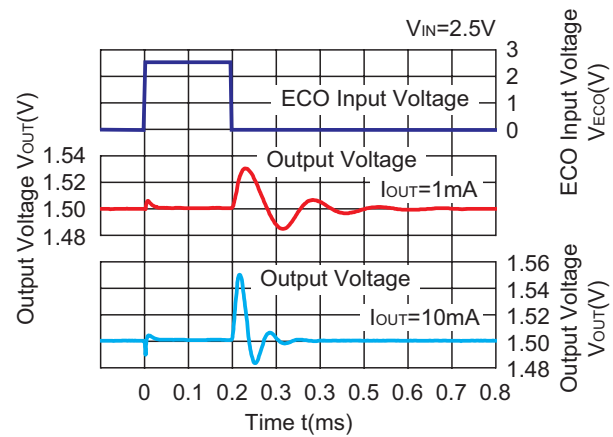


15) Mode Transient Response ($C_{IN}=C_{OUT}=\text{Ceramic } 1.0\mu F$)

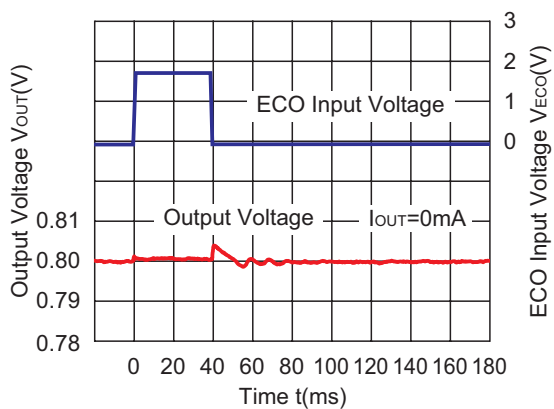
0.8V (VR1/VR2)



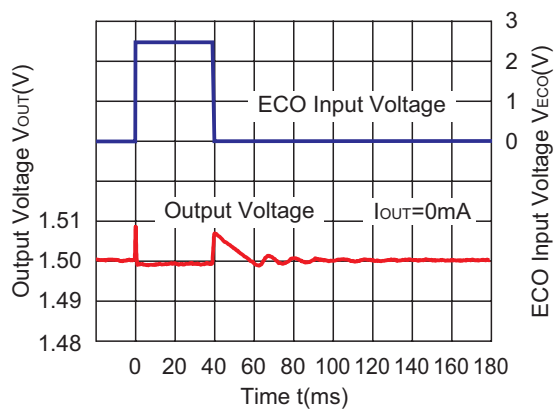
1.5V (VR1/VR2)



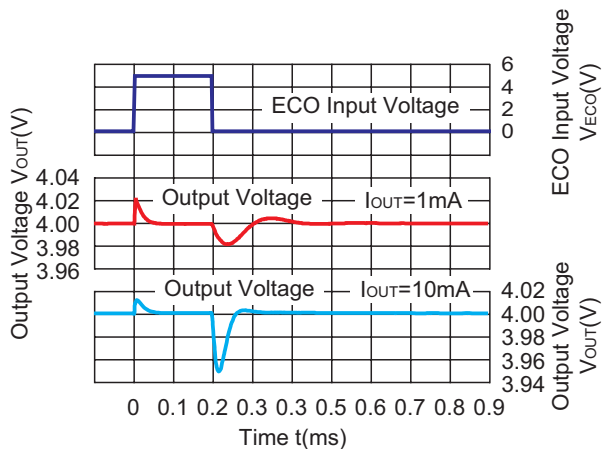
0.8V (VR1/VR2)



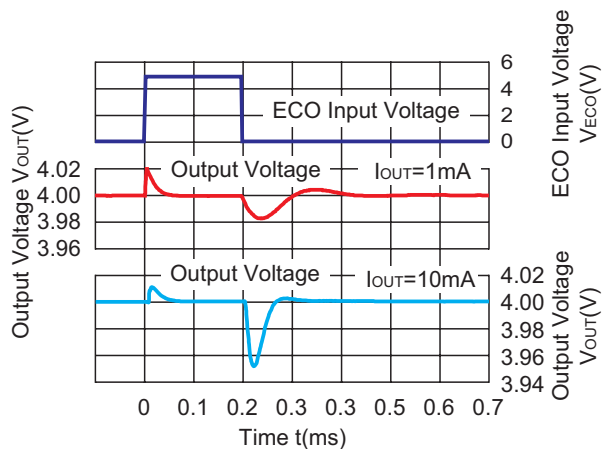
1.5V (VR1/VR2)



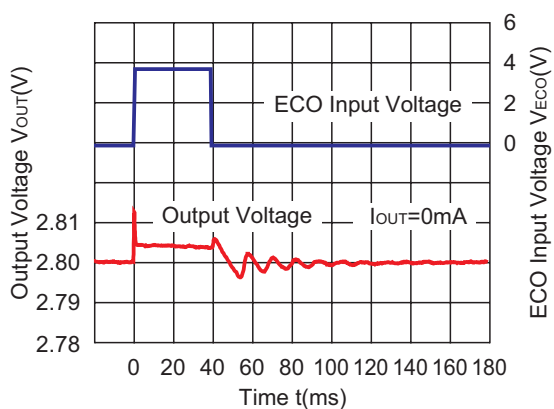
2.8V (VR1/VR2)



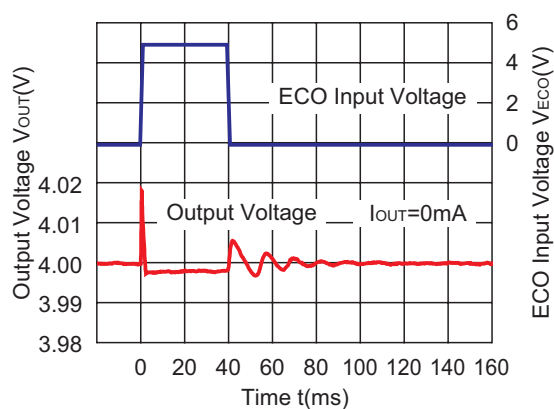
4.0V (VR1/VR2)



2.8V (VR1/VR2)



4.0V (VR1/VR2)



ESR vs. Output Current

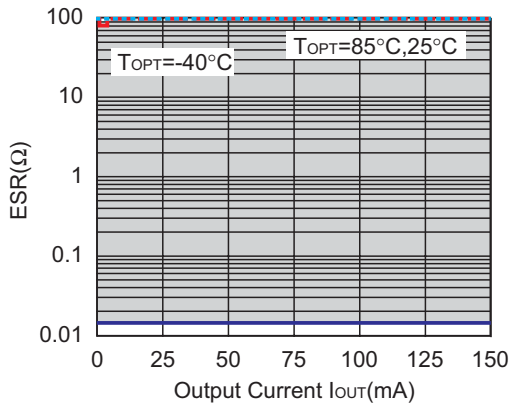
When using these ICs, consider the following points:

The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below.
 The conditions when the white noise level is under $40\mu V$ (Avg.) are marked as the hatched area in the graph.

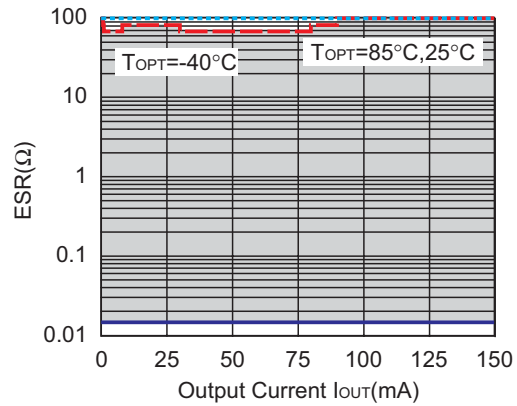
Measurement conditions

Frequency Band : 10Hz to 2MHz
 Temperature : $-40^{\circ}C$ to $85^{\circ}C$

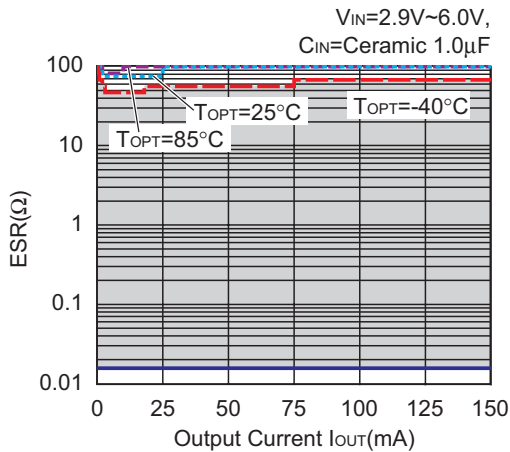
0.8V (VR1/VR2)



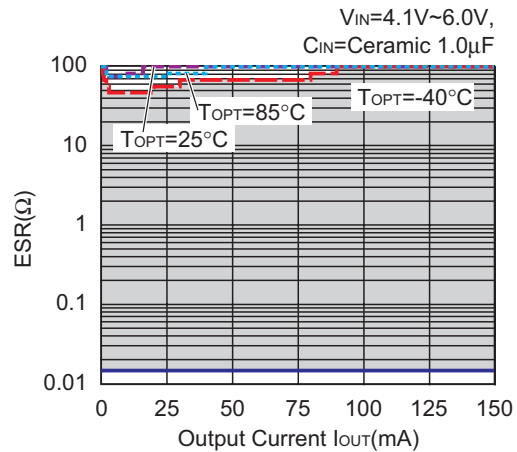
1.5V (VR1/VR2)



2.8V (VR1/VR2)



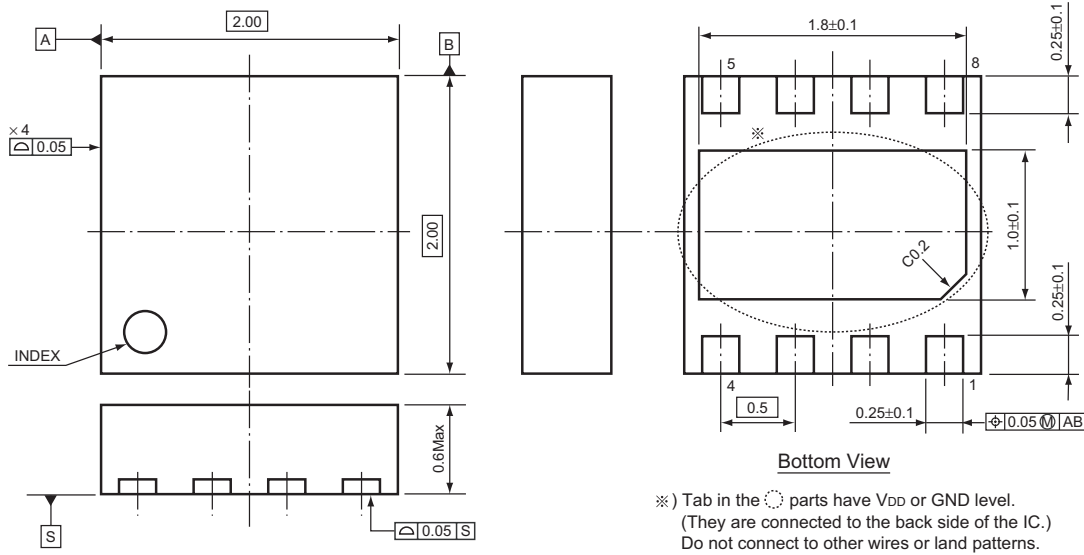
4.0V (VR1/VR2)



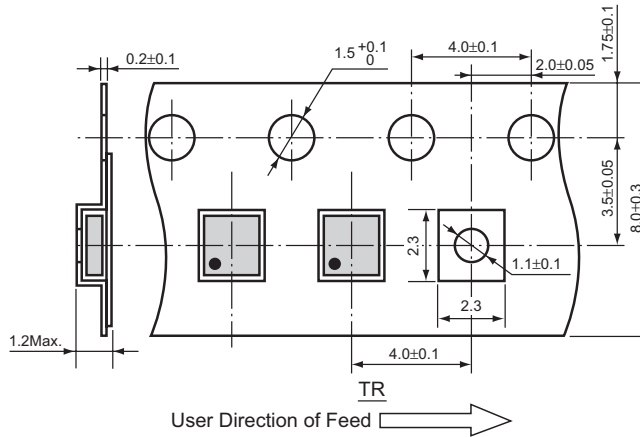
• DFN(PLP)2020-8

Unit: mm

PACKAGE DIMENSIONS

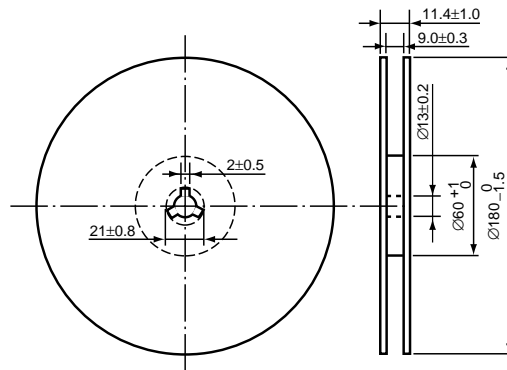


TAPING SPECIFICATION



TAPING REEL DIMENSIONS REUSE REEL (EIAJ-RRM-08Bc)

(1reel=5000pcs)



POWER DISSIPATION (DFN(PLP)2020-8)

This specification is at mounted on board. Power Dissipation (P_D) depends on conditions of mounting on board.

This specification is based on the measurement at the condition below:

(Power Dissipation (DFN(PLP)2020-8) is substitution of DFN(PLP)1820-6.)

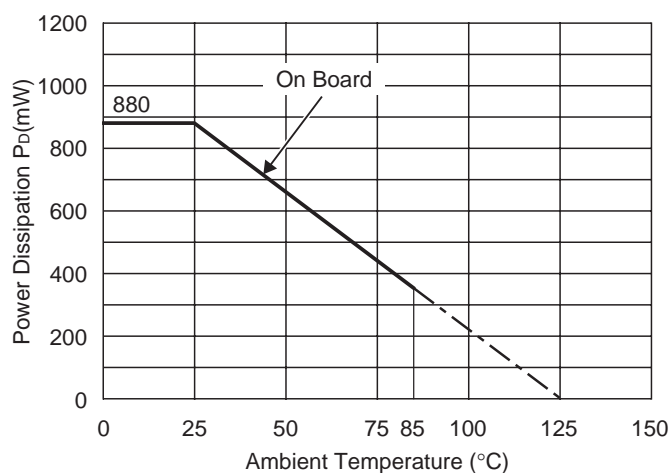
Measurement Conditions

	Standard Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plastic (Double sided)
Board Dimensions	40mm × 40mm × 1.6mm
Copper Ratio	Top side : Approx. 50% , Back side : Approx. 50%
Through-hole	φ0.54mm × 30pcs

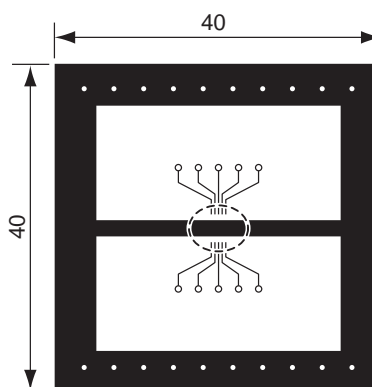
Measurement Result

($T_{opt}=25^{\circ}C$, $T_{jmax}=125^{\circ}C$)

	Standard Land Pattern
Power Dissipation	880mW
Thermal Resistance	$\theta_{ja}=(125-25^{\circ}C)/0.88W=114^{\circ}C/W$



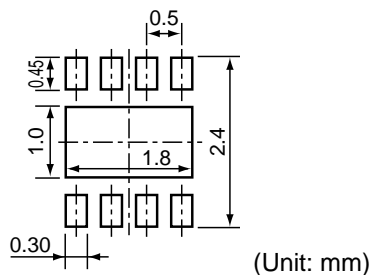
Power Dissipation



Measurement Board Pattern

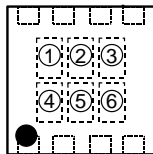
○ IC Mount Area Unit : mm

RECOMMENDED LAND PATTERN



R5328K SERIES MARK SPECIFICATION

• DFN(PLP)2020-8



① to ④ : Product Code (refer to Part Number vs. Product Code)

⑤, ⑥ : Lot Number

• Part Number vs. Product Code

Part Number	Product Code				Set V _{OUT}	
	①	②	③	④	VR1	VR2
R5328K001A	X	0	0	1	2.8V	2.8V
R5328K002A	X	0	0	2	1.8V	3.0V
R5328K003A	X	0	0	3	2.9V	2.9V
R5328K004A	X	0	0	4	1.8V	2.8V
R5328K005A	X	0	0	5	1.8V	2.5V
R5328K006A	X	0	0	6	1.2V	1.8V
R5328K007A	X	0	0	7	1.2V	2.9V

Part Number	Product Code				Set V _{OUT}	
	①	②	③	④	VR1	VR2
R5328K001B	W	0	0	1	2.8V	2.8V
R5328K002B	W	0	0	2	1.8V	3.0V
R5328K003B	W	0	0	3	2.9V	2.9V
R5328K004B	W	0	0	4	1.8V	2.8V
R5328K005B	W	0	0	5	1.8V	2.5V
R5328K006B	W	0	0	6	1.2V	1.8V
R5328K007B	W	0	0	7	1.2V	2.9V