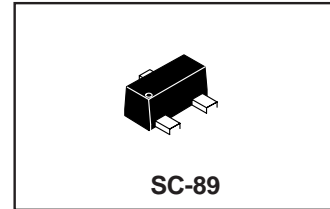


Bias Resistor Transistors

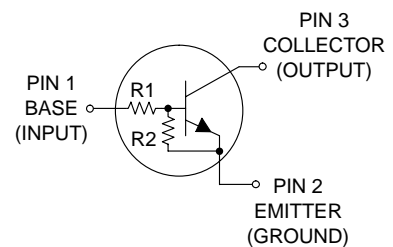
NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

LDTC114EET1G Series

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC-89 package which is designed for low power surface mount applications.



- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SC-89 package can be soldered using wave or reflow. The modified gull-winged leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- We declare that the material of product compliance with RoHS requirements.



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB0}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Total Device Dissipation, FR-4 Board (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	200	mW
		1.6	mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	600	$^\circ\text{C}/\text{W}$
Total Device Dissipation, FR-4 Board (Note 2) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300	mW
		2.4	mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	400	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0×1.0 Inch Pad

LDTC114EET1G Series

ORDERING INFORMATION AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Package	Shipping†
LDTC114EET1G	8A	10	10	SC-89	3000 Tape & Reel
LDTC124EET1G	8B	22	22	SC-89	3000 Tape & Reel
LDTC144EET1G	8C	47	47	SC-89	3000 Tape & Reel
LDTC114YET1G	8D	10	47	SC-89	3000 Tape & Reel
LDTC114TET1G	94	10	∞	SC-89	3000 Tape & Reel
LDTC143TET1G	8F	4.7	∞	SC-89	3000 Tape & Reel
LDTC123EET1G	8H	2.2	2.2	SC-89	3000 Tape & Reel
LDTC143EET1G	8J	4.7	4.7	SC-89	3000 Tape & Reel
LDTC143ZET1G	8K	4.7	47	SC-89	3000 Tape & Reel
LDTC124XET1G	8L	22	47	SC-89	3000 Tape & Reel
LDTC123JET1G	8M	2.2	47	SC-89	3000 Tape & Reel
LDTC115EET1G	8N	100	100	SC-89	3000 Tape & Reel
LDTC144WET1G	8P	47	22	SC-89	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0)	I _{CBO}	-	-	100	nAdc
Collector-Emitter Cutoff Current (V _{CE} = 50 V, I _B = 0)	I _{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current (V _{EB} = 6.0 V, I _C = 0)	I _{EBO}	-	-	0.5	mAdc
LDTC114EET1G		-	-	0.2	
LDTC124EET1G		-	-	0.1	
LDTC144EET1G		-	-	0.2	
LDTC114YET1G		-	-	0.9	
LDTC114TET1G		-	-	1.9	
LDTC143TET1G		-	-	2.3	
LDTC123EET1G		-	-	1.5	
LDTC143EET1G		-	-	0.18	
LDTC143ZET1G		-	-	0.13	
LDTC124XET1G		-	-	0.2	
LDTC123JET1G		-	-	0.05	
LDTC115EET1G		-	-	0.13	
LDTC144WET1G		-	-		
Collector-Base Breakdown Voltage (I _C = 10 μA, I _E = 0)	V _{(BR)CBO}	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	-	-	Vdc

LDTTC114EET1G Series

Characteristic	Symbol	Min	Typ	Max	Unit	
ON CHARACTERISTICS (Note 3)						
DC Current Gain ($V_{CE} = 10\text{ V}$, $I_C = 5.0\text{ mA}$)	LDTTC114EET1G LDTTC124EET1G LDTTC144EET1G LDTTC114YET1G LDTTC114TET1G LDTTC143TET1G LDTTC123EET1G LDTTC143EET1G LDTTC143ZET1G LDTTC124XET1G LDTTC123JET1G LDTTC115EET1G LDTTC144WET1G	h_{FE}	35 60 80 80 160 160 8.0 15 80 80 80 80 80	60 100 140 140 350 350 15 30 200 150 140 150 140	- - - - - - - - - - - - -	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 0.3\text{ mA}$) ($I_C = 10\text{ mA}$, $I_B = 5\text{ mA}$) LDTTC123EET1G ($I_C = 10\text{ mA}$, $I_B = 1\text{ mA}$) LDTTC143TET1G/LDTTC114TET1G/ LDTTC143EET1G/LDTTC143ZET1G/LDTTC124XET1G		$V_{CE(sat)}$	-	-	0.25	Vdc
Output Voltage (on) ($V_{CC} = 5.0\text{ V}$, $V_B = 2.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	LDTTC114EET1G LDTTC124EET1G LDTTC114YET1G LDTTC114TET1G LDTTC143TET1G LDTTC123EET1G LDTTC143EET1G LDTTC143ZET1G LDTTC124XET1G LDTTC123JET1G	V_{OL}	- - - - - - - - - -	- - - - - - - - - -	0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2	Vdc
($V_{CC} = 5.0\text{ V}$, $V_B = 3.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$) ($V_{CC} = 5.0\text{ V}$, $V_B = 5.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$) ($V_{CC} = 5.0\text{ V}$, $V_B = 4.0\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	LDTTC144EET1G LDTTC115EET1G LDTTC144WET1G		- - -	- - -	0.2 0.2 0.2	
Output Voltage (off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.25\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	LDTTC143TET1G LDTTC143ZET1G LDTTC114TET1G	V_{OH}	4.9	-	-	Vdc

3. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit	
Input Resistor	LDTTC114EET1G LDTTC124EET1G LDTTC144EET1G LDTTC114YET1G LDTTC114TET1G LDTTC143TET1G LDTTC123EET1G LDTTC143EET1G LDTTC143ZET1G LDTTC124XET1G LDTTC123JET1G LDTTC115EET1G LDTTC144WET1G	R_1	7.0 15.4 32.9 7.0 7.0 3.3 1.5 3.3 3.3 15.4 1.54 70 32.9	10 22 47 10 10 4.7 2.2 4.7 4.7 22 2.2 100 47	13 28.6 61.1 13 13 6.1 2.9 6.1 6.1 28.6 2.86 130 61.1	$k\Omega$
Resistor Ratio	LDTTC114EET1G/LDTTC124EET1G/ LDTTC144EET1G/LDTTC115EET1G LDTTC114YET1G LDTTC143TET1G/LDTTC114TET1G LDTTC123EET1G/LDTTC143EET1G LDTTC143ZET1G LDTTC124XET1G LDTTC123JET1G LDTTC144WET1G	R_1/R_2	0.8 0.17 - 0.8 0.055 0.38 0.038 1.7	1.0 0.21 - 1.0 0.1 0.47 0.047 2.1	1.2 0.25 - 1.2 0.185 0.56 0.056 2.6	

LDTC114EET1G Series

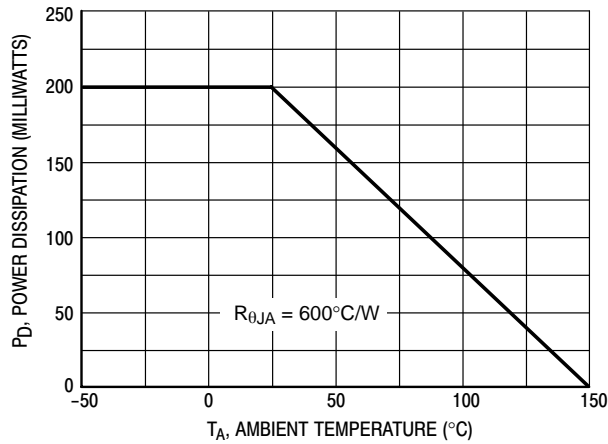


Figure 1. Derating Curve

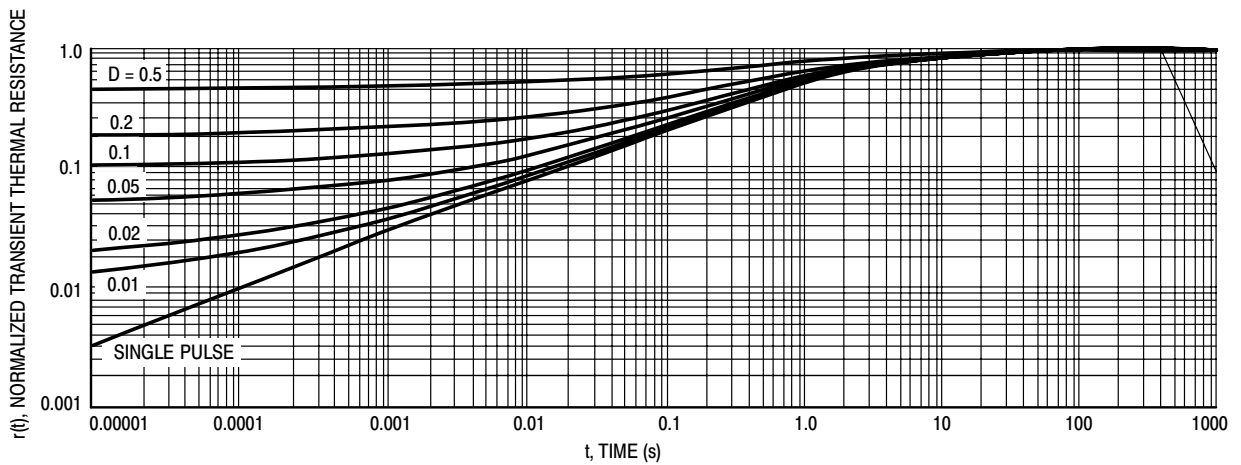


Figure 2. Normalized Thermal Response

LDTCT114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LDTCT114EET1G

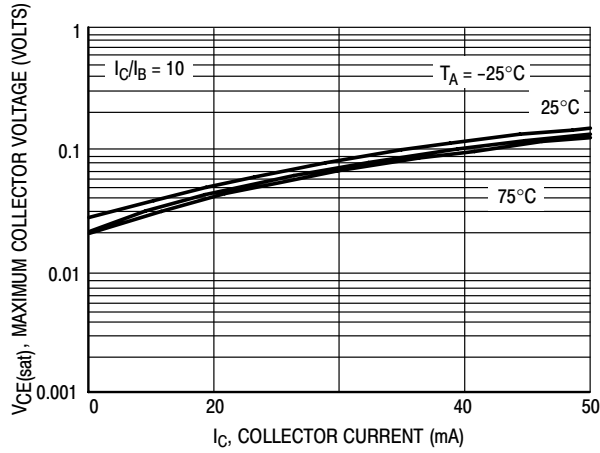


Figure 3. $V_{CE(sat)}$ versus I_C

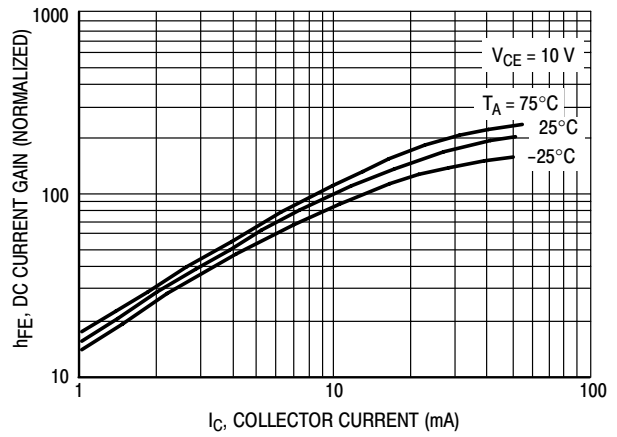


Figure 4. DC Current Gain

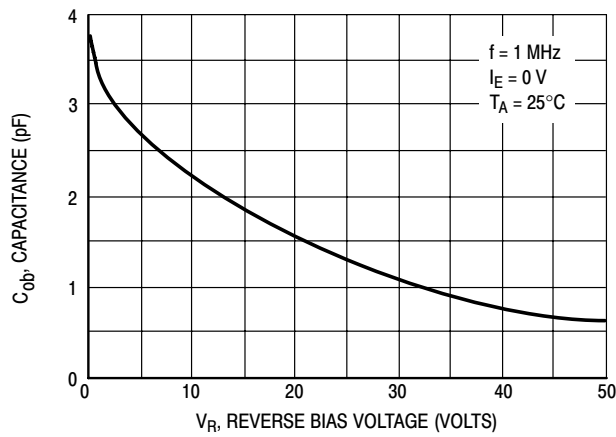


Figure 5. Output Capacitance

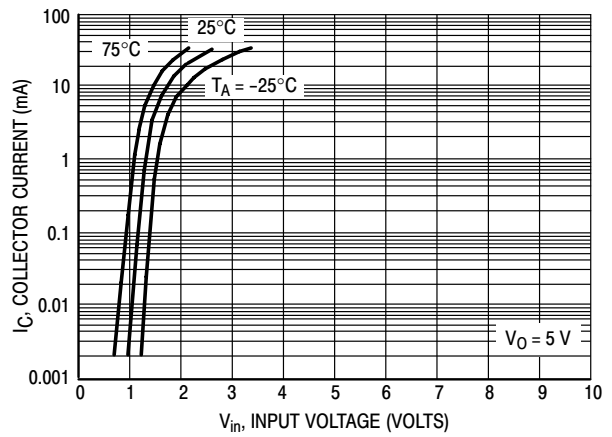


Figure 6. Output Current versus Input Voltage

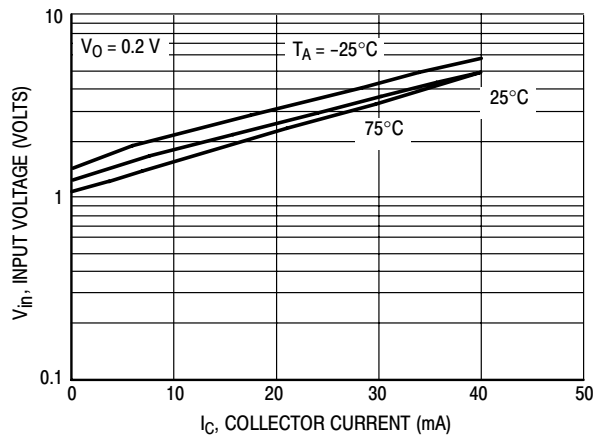


Figure 7. Input Voltage versus Output Current

LDTC114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LDTC123EET1G

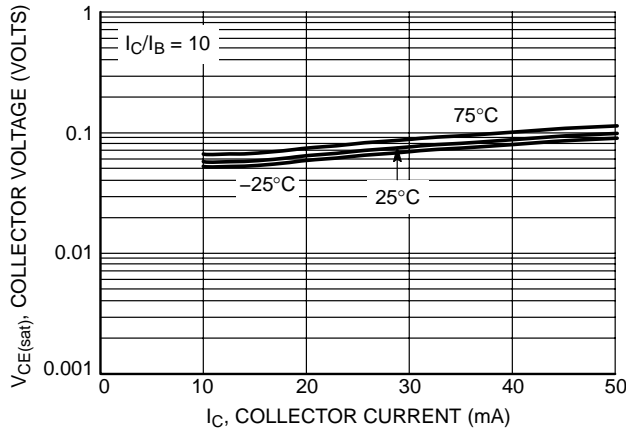


Figure 8. $V_{CE(sat)}$ versus I_C

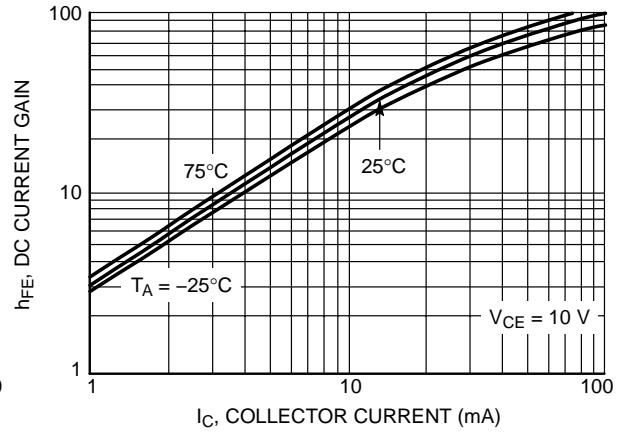


Figure 9. DC Current Gain

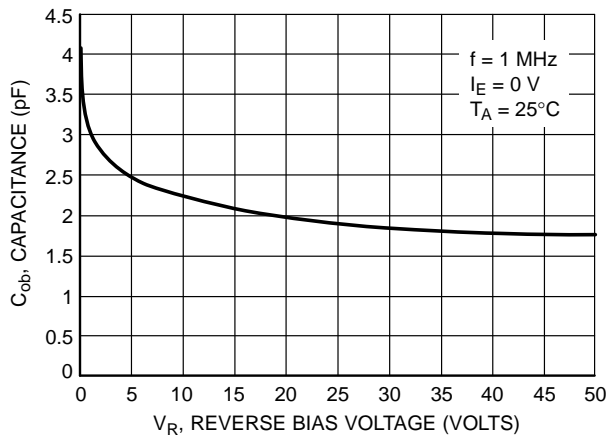


Figure 10. Output Capacitance

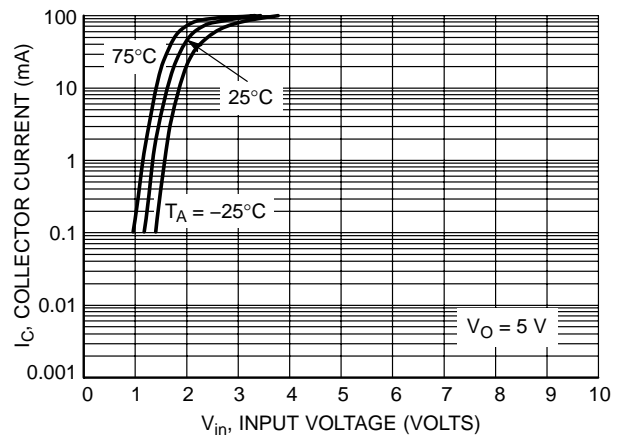


Figure 11. Output Current versus Input Voltage

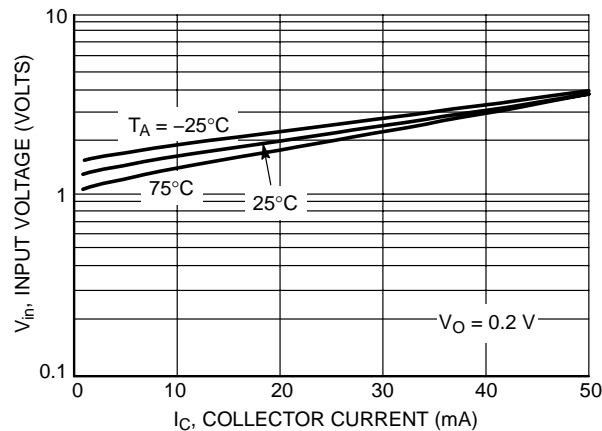


Figure 12. Input Voltage versus Output Current

LDTTC114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS - LDTTC124EET1G

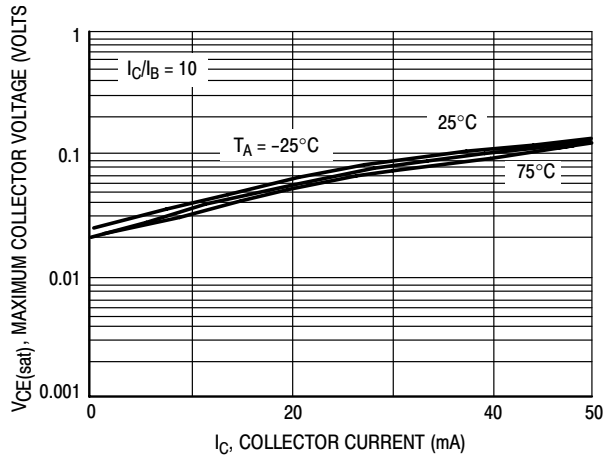


Figure 13. $V_{CE(sat)}$ versus I_C

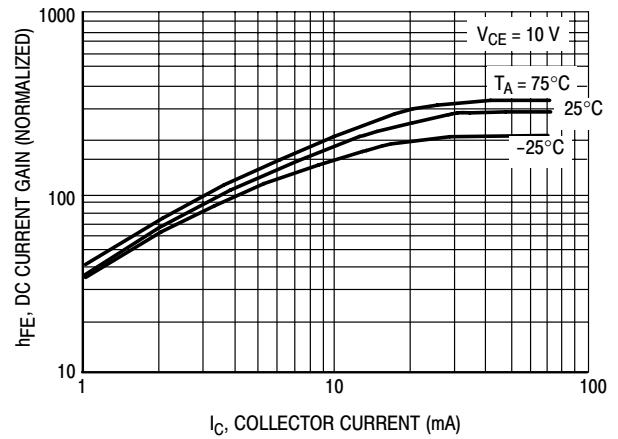


Figure 14. DC Current Gain

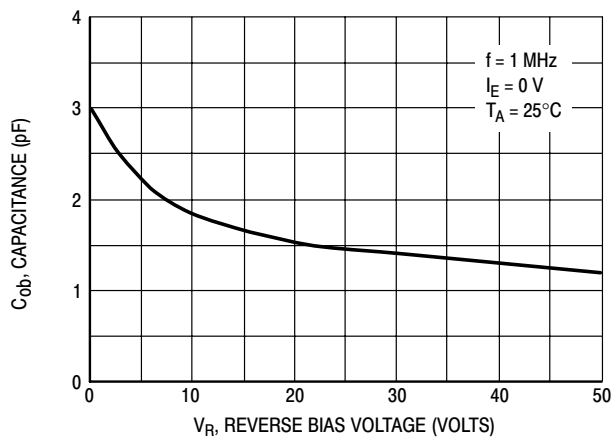


Figure 15. Output Capacitance

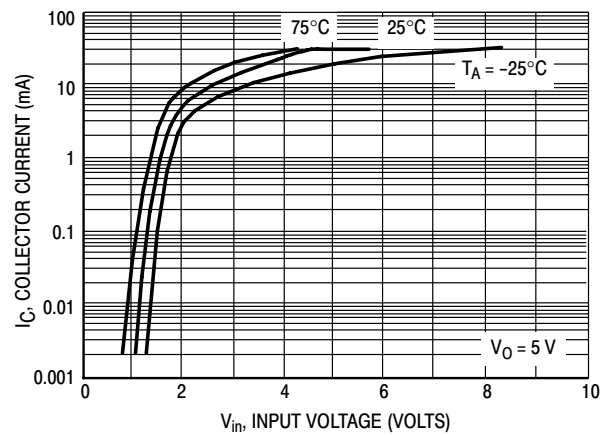


Figure 16. Output Current versus Input Voltage

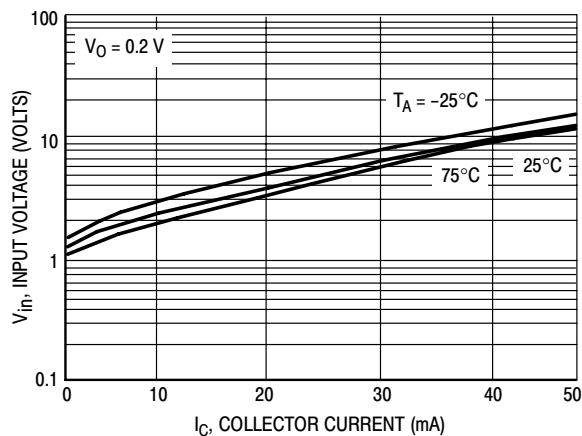


Figure 17. Input Voltage versus Output Current

LDTC114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LDTC144EET1G

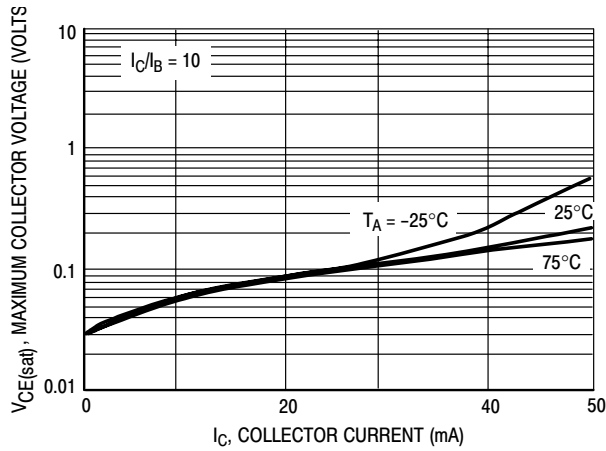


Figure 18. $V_{CE(sat)}$ versus I_C

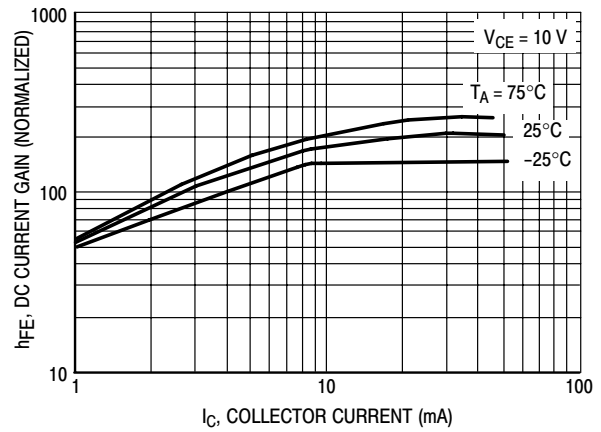


Figure 19. DC Current Gain

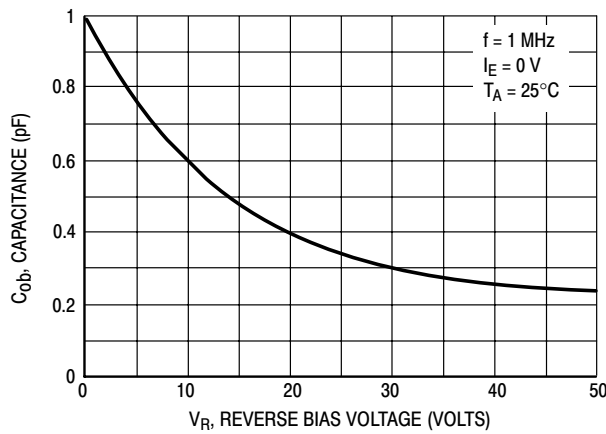


Figure 20. Output Capacitance

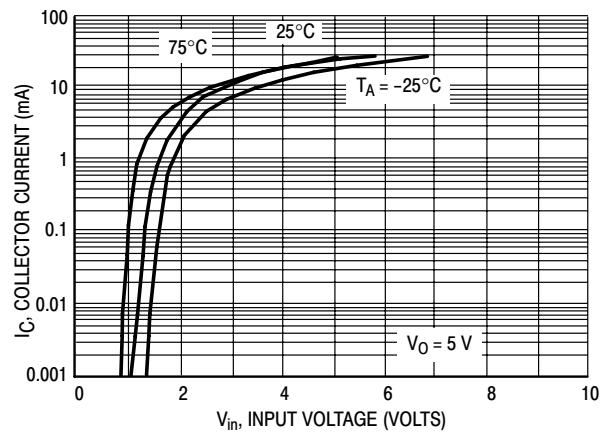


Figure 21. Output Current versus Input Voltage

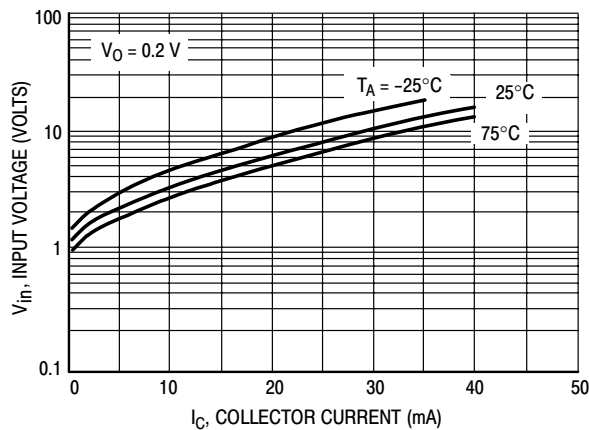


Figure 22. Input Voltage versus Output Current

LDTC114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS – LDTC114YET1G

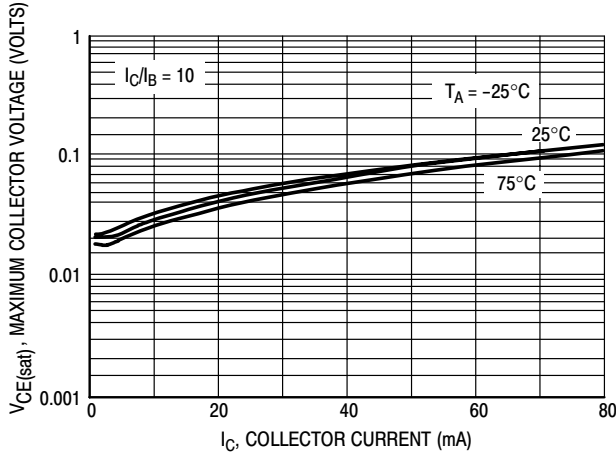


Figure 23. $V_{CE(sat)}$ versus I_C

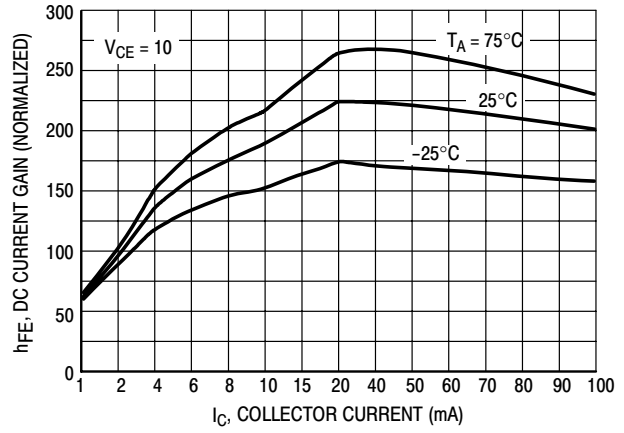


Figure 24. DC Current Gain

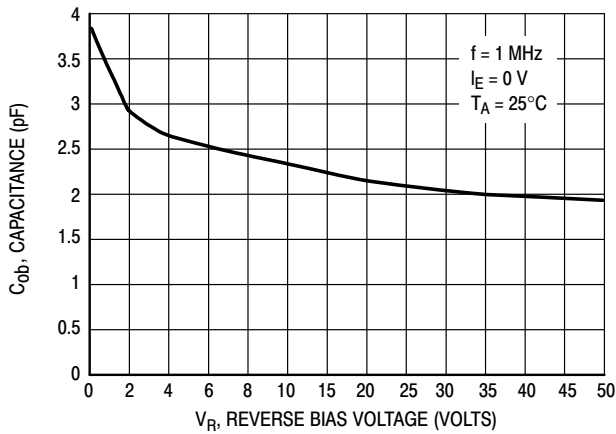


Figure 25. Output Capacitance

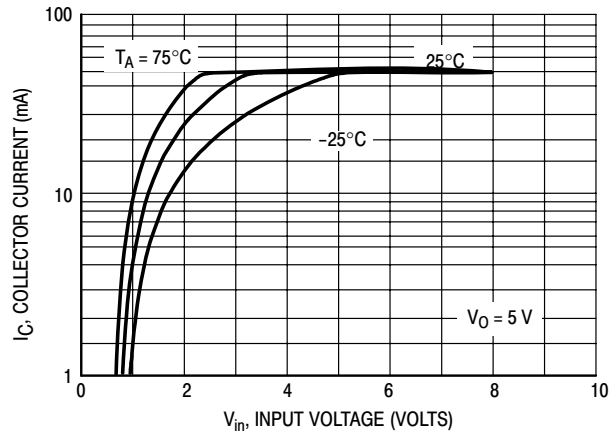


Figure 26. Output Current versus Input Voltage

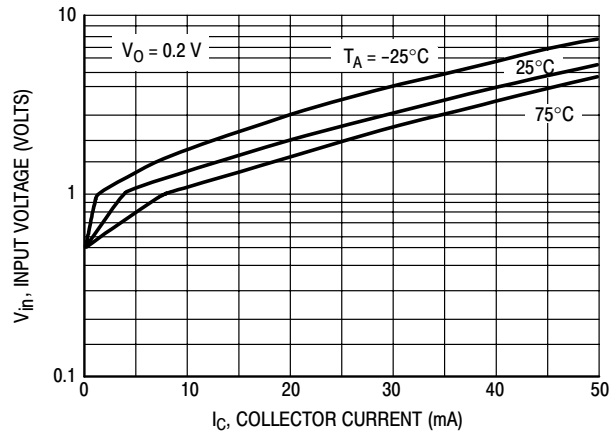


Figure 27. Input Voltage versus Output Current

LDTC114EET1G Series

TYPICAL APPLICATIONS FOR NPN BRTs

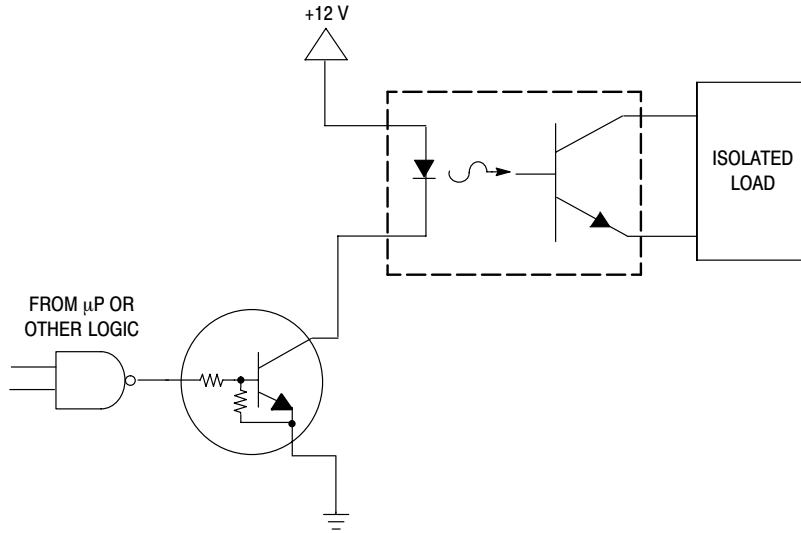


Figure 28. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

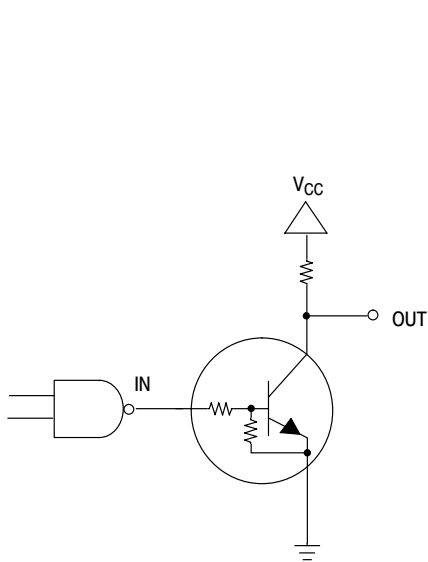


Figure 29. Open Collector Inverter: Inverts the Input Signal

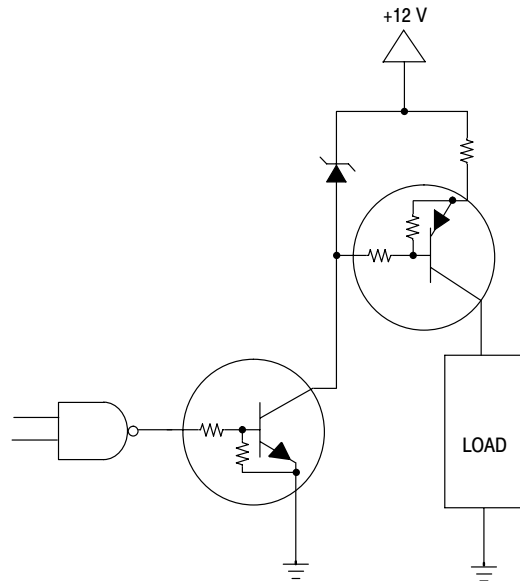
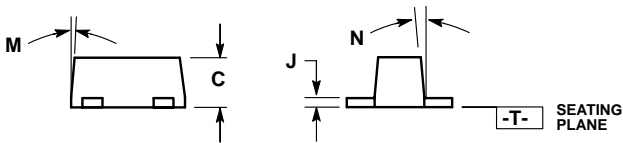
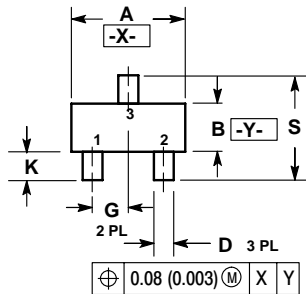


Figure 30. Inexpensive, Unregulated Current Source

LDTTC114EET1G Series

SC-89



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067

