AAT2505

Dual Channel, Step-Down Converter/Linear Regulator

SystemPower™

General Description

The AAT2505 is a member of AnalogicTech's Total Power Management IC™ (TPMIC™) product family. It is a low dropout (LDO) linear regulator and a step-down converter with an input voltage range of 2.7V to 5.5V, making it ideal for applications with single cell lithium-ion / polymer batteries.

The LDO has an independent input pin and is capable of delivering up to 300mA of current. The linear regulator has been designed for high-speed turn-on and turn-off performance, fast transient response, and good power supply rejection ratio (PSRR). Other features include low quiescent current, low dropout voltage, and a Power-OK (POK) open drain output signaling when V_{OUT} is in regulation.

The 600mA step-down converter is designed to operate with 1.4MHz of switching frequency, minimizing external component size and cost while maintaining a low 27µA no load quiescent current.

Peak current mode control with internal compensation provides a stable converter with a low equivalent series resistance (ESR) ceramic output capacitor for extremely low output ripple.

For maximum battery life with high voltage outputs, the step-down converter duty cycle increases to 100%. The output voltage is either fixed or adjustable with an integrated P- and N-channel MOSFET power stage and 1.4MHz switching frequency.

The AAT2505 is available in a Pb-free, 12-pin TDFN33 package and is rated over a temperature range of -40°C to +85°C.

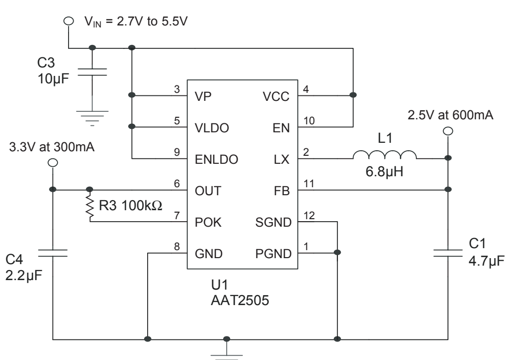
Features

- V_{IN} Range: 2.7V to 5.5V
- 300mA LDO
  - 400mV Dropout Voltage at 300mA
  - High Accuracy: ±1.5%
  - Fast Line / Load Transient Response
  - Power OK Output
- 600mA Step-Down Converter
  - Up To 98% Efficiency
  - 27µA No Load Quiescent Current
  - Shutdown Current <1µA
  - Low $R_{DS(ON)}$ Integrated Power Switches
  - Fast Turn-On Time (150µs Typical)
  - Low Dropout 100% Duty Cycle
  - 1.4MHz Switching Frequency
  - Internal Soft Start
- Over-Temperature and Current Limit Protection
- TDFN33-12 Package
- -40°C to +85°C Temperature Range

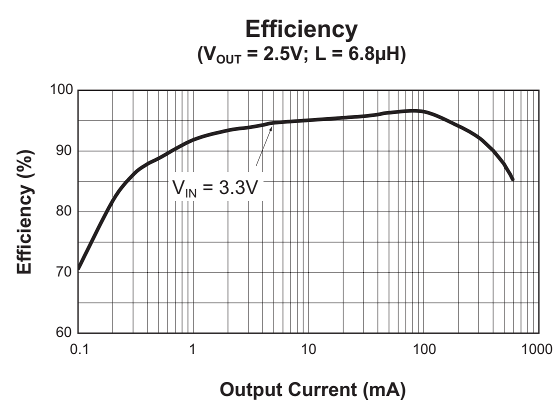
Applications

- Cellular Phones
- Digital Cameras
- Handheld Instruments
- Microprocessor/DSP Core/IO Power
- PDAs and Handheld Computers
- Portable Media Players

Typical Application



L1 Sumida CDRH3D16-4R7 C1 Murata GRM219R61A475KE19
C3 Murata GRM21BR60J106KE19



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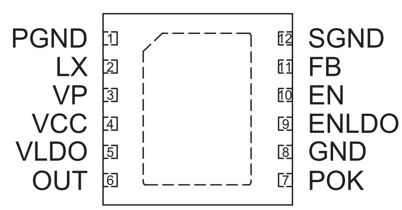
Pin Descriptions

Pin #	Symbol	Function
1	PGND	Step-down converter power ground return pin. Connect to the output and input capacitor return. See section on PCB layout guidelines and evaluation board layout diagram.
2	LX	Power switching node. Output switching node that connects to the output inductor.
3	VP	Step-down converter power stage supply voltage. Must be closely decoupled to PGND.
4	VCC	Step-down converter bias supply. Connect to VP.
5	VLDO	LDO input voltage; should be decoupled with 1µF or greater capacitor.
6	OUT	300mA LDO output pin. A 2.2µF or greater output low-ESR ceramic capacitor is required for stability.
7	POK	Power-OK output for the LDO. This open drain output is low when the OUT is out of regulation. Connect a pull-up resistor from POK to OUT or VLDO. When LDO is in shutdown (ENLDO = 0V), POK is pulled low.
8	GND	LDO ground connection pin.
9	ENLDO	Enable pin for LDO. When connected low, LDO is disabled and consumes less than 1µA of current.
10	EN	Step-down converter enable. When connected low, the step-down converter is disabled and consumes less than 1µA.
11	FB	Step-down converter feedback input pin. For fixed output voltage versions, this pin is connected to the converter output, forcing the converter to regulate to the specific voltage. For adjustable output versions, an external resistive divider ties to this point and programs the output voltage to the desired value.
12	SGND	Step-down converter signal ground. For external feedback, return the feedback resistive divider to this ground. For internal fixed version, tie to the point of load return. See section on PCB layout guidelines and evaluation board layout diagram.
EP		Exposed paddle (bottom). Use properly sized vias for thermal coupling to the ground plane. See section on PCB layout guidelines.

Pin Configuration

TDFN33-12
(Top View)



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Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_P, V_{LDO}	Input Voltages to GND	6.0	V
V_{LX}	Lx to GND	-0.3 to V_P + 0.3	V
V_{FB}	FB to GND	-0.3 to V_P + 0.3	V
V_{EN}	EN to GND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation	2.0	W
θ_{JA}	Thermal Resistance[2]	50	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board with exposed paddle connected to ground plane.

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Electrical Characteristics[1]

$V_{IN} = V_{LDO} = V_{OUT(NOM)}$ + 1V for V_{OUT} options greater than 1.5V. $V_{IN} = V_{LDO}$ = 2.5V for $V_{OUT} \leq$ 1.5V. I_{OUT} = 1mA, C_{OUT} = 2.2µF, C_{IN} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
LDO						
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA to 300mA, T_A = 25°C	-1.5		1.5	%
		I_{OUT} = 1mA to 300mA, T_A = -40°C to +85°C	-2.5		2.5	%
V_{IN}	Input Voltage		V_{OUT} + V_{DO}[2]		5.5	V
V_{DO}	Dropout Voltage[3, 4]	I_{OUT} = 300mA		400	600	mV
$\Delta V_{OUT}/V_{OUT} * V_{IN}$	Line Regulation	$V_{IN} = V_{OUT}$ + 1V to 5V			0.09	%/V
$\Delta V_{OUT(Line)}$	Dynamic Line Regulation	I_{OUT} = 300mA, $V_{IN} = V_{OUT}$ + 1V to V_{OUT} + 2V, T_R/T_F = 2µs		2.5		mV
$\Delta V_{OUT(Load)}$	Dynamic Load Regulation	I_{OUT} = 1mA to 300mA, T_R <5µs		60		mV
I_{OUT}	Output Current	V_{OUT} > 1.3V	300			mA
I_{SC}	Short-Circuit Current	V_{OUT} < 0.4V		1		A
I_{QLDO}	LDO Quiescent Current	V_{IN} = 5V, No Load, ENLDO = V_{IN}		70	125	µA
V_{POK}	POK Trip Threshold	V_{OUT} Rising, T_A = 25°C	90	94	98	% of V_{OUT}
V_{POKHYS}	POK Hysteresis			1.0		% of V_{OUT}
$V_{POK(OL)}$	POK Output Voltage Low	I_{SINK} = 1mA			0.4	V
I_{POK}	POK Output Leakage Current	V_{POK} < 5.5V, V_{OUT} in Regulation			1.0	µA
I_{SHDN}	Shutdown Current	V_{IN} = 5V; ENLDO = GND, EN = SGND = PGND			1.0	µA
PSRR	Power Supply Rejection Ratio	I_{OUT} = 10mA, 1kHz		65		dB
		I_{OUT} = 10mA, 10kHz		45		dB
		I_{OUT} = 10mA, 1MHz		42		dB
T_{SD}	Over-Temperature Shutdown Threshold			145		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
e_N	Output Noise			250		$µV_{RMS}$
T_C	Output Voltage Temperature Coefficient			22		ppm/°C

1. The AAT2505 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. To calculate the minimum LDO input voltage, use the following equation: $V_{IN(MIN)} = V_{OUT(MAX)} + V_{DO(MAX)}$, as long as $V_{IN} \geq$ 2.5V.
3. For V_{OUT} < 2.1V, V_{DO} = 2.5 - V_{OUT}.
4. V_{DO} is defined as $V_{IN} - V_{OUT}$ when V_{OUT} is 98% of nominal.

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Electrical Characteristics[1]

I_{OUT} = 600mA; typical values are T_A = 25°C, $V_{IN} = V_{CC} = V_P$ = 3.6V.

Symbol	Description	Conditions	Min	Typ	Max	Units
Buck Converter						
V_{IN}	Input Voltage		2.7		5.5	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising			2.7	V
		Hysteresis		100		mV
		V_{IN} Falling	1.8			V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 0 to 600mA, V_{IN} = 2.7V to 5.5V	-3.0		3.0	%
V_{OUT}	Output Voltage Range		0.6		V_{IN}	V
I_{QBUCK}	Step-Down Converter Quiescent Current	ENLDO = GND, No Load, 0.6V Adjustable Version		27	70	µA
I_{SHDN}	Shutdown Current	EN = SGND = PGND, ENLDO = GND			1.0	µA
I_{LIM}	P-Channel Current Limit		800			mA
$R_{DS(ON)H}$	High Side Switch On Resistance			0.45		Ω
$R_{DS(ON)L}$	Low Side Switch On Resistance			0.40		Ω
I_{LXLK}	LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 0 to V_{IN}, EN = SGND = PGND			1.0	µA
$\Delta V_{Linereg}$	Line Regulation	V_{IN} = 2.7V to 5.5V		0.1		%/V
V_{FB}	FB Threshold Voltage Accuracy	0.6V Output, No Load, T_A = 25°C	591	600	609	mV
I_{FB}	FB Leakage Current	0.6V Output			0.2	µA
R_{FB}	FB Impedance	> 0.6V Output	250			kΩ
T_S	Start-Up Time	From Enable to Output Regulation		150		µs
F_{OSC}	Oscillator Frequency	T_A = 25°C	1.0	1.4	2.0	MHz
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
Logic Signals						
$V_{EN(L)}$	Enable Threshold Low				0.6	V
$V_{EN(H)}$	Enable Threshold High		1.4			V
$I_{EN(H)}$	Leakage Current		-1.0		1.0	µA

1. The AAT2505 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

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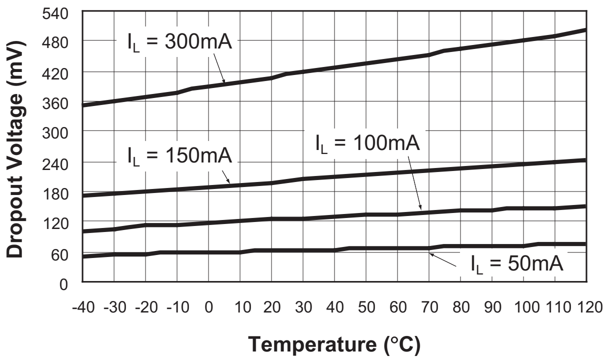
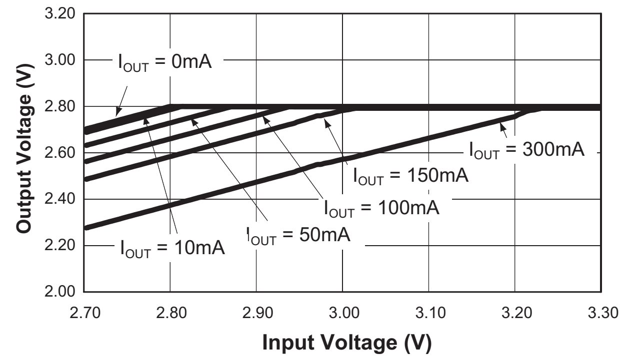
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

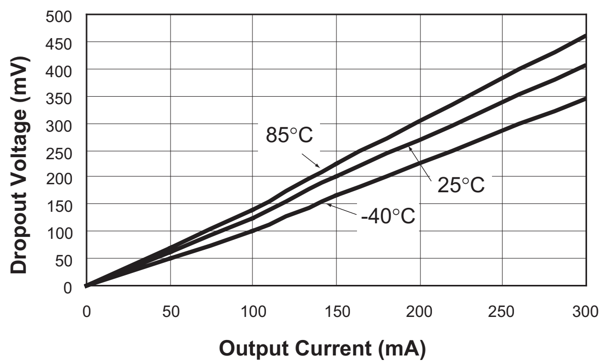
LDO Dropout Voltage vs. Temperature
(EN = GND; ENLDO = V_{IN})



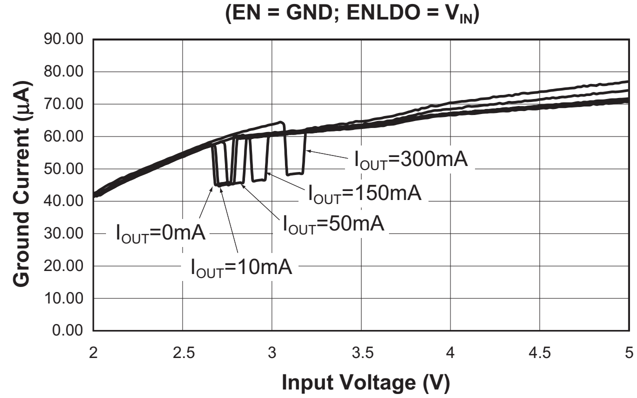
LDO Dropout Characteristics
(EN = GND; ENLDO = V_{IN})



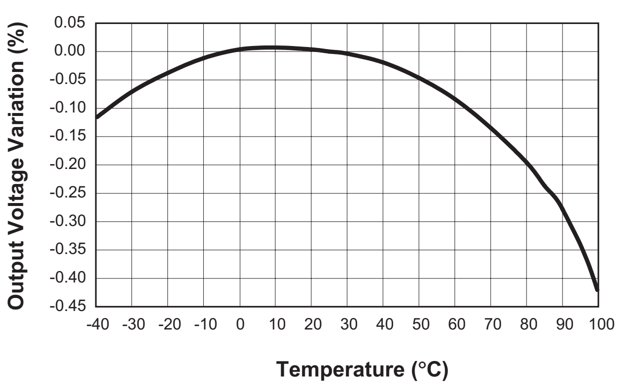
LDO Dropout Voltage vs. Output Current
(EN = GND; ENLDO = V_{IN})



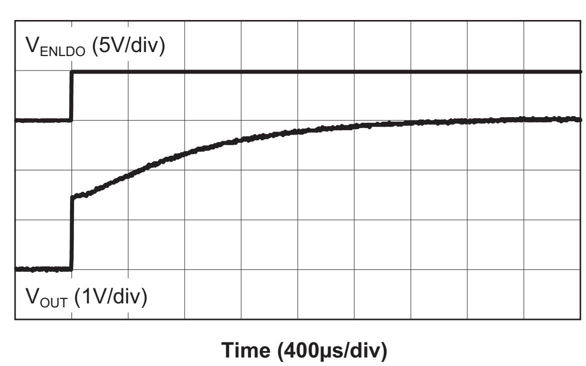
LDO Ground Current vs. Input Voltage
(EN = GND; ENLDO = V_{IN})



LDO Output Voltage vs. Temperature
(EN = GND; ENLDO = V_{IN})



LDO Initial Power-Up Response Time
(EN = GND; ENLDO = V_{IN})



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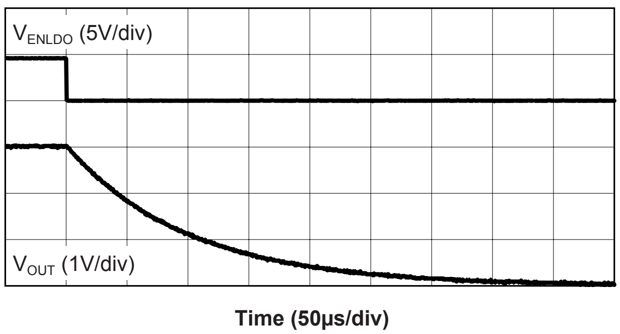
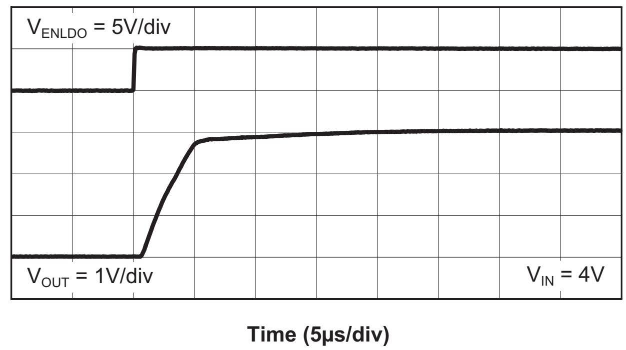
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

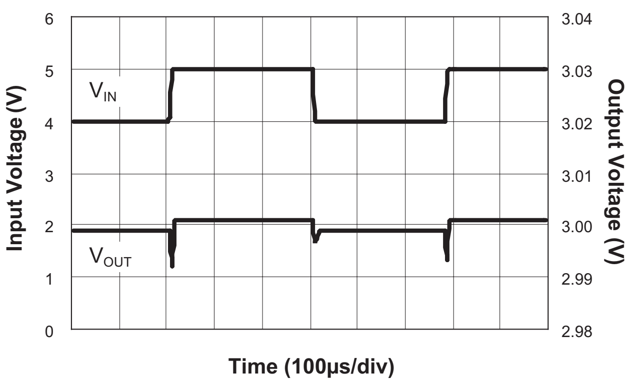
LDO Turn-Off Response Time
(EN = GND; ENLDO = V_{IN})



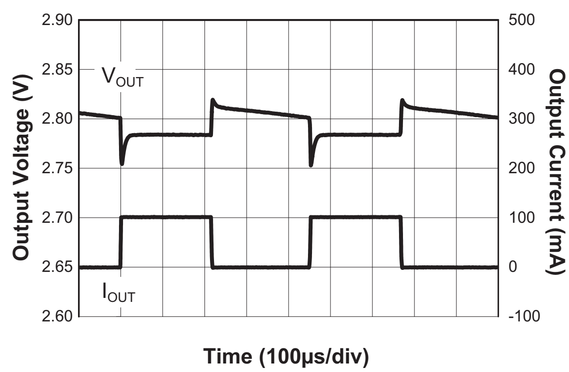
LDO Turn-On Time From Enable (V_{IN} present)
(EN = GND; ENLDO = V_{IN})



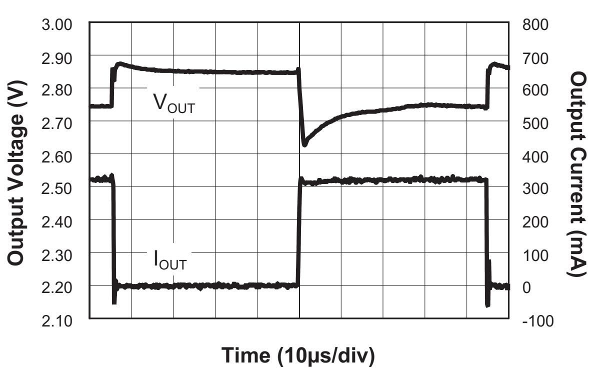
LDO Line Transient Response
(EN = GND; ENLDO = V_{IN})



LDO Load Transient Response
(EN = GND; ENLDO = V_{IN})



LDO Load Transient Response 300mA
(EN = GND; ENLDO = V_{IN})



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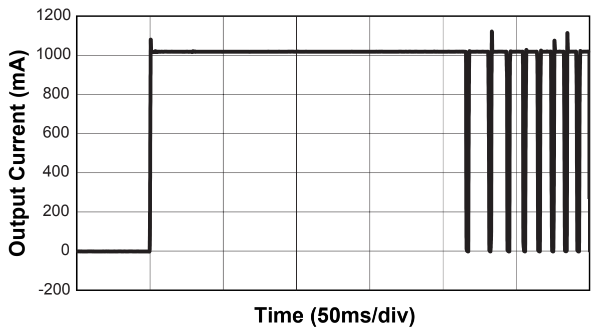
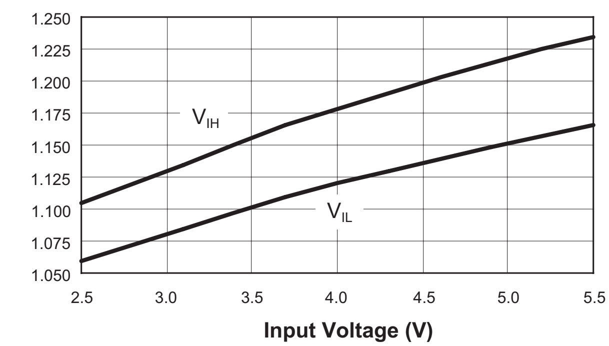
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

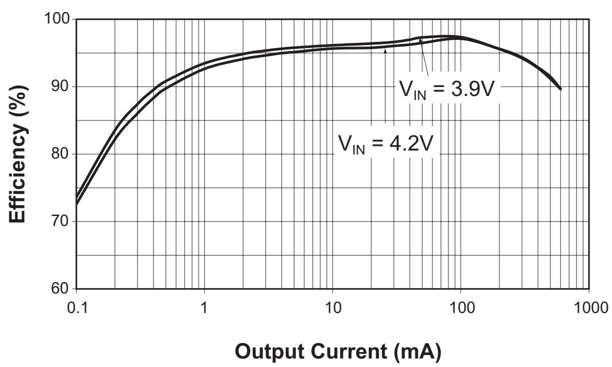
LDO Over-Current Protection
(EN = GND; ENLDO = V_{IN})



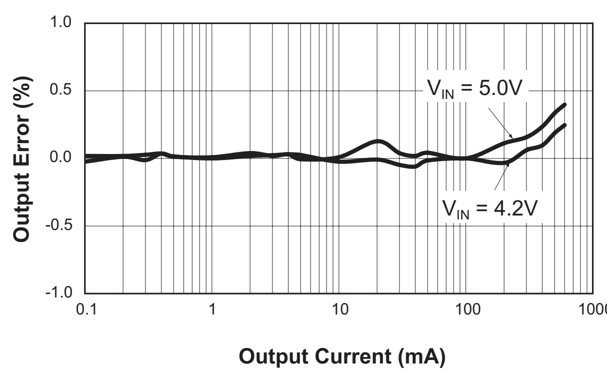
LDO ENLDO vs. V_{IN}



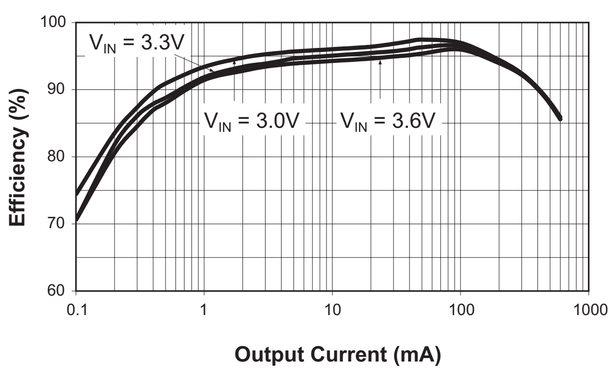
Step-Down Converter Efficiency vs. Load
(V_{OUT} = 3.3V; L = 10µH; ENLDO = GND)



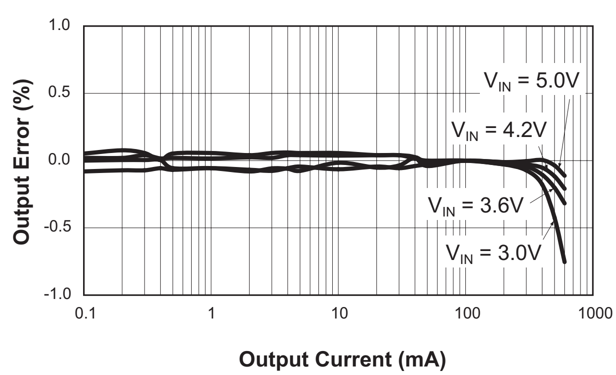
Step-Down Converter DC Regulation
(V_{OUT} = 3.3V; L = 6.8µH; ENLDO = GND)



Step-Down Converter Efficiency vs. Load
(V_{OUT} = 2.5V; L = 10µH; ENLDO = GND)



Step-Down Converter DC Regulation
(V_{OUT} = 2.5V; L = 6.8µH; ENLDO = GND)



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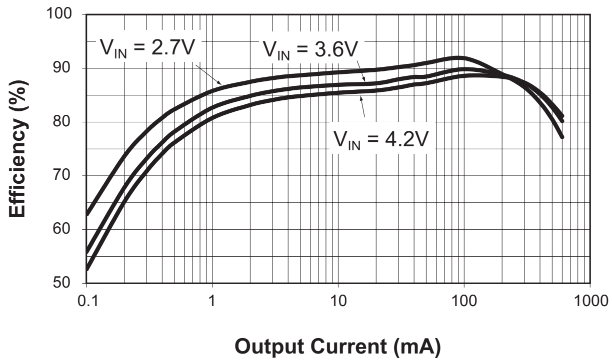
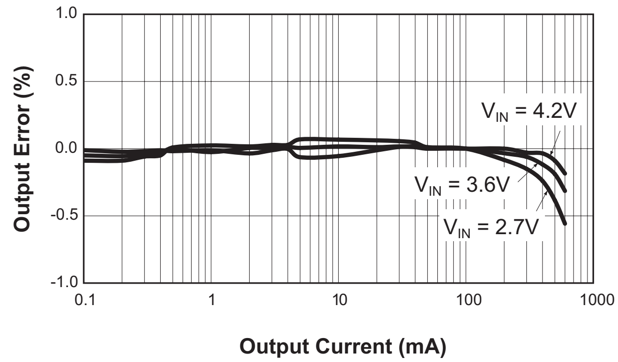
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

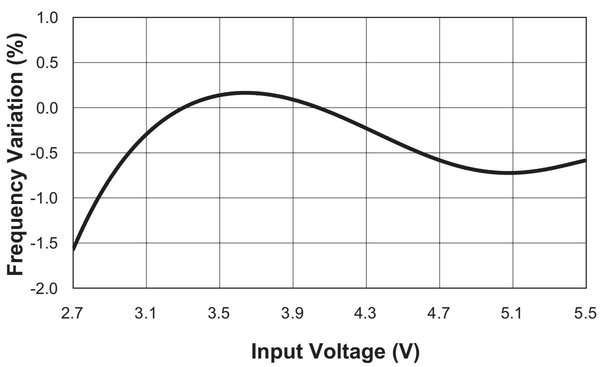
Step-Down Converter Efficiency vs. Load
(V_{OUT} = 1.5V; L = 4.7µH; ENLDO = GND)



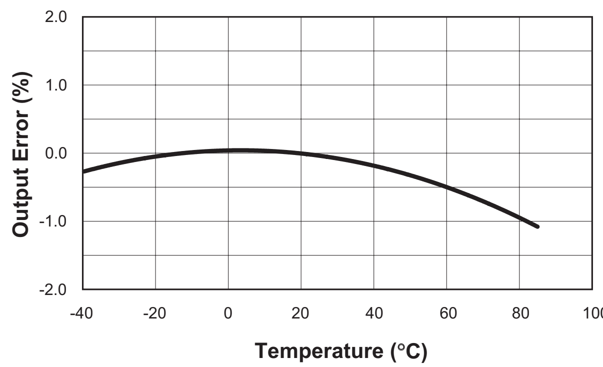
Step-Down Converter DC Regulation
(V_{OUT} = 1.8V; L = 4.7µH; ENLDO = GND)



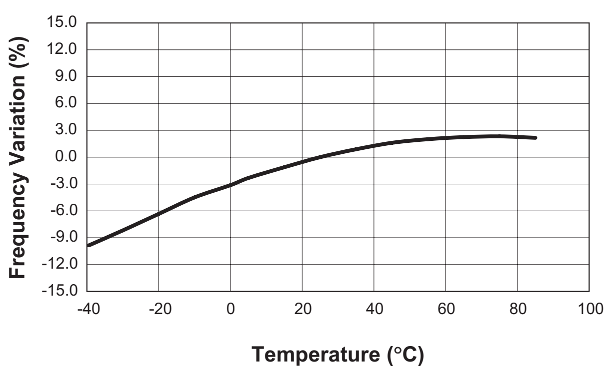
Step-Down Converter Frequency vs. Input Voltage
(V_{OUT} = 1.8V; EN = V_{IN}; ENLDO = GND)



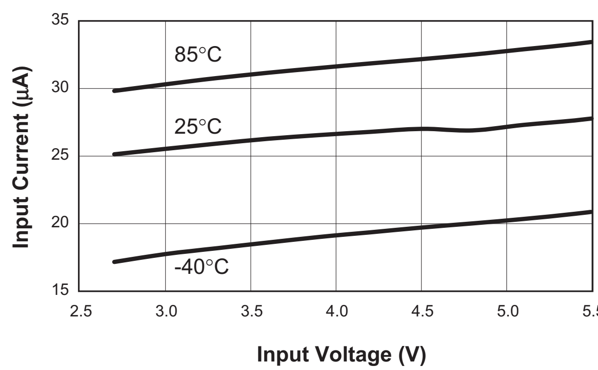
Step-Down Converter Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_O = 1.5V; EN = V_{IN}; ENLDO = GND)



Step-Down Converter Switching Frequency vs. Temperature
(V_{IN} = 3.6V; V_O = 1.5V; EN = V_{IN}; ENLDO = GND)



Step-Down Converter Input Current vs. Input Voltage
(V_O = 1.8V; EN = V_{IN}; ENLDO = GND)



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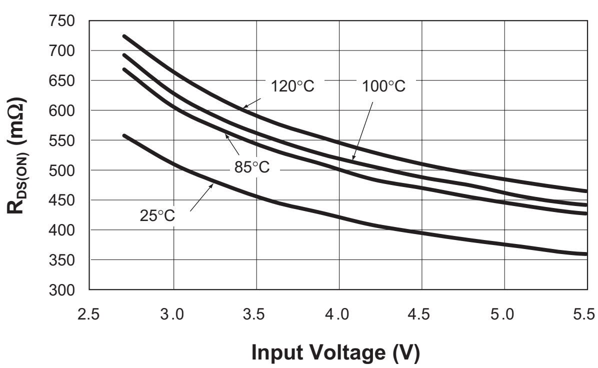
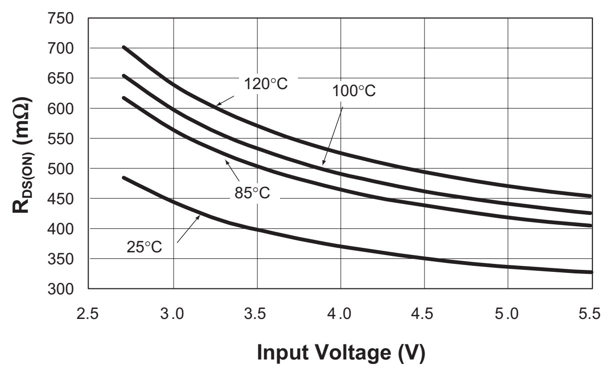
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

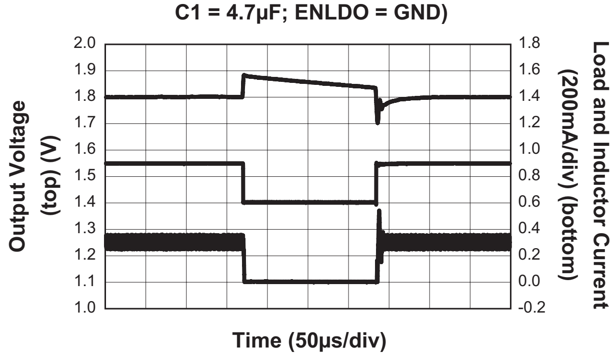
Step-Down Converter
P-Channel $R_{DS(ON)}$ vs. Input Voltage
(EN = V_{IN}; ENLDO = GND)



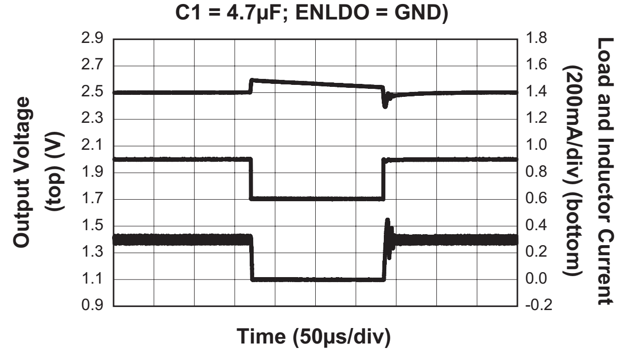
Step-Down Converter
N-Channel $R_{DS(ON)}$ vs. Input Voltage
(EN = V_{IN}; ENLDO = GND)



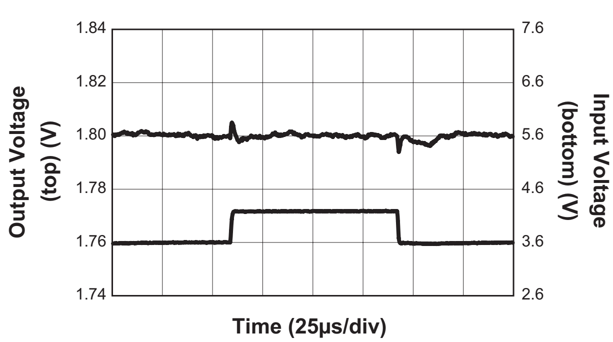
Step-Down Converter Load Transient Response
(1mA to 300mA; V_{IN} = 3.6V; V_{OUT} = 1.8V; C1 = 4.7µF; ENLDO = GND)



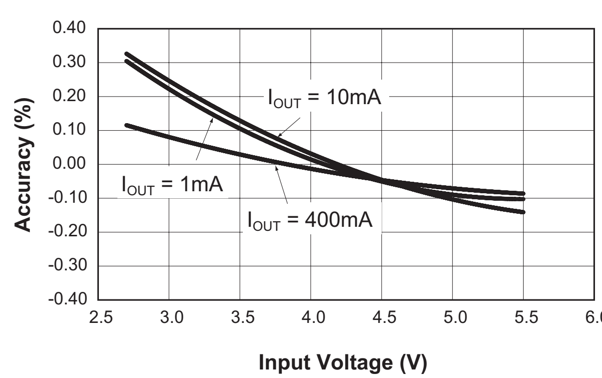
Step-Down Converter Load Transient Response
(1mA to 300mA; V_{IN} = 3.6V; V_{OUT} = 2.5V; C1 = 4.7µF; ENLDO = GND)



Step-Down Converter Line Transient
(V_{OUT} = 1.8V @ 400mA)



Step-Down Converter Line Regulation
(V_{OUT} = 1.8V)



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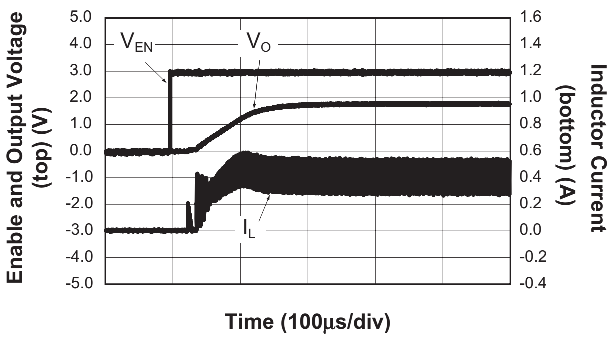
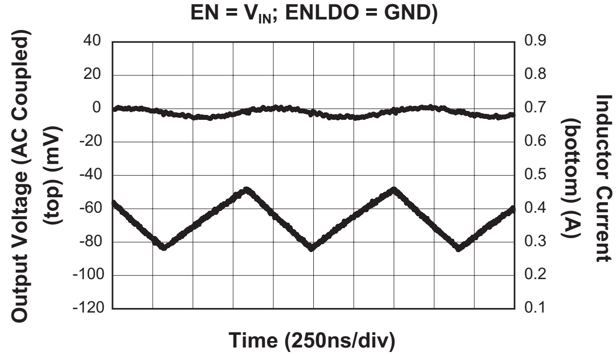
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

Step-Down Converter Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; 400mA;
EN = V_{IN}; ENLDO = GND)



Step-Down Converter Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.8V; 400mA;
EN = V_{IN}; ENLDO = GND)



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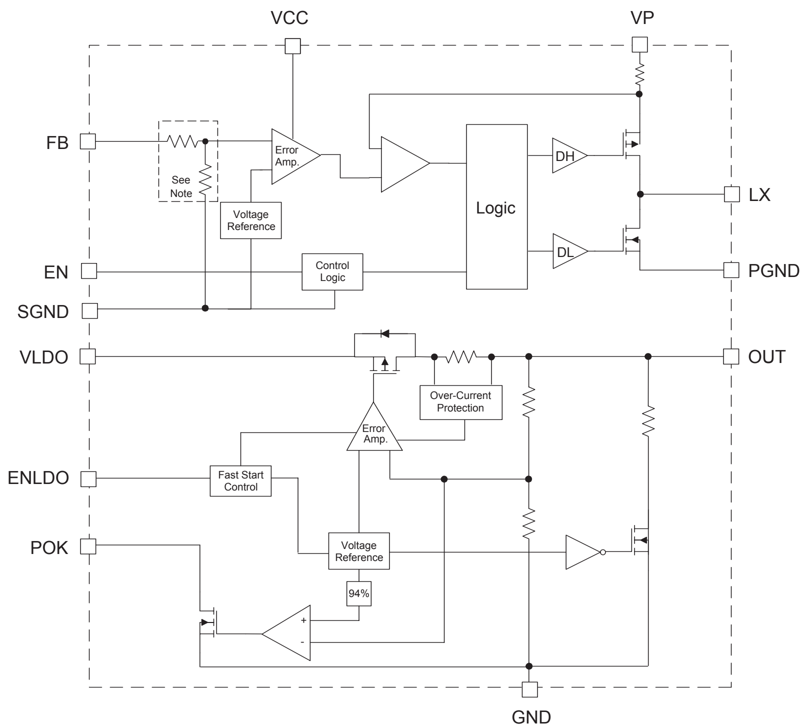
Functional Block Diagram



Note: Internal resistor divider included for ≥ 1.2V versions. For low voltage versions, the feedback pin is tied directly to the error amplifier input.

Functional Description

The AAT2505 is a high performance power management IC comprised of a buck converter and a linear regulator. The high efficiency buck converter is capable of delivering up to 600mA. Designed to operate at 1.4MHz, the converter requires only three external components (C_{IN}, C_{OUT}, and L_X) and is stable with a ceramic output capacitor. The linear regulator delivers 300mA and also is stable with a ceramic output capacitor.

Linear Regulator

The advanced circuit design of the linear regulator has been specifically optimized for very fast start-up and shutdown timing. This proprietary CMOS LDO has also been tailored for superior transient response characteristics. These traits are particularly important for applications that require fast power supply timing.

The high-speed turn-on capability is enabled through implementation of a fast-start control circuit which accelerates the power-up behavior of fundamental control and feedback circuits within the LDO regulator. Fast turn-off time response is achieved by an active output pull-down circuit, which is enabled when the LDO regulator is placed in shutdown mode. This active fast shutdown circuit has no adverse effect on normal device operation. The LDO regulator output has been specifically optimized to function with low-cost, low-ESR ceramic capacitors; however, the design will allow for operation over a wide range of capacitor types.

Other features include an integrated Power-OK comparator which indicates when the output is out of regulation. The POK open-drain output is low when OUT is 6% below its nominal regulation voltage. The open-drain signal is held low when the linear regulator is in shutdown mode. The regulator comes with complete short-circuit and thermal protection. The combination of these two internal protection circuits gives a comprehensive safety system to guard against extreme adverse operating conditions.

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The regulator features an enable/disable function. This pin (ENLDO) is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the ENLDO turn-on control level must be greater than 1.5V. The LDO regulator will go into the disable shutdown mode when the voltage on the EN pin falls below 0.6V. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

When the regulator is in shutdown mode, an internal 20kΩ resistor is connected between OUT and GND. This is intended to discharge C_{OUT} when the LDO regulator is disabled. The internal 20kΩ resistor has no adverse impact on device turn-on time.

Step-Down Converter

The AAT2505 buck is a constant frequency peak current mode PWM converter with internal compensation. It is designed to operate with an input voltage range of 2.7V to 5.5V. The output voltage ranges from 0.6V to the input voltage for the internally fixed version (see Figure 1) , and up to 3.3V for the externally adjustable version (see Figure 2). The 0.6V fixed model is also the adjustable version and is externally programmable with a resistive divider. The converter MOSFET power stage is sized for 600mA load capability with up to 96% efficiency. Light load efficiency exceeds 80% at a 500µA load.

Soft Start

The AAT2505 soft-start control prevents output voltage overshoot and limits inrush current when either the input power or the enable input is applied. When pulled low, the enable input forces the converter into a low-power, non-switching state with a bias current of less than 1µA. A startup time of 150µs is achieved across the operating range.

Low Dropout Operation

For conditions where the input voltage drops to the output voltage level, the converter duty cycle increases to 100%. As 100% duty cycle is approached, the minimum off-time initially forces the high side on-time to exceed the 1.4MHz clock cycle and reduce the effective switching frequency. Once the input drops below the level where the output can be regulated, the high side P-channel MOSFET is turned on continuously for 100% duty cycle. At 100% duty cycle, the output voltage tracks the input voltage minus the IR drop of the high side P-channel MOSFET $R_{DS(ON)}$.

Low Supply

The under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

Fault Protection

For overload conditions, the peak inductor current is limited. Thermal protection disables switching when the internal dissipation or ambient temperature becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis.

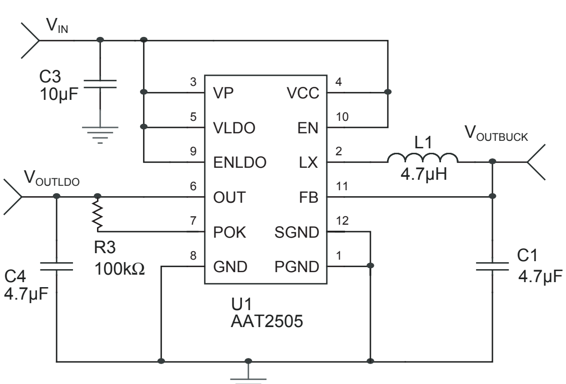

Figure 1: AAT2505 Fixed Output.

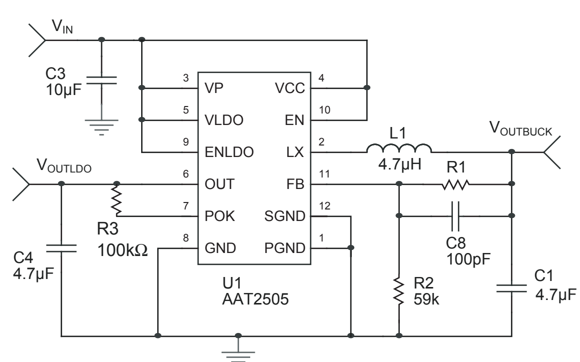

Figure 2: AAT2505 with Adjustable Step-Down Output and Enhanced Transient Response.

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Applications Information

Linear Regulator

Input and Output Capacitors: An input capacitor is not required for basic operation of the linear regulator. However, if the AAT2505 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation. Typically, a 1µF or larger capacitor is recommended for C_{IN} in most applications. C_{IN} should be located as closely to the device V_{IN} pin as practically possible.

An input capacitor greater than 1µF will offer superior input line transient response and maximize power supply ripple rejection. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}. However, for 300mA LDO regulator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

For proper load voltage regulation and operational stability, a capacitor is required between OUT and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as directly as practically possible for maximum device performance. Since the regulator has been designed to function with very low ESR capacitors, ceramic capacitors in the 1.0µF to 10µF range are recommended for best performance. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection should use 2.2µF or greater for C_{OUT}. In low output current applications, where output load is less than 10mA, the minimum value for C_{OUT} can be as low as 0.47µF.

Equivalent Series Resistance: ESR is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance associated with a capacitor that includes lead resistance, internal connections, size and area, material composition, and ambient temperature. Typically, capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Ceramic Capacitor Materials: Ceramic capacitors less than 0.1µF are typically made from NPO or C0G materials. NPO and C0G materials generally have tight tolerance and are very stable over temperature. Larger capacitor values are usually composed of X7R, X5R, Z5U, or Y5V dielectric materials. Large ceramic capacitors (i.e., greater than 2.2µF) are often available in low-cost Y5V and Z5U dielectrics. These two material types are not recommended for use with the regulator, since the capacitor tolerance can vary more than ±50% over the operating temperature range of the device. A 2.2µF Y5V capacitor could be reduced to 1µF over temperature; this could cause problems for circuit operation. X7R and X5R dielectrics are much more desirable. The temperature tolerance of X7R dielectric is better than ±15%.

Capacitor area is another contributor to ESR. Capacitors that are physically large in size will have a lower ESR when compared to a smaller sized capacitor of an equivalent material and capacitance value. These larger devices can improve circuit transient response when compared to an equal value capacitor in a smaller package size. Consult capacitor vendor datasheets carefully when selecting capacitors for LDO regulators.

Step-Down Converter

Inductor Selection: The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation for the adjustable and low-voltage fixed versions of the AAT2505 is 0.24A/µsec. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.5V output and 4.7µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.5V}{4.7\mu H} = 0.24 \frac{A}{\mu sec}$$

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This is the internal slope compensation for the adjustable (0.6V) version or low-voltage fixed versions. When externally programming the 0.6V version to 2.5V, the calculated inductance is 7.5µH.

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot V_O}{0.24A \frac{A}{\mu sec}} \approx 3\frac{\mu sec}{A} \cdot V_O$$

$$= 3\frac{\mu sec}{A} \cdot 2.5V = 7.5\mu H$$

In this case, a standard 6.8µH value is selected.

For high-voltage fixed versions (2.5V and above), m = 0.48A/µsec. Table 1 displays inductor values for the AAT2505 fixed and adjustable options.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 4.7µH CDRH3D16 series inductor selected from Sumida has a 105mΩ DCR and a 900mA DC current rating. At full load, the inductor DC loss is 17mW which gives a 2.8% loss in efficiency for a 400mA, 1.5V output.

Input Capacitor

Select a 4.7µF to 10µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_{OBUCK}}{V_{IN}} \cdot \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_{OBUCK}} - ESR\right) \cdot F_S}$$

$$\frac{V_{OBUCK}}{V_{IN}} \cdot \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \times V_{OBUCK}$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_{OBUCK}} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_{OBUCK} \cdot \sqrt{\frac{V_{OBUCK}}{V_{IN}} \cdot \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right)}$$

Configuration	Output Voltage	Inductor
0.6V Adjustable With External Feedback	1V, 1.2V	2.2µH
	1.5V, 1.8V	4.7µH
	2.5V, 3.3V	6.8µH
Fixed Output	0.6V to 3.3V	4.7µH

Table 1: Inductor Values.

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The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_{OBUCK}}{V_{IN}} \cdot \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \times V_{OBUCK}$

$$I_{RMS(MAX)} = \frac{I_{OBUCK}}{2}$$

The term $\frac{V_{OBUCK}}{V_{IN}} \cdot \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_{OBUCK} is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2505. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C2) can be seen in the evaluation board layout in Figure 3.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7μF to 10μF X5R or X7R ceramic capacitor provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

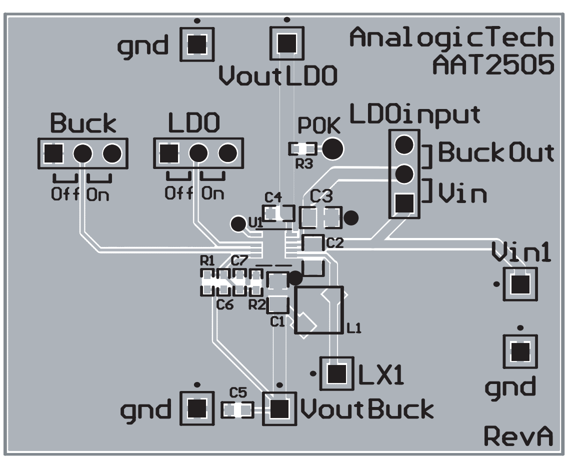

Figure 3: AAT2505 Evaluation Board Top Side.

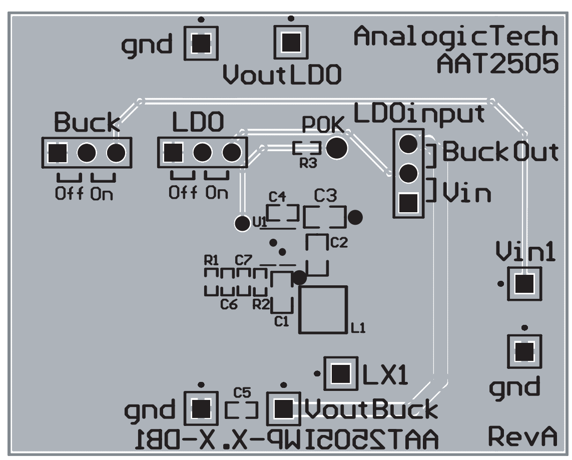

Figure 4: AAT2505 Evaluation Board Bottom Side.

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The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation limits the minimum output capacitor value to 4.7µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

Adjustable Output Resistor Selection

For applications requiring an adjustable output voltage, the 0.6V version can be externally programmed. Resistors R1 and R2 of Figure 5 program the output to regulate at a voltage higher than 0.6V.

To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 2 summarizes the resistor values for various output voltages with R2 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2 = \left(\frac{1.5V}{0.6V} - 1\right) \cdot 59k\Omega = 88.5k\Omega$$

The adjustable version of the AAT2505, combined with an external feedforward capacitor (C8 in Figures 2 and 5), delivers enhanced transient response for extreme pulsed load applications. The addition of the feedforward capacitor typically requires a larger output capacitor C1 for stability.

	R2 = 59kΩ	R2 = 221kΩ
V_{OUT} (V)	R1 (kΩ)	R1 (kΩ)
0.8	19.6	75
0.9	29.4	113
1.0	39.2	150
1.1	49.9	187
1.2	59.0	221
1.3	68.1	261
1.4	78.7	301
1.5	88.7	332
1.8	118	442
1.85	124	464
2.0	137	523
2.5	187	715
3.3	267	1000

Table 2: Adjustable Resistor Values For Use With 0.6V Step-Down Converter.

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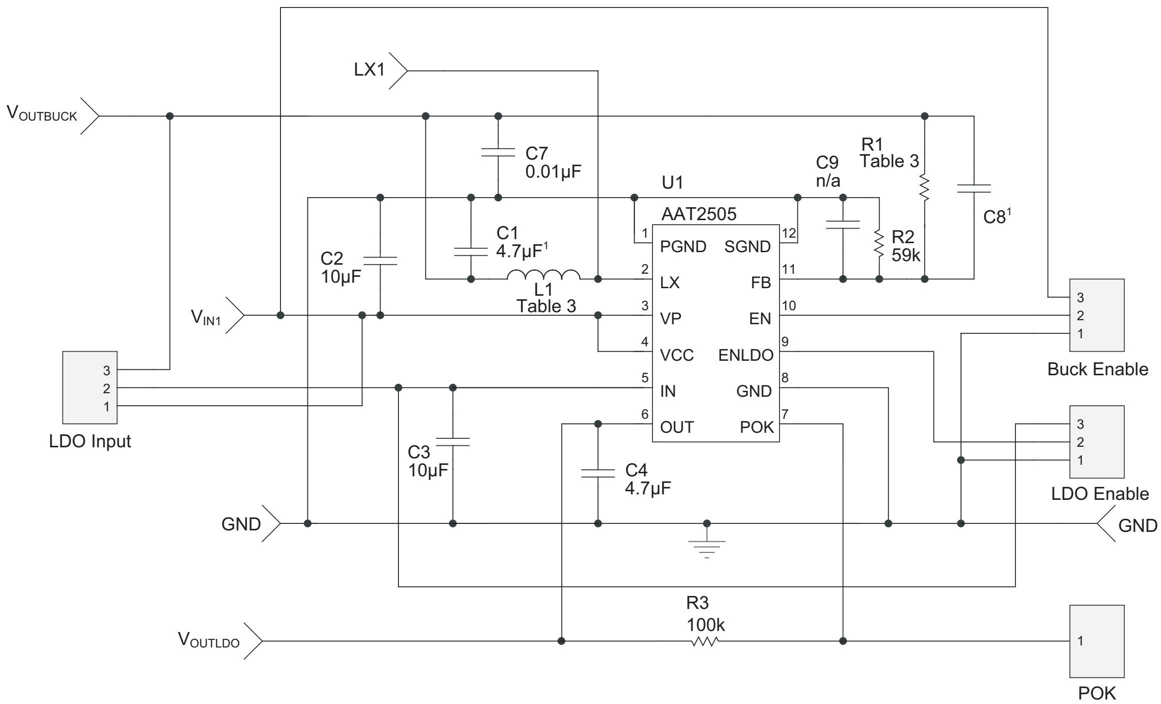

Figure 5: AAT2505 Evaluation Board Schematic.

Thermal Calculations

There are three types of losses associated with the AAT2505 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the step-down converter and LDO losses is given by:

$$P_{TOTAL} = \frac{I_{OBUCK}^2 \cdot (R_{DSON(H)} \cdot V_{OBUCK} + R_{DSON(L)} \cdot [V_{IN} - V_{OBUCK}])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_S \cdot I_{OBUCK} + I_{QBUCK} + I_{QLDO}) \cdot V_{IN} + I_{OLDO} \cdot (V_{IN} - V_{OLDO})$$

I_{QBUCK} is the step-down converter quiescent current and I_{QLDO} is the LDO quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses.

For the condition where the buck converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_{OBUCK}^2 \cdot R_{DSON(H)} + I_{OLDO} \cdot (V_{IN} - V_{OLDO})$$

$$+ (I_{QBUCK} + I_{QLDO}) \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

1. For step-down converter, enhanced transient configuration C8 = 100pF and C1 = 10µF.

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Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TDFN33-12 package which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

PCB Layout

The following guidelines should be used to ensure a proper layout.

1. The input capacitor C2 should connect as closely as possible to VP and PGND, as shown in Figure 4.
2. The output capacitor and inductor should be connected as closely as possible. The connection of the inductor to the LX pin should also be as short as possible.
3. The feedback trace should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB pin. This prevents noise from being coupled into the high impedance feedback node.
4. The resistance of the trace from the load return to GND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. For good thermal coupling, PCB vias are required from the pad for the TDFN paddle to the ground plane. The via diameter should be 0.3mm to 0.33mm and positioned on a 1.2mm grid.

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Step-Down Converter Design Example

Specifications

V_{OBUCK} = 1.8V @ 400mA (adjustable using 0.6V version), Pulsed Load ΔI_{LOAD} = 300mA

V_{OLDO} = 3.3V @ 300mA

V_{IN} = 2.7V to 4.2V (3.6V nominal)

F_S = 1.4MHz

T_{AMB} = 85°C

1.8V Buck Output Inductor

$$L1 = 3\frac{\mu sec}{A} \cdot V_{O2} = 3\frac{\mu sec}{A} \cdot 1.8V = 5.4\mu H$$ (use 4.7µH; see Table 1)

For Sumida inductor CDRH3D16, 4.7µH, DCR = 105mΩ.

$$\Delta I_{L1} = \frac{V_O}{L1 \cdot F_S} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1.8V}{4.7\mu H \cdot 1.4MHz} \cdot \left(1 - \frac{1.8V}{4.2V}\right) = 156mA$$

$$I_{PKL1} = I_O + \frac{\Delta I_{L1}}{2} = 0.4A + 0.068A = 0.468A$$

$$P_{L1} = I_O^2 \cdot DCR = 0.4A^2 \cdot 105m\Omega = 17mW$$

1.8V Buck Output Capacitor

V_{DROOP} = 0.1V

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.3A}{0.1V \cdot 1.4MHz} = 6.4\mu F\text{; use } 10\mu F$$

$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_O) \cdot (V_{IN(MAX)} - V_O)}{L1 \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.8V \cdot (4.2V - 1.8V)}{4.7\mu H \cdot 1.4MHz \cdot 4.2V} = 45mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (45mA)^2 = 10\mu W$$

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1.8V Buck Input Capacitor

Input Ripple V_{PP} = 25mV

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_{OBUCK}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{25mV}{0.4A} - 5m\Omega\right) \cdot 4 \cdot 1.4MHz} = 4.75\mu F$$

$$I_{RMS} = \frac{I_{OBUCK}}{2} = 0.2Arms$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (0.2A)^2 = 0.2mW$$

AAT2505 Total Losses

$$P_{TOTAL} = \frac{I_{OBUCK}^2 \cdot (R_{DSON(H)} \cdot V_{OBUCK} + R_{DSON(L)} \cdot [V_{IN} - V_{OBUCK}])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_S \cdot I_{OBUCK} + I_{QBUCK} + I_{QLDO}) \cdot V_{IN} + (V_{IN} - V_{OLDO}) \cdot I_{OLDO}$$

$$= \frac{0.4^2 \cdot (0.725\Omega \cdot 1.8V + 0.7\Omega \cdot [4.2V - 1.8V])}{4.2V}$$

$$+ (5ns \cdot 1.4MHz \cdot 0.4A + 50\mu A + 125\mu A) \cdot 4.2V + (4.2V - 3.3V) \cdot 0.3A = 395mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 395mW = 105°C$$

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V_{OUT} (V)	R1 (kΩ)	R1 (kΩ)	L1 (μH)
Adjustable Version (0.6V device)	R2 = 59kΩ	R2 = 221kΩ[1]	
0.8	19.6	75.0	4.7
0.9	29.4	113	4.7
1.0	39.2	150	4.7
1.1	49.9	187	4.7
1.2	59.0	221	4.7
1.3	68.1	261	4.7
1.4	78.7	301	4.7
1.5	88.7	332	4.7
1.8	118	442	4.7
1.85	124	464	4.7
2.0	137	523	4.7 or 6.8
2.5	187	715	10
3.3	267	1000	10
V_{OUT} (V)	**R1 (kΩ)**		**L1 (μH)**
Fixed Version	**R2 Not Used**		
0.6-3.3V	0		4.7

Table 3: Evaluation Board Component Values.

Manufacturer	Part Number	Inductance (μH)	Max DC Current (A)	DCR (Ω)	Size (mm) LxWxH	Type
Sumida	CDRH3D16-4R7	4.7	0.90	0.11	4.0x4.0x1.8	Shielded
Sumida	CDRH3D16/HP100	10	0.84	0.23	4.0x4.0x1.8	Shielded
MuRata	LQH32CN4R7M23	4.7	0.45	0.20	2.5x3.2x2.0	Non-Shielded
MuRata	LQH32CN4R7M33	4.7	0.65	0.15	2.5x3.2x2.0	Non-Shielded
MuRata	LQH32CN4R7M53	4.7	0.65	0.15	2.5x3.2x1.55	Non-Shielded
Coilcraft	LPO6610-472	4.7	1.10	0.20	5.5x6.6x1.0	1mm
Coilcraft	LPO3310-472	4.7	0.80	0.27	3.3x3.3x1.0	1mm
Coiltronics	SDRC10-4R7	4.7	1.53	0.117	4.5x3.6x1.0	1mm Shielded
Coiltronics	SDR10-4R7	4.7	1.30	0.122	5.7x4.4x1.0	1mm Shielded
Coiltronics	SD3118-4R7	4.7	0.98	0.122	3.1x3.1x1.85	Shielded
Coiltronics	SD18-4R7	4.7	1.77	0.082	5.2x5.2x1.8	Shielded

Table 4: Typical Surface Mount Inductors.

1. For reduced quiescent current R2 = 221kΩ.

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Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
MuRata	GRM219R61A475KE19	4.7µF	10V	X5R	0805
MuRata	GRM21BR60J106KE19	10µF	6.3V	X5R	0805

Table 5: Surface Mount Capacitors.

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Ordering Information

Package	Voltage: Buck Converter	Voltage: LDO	Marking[1]	Part Number (Tape and Reel)[2]
TDFN33-12	Adj.	2.8V	POXYY	**AAT2505IWP-AQ-T1**
TDFN33-12	Adj.	2.6V	PPXYY	**AAT2505IWP-AO-T1**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/pbfree.

Legend: Voltage	Code
Adjustable (0.6V)	A
0.9	B
1.2	E
1.5	G
1.8	I
1.9	Y
2.5	N
2.6	O
2.7	P
2.8	Q
2.85	R
2.9	S
3.0	T
3.3	W
4.2	C

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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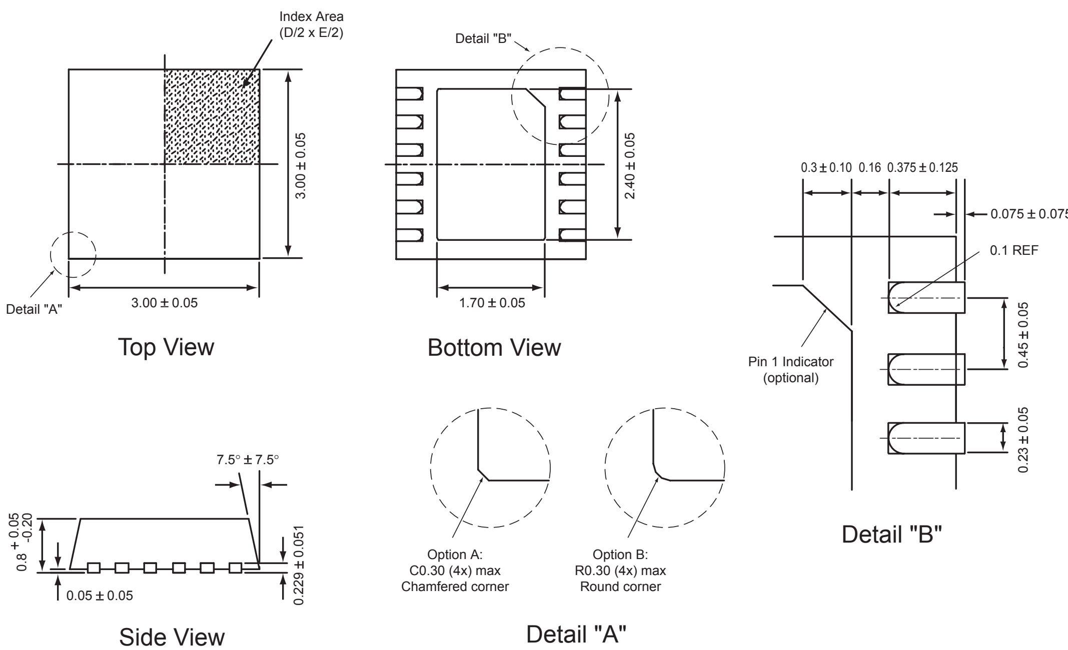
TDFN33-12



All dimensions in millimeters.

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