National Semiconductor

August 2005

# LMH1251
# $YP_BP_R$ to RGB Decoder and 2:1 Video Switch

## General Description

The LMH™1251 is a wideband 2:1 analog video switch with an integrated $YP_BP_R$ to RGB decoder. The device accepts one set of $YP_BP_R$ inputs and one set of RGB/HSYNC/VSYNC inputs. Based on the input selected, the output will be either a decoded TV or buffered PC video signal.

The LMH1251 has a SYNC separator and processor that is capable of extracting sync timing information from both Standard Definition Television (SDTV) and High Definition Television (HDTV) inputs. It provides bi-level sync, and tri-level sync separation.

The color space conversion from $YP_BP_R$ to RGB in the LMH1251 is realized with a very high precision fully analog dematrixer that provides chrominance accuracy that is less than 2.5% of amplitude & 1.5° of phase error on a vectorscope. It is equipped with a smart video detection circuit which automatically senses SDTV and HDTV video formats and applies the appropriate color space conversion.

The LMH1251 is capable of handling SDTV, HDTV, XGA, SXGA, and UXGA video formats, which makes it an ideal solution for enhancing value in applications ranging from LCD monitors, to set-top boxes, to projectors. The LMH1251 is available in a TSSOP-24 package.

## Features

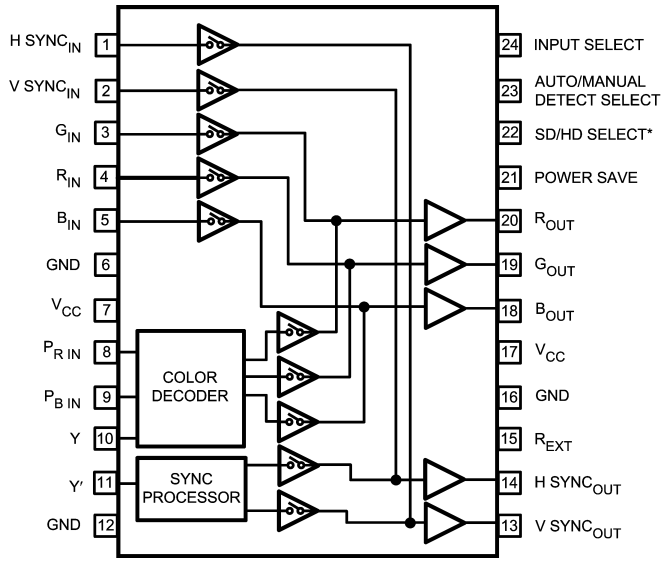
- $YP_BP_R$ to RGB decoding
- $YP_BP_R$ path: 70 MHz, –3 dB, 700 $mV_{PP}$ bandwidth
- RGB path: 400 MHz, –3 dB, 700 $mV_{PP}$ bandwidth
- Supports PC video display resolutions up to UXGA (1600 x 1200 @ 75 Hz)
- Supports 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p
- Smart video format detection for SD and HD
- Power save mode

## Applications

- TFT LCD monitor
- CRT monitor
- Set-top box
- Display projector

## Connection Diagram

**24-Pin TSSOP**




20151927

**Top View**

LMH™ is a trademark of National Semiconductor Corporation.

## Truth Table

### TABLE 1. Input Select

| Pin 24 | OUT |
|---|---|
| 0 | RGBhv input Ch |
| 1 | $YP_BP_R$ input Ch |

### TABLE 2.

| Pin 23 | Pin 22 | SYNC | Format Detection | Decoding Scheme |
|---|---|---|---|---|
| 0 | 0 | Bi-Level | Manual | 480p |
| 0 | 1 | Tri-Level | Manual | 720p/180i |
| 1 | *Outputs 0 | Bi-Level | Auto | 480p |
| 1 | *Outputs 1 | Tri-Level | Auto | 720p/1080i |

**Note:** * When Pin 23 is set high, the LMH1251 is in Auto Mode, in which it can detect the incoming video format (SD or HD) and apply the appropriate color decoding and sync processing. With Auto Mode, Pin 22 becomes an output pin, and will either output a logic high or low to notify the user of the format that is being detected by the LMH1251. If Pin 23 is set low, the LMH1251 is in Manual Mode, in which the user must specify the format with Pin 22. With Manual Mode, Pin 22 is an input pin. Since Pin 22 is a bi-directional pin, care must be taken to not apply any voltages to it when it is in the Auto Mode, in which it functions as an output pin. The use of the Auto Mode with Pin 22 left floating is typically recommended.

### TABLE 3. Power Save

| Pin 21 | Low Power Mode |
|---|---|
| 0 | Disable |
| 1 | Enabled |

## Ordering Information

| Package | Part Number | Package Marking | Transport Media | NSC Drawing |
|---|---|---|---|---|
| 24-Pin TSSOP | LMH1251MT | LMH1251MT | 61 Units/Rail | MTC24 |
| | LMH1251MTX | | 2.5k Units Tape and Reel | |

## Absolute Maximum Ratings (Notes 1, 3)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| ESD Tolerance | |
| Susceptibility(Note 4) | 4.0 kV |
| Machine Model (Note 11) | 400V |
| Supply Voltage $V_{CC}$, Pins 7 and 17 | 5.5V |
| Voltage at any Input Pin ($V_{IN}$) | $V_{CC}$ −0.5 ≥ $V_{IN}$ ≥ 0V |
| Video Inputs (pk-pk) | 0.0V ≤ $V_{IN}$ ≤ 1.2V |
| Thermal Resistance to Ambient ($\theta_{JA}$) | 110˚C/W |
| Thermal Resistance to Case ($\theta_{JC}$) | 25˚C/W |
| Junction Temperature ($T_J$) | +150˚C |
| Storage Temperature Range | −65˚C to +150˚C |
| Lead Temperature (soldering 10 sec.) | 265˚C |

## Operating Ratings (Note 2)

| | |
|---|---|
| Operating Temperature Range | 0˚C to +70˚C |
| Supply Voltage ($V_{CC}$) | 4.75V ≤ $V_{CC}$ ≤ 5.25V |
| RGB Video Inputs (pk-pk) | 0.0V ≤ $V_{IN}$ ≤ 0.7V |
| Y Video Inputs (incl. Sync) | -0.3V ≤ $V_{IN}$ ≤ 0.7V |
| $P_BP_R$ Video Inputs | -0.35V ≤ $V_{IN}$ ≤ 0.35V |

## Video Signal Electrical Characteristics

Unless otherwise noted: $T_A$ = 25˚C, $V_{CC}$ = +5.0V, RGB $Video_{IN}$ = 0.70, Y $Video_{IN}$ = 0.7 $V_{PP}$, $P_BP_R$ $Video_{IN}$ = ±350 VmV, $C_L$ = 8 pF, Video Outputs = 0.7 $V_{PP}$. See (Note 7) for Min and Max parameters and (Note 6) for typicals.

| Symbol | Parameter | Conditions (Note 2) | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{S, RGB}$ | Supply Current | No Output Loading, 80 kHz | 28 | 34 | 41 | mA |
| $I_S$, $YP_BP_R$ | Supply Current | No Output Loading, 480p see (Note 8) | 60 | 70 | 80 | mA |
| $I_{S-PS}$ | Supply Current, Power Save Mode | Power Save Mode, No Output Loading, 80 kHz, see (Note 8) | 4 | 8 | 12 | mA |
| $I_{OUT}$ | Output Current | | | 3 | | mA |
| $V_{O\ BLK}$ | Typical DC Active Video Black Level Output Voltage | No AC Input Signal | 1.8 | 2.1 | 2.4 | VDC |
| $Gain_{RGB}$ | RGB Video Unity Gain | RGB $Video_{IN}$ = 0.7 $V_{PP}$ | | 0.07 | | dB |
| Ch-Ch $Match_{RGB}$ | RGB Ch to Ch Matching | RGB $Video_{IN}$ = 0.7 $V_{PP}$ | | 0.02 | | dB |
| $LE_{RGB}$ | RGB Input: Linearity Error | Staircase Input Signal see (Note 9) | | 0 | | % |
| **Video Time Domain Response** | | | | | | |
| RGB $t_r$ | RGB Input: Video Rise Time | 10% to 90%, AC Input Signal (Note 5) | | 1.55 | | ns |
| RGB $OS_R$ | RGB Input: Rising Edge Overshoot | AC Input Signal (Note 5) | | 3 | | % |
| RGB $t_f$ | RGB Input: Video Fall Time | 90% to 10%, AC Input Signal (Note 5) | | 1.55 | | ns |
| RGB $OS_F$ | RGB Input: Rising Edge Overshoot | AC Input Signal (Note 5) | | 3 | | % |
| SD $YP_BP_R$ $t_r$ | SD $YP_BP_R$ Input: Video Rise Time | 10% to 90%, AC Input Signal (Note 5) | | 1.54 | | ns |
| RGB OSF | RGB Input: Falling Edge Overshoot | (Note 5), AC Input Signal | | 3 | | % |
| SD $YP_BP_R$ $t_r$ | SD $YP_BP_R$ Input: Video Rise Time | 10% to 90%, AC Input Signal (Note 5) | | 15.4 | | ns |
| SD $YP_BP_R$ $OS_R$ | SD $YP_BP_R$ Input: Rising Edge Overshoot | AC Input Signal (Note 5) | | 3 | | % |
| SD $YP_BP_R$ $t_f$ | SD $YP_BP_R$: Video Fall Time | 90% to 10%, AC Input Signal (Note 5) | | 15.4 | | ns |
| SD $YP_BP_R$ $OS_F$ | SD $YP_BP_R$: Falling Edge Overshoot | AC Input Signal (Note 5) | | 3 | | % |

## Video Signal Electrical Characteristics (Continued)

Unless otherwise noted: $T_A$ = 25˚C, $V_{CC}$ = +5.0V, RGB $Video_{IN}$ = 0.70, Y $Video_{IN}$ = 0.7 $V_{PP}$, $P_BP_R$ $Video_{IN}$ = ±350 VmV, $C_L$ = 8 pF, Video Outputs = 0.7 $V_{PP}$. See (Note 7) for Min and Max parameters and (Note 6) for typicals.

| Symbol | Parameter | Conditions (Note 2) | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| HD $YP_BP_R$ $t_r$ | HD $YP_BP_R$ Input: Video Rise Time | 10% to 90%, AC Input Signal (Note 5) | | 8.4 | | ns |
| HD $YP_BP_R$ $OS_R$ | HD $YP_BP_R$ Input: Rising Edge Overshoot | AC Input Signal (Note 5) | | 3 | | % |
| HD $YP_BP_R$ $t_f$ | HD $YP_BP_R$: Video Fall Time | 90% to 10%, AC Input Signal (Note 5) | | 8.4 | | ns |
| HD $YP_BP_R$ $OS_F$ | HD $YP_BP_R$: Falling Edge Overshoot | AC Input Signal (Note 5) | | 3 | | % |
| **Video Frequency Domain Response** | | | | | | |
| RGB BW | RGB Input: Channel Bandwidth (–3 dB) | Large Signal BW | | 400 | | MHz |
| $YP_BP_R$ BW | $YP_BP_R$ Input (SD & HD): Channel Bandwidth (–3 dB) | Large Signal BW | | 70 | | MHz |
| $V_{SEP\ Ch\text{-}Ch}$ 10 MHz | Video Amplifier 10 MHz Isolation Channel to Channel | (Note 12) | | –50 | | dB |
| $V_{SEP\ INPUT\text{-}INPUT}$ 10 MHz | Video Amplifier 10 MHz Isolation RGB Input to $YP_BP_R$ Input | (Note 12) | | –55 | | dB |
| SNR | Signal to Noise Ratio | AC Input Signal, $C_L$ = 8 pF (Note 12) | | 55 | | dB |

## Color Decoding Accuracy

Unless otherwise noted: $T_A$ = 25˚C, $V_{CC}$ = +5.0V, Y $Video_{IN}$ = 0.7 $V_{PP}$, $P_BP_R$ $Video_{IN}$ = ±350 VmV, $C_L$ = 8 pF, Video Outputs = 0.7 $V_{PP}$. See (Note 7) for Min and Max parameters and (Note 6) for typicals.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{COLOR\ ERROR}$ | $\lvert P_BP_R \rvert$ Amplitude (Calculated from RGB Outputs) | $YP_BP_R$ Video Input, 100% Color Bar (any 3 colors), (Note 13) | | ±0.3 | ±2.5 | % |
| $\theta_{COLOR\ ERROR}$ | $P_BP_R$ Phase Angle Calculated from RGB Outputs) | $YP_BP_R$ Video Input, 100% Color Bar (any 3 colors), (Note 13) | | ±0.2 | ±1.5 | deg |

## Sync Signal Electrical Characteristics

Unless otherwise noted: $T_A$ = 25˚C, $V_{CC}$ = +5.0V, Y $Video_{IN}$ = 0.7 $V_{PP}$, $P_BP_R$ $Video_{IN}$ = ±350 VmV, $C_L$ = 8 pF, Video Outputs = 0.7 $V_{PP}$. See (Note 7) for Min and Max parameters and (Note 6) for typicals.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{SYNCL}$ | H & V SYNC Low Input | Pins 1 & 2 | –0.5 | | 1.5 | V |
| $V_{SYNCH}$ | H & V SYNC High Input | Pins 1 & 2 | 3.0 | | $V_{CC}$ +0.5 | V |
| $I_{O\text{-}SYNCH}$ | H & V SYNC Current Sink/Source Capability | 5 kΩ Load | | 3 | | mA |
| $t_{R/F\text{-}SYNC}$ | H & V SYNC Rise/Fall Time | | | 15 | | ns |
| $t_{SYNC\text{-}WIDTH}$ | H & V SYNC Width Error Relative to H & V SYNC Input | H & V SYNC Input | | 5 | | % |
| $t_{Y\text{-}SYNC\text{-}WIDTH}$ | H & V SYNC Width Error Relative to Composite SYNCS on Y | Composite SYNC on Y Input | | 5 | | % |
| $t_{SYNC\text{-}DELAY}$ | 50% of H & V SYNC Input to Output | H & V SYNC Input | | 40 | | ns |

## Sync Signal Electrical Characteristics (Continued)

Unless otherwise noted: $T_A$ = 25˚C, $V_{CC}$ = +5.0V, Y $Video_{IN}$ = 0.7 $V_{PP}$, $P_BP_R$ $Video_{IN}$ = ±350 VmV, $C_L$ = 8 pF, Video Outputs = 0.7 $V_{PP}$. See (Note 7) for Min and Max parameters and (Note 6) for typicals.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{Y\text{-}HSYNC\text{-}DELAY}$ | 50% of H SYNC Input to Output | Composite SYNC on Y Input (Not During Vertical Period) | | 70 | | ns |

## System Interface Signal Characteristics

Unless otherwise noted: $_{TA}$ = 25˚C, $V_{CC}$ = +5.0V, Y $Video_{IN}$ = 0.7 $V_{PP}$, $P_BP_R$ $Video_{IN}$ = ±350 VmV, $C_L$ = 8 pF, Video Outputs = 0.7 $V_{PP}$. See (Note 7) for Min and Max parameters and (Note 6) for typicals

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Logic Low Input Voltage (Pins 24, 23, 22, 21) | | –0.5 | | 1.5 | V |
| $V_{IH}$ | Logic High Input Voltage (Pins 24, 23, 22, 21) | | 3.0 | | $V_{CC}$ +0.5 | V |
| $I_L$ | Logic Low Input Current (Pins 24, 23, 22, 21) | Input Voltage = 0.4V | | ±10 | | µA |
| $I_H$ | Logic High Input Voltage (Pins 24, 23, 22, 21) | Input Voltage = 0.4V | | ±10 | | µA |
| $V_{OL}$ | Logic Low Output Voltage (Pins 24, 23, 22, 21) | IO = 3 mA | | 0.5 | | V |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

**Note 2:** Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. All video inputs must be properly terminated.

**Note 3:** All voltages are measured with respect to GND, unless otherwise specified.

**Note 4:** Human Body Model: 100 pF discharged through a 1.5 kΩ resistor.

**Note 5:** Input from RGB signal generator: $t_r$, $t_f$ = 1.5 ns. Input from SDTV $YP_BP_R$ signal generator: $t_r$, $t_f$ = 15 ns. Input from HDTV $YP_BP_R$ signal generator: $t_r$, $t_f$ = 8 ns.

**Note 6:** Typical specifications are specified at +25˚C and represent the most likely parametric norm.

**Note 7:** Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

**Note 8:** The supply current specified is the quiescent current for $V_{CC}$ and 5V with $R_L$ = ∞. Load resistors are not required and are not used in the test circuit; therefore, all the supply current is used by the device.

**Note 9:** Linearity Error is the maximum variation in step height of a 16 step staircase input signal waveform with a 0.7 $V_{PP}$ level at the input. All 16 are steps equal, with each at least 100 ns in duration.

**Note 10:** $\Delta A_V$ track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three gain stages. It is the difference in gain change between any two amplifiers with the contrast set to $A_V$C-50% and measured relative to the $A_V$ max condition. For example, at $A_V$ max the three amplifiers' gains might be 12.1 dB, 11.9 dB, and 11.8 dB and change to 2.2 dB, 1.9 dB and 1.7 dB respectively for contrast set to $A_V$C-50%. This yields a typical gain change of 10.0 dB with a tracking change of ±0.2 dB.

**Note 11:** The Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200 pF cap is charged to the specific voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

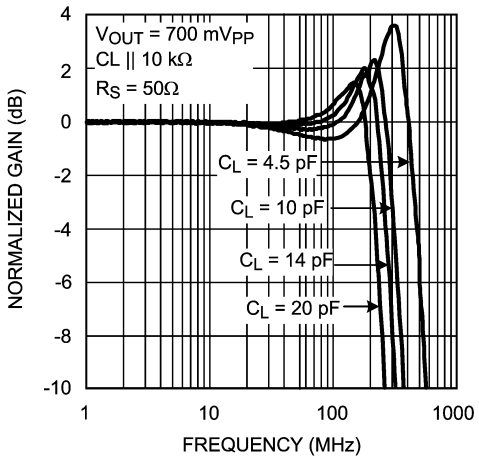
**Note 12:** Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at $f_{IN}$ = 10 MHz for $V_{SEP}$ 10 MHz.

**Note 13:** Any three color bar signals can be used as test signals. The RGB outputs shall be used to calculate the amplitudes and phases of the chrominance results. These should fall within the limits specified.

## Typical Performance Characteristics

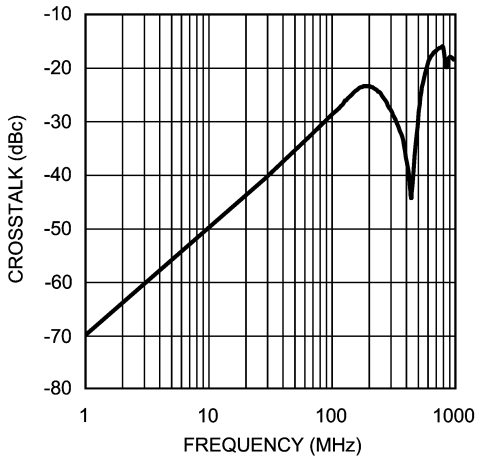
Unless otherwise noted: $T_A$ = 25˚C, $V_{CC}$ = +5.0V, RGB $Video_{IN}$ = 0.70, Y $Video_{IN}$ = 0.7 $V_{PP}$, $P_BP_R$ $Video_{IN}$ = ±350 VmV, $C_L$ = 8 pF, Video Outputs = 0.7 $V_{PP}$. See (Note 7) for Min and Max parameters and (Note 6) for typicals.

**Large Signal Frequency Response**



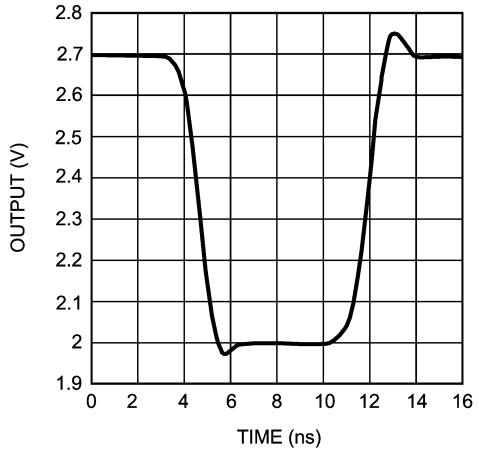

20151903

**Crosstalk vs. Frequency**



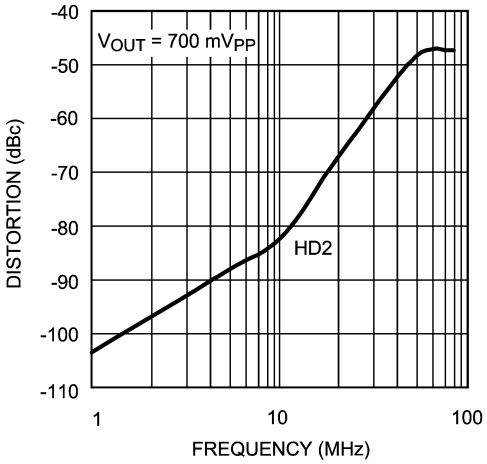

20151904

**Pulse Response**



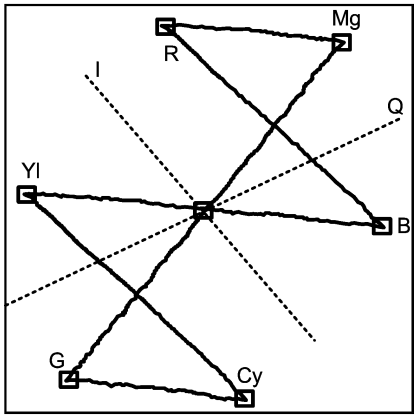

20151901

**Harmonic Distortion vs. Frequency**




20151902

**720p Color Bar Vectorscope**




20151906

# Application Notes

## GENERAL INFORMATION

The LMH1251 is a high-speed triple 2:1 video multiplexer with an integrated sync processor and color space converter. One input channel accepts standard RGBHV PC graphics video and the second input channel accepts $YP_BP_R$ component video. If the first input of the MUX is selected, the device will output the RGBHV video from the input with unity gain. If the second input of the MUX is selected, sync processing and color space conversion will be performed on the $YP_BP_R$ component signals to provide an equivalent RGBHV signal at the output.

## $YP_BP_R$ to RGBHV PROCESSING

The LMH1251 is capable of processing 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p/60 $YP_BP_R$ component video signals only. S-Video, composite NTSC, or composite PAL video will not be decoded by the LMH1251. For High Definition, 720p and 1080i video, the LMH1251 will decode the luminance and color difference signals into primary RGB signals according to the linear arithmetic formula specified in the EIA/CEA-770.3-C Standard for High Definition Analog Component TV. For Standard Definition video, the LMH1251 will perform the decoding according to the linear arithmetic formula specified in the EIA/CEA-770.2-C Standard for Standard Definition Analog Component TV. The advanded analog architecture that is employed to perform the color space conversion is precise to within 2.5% of amplitude & 1.5˚ of phase error on a vectorscope with a color bar test signal. This is illustrated with a vectorscope plot of a decoded color bar signal in the 720p format show in the Typical Performance Characteristics section.

Note that although 480i/576i component video is supported by the LMH1251, most PC Display Monitors cannot handle such line rates. Typically, only 480p, 576p, 720p, and 1080i/1080p are within the displayable line rate range of LCD and CRT monitors. Furthermore, the scaler in LCD monitor systems must include a de-interlacer for it to display interlaced video such as with 1080i.

**Component Video Formats supported by the LMH1251**

480i

480p

576i

576p

720p

1080i23/25/30

1080p50/59/60

## AUTO/MANUAL FORMAT DETECTION

The LMH1251 can either automatically detect the input format of the component video source, or it can be put in a manual mode where the MCU has the flexibility to specify which $YP_BP_R$ to RGBHV processing scheme for the device to apply depending on the input format. If a logic high is applied to Pin 23, the LMH1251 will be in the AUTO detection mode, which is typically recommended. In this mode, the device will appropriately use the correct $YP_BP_R$ to RGBHV processing scheme based on its input format detection. If a logic high is applied to Pin 23, the LMH1251 will be in the Manual detection mode. In this mode, the MCU must apply a logic low to Pin 22 if the processing scheme is for SD Video formats, and a logic high if the processing scheme is for HD Video formats.

Note that in the AUTO mode, Pin 22 becomes an output pin, and outputs a logic low if a SD video input is detected and a logic high if a HD video input is detected, as notification to the MCU.

## MACROVISION COMPATIBILITY

The on-chip sync processor of the LMH1251 is fully compatible with DVD video sources which are embedded with Macrovision copyright protection. The LMH1251 will output Horizontal Sync pulses with consistent periodicity even during the “Macrovision Sync” pulse period.

## POWER SAVE MODE

The LMH1251 is equipped with a power saving mode which is controlled by Pin 21. This pin is a logic level input. The device will enter a low power mode when the power save pin is applied with a logic high by the MCU. Under these conditions, the IC reduces its current consumption to a minimum as specified in the Electrical Characteristics section. However, the sync processor and switch will always remain active. During power save mode, the RGB video outputs are held to the blank level, while the sync signals are allowed to continue to be processed and/or passed through. Based on the absence or presence of sync signals at the output of the LMH1251, the MCU can determine whether to bring the system to a low power consumption state.

## OUTPUT DRIVE CHARACTERISTICS

The LMH1251 is designed to interface with an ADC or preamplifier through an AC coupling capacitor as shown below in *Figure 1*. The RGB outputs of the LMH1251 are 700 $mV_{PP}$ video signals with the black level at approximately 2V, which is the chip’s internal voltage reference level. The H Sync and V Sync outputs are CMOS logic outputs that swing from 0 to 5V. These RGBHV outputs do not have any current drive capability and should not have any load on them. The PCB trace length at the output should be kept as short as possible to minimize resisitive and capacitive loading.

If the LMH1251 is to be designed into a stand-alone converter box application, the configuration in *Figure 2* is recommended. The LMH6739, triple op amp with an internally set gain of 2, can be used to drive RGB video over the VGA cable out to a display monitor. Logic inverters are used for driving the sync signals over the VGA cable.

## Application Notes (Continued)

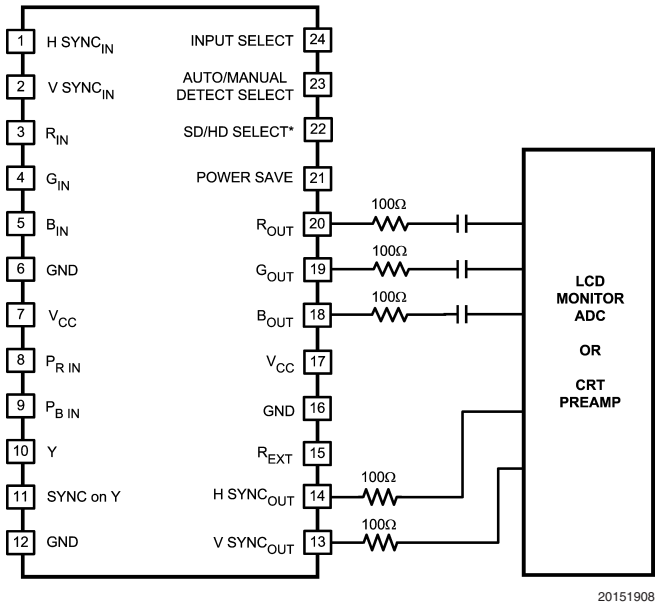



**FIGURE 1. Typical LMH1251 Application**

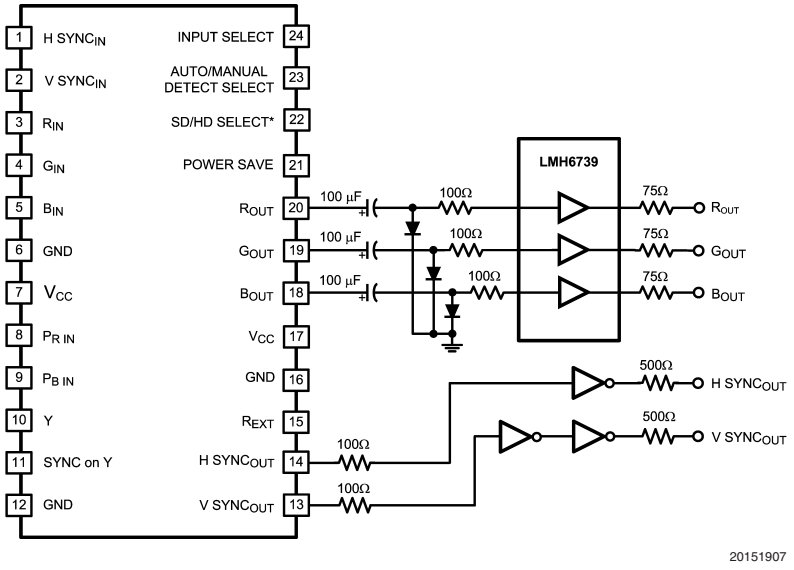



**FIGURE 2. Simplified Application Diagram for Driving a VGA Cable**

### LAYOUT CONSIDERATIONS

The most important point to note regarding the layout of the LMH1251 on a PCB is that the trace length between the output pins of the LMH1251 and the input AC coupling capacitors of the next stage ADC or preamplifier must be as minimal as possible. The trace lengths of the H Sync and V Sync outputs should also be minimized, as the capacitive loading on these outputs must not exceed 6 pF. For long signal paths leading up to the input of the LMH1251, controlled impedance lines should be used, along with impedance matching elements. Bypass capacitors should be placed as close as possible to the supply pins of the device. The larger electrolytic bypass capacitor can be located farther from the device. The 10K external resistor should also be placed as close as possible to the $R_{EXT}$ pin.

## Test Circuit

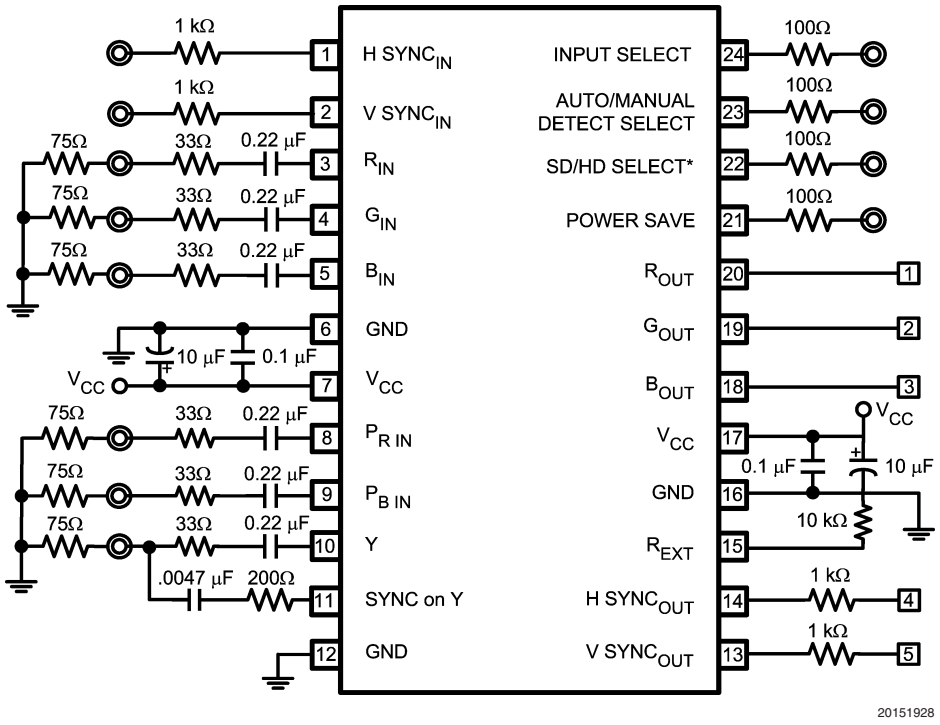
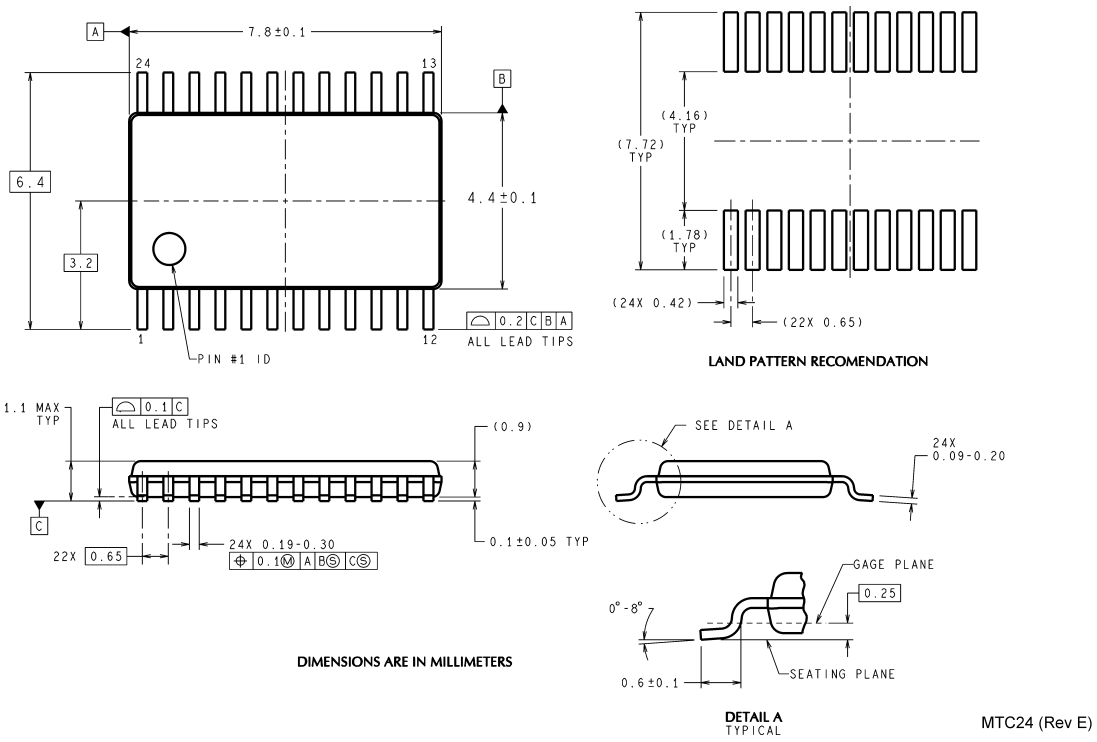



**FIGURE 3. Test Circuit**

## Physical Dimensions inches (millimeters)

unless otherwise noted




MTC24 (Rev E)

**24-Pin TSSOP**
**NS Package Number MTC24**



**National Semiconductor**
**Americas Customer**
**Support Center**
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

**National Semiconductor**
**Europe Customer Support Center**
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor**
**Asia Pacific Customer**
**Support Center**
Email: ap.support@nsc.com

**National Semiconductor**
**Japan Customer Support Center**
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560